Pico LCD 1.14

Overview

1.14inch LCD Display Module For Raspberry Pi Pico, 65K RGB Colors, 240×135 Pixels, SPI Interface

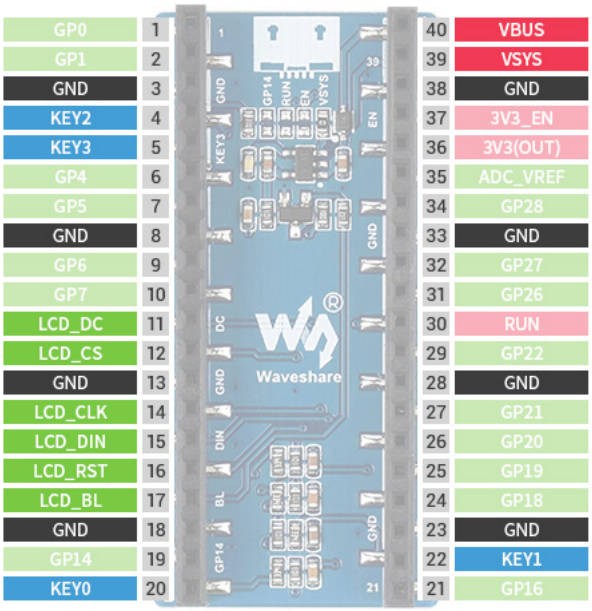
Features

- 240×135 resolution, IPS screen, 65K RGB colors, clear and colorful displaying effect
- SPI interface, requires minimal IO pins
- 4x user buttons for easy interacting

Specifications

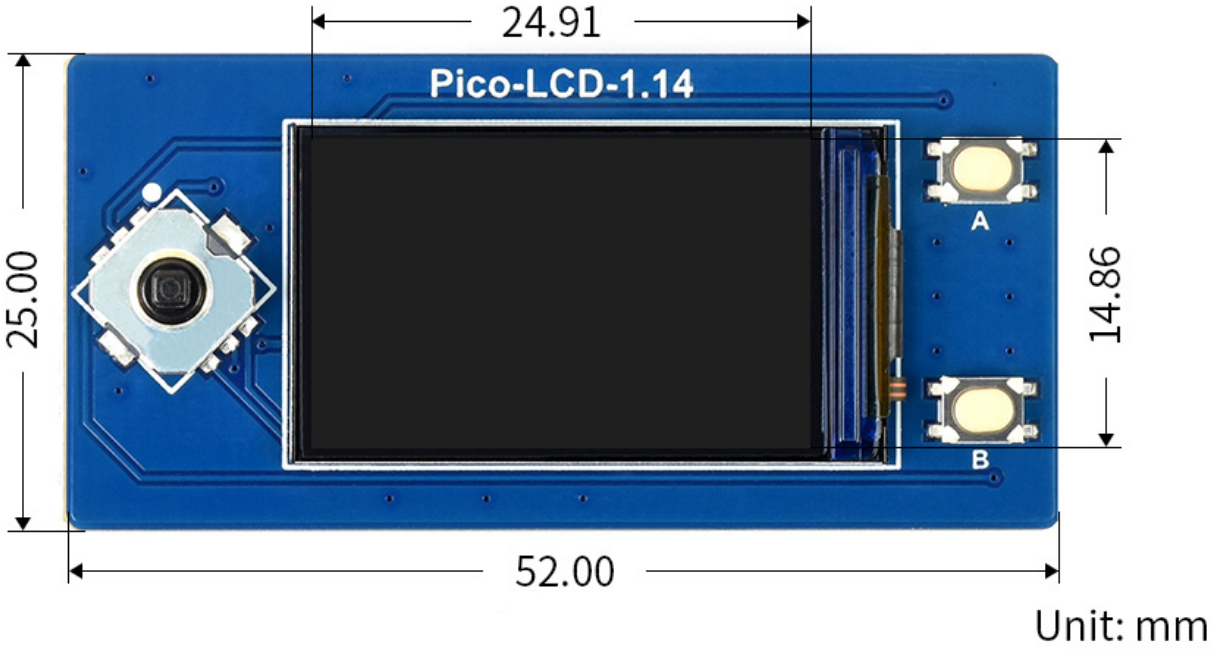
- Operating voltage: 2.6~5.5V
- Resolution: 240x135 pixels
- Communication interface: 4-wire SPI
- Display size: 24.91 x 14.86mm
- Display panel: IPS
- Pixel size: 0.1101 x 0.1035mm
- Driver: ST7789
- Dimensions 52.00 x 25.00mm

Pinout



VBUS	Power input 3.3V~5.5V
VSYS	Power input 1.8V~5.5V
GND	Ground
KEY0	User key 0
KEY1	User key 1
KEY2	User key 2
KEY3	User key 3
LCD_DC	Data/Command control pin (high for data, low for command)
LCD_CS	Chip select (low active)
LCD_CLK	SPI clock input
LCD_DIN	SPI data input
LCD_RST	Reset (low active)
LCD_BL	Backlight

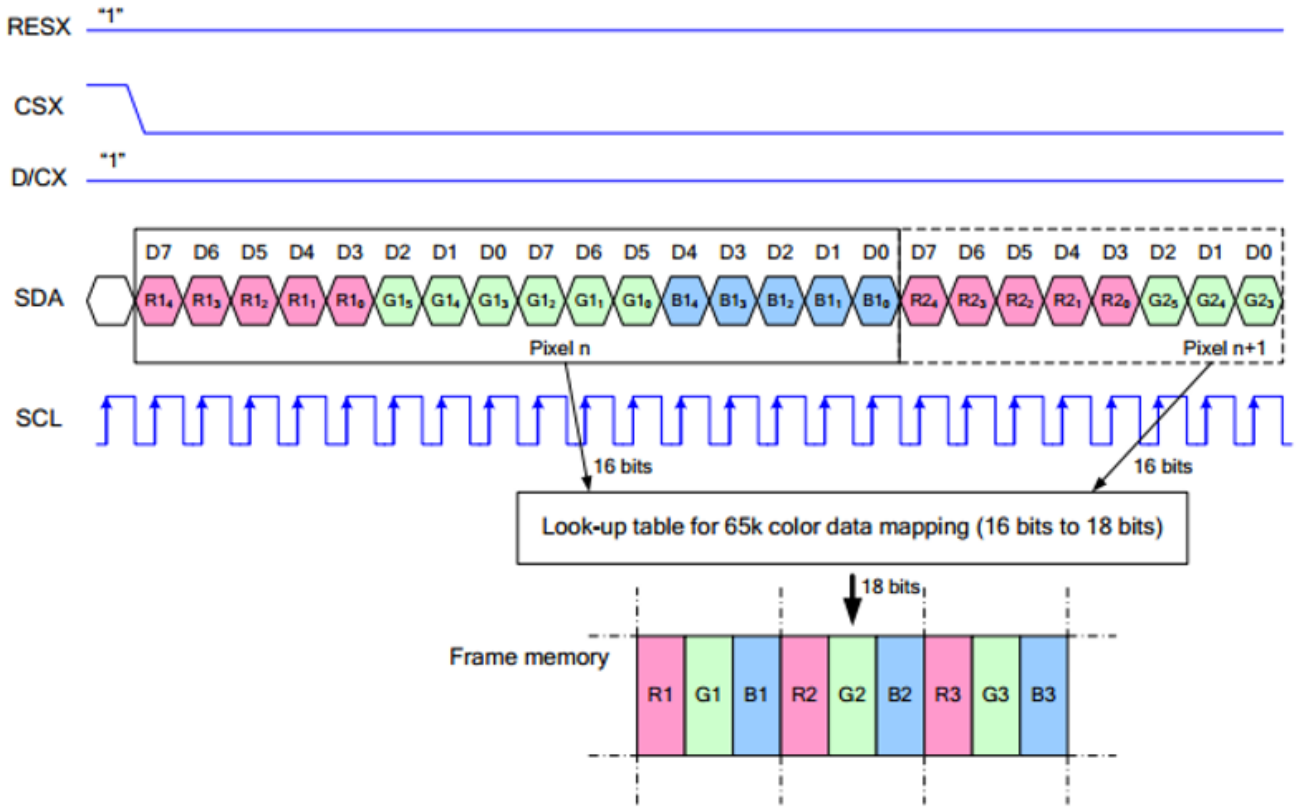
Dimension



LCD and the controller

The ST7789VW is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 240 source line and 320 gate line driving circuits. The resolution of this LCD is 135(H)RGB x 240(V), it supports horizontal mode and vertical mode, and it doesn't use all the RAM of the controller.
This LCD accepts 8-bits/9-bits/16-bits/18-bits parallel interface, that are RGB444, RGB565, RGB666. The color format used in demo codes is RGB565.
This LCD uses a 4-line SPI interface for reducing GPIO and fast speed.LCD

Working Protocol



Note: Different from the traditional SPI protocol, the data line from the slave to the master is hidden since the device only has a display requirement.
RESX Is the reset pin, it should be low when powering the module and be higher at other times; ;
CSX is slave chip select, when CS is low, the chip is enabled.
D/CX is data/command control pin, when DC = 0, write command, when DC = 1, write data
SDA is the data pin for transmitting RGB data, it works as the MOSI pin of SPI interface;
SCL work s the SCLK pins of SPI interface.
SPI communication has data transfer timing, which is combined by CPHA and CPOL.
CPOL determines the level of the serial synchronous clock at an idle state. When CPOL = 0, the level is Low. However, CPOL has little effect on the transmission.
CPHA determines whether data is collected at the first clock edge or at the second clock edge of the serial synchronous clock; when CPHL = 0, data is collected at the first clock edge.
There are 4 SPI communication modes. SPI0 is commonly used, in which CPHL = 0, CPOL = 0.