

-30V P-Channel Enhancement Mode MOSFET

Description

The UMW 30P03D uses advanced trench technology

to provide excellent $R_{DS(ON)}$, low gate charge and

operation with gate voltages as low as 4.5V. This

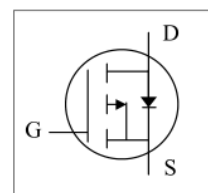
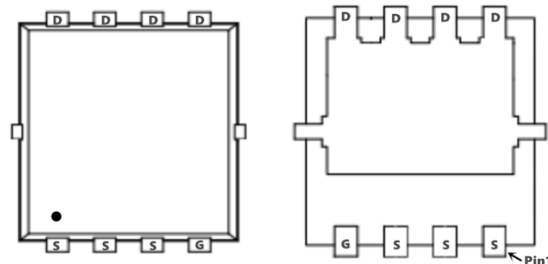
device is suitable for use as a

Battery protection or in other Switching application.

General Features

$V_{DS} = -30V$ $I_D = -60A$

$R_{DS(ON)} < 11 m\Omega @ V_{GS}=10V$



Application

Battery protection

Load switch

Uninterruptible power supply

Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating		Units
		10s	Steady State	
VDS	Drain-Source Voltage	-30		V
VGS	Gate-Source Voltage	±20		V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-60		A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-27		A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-14.3	-9	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-11.4	-7.2	A
IDM	Pulsed Drain Current ²	-130		A
EAS	Single Pulse Avalanche Energy ³	125		mJ
IAS	Avalanche Current	-50		A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	37		W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	4.2	1.67	W
TSTG	Storage Temperature Range	-55 to 150		°C
T _J	Operating Junction Temperature Range	-55 to 150		°C
R _{θJA}	Thermal Resistance Junction-Ambient ¹	75		°C/W
R _{θJA}	Thermal Resistance Junction-Ambient ¹ (t ≤10s)	30		°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	3.36		°C/W

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Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C , I _D =-1mA	---	-0.0232	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V , I _D =-30A	---	---	11	mΩ
		V _{GS} =-4.5V , I _D =-15A	---	---	20	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	---	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.6	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V , V _{GS} =0V , T _J =25°C	---	---	-1	uA
		V _{DS} =-24V , V _{GS} =0V , T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} = ± 20V , V _{DS} =0V	---	---	± 100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V , I _D =-30A	---	30	---	S
R _g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz	---	9	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V , V _{GS} =-4.5V , I _D =-15A	---	22	---	nC
Q _{gs}	Gate-Source Charge		---	8.7	---	
Q _{gd}	Gate-Drain Charge		---	7.2	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V , V _{GS} =-10V , R _G =3.3 , I _D =-15A	---	8	---	ns
T _r	Rise Time		---	73.7	---	
T _{d(off)}	Turn-Off Delay Time		---	61.8	---	
T _f	Fall Time		---	24.4	---	
C _{iss}	Input Capacitance	V _{DS} =-15V , V _{GS} =0V , f=1MHz	---	2215	---	pF
C _{oss}	Output Capacitance		---	310	---	
C _{rss}	Reverse Transfer Capacitance		---	237	---	
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V , Force Current	---	---	-42	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-130	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =-1A , T _J =25°C	---	---	-1	V
t _{rr}	Reverse Recovery Time	I _F =-15A , dI/dt=100A/μs , T _J =25°C	---	19	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	9	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD} =-25V V_{GS} =-10V, L=0.1mH, I_{AS}=-50A,
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics

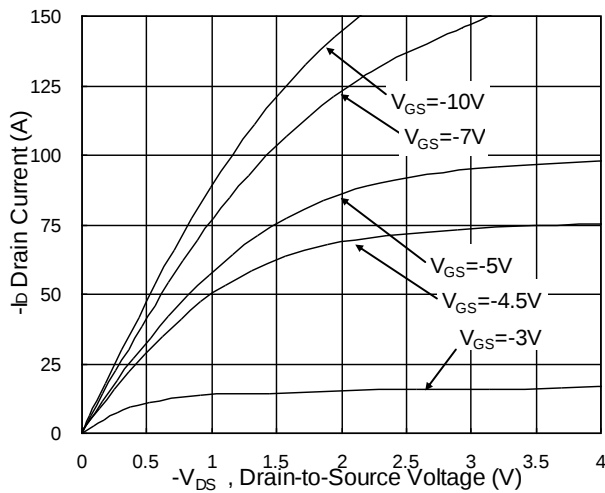


Fig.1 Typical Output Characteristics

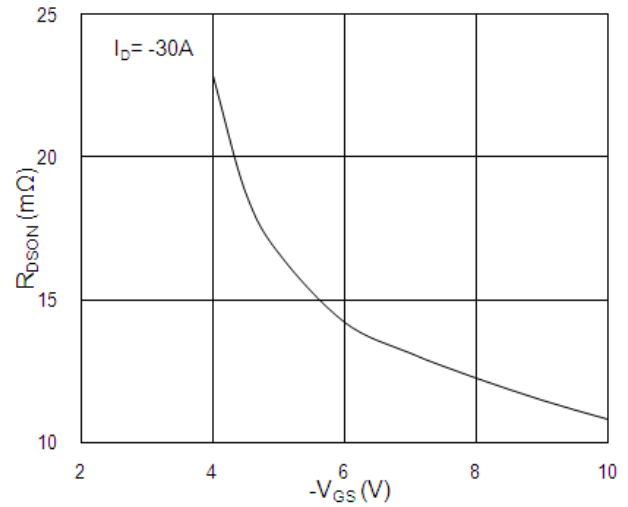


Fig.2 On-Resistance vs. G-S Voltage

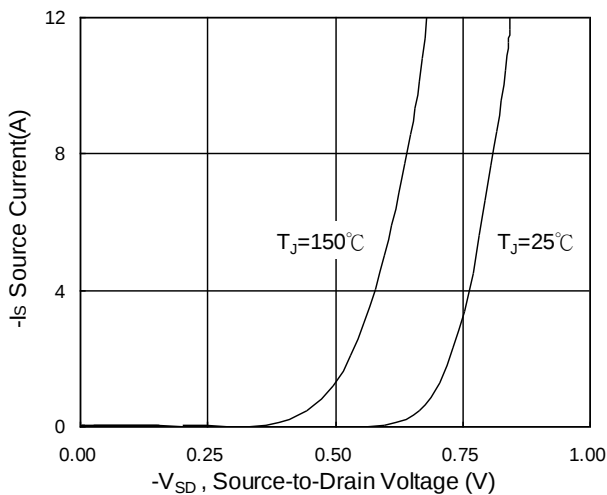


Fig.3 Forward Characteristics of Reverse

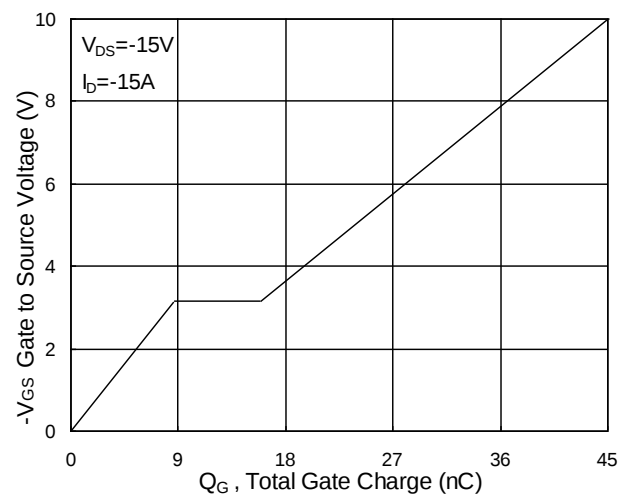


Fig.4 Gate-Charge Characteristics

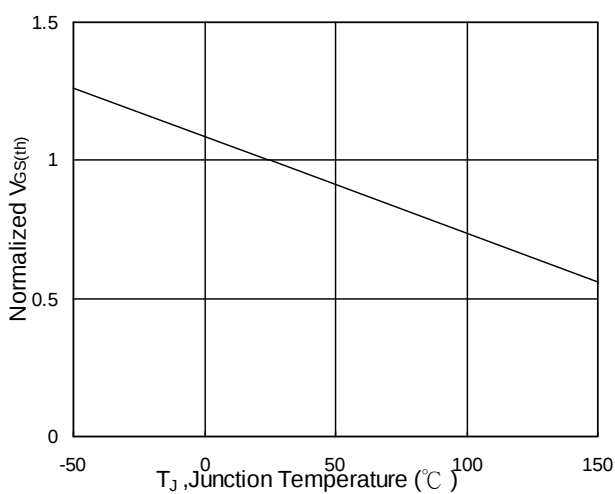


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

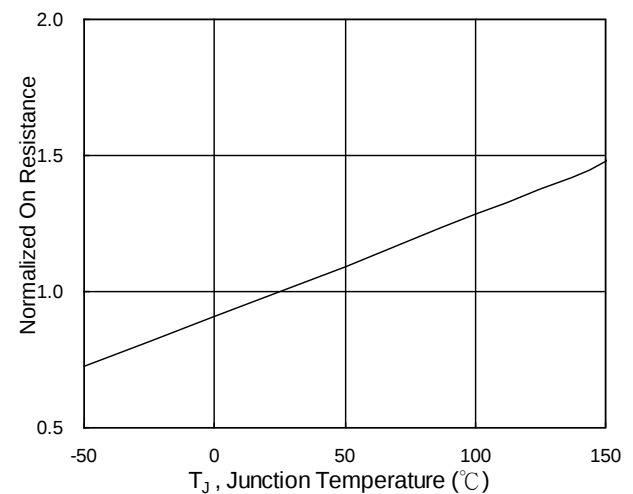


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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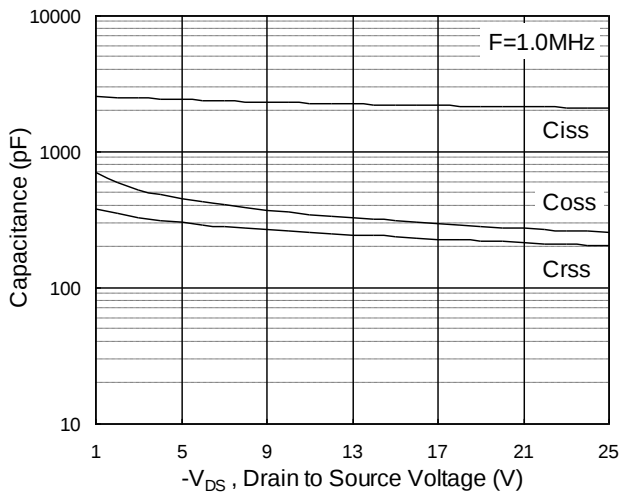


Fig.7 Capacitance

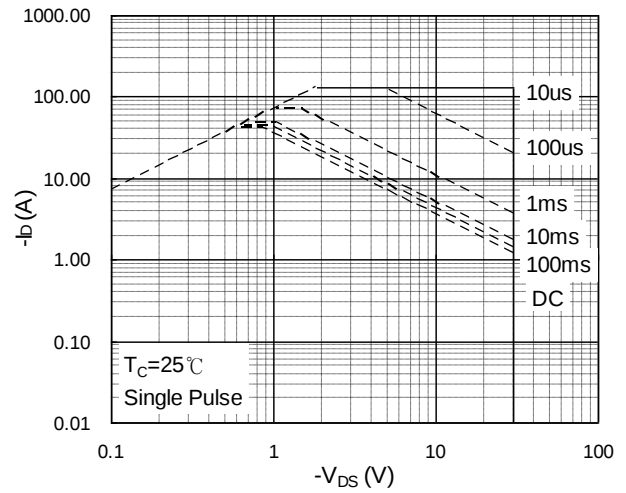


Fig.8 Safe Operating Area

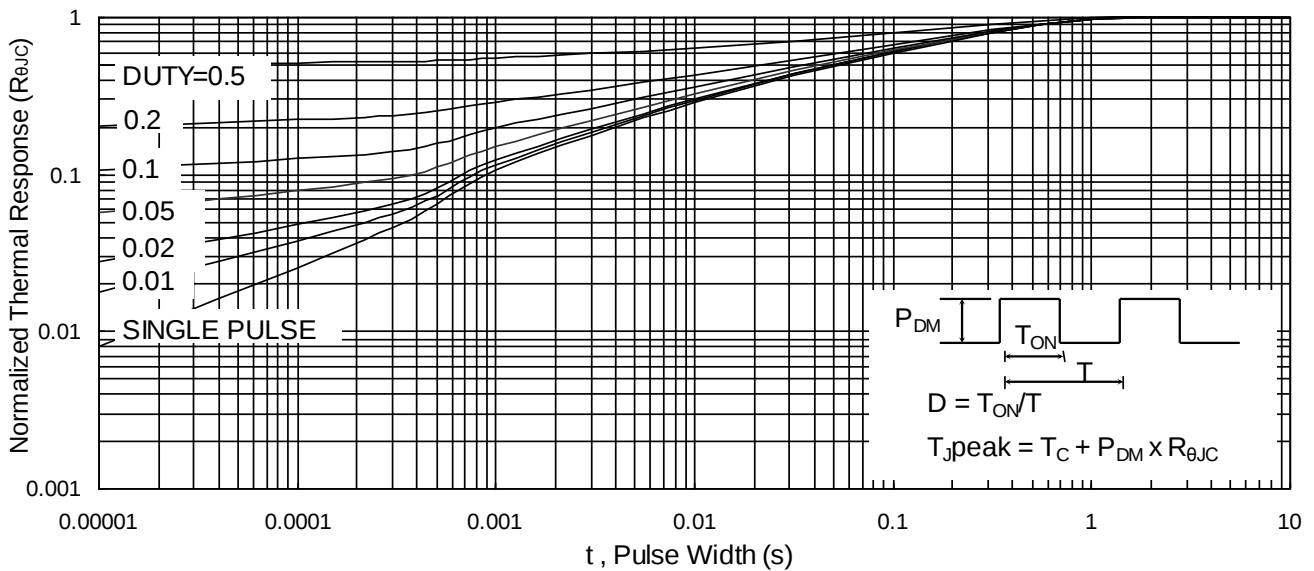


Fig.9 Normalized Maximum Transient Thermal Impedance

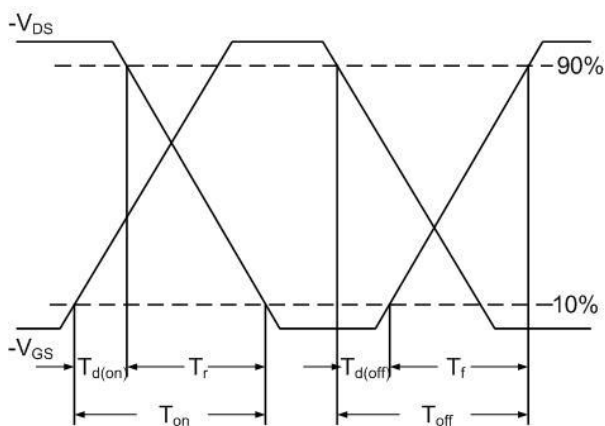


Fig.10 Switching Time Waveform

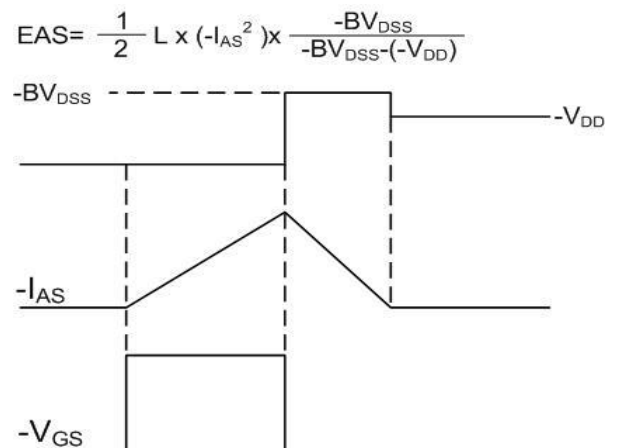
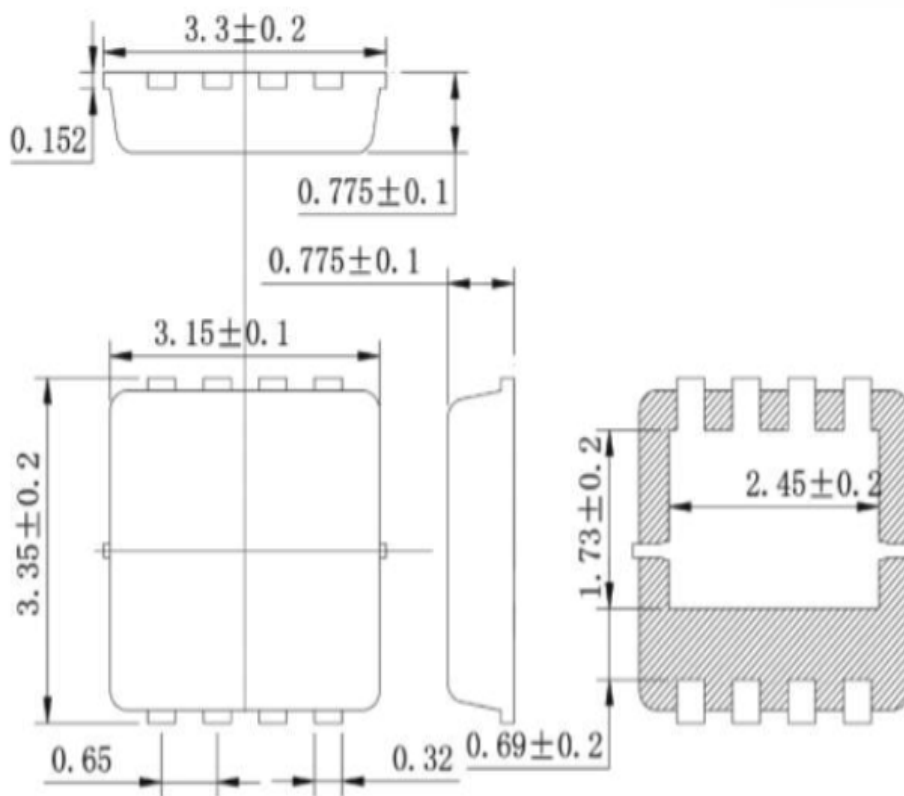


Fig.11 Unclamped Inductive Switching Waveform

DFN3×3-8L



Marking



Ordering information

Order code	Package	Baseqty	Delivermode
UMW 30P03D	DFN3x3-8L	5000	Tape and reel