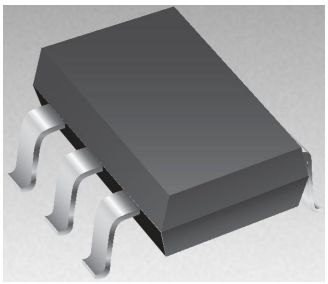
Four-Lines ESD Protection -ESD5V0J4

Description

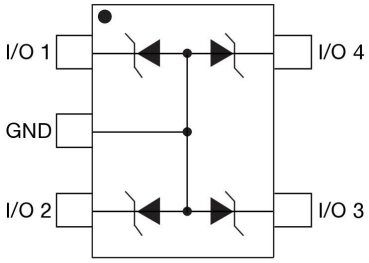
The ESD5V0J4 TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD and other voltage-induced transient events. They are designed for use in applications where board space is at a premium. Each device will protect up to four lines. They are unidirectional devices and may be used on lines where the signal polarities are above ground. TVS diodes are solid-state devices designed specifically for transient suppression. They feature large cross-sectional area junctions for conducting high transient currents. They offer desirable characteristics for board level protection including fast response time.



Feature

- Case :JEDEC SOT353 package
- Low clamping voltage
- Protects four I/O lines
- Solid-state silicon-avalanche technology
- Compatible with IEC 61000-4-2(ESD) :Air 15KV , Contact 8KV
- Compatible with IEC 61000-4-4(EFT) :40A ,5/50 nS

Schematic & PIN Configuration



Applications

- Portable Electronics
- Industrial Controls
- Wireless systems
- Security systems

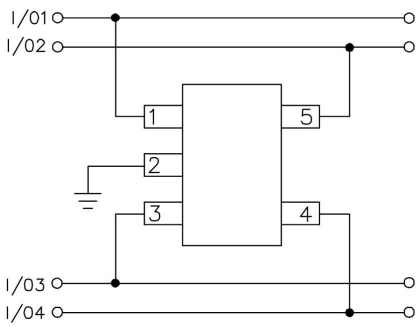
Absolute Maximum Ratings

Parameter		Symbol	Limits	Unit
IEC61000−4−2(ESD)	Air		±15	KV
	Contact		±15	
ESD voltage	Per Human Body Model		16	KV
	Per Machine Model		400	V
Peak Power Dissipation @ 8 X 20 ms @TA ≤ 25°C (Note 1)		P_{PK}	100	W
Steady State Power -- 1 Diode (Note 2)		P_D	200	mW
Thermal Resistance Junction−to−Ambient		$R_{\Theta JA}$	625	℃/W
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	℃
Junction and Storage temperature range		T_j, T_{stg}	-55 ~ +150	℃

Electrical Characteristics (T =25° C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA	6		7.2	V
Reverse Leakage Current	I_R	V_R =V_{RWM}			5	μA
Clamping Voltage	V_C	I_{PP}=5A, t_P = 8/20μs			12.5	V
Junction Capacitance	C_J	V_R=0V, f = 1MHz Between I/O pins and GND		35		pF

Circuit Board Layout Recommendations for Suppression of ESD.

Mode	Pin Connection	Description
4-line protection mode		Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended: A: Place the ESD5V0J4 near the input terminals or connectors to restrict transient coupling. B: Minimize the path length between the ESD5V0J4 and the protected line. C: Minimize all conductive loops including power and ground loops. D: The ESD transient return path to ground should be kept as short as possible. E: Never run critical signals near board edges. F: Use ground planes whenever possible.

Rating & Characteristic Curves

Figure 1- Power Derating Curve

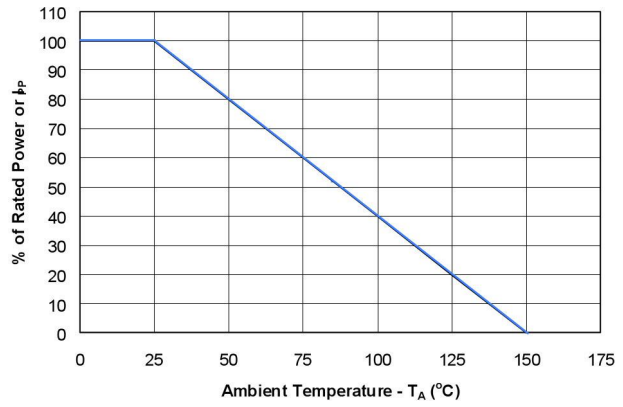


Figure 2- Pulse Waveform

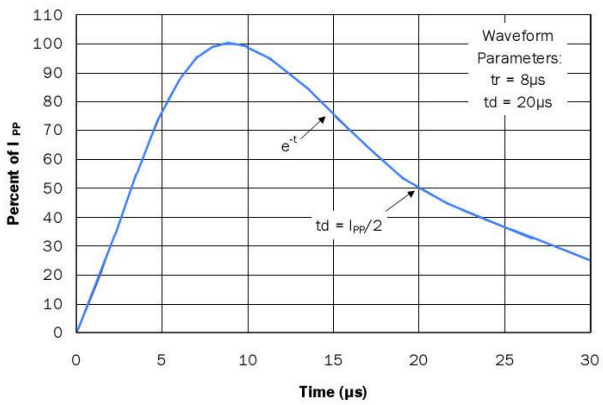
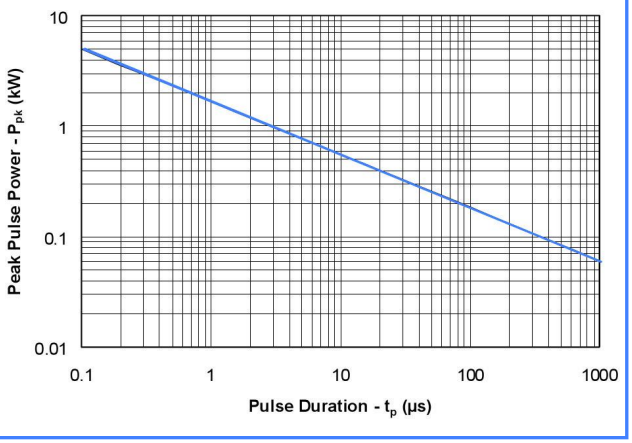
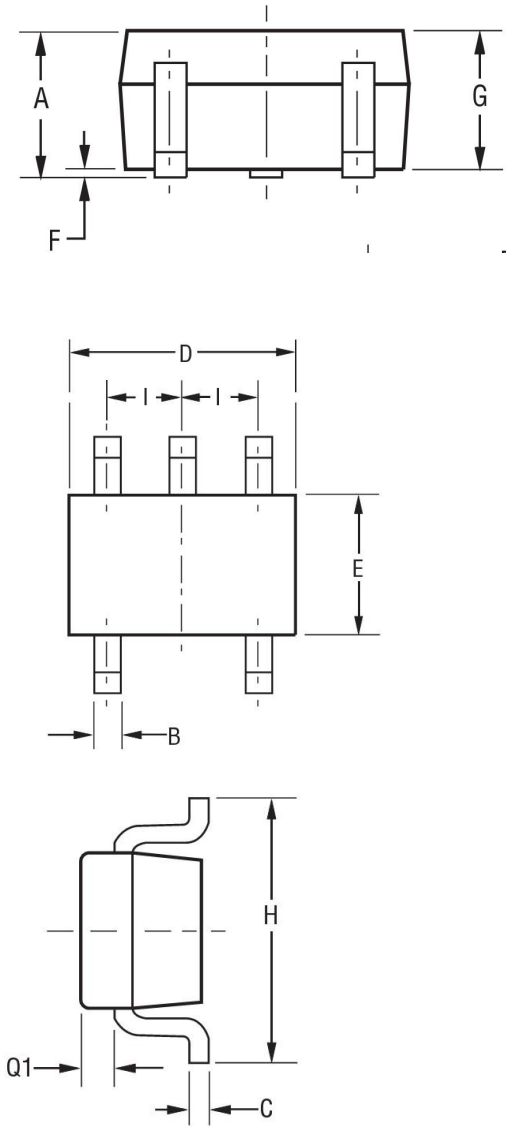


Figure 3- Peak Power Derating Curve



PACKAGE OUTLINE DIMENSIONS : **SOT - 353**



MM (INCHES)		
Dimension	**Min.**	**Max.**
A	0.80 (0.031)	1.10 (0.043)
B	0.15 (0.006)	0.30 (0.012)
C	0.10 (0.004)	0.18 (0.007)
D	1.80 (0.071)	2.20 (0.087)
E	1.15 (0.045)	1.35 (0.053)
F	-	0.10 (0.004)
G	0.80 (0.031)	1.00 (0.039)
H	1.80 (0.071)	2.40 (0.094)
I	TYP: 0.65 (0.026)	
Q1	0.10 (0.004)	0.40 (0.016)

Disclaimer

Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.

Users should verify actual device performance in their specific applications.