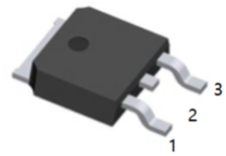
40V N-Channel MOSFET

Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Electronic ballast applications
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters

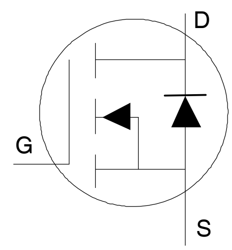


1.G 2.D 3.S

TO-252(DPAK) top view

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and dI/dt Capability
- Lead-Free
- RoHS Compliant containing no Lead, no Bromide, and no Halogen



- V_{DS}(V) =40V
- I_D =90A (V_{GS}= 10V)
- $R_{DS(ON)}$ <2.4mΩ (V_{GS} =10V)

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	180①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	125①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	90	
I_{DM}	Pulsed Drain Current ②	760	
P_D @T_C = 25°C	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	4.4	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	160	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑩	376	
I_{AR}	Avalanche Current ②	See Fig 15,16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ
$R_{\theta JC}$	Junction-to-Case ⑨	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	50	
$R_{\theta JA}$	Junction-to-Ambient ⑨	110	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			V	V_{GS} = 0V, I_D = 250μA ②
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		28		mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		1.9	2.4	mΩ	V_{GS} = 10V, I_D = 90A ⑤
			2.8		mΩ	V_{GS} = 6.0V, I_D = 50A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	V_{DS} = V_{GS}, I_D = 100μA
I_{DSS}	Drain-to-Source Leakage Current			1	μA	V_{DS} = 40V, V_{GS} = 0V
				150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage			-100		V_{GS} = -20V
R_G	Internal Gate Resistance		2.6		Ω	

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 90A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.04mH R_G = 50Ω, I_{AS} = 90A, V_{GS} =10V.

④ I_{SD} ≤ 100A, di/dt ≤ 1306A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

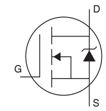
⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material).

⑨ R_θ is measured at T_J approximately 90°C.

⑩ Limited by T_{Jmax} starting T_J = 25°C, L= 1mH, R_G = 50Ω, I_{AS} = 27A, V_{GS} =10V.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	280			S	V_{DS} = 10V, I_D = 90A
Q_g	Total Gate Charge		89	134	nC	I_D =90A
Q_{gs}	Gate-to-Source Charge		26			V_{DS} =20V
Q_{gd}	Gate-to-Drain ("Miller") Charge		26			V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})		63			I_D = 90A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time		11		ns	V_{DD} = 20V
t_r	Rise Time		39			I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time		51			R_G = 2.7Ω
t_f	Fall Time		34			V_{GS} = 10V ⑤
C_{iss}	Input Capacitance		4610		pF	V_{GS} = 0V
C_{oss}	Output Capacitance		690			V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance		460			*ƒ* = 1.0 MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)		855			V_{GS} = 0V, V_{DS} = 0V to 32V ⑦ See Fig. 12
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)		1210			V_{GS} = 0V, V_{DS} = 0V to 32V ⑥
I_S	Continuous Source Current (Body Diode)			180①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②			760	A	
V_{SD}	Diode Forward Voltage		0.9	1.3	V	T_J = 25°C, I_S = 90A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time		34		ns	T_J = 25°C V_R = 34V,
			35			T_J = 125°C I_F = 90A
Q_{rr}	Reverse Recovery Charge		33		nC	T_J = 25°C di/dt = 100A/μs ⑤
			34			T_J = 125°C
I_{RRM}	Reverse Recovery Current		1.8		A	T_J = 25°C

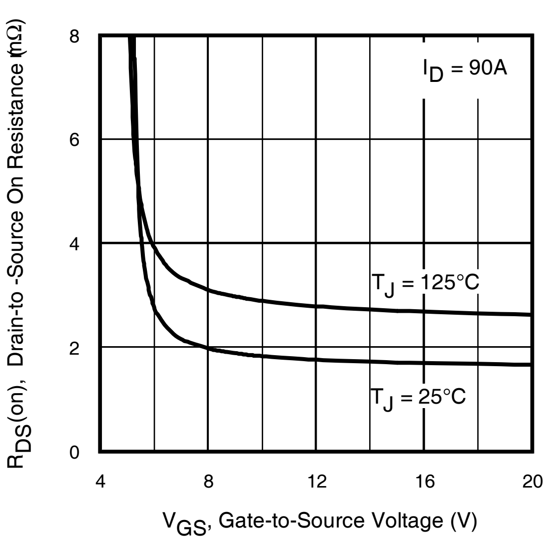


Fig 1. Typical On-Resistance vs. Gate Voltage

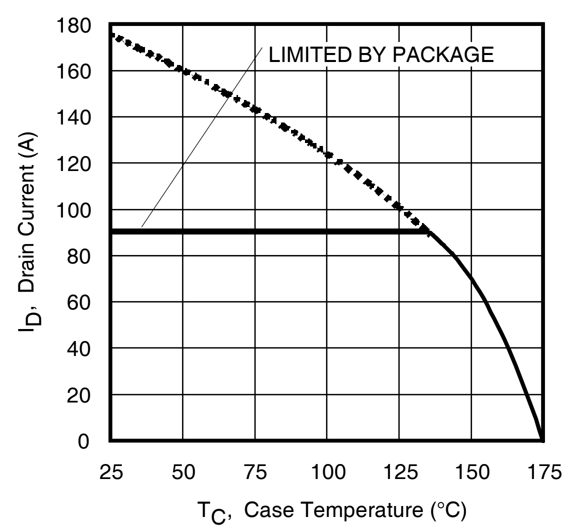


Fig 2. Maximum Drain Current vs. Case Temperature

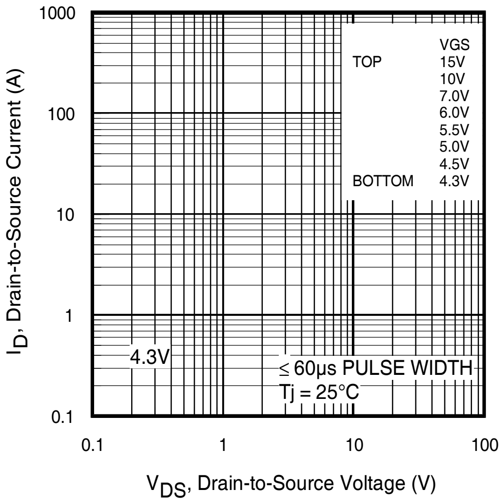


Fig 3. Typical Output Characteristics

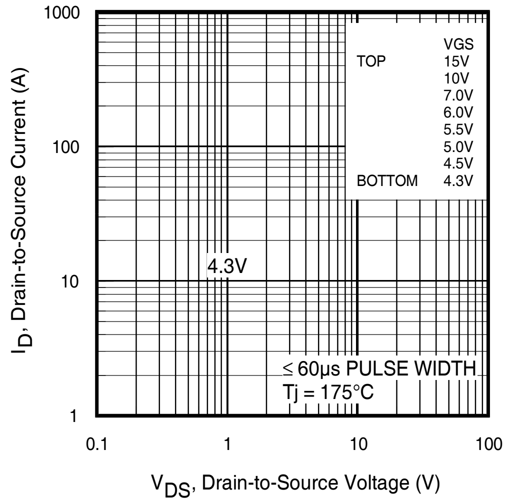


Fig 4. Typical Output Characteristics

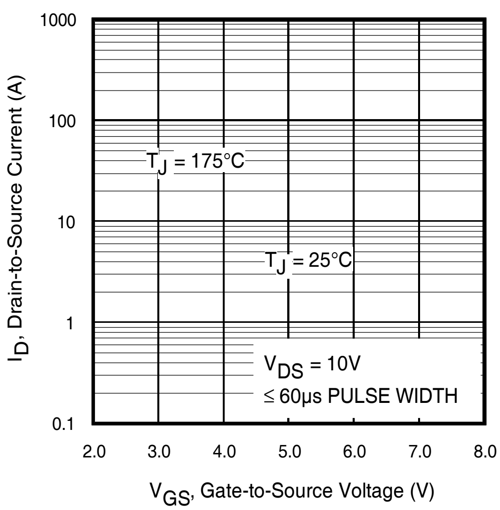


Fig 5. Typical Transfer Characteristics

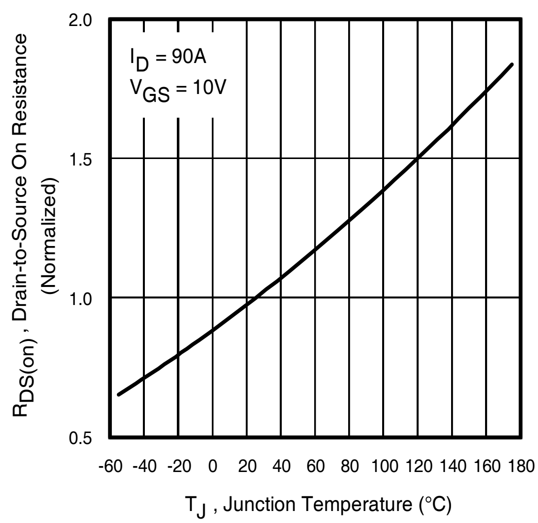


Fig 6. Normalized On-Resistance vs. Temperature

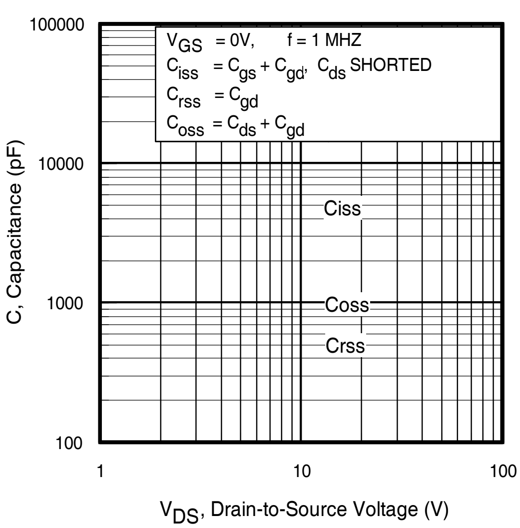


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

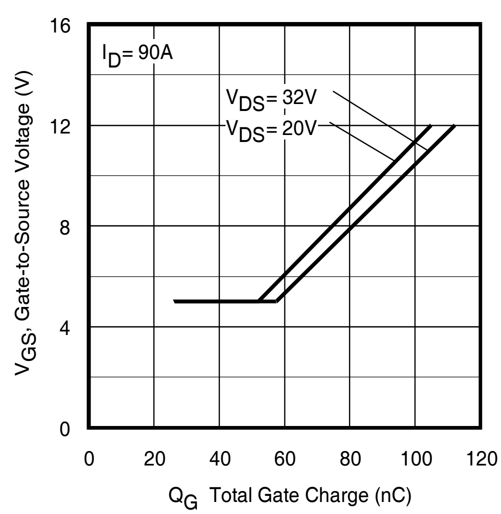


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

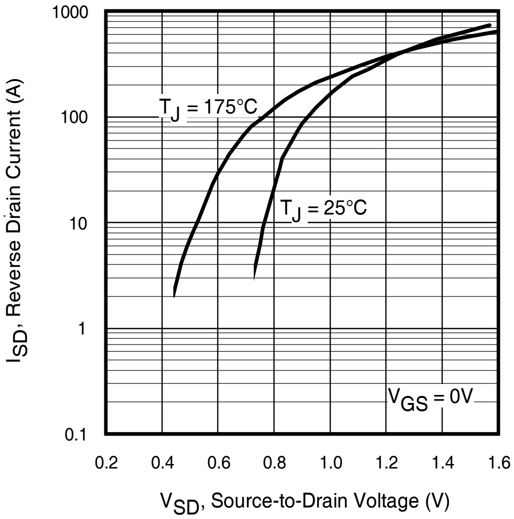


Fig 9. Typical Source-Drain Diode Forward Voltage

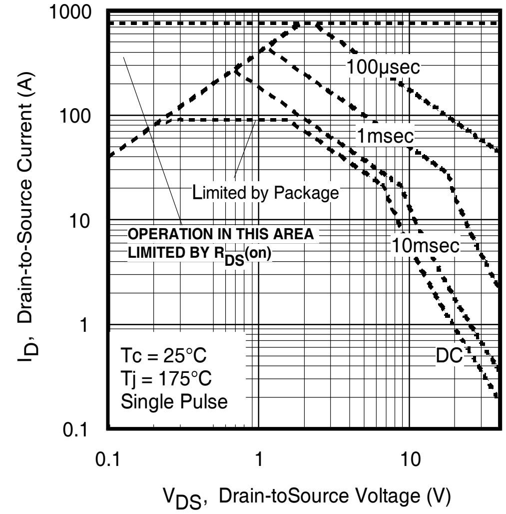


Fig 10. Maximum Safe Operating Area

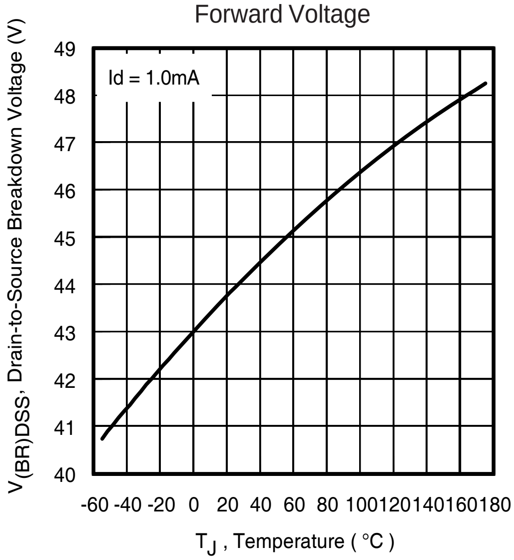


Fig 11. Drain-to-Source Breakdown Voltage

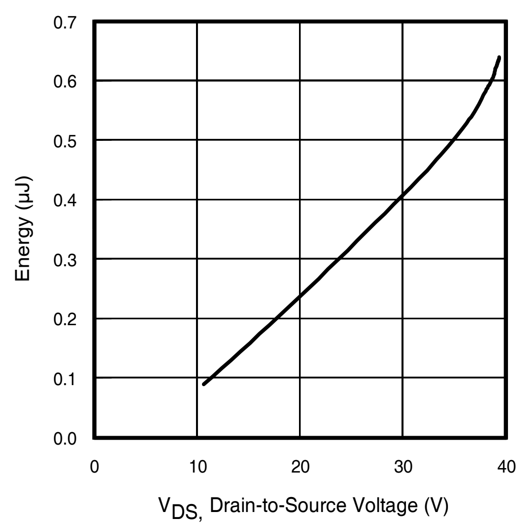


Fig 12. Typical C_{OSS} Stored Energy

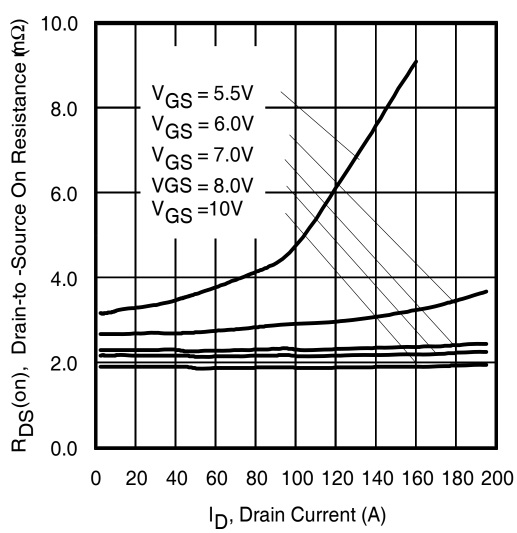


Fig 13. Typical On-Resistance vs. Drain Current

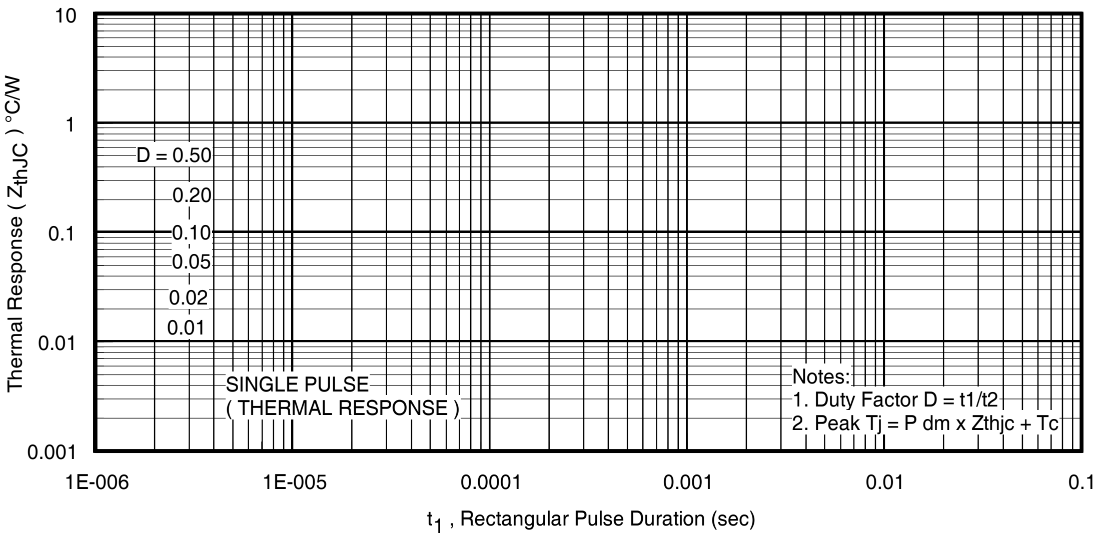


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

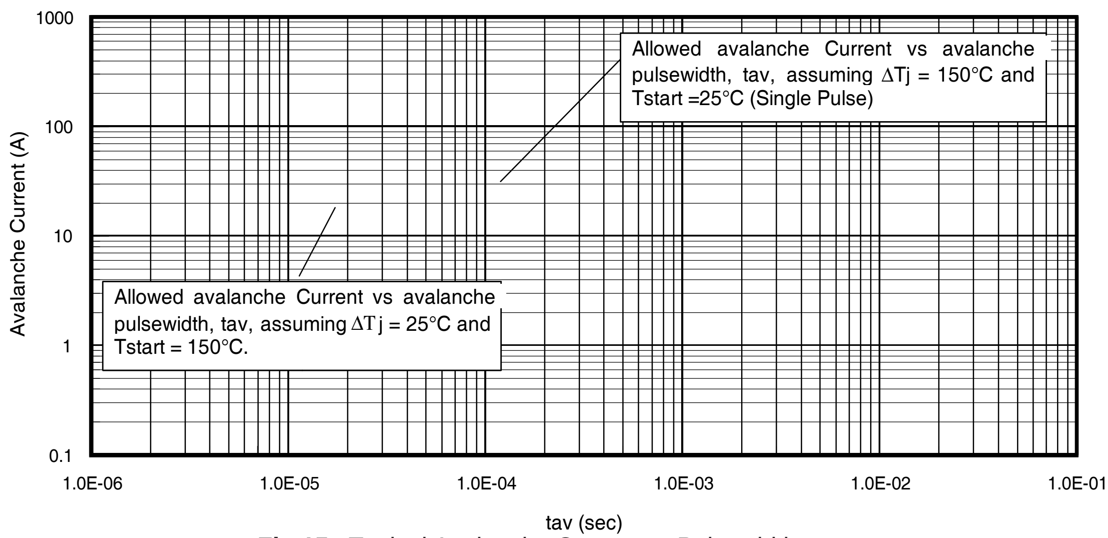


Fig 15. Typical Avalanche Current vs.Pulsewidth

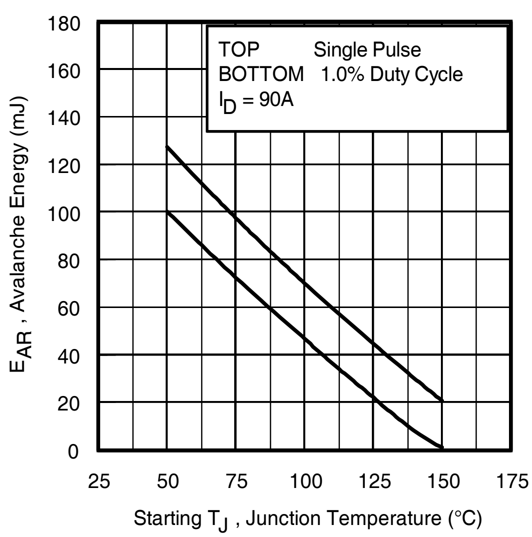


Fig 16. Maximum Avalanche Energy vs. Temperature

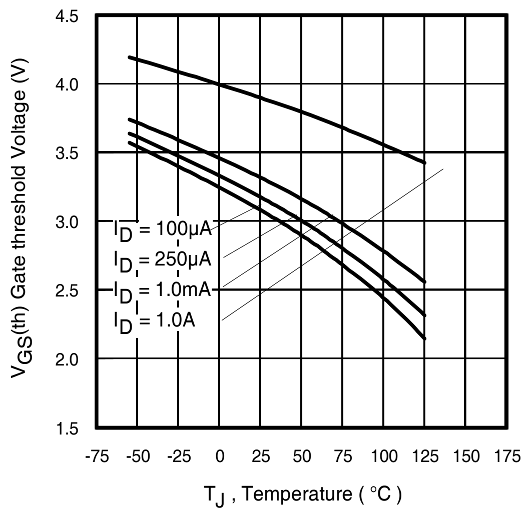


Fig 17. Threshold Voltage vs. Temperature

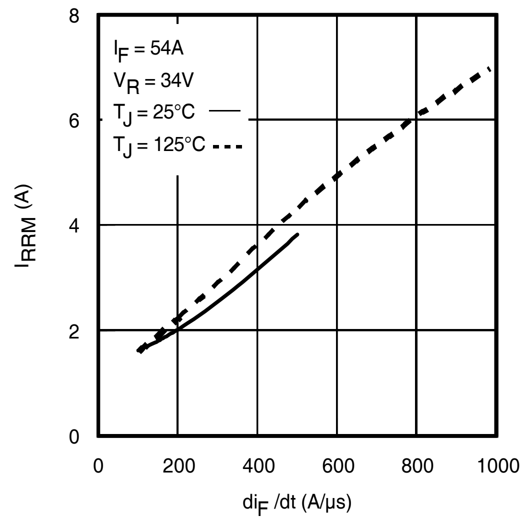


Fig. 18 - Typical Recovery Current vs. dir/dt

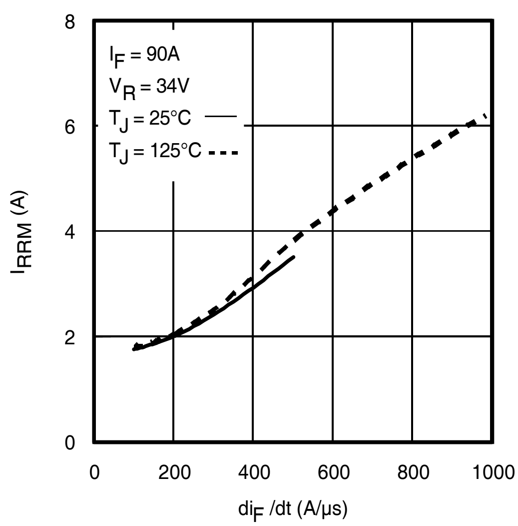


Fig. 19 - Typical Recovery Current vs. di/dt

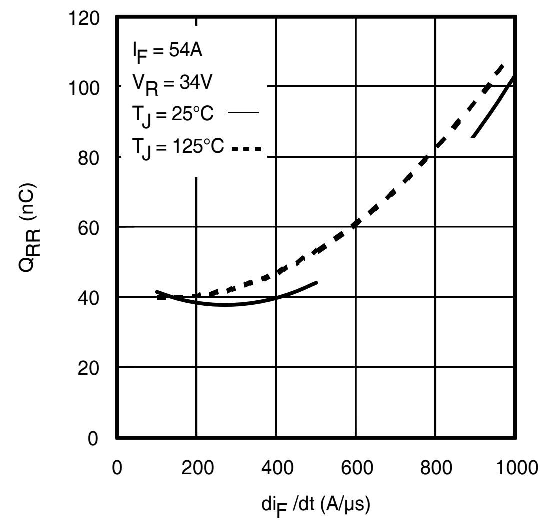


Fig. 20 - Typical Stored Charge vs. di/dt

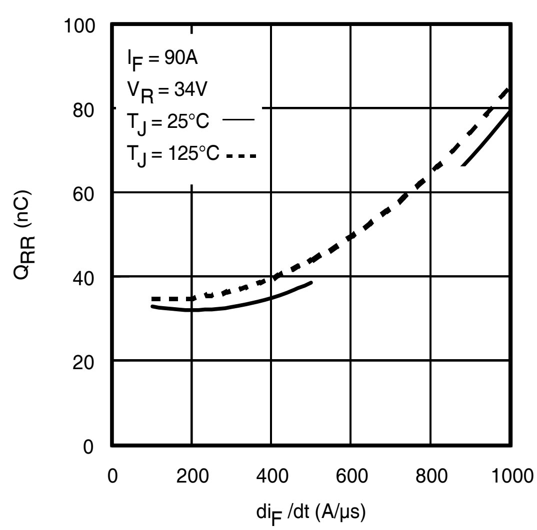
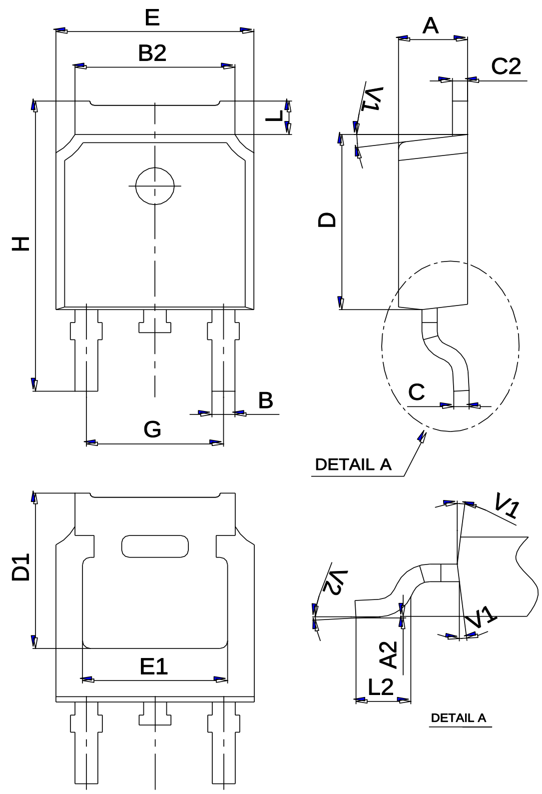
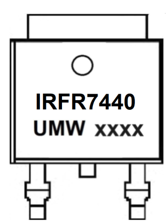


Fig. 21 - Typical Stored Charge vs. dir/dt

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRFR7440TR	TO-252	2500	Tape and reel