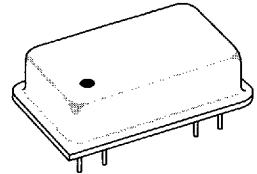


- Quartz Frequency Stability
- Excellent Jitter and Symmetry Performance
- Rugged, Hermetic Metal DIP Case

The HC1282 digital clock is designed for use with high speed CPUs operating at 66.6, 83.25, 111 or 166.5 MHz. The 333 MHz fundamental oscillation mode, made possible by surface acoustic wave (SAW) technology, provides low jitter, compact size, and low power consumption. The differential outputs are capable of driving CMOS, 100K ECL, ECLinPS™ and other logic families.

333.0 MHz Digital Clock



ABSOLUTE MAXIMUM RATINGS

Rating		Value	Units
Power Supply Voltage (Pin 1 to Case Ground)		0 to +8	VDC
Input Voltage (ENABLE, Pin 14)		0 to V _{CC}	VDC
Output Current (CLOCK, Pin 7 or $\overline{\text{CLOCK}}$, Pin 8)		50	mA
Case Temperature	Powered	0 to +70	°C
	Storage	-40 to +85	

ELECTRICAL CHARACTERISTICS

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Output Frequency	Absolute Frequency	F _O	1	332.9334	—	333.0666	MHz
	Relative to 333.000 MHz	ΔF _O		—	—	±200	ppm
Output (Enabled)	Output HIGH Voltage	V _{OH}	2	+3.98	—	+4.28	V
	Output LOW Voltage	V _{OL}		+3.05	—	+3.39	V
	Rise or Fall Time (20-80%)	t _r or t _f		—	480	—	ps
	Symmetry		3	45	—	55	%
Output (Disabled)	Period or Delay Jitter (rms)		4	—	1	—	ps
	Amplitude		5	—	70	150	mV _{P-P}
ENABLE Characteristics	Input HIGH Voltage	V _{IH}	2,5	+3.83	—	+4.28	V
	Input LOW Voltage	V _{IL}		+3.05	—	+3.53	V
	Input HIGH Current	I _{IH}		—	—	150	μA
	Input LOW Current	I _{IL}		0.5	—	—	μA
	Propagation Delay	t _{pd}	6	—	—	20	ns
DC Power Supply	Operating Voltage	V _{CC}	1,2	+4.75	+5	+5.25	VDC
	Operating Current	I _{CC}		—	85	110	mA
Operating Ambient Temperature		T _A	1	0	—	+70	°C

Lid Symbolization (YY = year, WW = week number)

RFM HC1282 333 MHz YYWW

1. Unless noted otherwise, all specifications apply with CLOCK and $\overline{\text{CLOCK}}$ terminated in 50 Ω to +3.0 VDC per the specified test fixture for any combination of V_{CC} and T_A within the specified operating ranges.
2. Input/output voltage limits apply only for V_{CC} = 5.00 ±0.01 VDC. Additional V_{CC} variation (within specification) must be added to these limits.
3. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of CLOCK and $\overline{\text{CLOCK}}$.
4. Applies to delay jitter between CLOCK and $\overline{\text{CLOCK}}$ after 20 cycles and to period jitter of $\overline{\text{CLOCK}}$ or CLOCK. Measurements are made with the Tektronix CSA803 communications signal analyzer with at least 1000 samples. Jitter induced by electrical noise on the V_{CC} input or mechanical vibration is not included. Dedicated external voltage regulation and careful PCB layout are recommended for minimum jitter.
5. The output is disabled (with CLOCK at logic HIGH) for ENABLE at logic HIGH and enabled for ENABLE at logic LOW or unterminated.
6. Propagation delay is defined as the time from the 50% point of ENABLE to the 50% point of the leading edge of the first pulse or the trailing edge of the last pulse. The minimum width of the first or last pulse is not specified.
7. The design, manufacturing process, and specifications of this device are subject to change without notice.
8. One or more of the following U. S. patents apply: 4,616,197, 4,670,681, and 4,760,352.
9. ECLinPS™ is a trademark of Motorola, Inc. RFM® is a registered trademark of RF Monolithics, Inc.
10. CAUTION: ELECTROSTATIC SENSITIVE DEVICE. Observe precautions for handling.



HC1282.CHP-A-01-101194AC ⚡HCSVBACK.CHP ©1994 RF Monolithics, Inc.

7493828 0000509 087