Low Noise Quasi-Resonant Control DC/DC converter IC for AC/DC Converter

BD7682FJ-LB BD7683FJ-LB BD7684FJ-LB BD7685FJ-LB

General Description

This is the product guarantees long time support in the Industrial market.

BD768xFJ series is a Quasi-resonant controller type DC/DC converters that provide an optimum system for all products that include an electrical outlet. Quasi-resonant operation enables soft switching and helps to keep EMI low. Design with a high degree of flexibility is achieved with switching MOSFETs and current detection resistors as external devices.

The built-in brown out function monitors the input voltage as part of system optimization. The burst mode function reduces input power at low power.

BD768xFJ series include various protection functions, such as a soft start function, burst function, per-cycle over-current limiter function, overvoltage protection function, overload protection function, and brown out function.

BD768xFJ series include a gate-clamp circuit for optimal driving SIC-MOSFET.

Features

- Pin 8 : SOP-J8 Package (6.00mm × 4.90mm : 1.27mm pitch <TYP>)
- Quasi-resonant type (low EMI)
- Frequency reduction mode
- Low current consumption (19μA), during standby
- Low current consumption when no load (burst operation when light load)
- Maximum frequency (120kHz)
- CS Pin Leading-Edge Blanking
- VCC UVLO (Under Voltage Drop Out protection)
- VCC OVP (Over Voltage Protection)
- Per-cycle over-current protection circuit
- Soft start
- ZT trigger mask function
- Voltage protection function (brown out)
- ZT OVP (Over Voltage Protection)
- Gate-clamp circuit

Key Specifications

- Operating Power Supply Voltage Range: VCC 15.0V to 27.5V
- Normal Operating Current: 0.80mA(Typ)
- Burst Operating Current: 0.50mA(Typ)
- Maximum Frequency: 120kHz(Typ)
- Operating Temperature: -40°C to +105°C

Package 4.90mm x 6.00mm x 1.65mm pitch 1.27mm
(Typ.) (Typ.) (TYP.) (TYP.)

SOP-J8
4.90mm x 6.00mm x 1.65mm

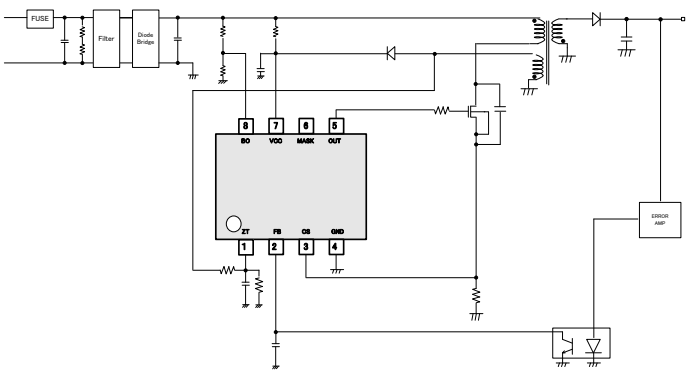
Lineup

	FBOLP	VCCOVP
BD7682FJ	AutoRestart	Latch
BD7683FJ	Latch	Latch
BD7684FJ	AutoRestart	AutoRestart
BD7685FJ	Latch	AutoRestart

Applications

Industrial equipment, AC Adaptor, Household appliances

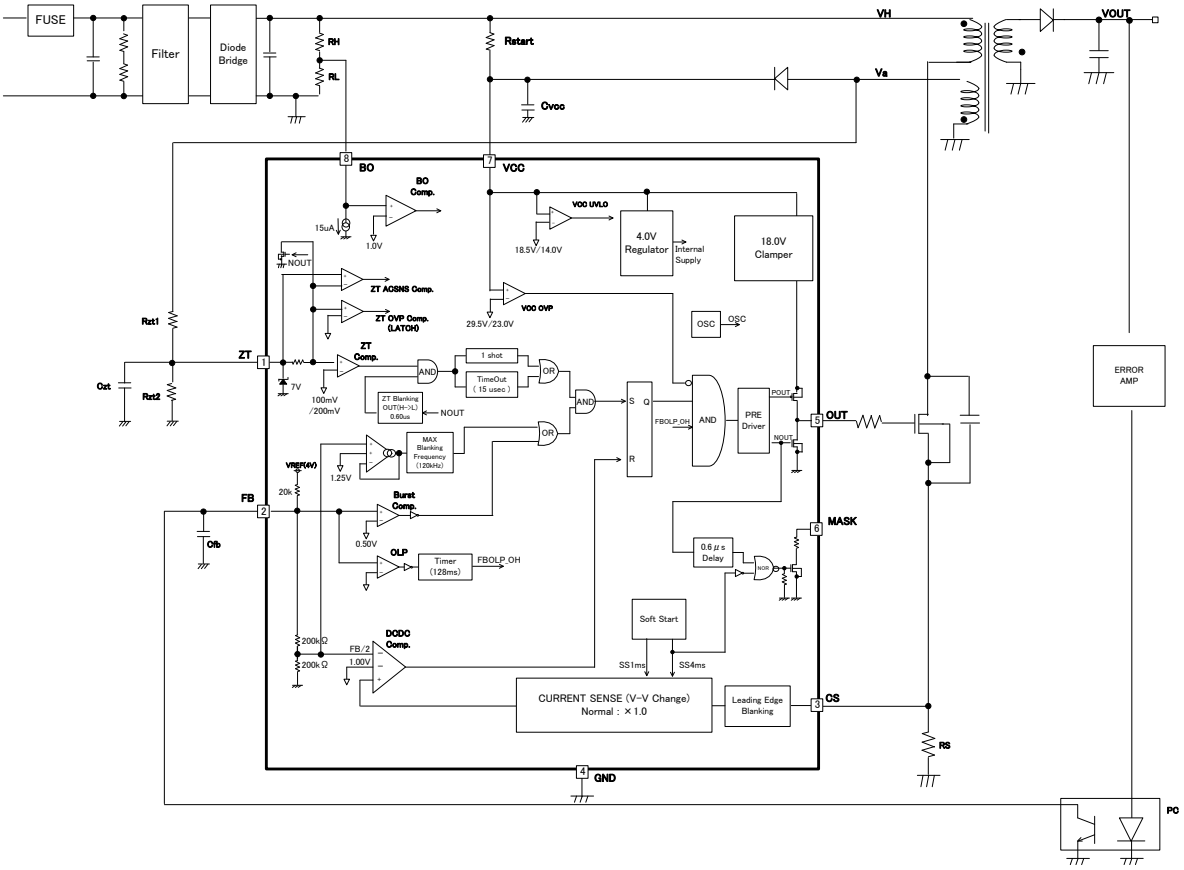
Typical Application Circuit



Pin Descriptions

No.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	ZT	I	Zero Current Detect pin	-	✓
2	FB	I	Feedback signal input pin	✓	✓
3	CS	I	Current Sense pin	✓	✓
4	GND	I/O	GND pin	✓	-
5	OUT	O	MOSFET drive pin	✓	✓
6	MASK	O	External TR drive	-	✓
7	VCC	I	Power Supply pin	-	✓
8	BO	O	Brown IN/OUT monitor pin	-	✓

Block Diagram



Absolute Maximum Ratings (Ta= 25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{max1}	-0.3 to +32.0	V	OUT, VCC, MASK
Maximum Applied Voltage 2	V_{max2}	-0.3 to +6.5	V	ZT, CS, FB, BO
Maximum Applied Voltage 3	V_{max3}	-0.3 to +25.0	V	OUT
ZT Pin Maximum Current1	I_{SZT1}	-3.0	mA	
ZT Pin Maximum Current2	I_{SZT2}	3.0	mA	
Power Dissipation	P_d	0.67 (Note1)	W	
Operating Temperature Range	T_{opr}	-40 to +105	°C	
MAX Junction Temperature	T_{jmax}	150	°C	
Storage Temperature Range	T_{str}	-55 to +150	°C	

(Note1) SOP-J8 : When mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate)
De-rated by 5.4mW/°C when operating above Ta=25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Power Supply Voltage Range	V_{CC}	15.0 to 27.5	V	VCC pin voltage

Electrical Characteristics (unless otherwise noted, Ta = 25 °C, V_{CC}= 24 V)

Parameter	Symbol	Specifications			Unit	Conditions
		MIN	TYP	MAX		
[Circuit Current]						
Circuit Current (OFF)	I_{OFF}	10	19	30	µA	V_{CC}=18.0V (VCC UVLO=Disable)
Circuit Current (ON) 1	I_{ON1}	300	800	1500	µA	FB=1.0V (at pulse operation)
Circuit Current (ON) 2	I_{ON2}	150	500	1000	µA	FB=0.0V (at burst operation)
Circuit Current (Protect circuit is on)	$I_{protect}$	800	1600	2200	µA	FBOLP,VCCOVP,ZTOVP
[Brown Out Block (B.O.)]						
B.O. Detection Voltage	V_{BO}	0.920	1.000	1.080	V	
B.O. Detection Hysteresis Current	I_{BO}	10	15	20	µA	
[VCC Pin Protection Functions]						
VCC UVLO Voltage 1	V_{UVLO1}	19.00	19.50	20.00	V	VCC rise
VCC UVLO Voltage 2	V_{UVLO2}	13.00	14.00	15.00	V	VCC fall
VCC UVLO Hysteresis	V_{UVLO3}	-	5.50	-	V	V_{UVLO3}= V_{UVLO1}-V_{UVLO2}
VCC OVP Voltage 1	V_{OVP1}	27.50	29.50	31.50	V	VCC rise
VCC OVP Voltage 2	V_{OVP2}	21.00	23.00	25.00	V	VCC fall
VCC OVP Hysteresis	V_{OVP3}	-	6.50	-	V	V_{OVP3}= V_{OVP1}-V_{OVP2}
Latch Release Voltage	V_{LATCH}	-	V_{UVLO2}-3.5	-	V	VCC voltage
Latch Mask Time	t_{LATCH}	50	150	250	µs	

Electrical Characteristics – continued (unless otherwise noted, Ta = 25 °C, V_{CC}=24 V)

Parameter	Symbol	Specifications			Unit	Conditions
		MIN	TYP	MAX		
[DCDC Converter Block (Turn OFF)]						
FB Pin pull-up Resistance	R_{FB}	15	20	25	kΩ	
CS Over-Current Sensor Voltage 1A	V_{LIM1A}	0.950	1.000	1.050	V	FB=2.2V (I_{ZT}>-1mA)
CS Over-Current Sensor Voltage 1B	V_{LIM1B}	0.620	0.700	0.780	V	FB=2.2V (I_{ZT}<-1mA)
CS Over-Current Sensor Voltage 2A	V_{LIM2A}	0.200	0.300	0.400	V	FB=0.6V (I_{ZT}>-1mA)
CS Over-Current Sensor Voltage 2B	V_{LIM2B}	0.140	0.210	0.280	V	FB=0.6V (I_{ZT}<-1mA)
CS Switching ZT Current	I_{ZT}	0.900	1.000	1.100	mA	
CS Leading Edge Blanking Time	t_{LEB}	-	0.250	-	µs	
Minimum ON Width	t_{MIN}	-	0.500	-	µs	
[DCDC Converter Block (Turn ON)]						
Maximum Operating Frequency 1	f_{SW1}	106	120	134	kHz	FB=2.0V
Maximum Operating Frequency 2	f_{SW2}	20	30	40	kHz	FB=0.5V
Frequency Reduction Start FB Voltage	V_{FBSW1}	1.100	1.250	1.400	V	
Frequency Reduction End FB Voltage 1	V_{FBSW2}	0.400	0.500	0.600	V	
Frequency Reduction End FB Voltage 2	V_{FBSW3}	-	0.550	-	V	
Voltage Gain	AV_{CS}	1.700	2.000	2.300	V/V	$\Delta V_{FB}/\Delta V_{CS}$
ZT Comparator Voltage 1	V_{ZT1}	60	100	140	mV	ZT fall
ZT Comparator Voltage 2	V_{ZT2}	120	200	280	mV	ZT rise
ZT Trigger Mask Time	t_{ZTMASK}	0.25	0.60	0.95	µs	For noise prevention after OUT H ⇒L
ZT Trigger Timeout Period 1	t_{ZTOUT}	8.0	15.0	24.0	µs	Count from final ZT trigger (1-stage)
ZT Trigger Timeout Period 2	t_{ZTOUT2}	2.0	5.0	8.0	µs	Count from final ZT trigger (2-stage)
Maximum ON Time	t_{ZTON}	27.0	45.0	62.0	µs	
[DCDC Protection Functions]						
Soft Start Time 1	t_{SS1}	0.600	1.000	1.400	ms	
Soft Start Time 2	t_{SS2}	2.400	4.000	5.600	ms	
FB OLP Voltage 1	V_{FOLP1}	2.500	2.800	3.100	V	FB rise
FB OLP Voltage 2	V_{FOLP2}	2.300	2.600	2.900	V	FB fall
FB OLP Timer	t_{FOLP}	90	128	166	ms	
ZT OVP Voltage	V_{ZTL}	3.250	3.500	3.750	V	
[OUT Pin]						
OUT Pin Clamp Voltage	V_{OUT}	16.00	18.00	20.00	V	
OUT pin Nch MOS Ron	R_{NOUT}	2.0	4.5	9.0	Ω	
[MASK Pin]						
MASK Pin Delay Time	t_{MASK}	0.25	0.60	0.95	µs	
MASK Pin Ron	R_{MASK}	20	50	80	Ω	

Application Information

Description of Blocks

(1) Start-Up sequences (FBOLP:auto recovery mode)
The BD768xFJ's start up sequence is shown in Figure 1.
See the sections below for detailed descriptions.

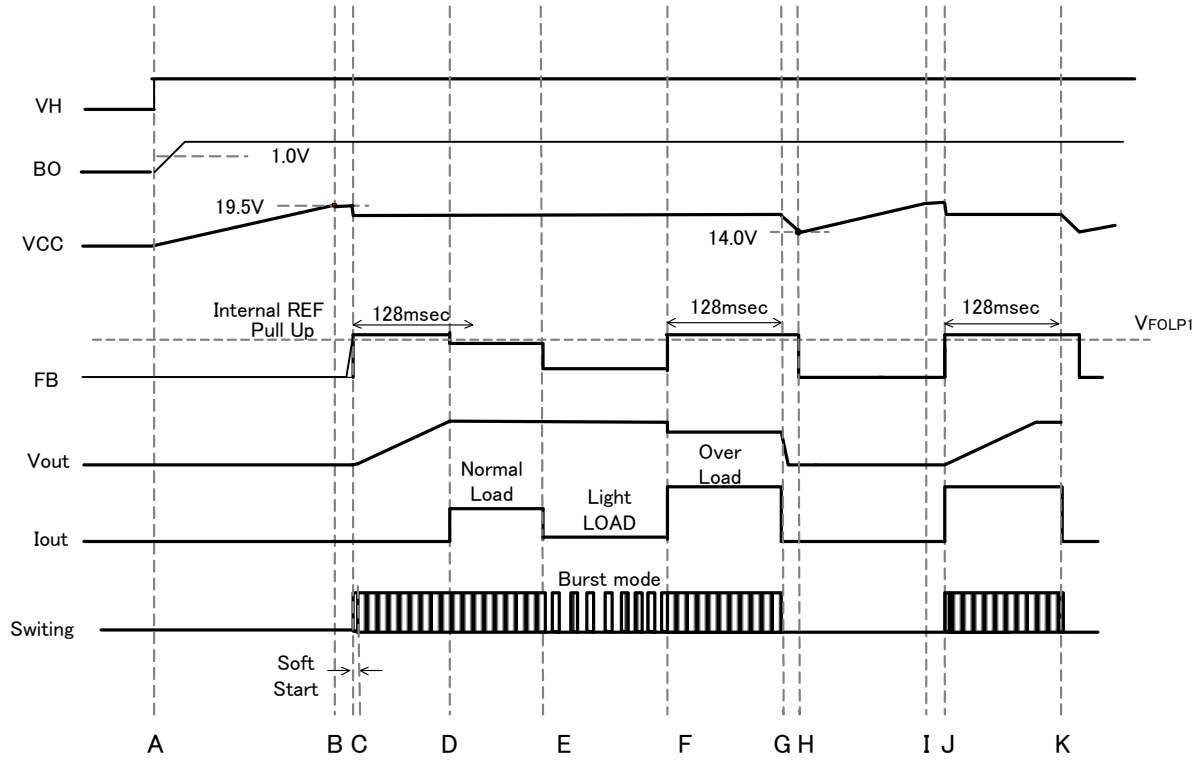


Figure 1. Start-up Sequence Timing Chart

A: Input voltage VH is applied
B: VCC pin voltage rises due to start resistor R_{START}, and this IC starts operating when VCC > V_{UVLO1} (19.5V typ).
Switching starts when the status of the brown out function is normal (BO > 1.0 V), other protection functions are also considered normal. At that time, the VCC value always drops due to the pin's consumption current, so V_{CC} > V_{UVLO2} (14.0 V typ) should be set.
C: There is a soft start function which regulates the voltage level at the CS pin to prevent a rise in voltage and current.
D: When the switching operation starts, V_{OUT} rises.
Once the output voltage starts, set the rated voltage to within the T_{FOLP} period (128ms typ).
E: When there is a light load, burst operation is order to keep power consumption down.
F: Overload operation.
G: When the FB pin voltage keeps FB > V_{FOLP1} (=2.8V typ) at or above T_{FOLP} (128ms typ), switching is stopped by the overload protection circuit.
If the FB pin voltage status becomes FB < V_{FOLP2} even once, the IC's internal 128ms timer is reset.
H: If the VCC voltage drops to VCC < V_{UVLO2} (14.0V typ) or below, restart is executed.
I: The IC's circuit current is reduced and the VCC pin value rises. (Same as B)
J: Same as F
K: Same as G

Start resistance R_{START} is the resistance required to start the IC.
When the start resistance R_{START} value is reduced, standby power is increased and the startup time is shortened.
Conversely, when the start resistance R_{START} value is increased, standby power is reduced and the startup time is lengthened.
When BD768xFJ is in standby mode, current I_{OFF} becomes 30µA Max
However, this is the minimum current required to start the IC. Use the appropriate current for the set target.

Example: Start Resistance R_{START} Setting
$R_{START} = (V_{MIN} - V_{UVLO}(max)) / I_{OFF}$
When V_{AC} = 100 V, if the margin is -20%, then V_{MIN} = 113V
Since V_{UVLO1} (max) = 20.0V,
And since R_{START} < (113-20) / 30µA = 3.10 MΩ, the start resistance is 3.0MΩ. (Set according to the start time.)
In this case: R_{START} power consumption $Pd(R_{START}) = (V_H - V_{CC})^2 / R_{START} = (141V - 14V)^2 / 3.0M = 5.4mW$

(2) Brown Out function (B.O.)

BD768xFJ has a built-in brown out function. When the input VH value is low, the brown out function stops the DC/DC operations (The IC itself continues to operate). An example is shown in Figure 2. The input voltage which is resistance-divided is inputted to the BO pin. If the BO pin value exceeds V_{BO} (1.0 V typ), the circuit detects as normal state, and DCDC operations are started. There is a current hysteresis I_{BO} in the circuit.

The current hysteresis flow is described below.

- BO < V_{BO} (1.0 V typ) (abnormal) I_{BO} with sync
- BO≧V_{BO} (1.0 V typ) (normal status) I_{BO} without sync

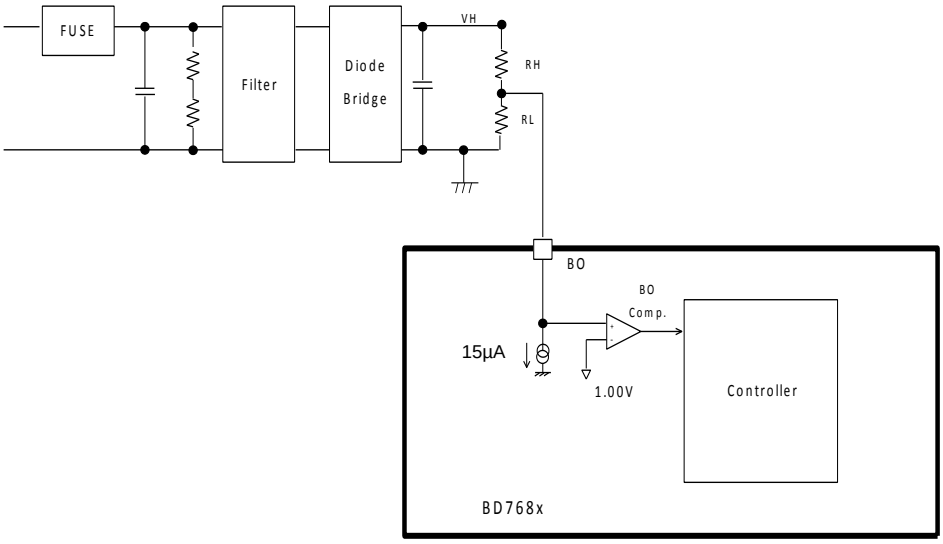


Figure 2. Block Diagram of Brown Out Function

Example: R_H and R_L Setting

In the following example, V_{HON} is the operation start V_H voltage (L to H), and V_{HOFF} is the operation stop V_H voltage (H to L).

IC operation start (OFF => ON) $(V_{HON}\text{-}1.0) / R_H = 1.0/R_L + 15*10e\text{-}6$

IC operation stop (ON => OFF) $(V_{HOFF}\text{-}1.0) / R_H = 1.0/R_L$

Based on the above, R_H and R_L can be calculated as follows.

$R_H = (V_{HON} - V_{HOFF}) / (15 * 10e-6)$, $R_L = 1.0 / (V_{HOFF} - 1.0) * R_H$

Example 1: When using 100 V AC (140 V DC)

When R_H = 2350kΩ and R_L = 34kΩ, V_{HON} = 105.8V (-25%) and V_{HOFF} = 70.8V (-51%)

Current consumption is 8.0mW for both R_H and R_L.

Example 2: When using 230V AC (322V DC)

R_H = 5200kΩ, R_L = 42kΩ

V_{HON} = 202.8V (-37%), V_{HOFF} = 124.8V (-62%)

Current consumption is 20.1 mW for both R_H and R_L.

(3) VCC Pin Protection Function

BD768xFJ includes the VCC low voltage protection function VCC UVLO (Under Voltage Protection) and the VCC over voltage protection function VCC OVP (Over Voltage Protection). These functions prevent abnormal voltage-related damage in MOSFETs used for switching.

The VCC UVLO function uses an auto recovery type comparator with voltage hysteresis and the VCC OVP function uses latch mode or auto recovery.

After latch function is detected by VCCOVP, latching is released (reset) when the condition V_{CC}< V_{LATCH} (typ= V_{UVLO2} -3.5V) is met.

This operation is shown in Figure 3.

VCCOVP has a built-in mask time t_{LATCH} (typ = 150 µs).

This function masks any surges, etc., that occur at the pin.

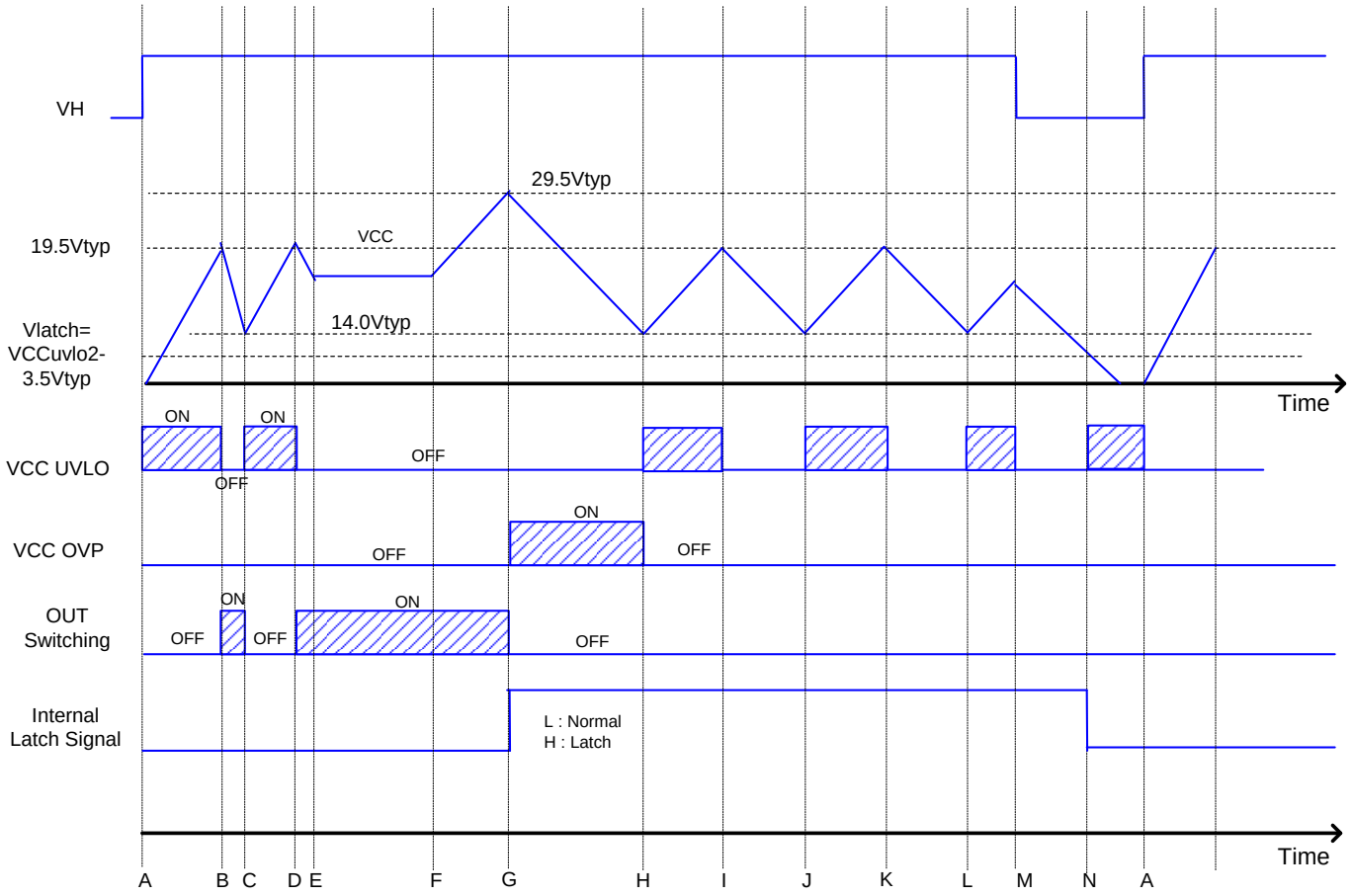


Figure 3. VCC UVLO / OVP (Latch Mode)

A: VH is applied, VCC voltage rises
B: When VCC > V_{UVLO1}, DC/DC operation starts.
C: When VCC < $V_{UVLO2,}$ DC/DC operation stops.
D: When VCC > V_{UVLO1}, DC/DC operation starts.
E: VCC voltage drops until DC/DC operation starts.
F: VCC rises.
F: When VCC > $V_{OVP1,}$ DC/DC operation stops (latch mode). Switching is stopped by an internal latch signal.
G: When DC/DC operation stops, power supply from the auxiliary coil stops and VCC voltage drops.
H: When VCC < V_{UVLO2}, VCC voltage rises because IC current consumption drops.
I: When VCC > V_{UVLO1}, latching occurs and so there are no DC/DC operations. VCC voltage drops because IC current consumption is lowered.
K: Same as H
L: Same as I
M: VH is OPEN (unplugged). VCC drops.
N: When VCC < $V_{LATCH,}$ latch is released.

(4) DCDC Converter Function

BD768xFJ uses PFM (Pulse Frequency Modulation) mode control.
The FB pin, ZT pin, and CS pin are all monitored to provide a system optimized for DC/DC.
The switching MOSFET ON width (turn OFF) is controlled via the FB pin and CS pin, and the OFF width (turn ON) is controlled via the ZT pin.
PFM mode sets the maximum frequency to meet noise standards.
A detailed description appears below. (See Figure 4)

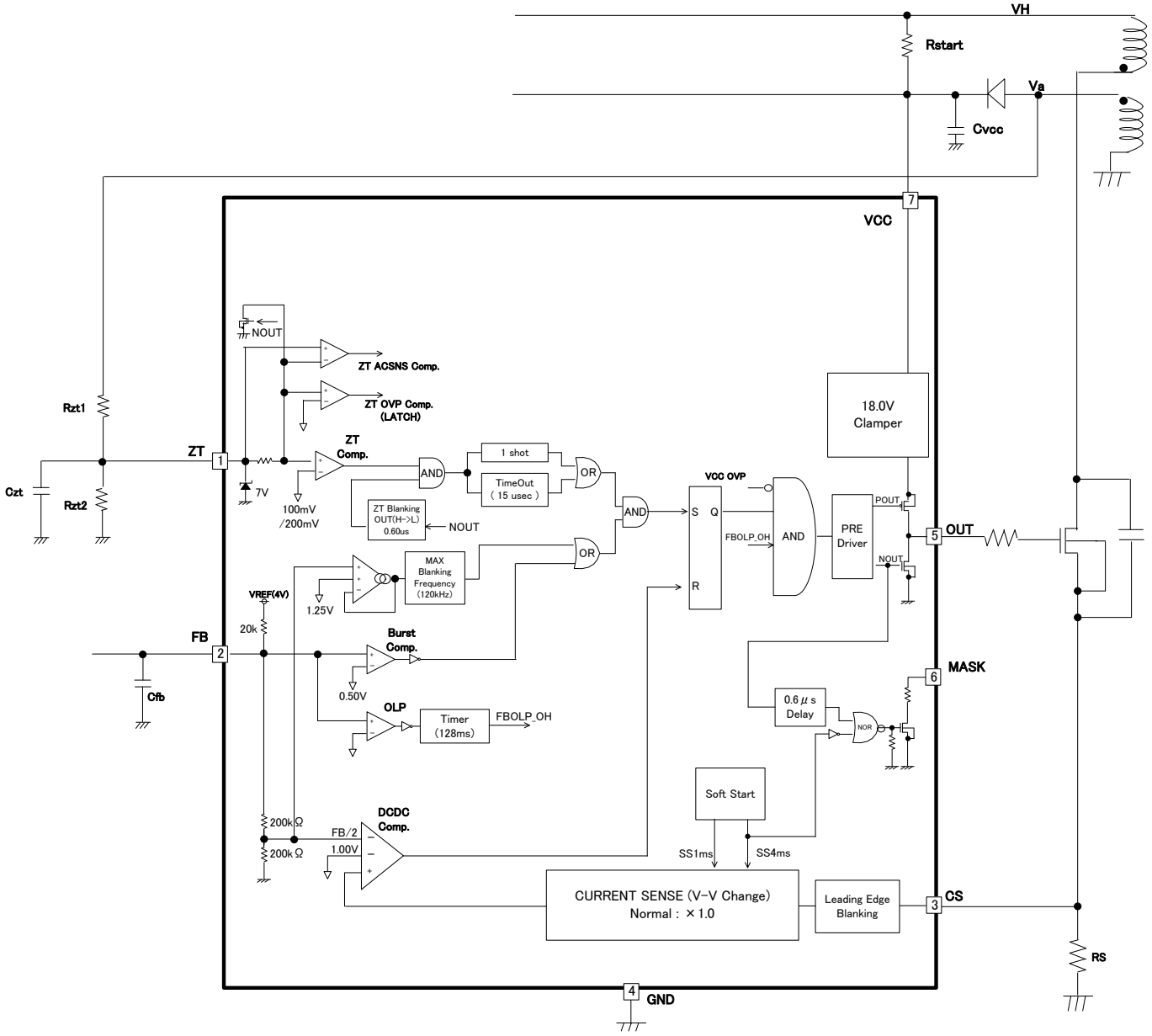


Figure 4. Block Diagram of DC/DC Operations

(a) Determination of ON Width (Turn OFF)
ON width is controlled via the FB pin and CS pin.
The ON width is determined by comparing FB pin voltage at 1/ AV_{CS} (typ = 1/2) with the CS pin voltage.
In addition, it is compared with the IC's internally generated V_{LIM1A} (1.0V typ) voltage and the comparator level changes linearly, as is shown in Figure 5.
The CS pin is also used for the per-pulse over-current limiter circuit.
Changes at the FB pin result in changes in the maximum blanking frequency and over-current limiter level.

- mode1: Burst operation
- mode2: Frequency reduction operation (reduces maximum frequency)
- mode3: Maximum frequency operation (operates at maximum frequency)
- mode4: Overload operation (pulse operation is stopped when overload is detected)

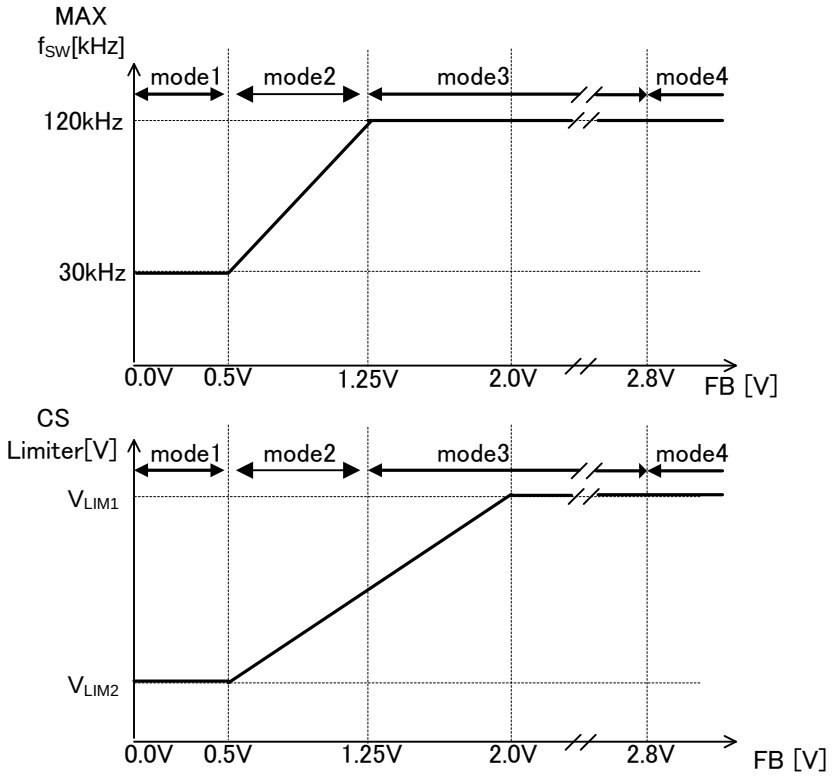


Figure 5. Relationship of FB Pin to Over-Current Limiter and Maximum Frequency

The over-current limiter level is adjusted for soft start function (section 5) and over-current protection of the input voltage compensation (section 4 (c))
In this case, the V_{LIM1} and V_{LIM2} values are as listed below.

Table 1 Over-Current Protection Voltage

Soft Start	I_{ZT} ≥ -1.0mA		I_{ZT} < -1.0mA	
	V_{LIM1}	V_{LIM2}	V_{LIM1}	V_{LIM2}
Start to 1ms	0.250V (25.0%)	0.063V (6.0%)	0.175V (17.5%)	0.047V (4.5%)
1ms to 4ms	0.500V (50.0%)	0.125V (12.0%)	0.350V (35.0%)	0.094V (9.0%)
>4ms	1.000V (100.0%)	0.250V (25.0%)	0.700V (70.0%)	0.188V (18.8%)

(Note) Values in parentheses are relative values when compared to V_{LIM1} (1.0V typ) during I_{ZT} ≥ -1.0mA.

(b) LEB (Leading Edge Blanking) Function
When the switching MOSFET is turned ON, surge current occur at each capacitor component and drive current. Therefore, when the CS pin voltage rises temporarily, detection errors may occur in the over-current limiter circuit.
To prevent detection errors, BD768xFJ has the blanking function. This function masks the CS voltage for T_{LEB} (typ = 250ns) after the OUT pin changes from low to high.
This blanking function reduces CS pin filter.

(c) CS Over-Current Protection Switching Function

When the input voltage (VH) becomes high, the ON time is shortened and the operating frequency increases. As a result, the maximum rated power is increased for a certain over-current limiter. As a countermeasure, switching is performed by the IC's internal over-current protection function.

When at high voltage, the over-current comparator value which determines the ON time is always multiplied by 0.7.

Detection is performed by monitoring the ZT inflow current and then switching.

When the MOSFET is turned ON, Va becomes a negative voltage dependent upon the input voltage (VH). The ZT pin is clamped to nearly 0V in the IC.

The formula used to calculate this is shown below. A block diagram is shown in Figure 6. Also, graphs are shown in Figure 7, Figure 8 and Figure 9.

$$I_{ZT} = (Va - V_{\backslash ZT}) / R_{ZT1} = Va / R_{ZT1} = V_H * Na / Np / R_{ZT1}$$

$$R_{ZT1} = Va / I_{ZT}$$

Therefore, the VH voltage is set with a resistance value (R_{ZTL}). The ZT bottom detection voltage has now been determined, so C_{ZT} should be used to set the timing.

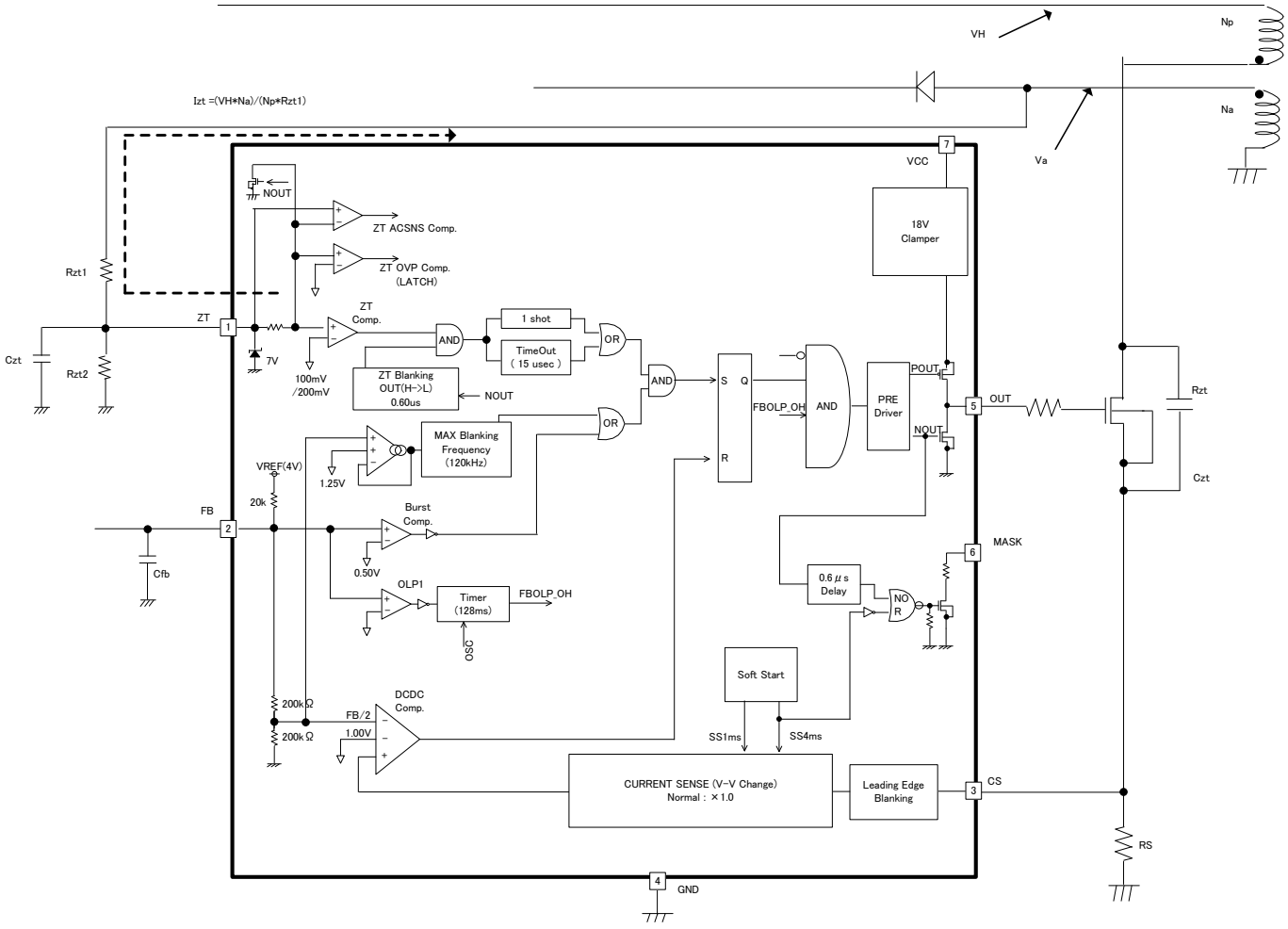


Figure 6. Block Diagram of CS Switching Current

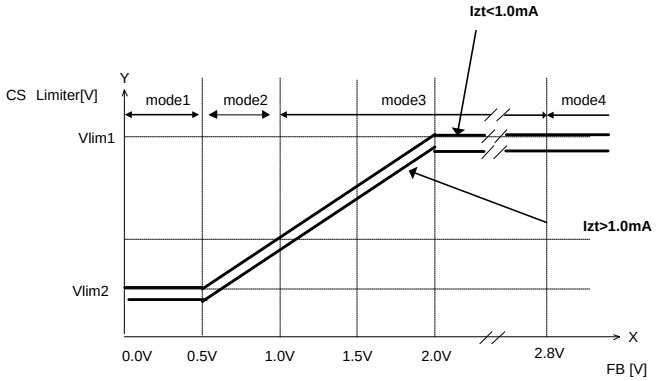


Figure 7. CS Switching: FB Voltage vs CS Voltage

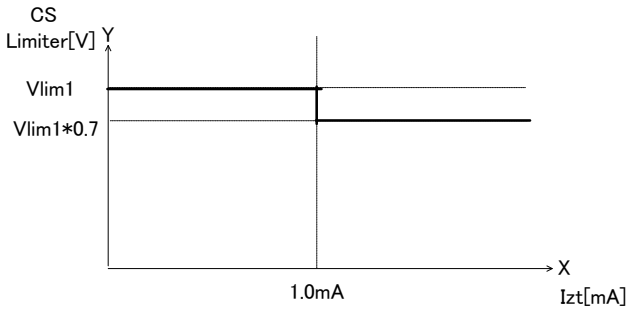


Figure 8. CS Switching: ZT Current vs CS Voltage

Example: Setup method (for switching between 100-V AC and 220-V AC.)
100-V AC: 141V ±42V (±30% margin)
220-V AC: 308V ±62V (±20% margin)

In the above cases, the CS current is switched in the range from 182V to 246V. This is done when => VH = 214 VH.

Given: Np = 100, Na = 15.

$$Va = V_{IN} * Na / Np = 214V * 15 / 100 * (-1) = -32.1V$$

$$R_{ZC} = Va / I_{ZT} = -32.1V / -1mA = 32.1k\Omega$$

According to the above, R_{ZT} = 32 KΩ is set.

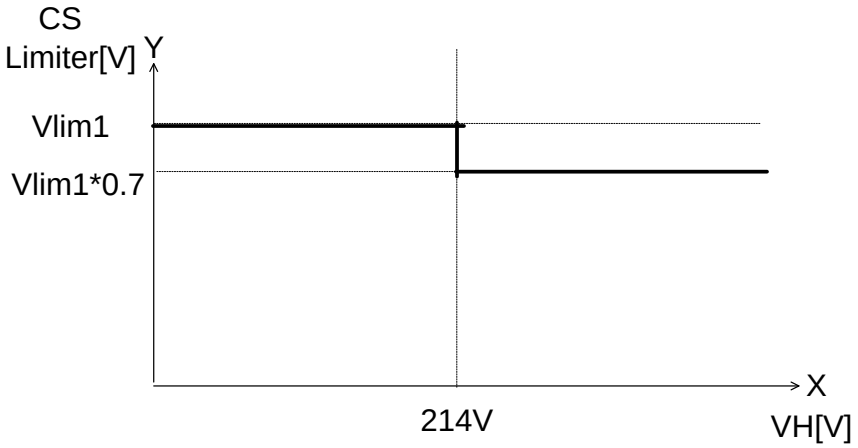


Figure 9. CS Switching: VH Voltage vs CS Voltage

(d) Determination of OFF Width (Turn ON)

OFF width is controlled at the ZT pin.
When switching is OFF, the power stored in the coil is supplied to the secondary-side output capacitor.
When this power supply ends, there is no more current flowing to the secondary side, so the switching MOS drain pin voltage drops.
Consequently, the voltage on the auxiliary coil side also drops.
A voltage that was resistance-divided from the ZT pin by R_{ZT1} and R_{ZT2} is applied. When this voltage level drops to V_{ZT1} (100 mV typ) or below, switching is turned ON by the ZT comparator. Since zero current status is detected at the ZT pin, time constants are generated using C_{ZT}, R_{ZT1}, and R_{ZT2}.
Additionally, a ZT trigger mask function (described in section 4 (e)) and a ZT timeout function (described in section 4 (f)) are built in.

(e) ZT Trigger Mask Function (Figure 10)

When switching is set ON / OFF, superposition of noise may occur at the ZT pin.
At this time, the ZT comparator is masked for the T_{ZTMASK} time to prevent ZT comparator operation errors.

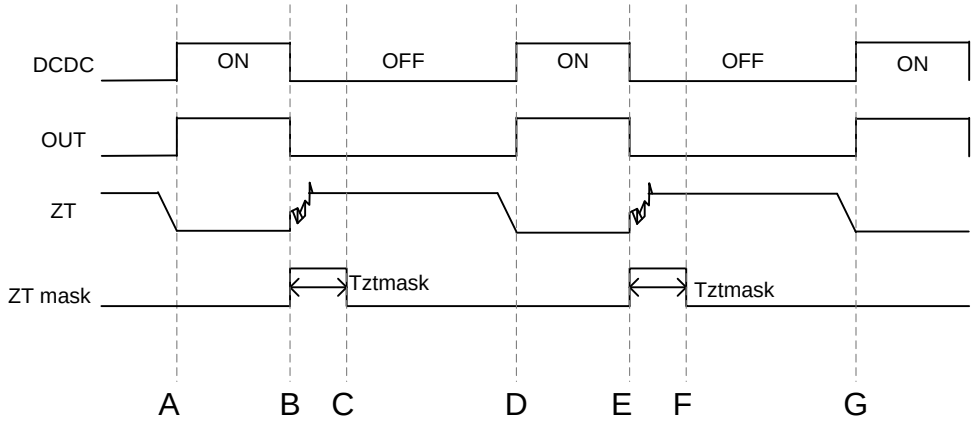


Figure 10. ZT Trigger Mask Function

A: DC/DC OFF=>ON
B: DC/DC ON=>OFF
C: Noise occurs at ZT pin, and ZT comparator is not operated by T_{ZTMASK}.
D: Same as A
E: Same as B
F: Same as C
G: Same as A

(f) ZT Timeout Function

- ZT Timeout Function1
  When ZT pin voltage is not higher than V_{ZT2} (typ=200mV) for t_{ZTOUT} (typ=15µs) such as start or low output voltage, ZT pin short, IC turns on MOSFET by force.

- ZT Timeout Function 2
  After ZT comparator detects bottom, IC turns on MOSFET by force when IC does not detect next bottom within t_{ZTOUT2} (typ =5µs). After ZT comparator detects bottom at once, the function operates. For that, it does not operate at start or at low output voltage. When IC is not able to detect bottom by decreasing auxiliary winding voltage, the function operates.

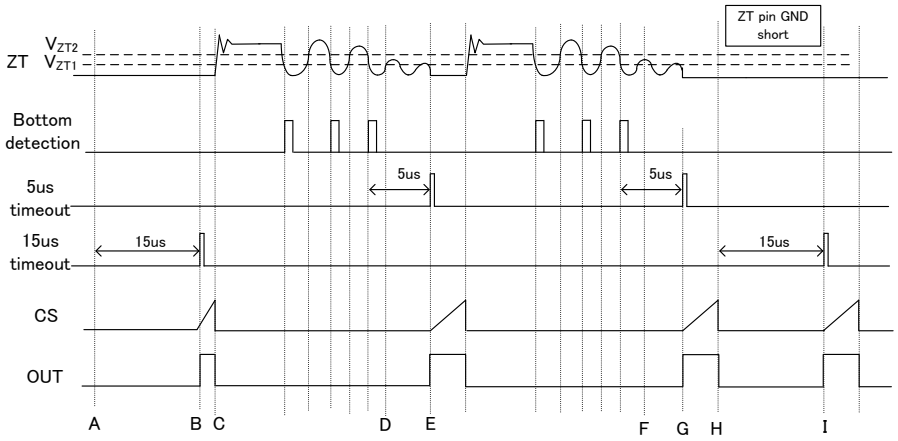


Figure 11. ZT Time-out Function

A: At starting, IC starts to operate by ZT timeout function1 for ZT=0V.
B: MOSFET turns ON
C: MOSFET turns OFF
D: ZT voltage is lower than V_{ZT2}(typ=200mV) by ZT dump decreasing.
E: MOSFET turns ON by ZT timeout fucntion2 after t_{ZTOUT2}(typ=5µs) from D point.
F: ZT voltage is lower than V_{ZT2}(typ=200mV) by ZT dump decreasing.
G: MOSFET turns ON by ZT timeout fucntion2 after t_{ZTOUT2}(typ=5µs) from F point.
H: ZT pin is short to GND.
I : MOSFET turns ON by ZT timeout function1 after t_{ZTOUT}(typ=15µs)

(5) Soft Start Operations

Normally, a large current starts flowing to the AC/DC power supply when the AC power supply is turned ON.
BD768xFJ includes a soft start function to prevent large changes in the output voltage and output current during startup.
This function is reset when the VCC pin voltage is at V_{UVLO2} (14.0V typ) or below, or when the BO pin is at the B.O. detection voltage (1.00V typ) or below (that is, when the AC power supply is unplugged), and soft start is performed again at the next AC power-ON.

During a soft start, the following post-startup operations are performed. (See turn OFF described above in section (4)- (a)).

- Start to 1ms => Set to 25% of normal CS limiter value
- 1ms to 4ms => Set to 50% of normal CS limiter value
- > 4 ms… => Normal operation

(6) Over Load Protection Function

The overload protection function monitors the overload status of the secondary output current at the FB pin, and fixes the OUT pin at low level when overload status is detected.
During overload status, current no longer flows to the photo-coupler, so the FB pin voltage rises.
When this status continues for the T_{FOLP} time (128ms typ), it is considered an overload and the OUT pin is fixed at low level.
Once the FB pin voltage exceeds V_{FOLP1} (2.8V typ), if it drops to lower than V_{FOLP2} (2.6V typ) within the T_{FOLP} time (128ms typ), the overload protection timer is reset.
At startup, the FB voltage is pulled up to the internal voltage by a pull-up resistor and operation starts once the voltage reaches V_{FOLP1} (2.8V typ) or above. Therefore, the design must be set the FB voltage at V_{FOLP2} (2.6V typ) or below within the t_{FOLP} (128ms typ) time.
In other words, the secondary output voltage start time must be set to within T_{FOLP} (128ms typ) after IC startup.

To release latching after selecting latch mode, first unplug the power supply, and then set $V_{CC} < V_{LATCH}$ (typ= V_{UVLO2} -3.5V)

(7) ZT Pin OVP (Over Voltage Protection)

ZT OVP (Over Voltage Protection) function is built in for ZT pin.
When the ZT pin voltage reaches V_{ZTL} (typ = 3.5V), overvoltage status is detected. ZT pin OVP protection is performed in latch mode.
A mask time defined as t_{LATCH} (typ = 150µs) is built in for the ZT pin OVP function. When ZT OVP status continues within 150 µs, overvoltage is detected. This function masks any surges (etc.) that occur at the pin. See the illustration in Figure 12.
(A similar t_{LATCH} (typ = 150µs) is VCCOVP)

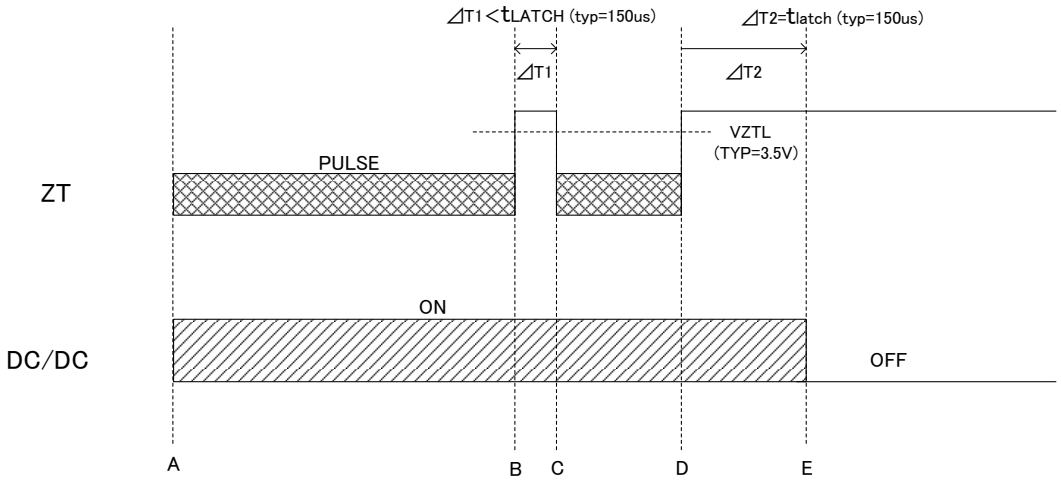


Figure 12. ZTOVP and Latch Mask Function

A: DC/DC pulse operation, ZT pin also has pulse operation
B: ZT pin voltage > V_{ZTL} (typ = 3.5V)
C: ZT pin voltage > V_{ZTL} (typ = 3.5V) status is within t_{LATCH} (typ = 150µs) period, so DC/DC normal operations are reset
D: ZT pin voltage > V_{ZTL} (typ = 3.5V)
E: ZT pin voltage > V_{ZTL} (typ = 3.5V) status continues for t_{LATCH} (typ = 150µs), so latching occurs and DC/DC OFF is set

(8) MASK Pin Function

The MASK pin is used for control that maintains constant voltage at the BD768xFJ's power supply pin (VCC pin). Figure 13 shows an application diagram using the MASK signal.
At the timing of DC/DC ON => OFF switching, a surge voltage in the auxiliary coil makes Va pin voltage rise. This also causes the VCC pin voltage to rise. The MASK pin outputs a signal that has been delayed by the time T_{MASK} relative to the OUT pin. (See Figure 14)

The MASK pin is an open drain output, and an external transistor is used for ON/OFF control. This function is able to maintain a constant VCC pin voltage.
During a soft start, the MASK pin is fixed at Hiz level. Consequently, the external transistor status is ON. (See Figure 13)

Leave open when not using the MASK pin.

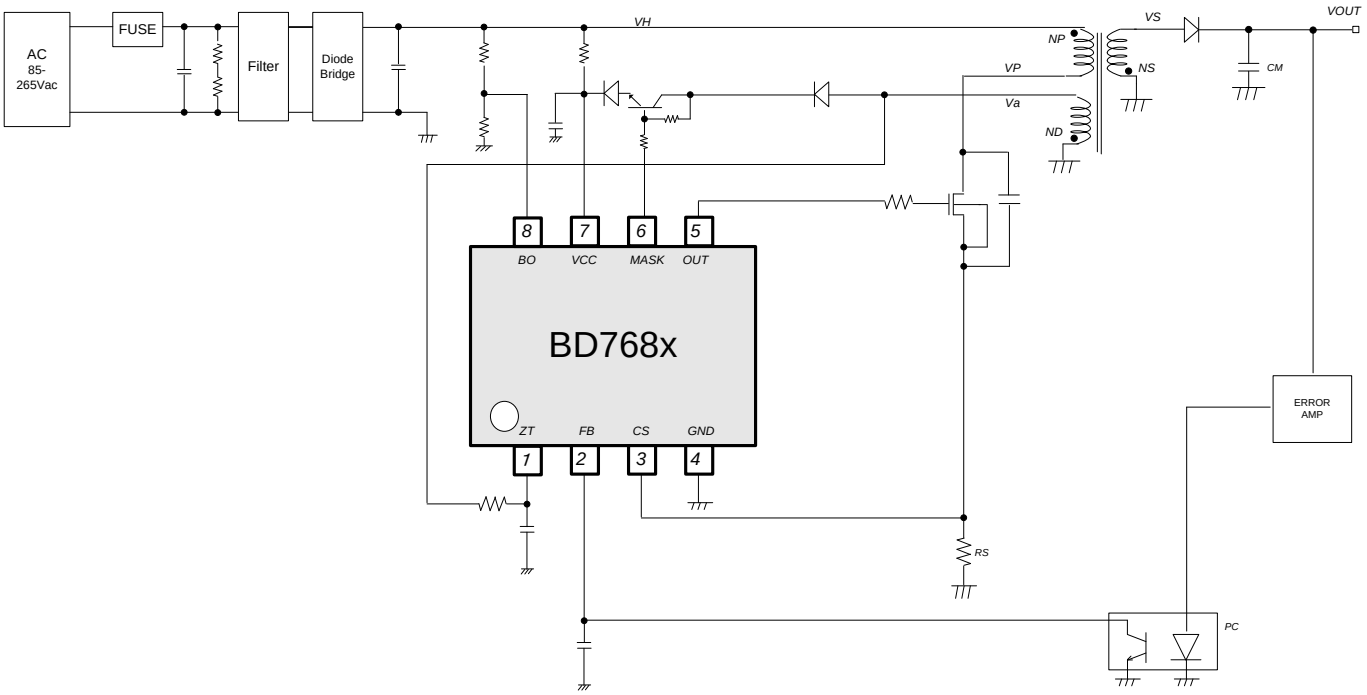


Figure 13. Application Circuit Example Using MASK Pin

(Note) In case of low output power, it isn't much power from the aux. window to VCC pin.
Please adjust a set value.

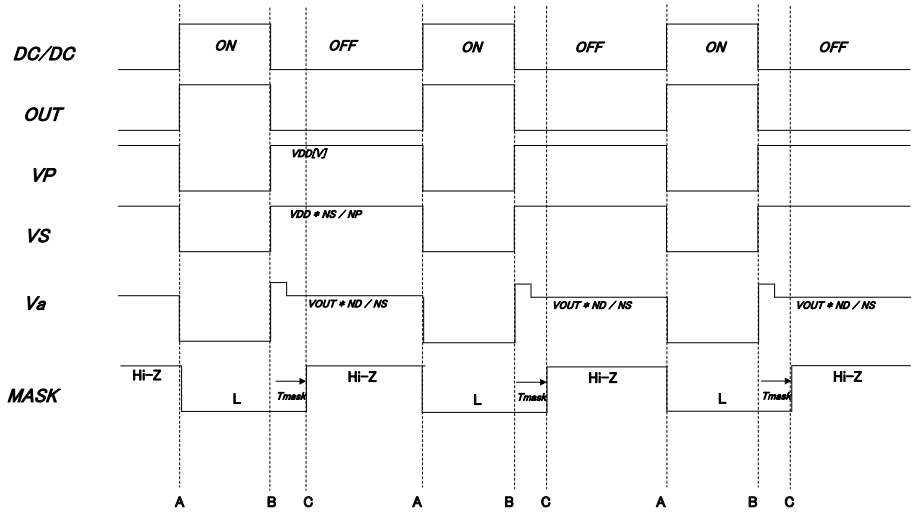


Figure 14. MASK Pin Timing Chart (Normal Operation)

A : DC/DC OFF=>ON
B : DC/DC ON=>OFF
C : During TMASK time, MASK pin is L

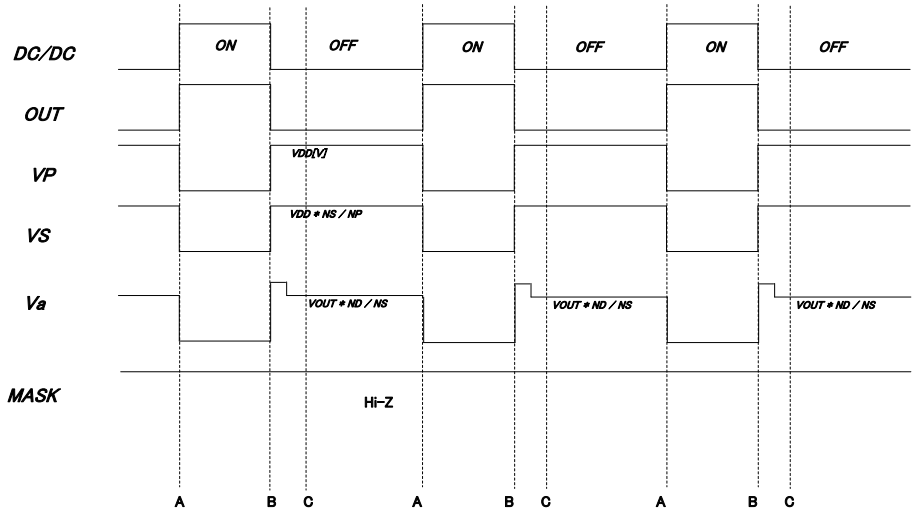


Figure 15. MASK Pin Timing Chart (Soft Start Operation)

A: DC/DC OFF => ON
B: DC/DC ON => OFF
C: MASK pin is fixed at Hiz level.

(9) OUT Pin Gate Clamp Circuit
OUT pin is connected to external MOSFET's gates.
For MOSFET's gates is safety, OUT voltage is clamped to Gate Clamp circuit.

(10) Thermal Shut-Down Function
Thermal Shut-Down function is auto restart type. When VCC UVLO is released, BD768xFJ starts on State2 because of preventing from thermal error of external parts. At start up, it does not start until T1 below.

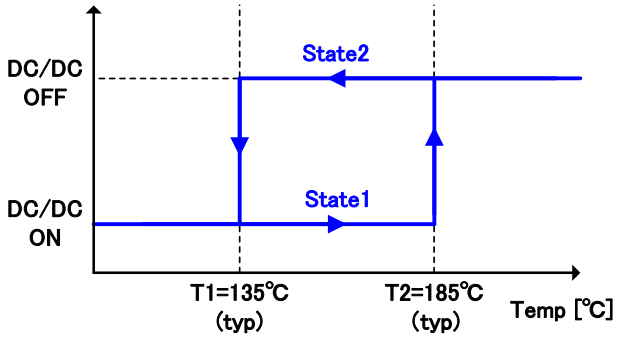


Figure 16. Thermal Shut-Down

Protection Circuit Operation Modes

Table 2 below lists the operation modes of the various protection functions.

Table 2 Protection Circuit Operation Modes

Item	Operation Mode
Brown Out Protection	Auto recovery
VCC Under Voltage Locked Out	Auto recovery
VCC Over Voltage Protection	BD7682/7683 = Latch BD7684/7685 = Auto recovery
FB Over Limited Protection	BD7682/7684 = Auto recovery BD7683/7685 = Latch
ZT Over Voltage Protection	Latch
Thermal Shutdown	Auto recovery

Power Dissipation

The thermal design should be set operation for the following conditions.
(Since the temperature shown below is the guaranteed temperature, be sure to take a margin into account.)

1. The ambient temperature Ta must be 105°C or less.
2. The IC's loss must be within the allowable dissipation Pd.

The thermal dissipation characteristics are as follows.
(PCB: 70 mm × 70mm × 1.6 mm, mounted on glass epoxy substrate)

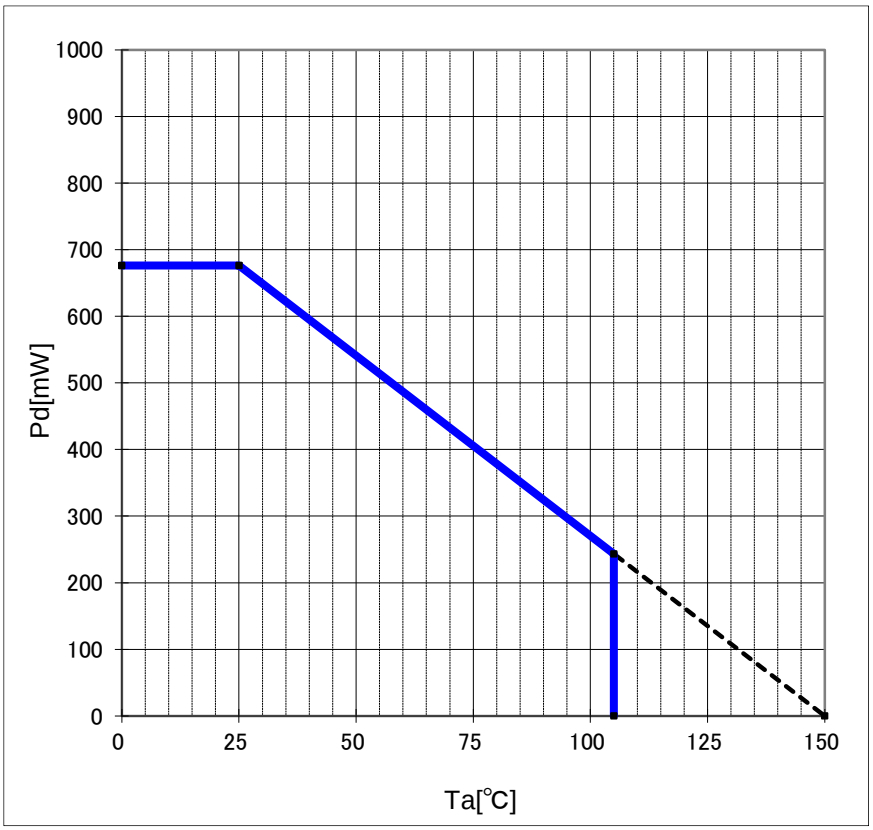
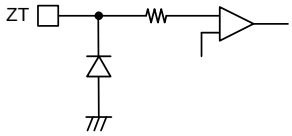
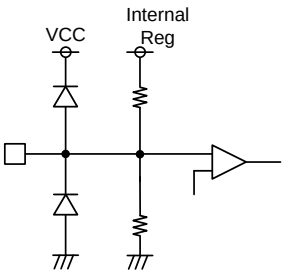
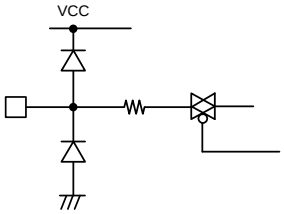
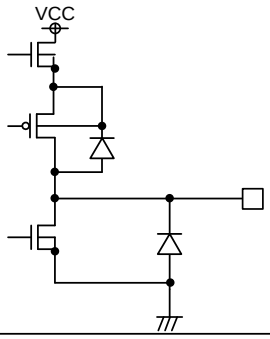
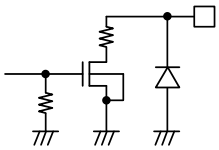
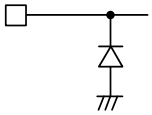
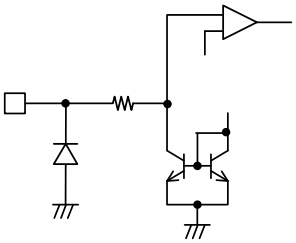
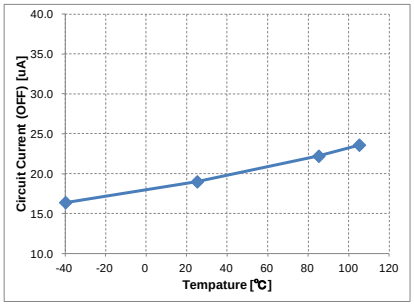


Figure 17. SOP-J8 Thermal De-rating Curve

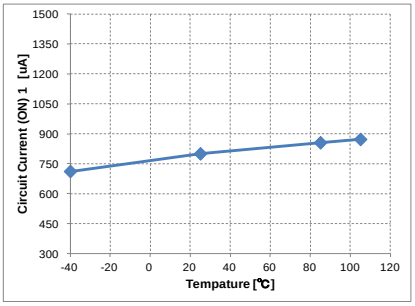
I/O Equivalent Circuit

1	ZT	2	FB	3	CS	4	GND
							
5	OUT	6	MASK	7	VCC	8	BO
							

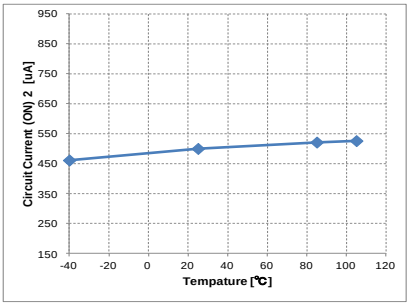
●Characteristic Data (They are only reference data)



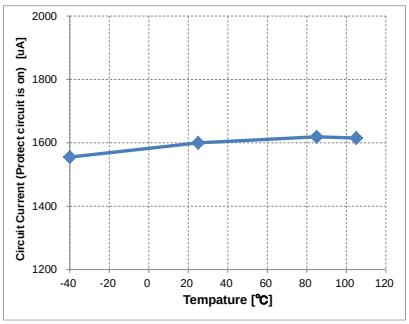
Circuit Current (OFF)



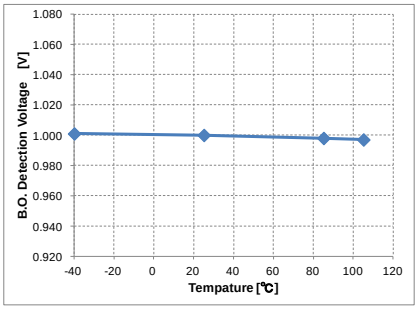
Circuit Current (ON) 1



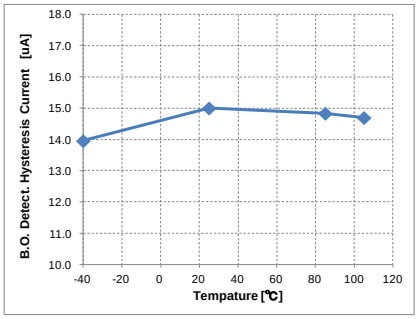
Circuit Current (ON) 2



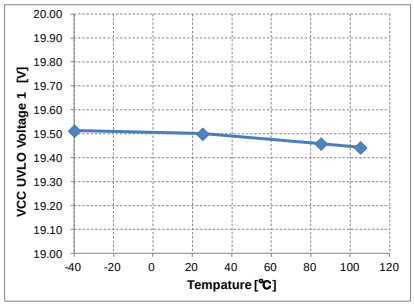
Circuit Current (Protect circuit is on)



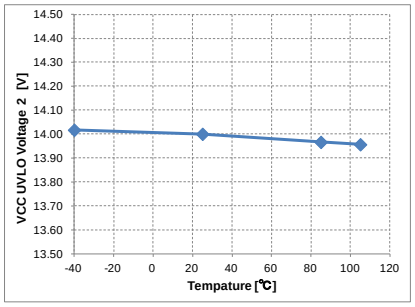
B.O. Detection Voltage



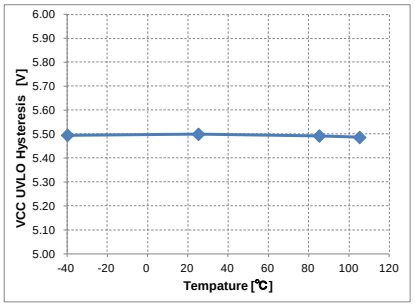
B.O. Detection Hysteresis Current



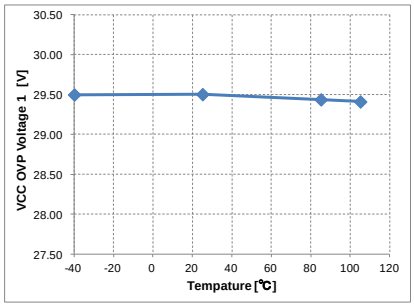
VCC UVLO Voltage 1



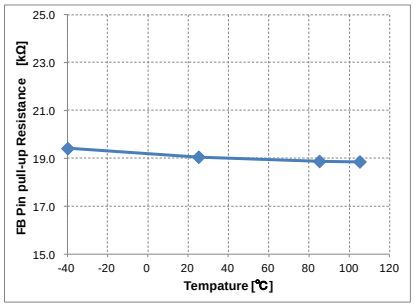
VCC UVLO Voltage 2



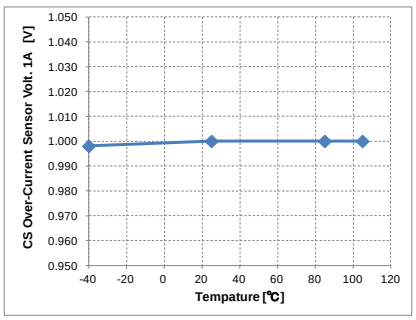
VCC UVLO Hysteresis



VCC OVP Voltage 1

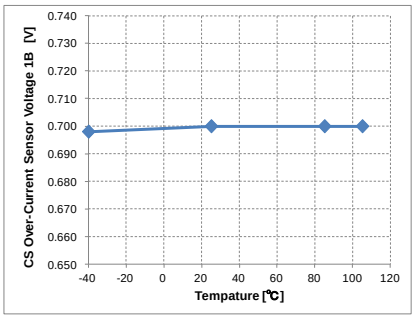


FB Pin pull-up Resistance

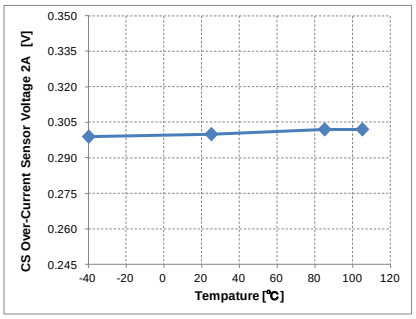


CS Over-Current Sensor Voltage 1A

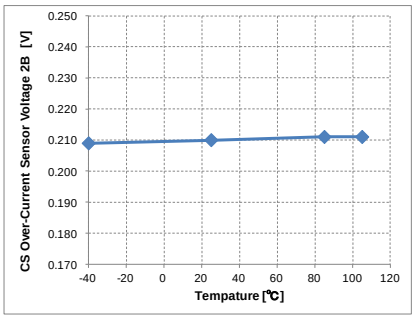
●Characteristic Data (They are only reference data)



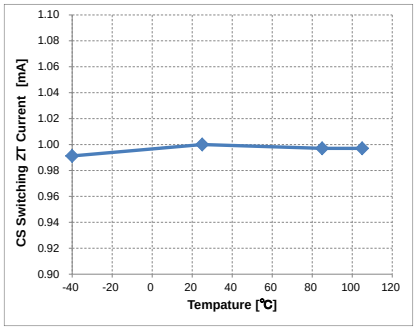
CS Over-Current Sensor Voltage 1B



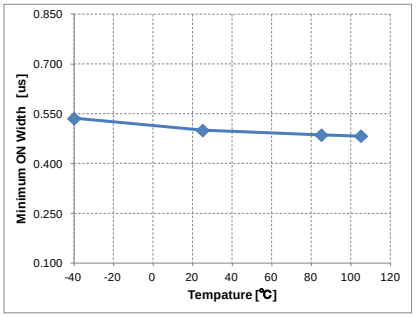
CS Over-Current Sensor Voltage 2A



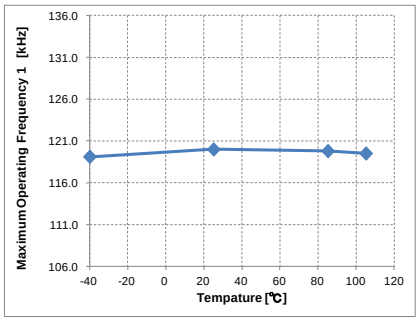
CS Over-Current Sensor Voltage 2B



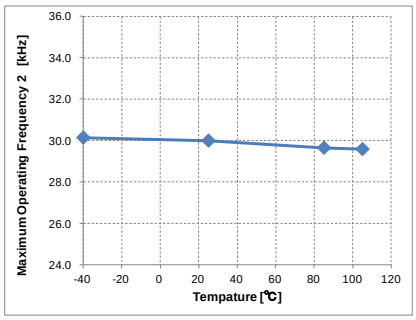
CS Switching ZT Current



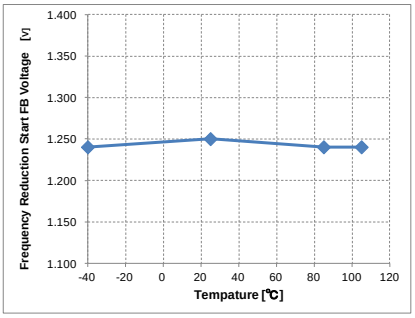
Minimum ON Width



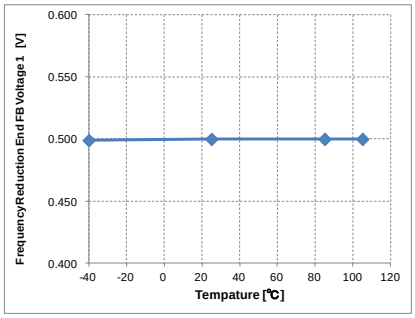
Maximum Operating Frequency 1



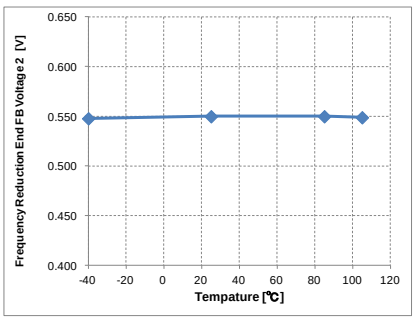
Maximum Operating Frequency 2



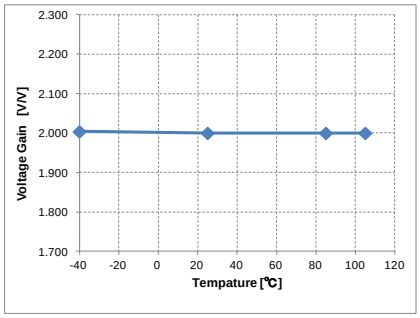
Frequency Reduction Start FB Voltage



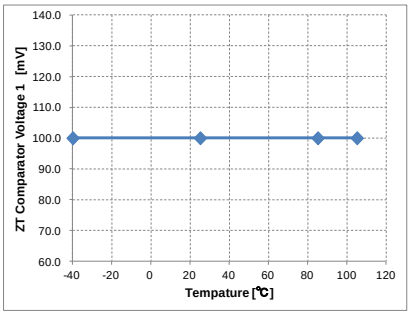
Frequency Reduction End FB Voltage 1



Frequency Reduction End FB Voltage 2

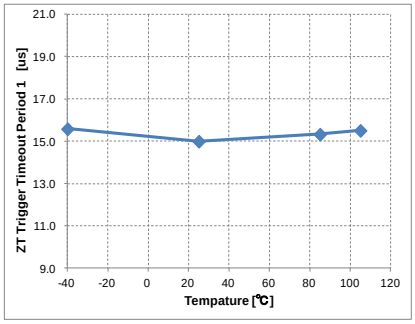


Voltage Gain

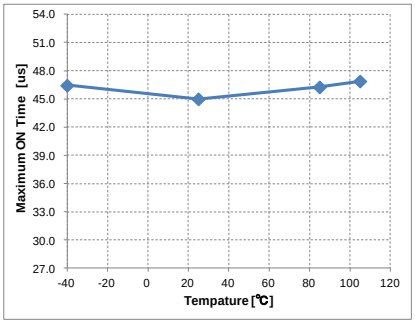


ZT Comparator Voltage 1

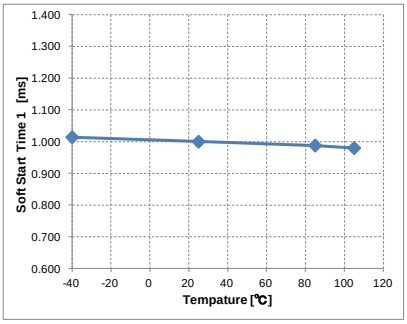
●Characteristic Data (They are only reference data)



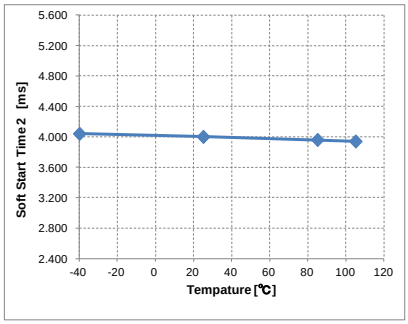
ZT Trigger Mask Time



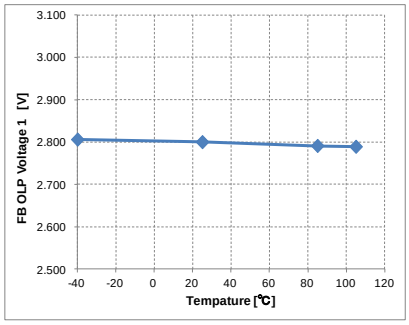
Maximum ON Time



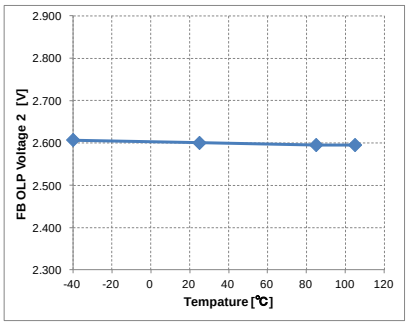
Soft Start Time 1



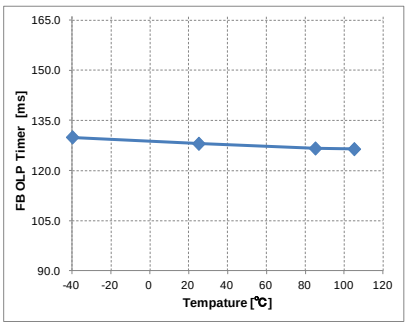
Soft Start Time 2



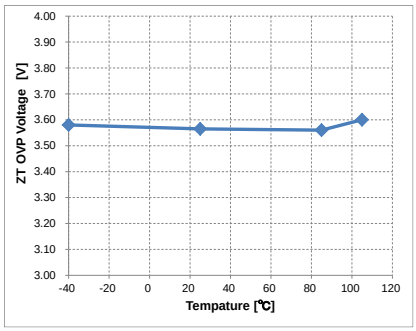
FB OLP Voltage 1



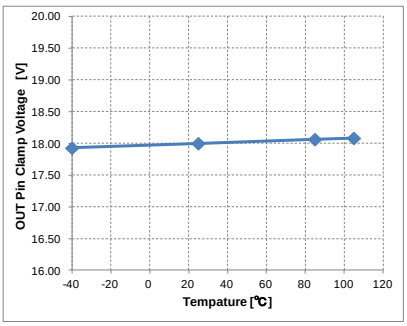
FB OLP Voltage 2



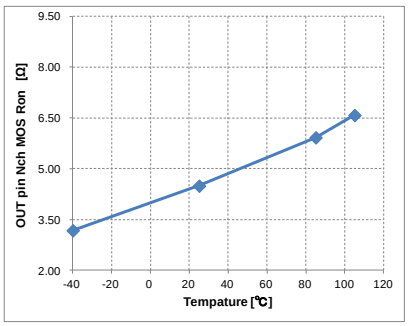
FB OLP Timer



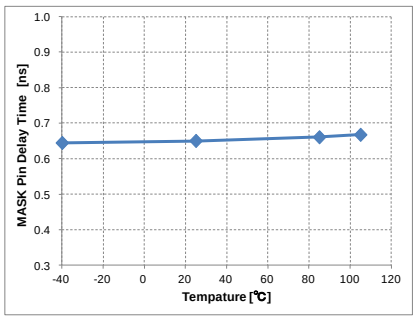
ZT OVP Voltage



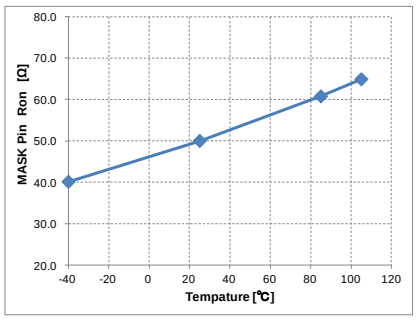
OUT Pin Clamp Voltage



OUT pin Nch MOS Ron



MASK Pin Delay Time



MASK Pin Ron

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the GND and supply lines of the digital and analog blocks to prevent noise in the GND and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to GND at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **GND Voltage**
   Ensure that no pins are at a voltage below that of the GND pin at any time, even during transient condition.

4. **GND Wiring Pattern**
   When using both small-signal and large-current GND traces, the two GND traces should be routed separately but connected to a single GND at the reference point of the application board to avoid fluctuations in the small-signal GND caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The GND lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, GND the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to GND, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Terminals**
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or GND line.

Operational Notes – continued

12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

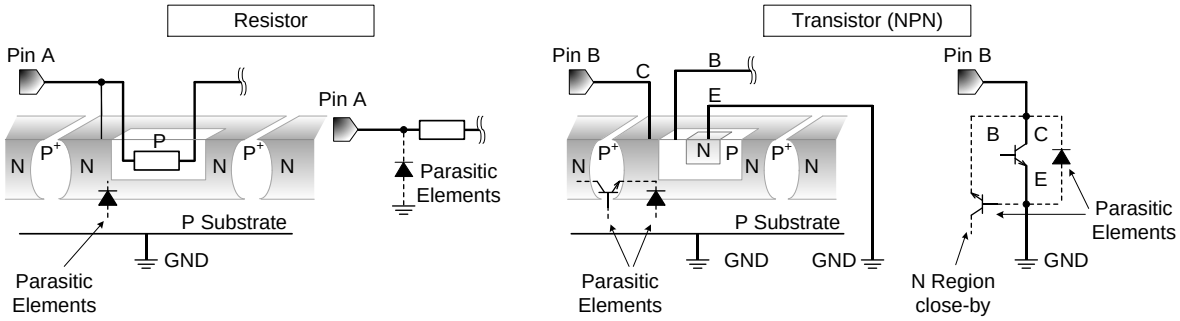


Figure 17. Example of Monolithic IC Structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

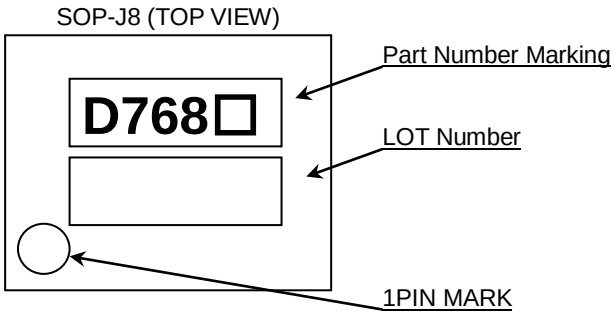
B D 7 6 8 X F J - L B E 2

Product name

Package
FJ : SOP-J8

Product class
LB for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel

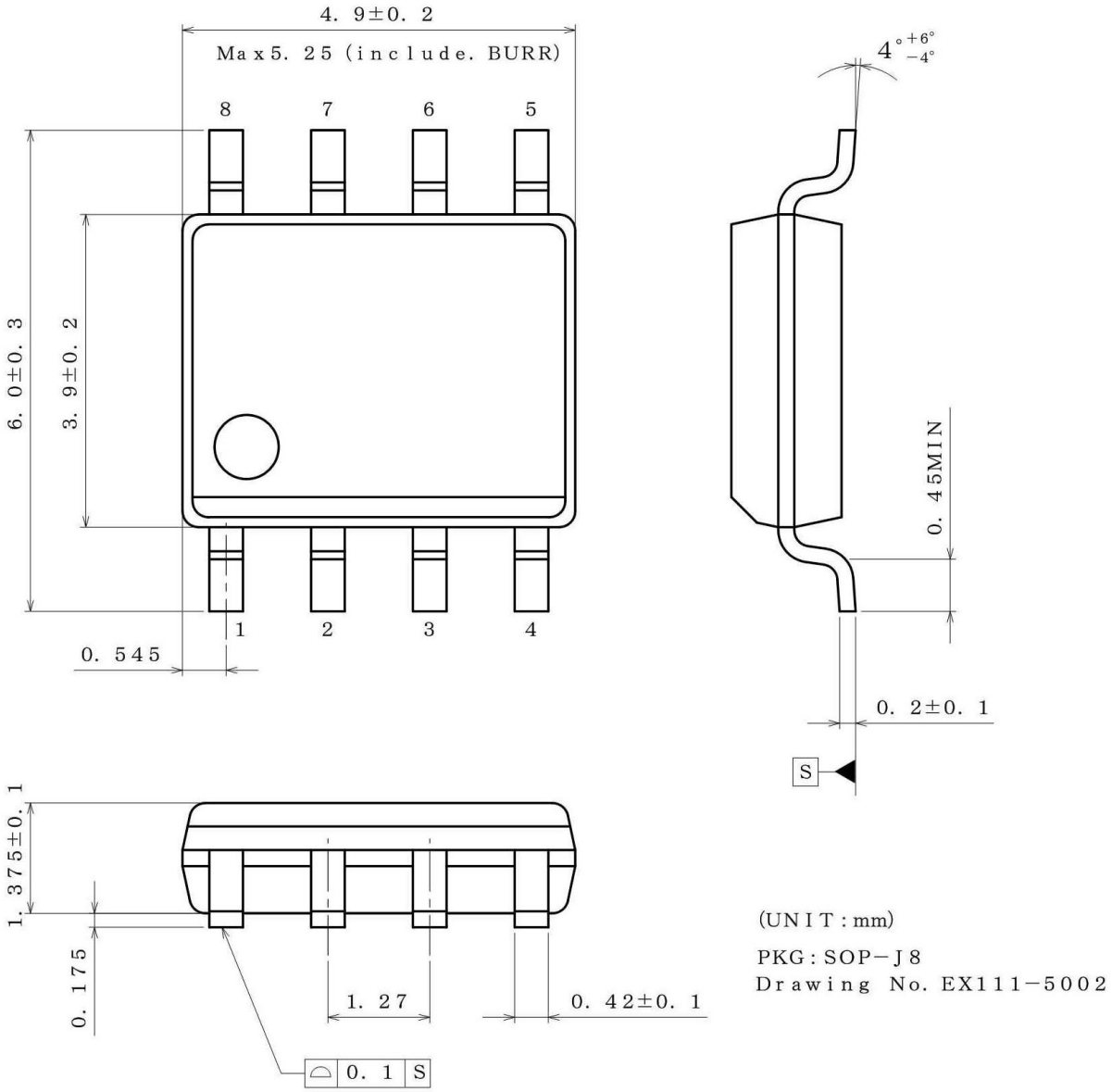
Marking Diagram



	Product name	Part Number Marking
1	BD7682FJ-LB	D7682
2	BD7683FJ-LB	D7683
3	BD7684FJ-LB	D7684
4	BD7685FJ-LB	D7685

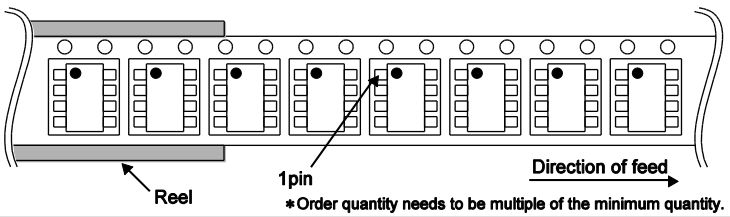
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
23.Mar.2015	001	New Release
29.Jun.2016	002	P2 values in the Block diagram P3 an explanation of Absolute Maximum Rating P7 a value of Figure 3 P8 values of Figure 4 P10 values of Figure 6 P11 a value of Figure 8 P14 an explanation of Soft start operations P14 a value of Figure 12 P17 an explanation of Table 2
29.Nov.2018	003	P26 Package of Ordering Information

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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