



# A7682E

## Hardware Design

LTE Module

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# 1 Introduction

This document describes the hardware interface of the module, which can help users quickly understand the interface definition, electrical performance and structure size of the module. Combined with this document and other application documents, users can understand and use A7682E module to design and develop applications quickly.

SIMCom provides a set of evaluation boards to facilitate A7682E module testing and use. The evaluation board tools include an EVB board, a USB cable, an antenna, and other peripherals.

## 1.1 Product Outline

A7682E module supports GSM and LTE-FDD. Please refer to the following table for detailed frequency band description:

**Table 1: A7682E Frequency Bands**

STANDARD	BAND	A7682E
GSM	900MHz	✓
	1800MHz	✓
LTE-FDD	FDD B1	✓
	FDD B3	✓
	FDD B5	✓
	FDD B7	✓
	FDD B8	✓
	FDD B20	✓
Category		CAT1

With a small physical dimension of 19.6 \* 19.6 \* 2.4 mm, which can meet the requirements of space size in almost all M2M applications, such as vehicle, metering, security, routing, wireless POS, mobile computing equipment, PDA, tablet computer, etc.

A7682E provides 85 pins, including 50 LGA pins in the outer ring and 35 LGA pins in the inner ring. This document will introduce all the functional pins.

## 1.2 Hardware Interface Overview

A7682E provides the following hardware interfaces.

- Power input
- USB 2.0 interface
- Three UART interfaces (one main serial port, one debug serial port and one ordinary two-wire serial port)
- I2C interface
- Two USIM card interfaces
- ADC interface
- Power supply output
- USB boot download and guidance interface
- Two audio interfaces, one MIC port and one Receiver port.
- General input and output interfaces (GPIO)
- Network status indication interface
- Antenna interface
- Module operation status indication interface

## 1.3 Hardware Block Diagram

The block diagram of the A7682E module is shown in the figure below.

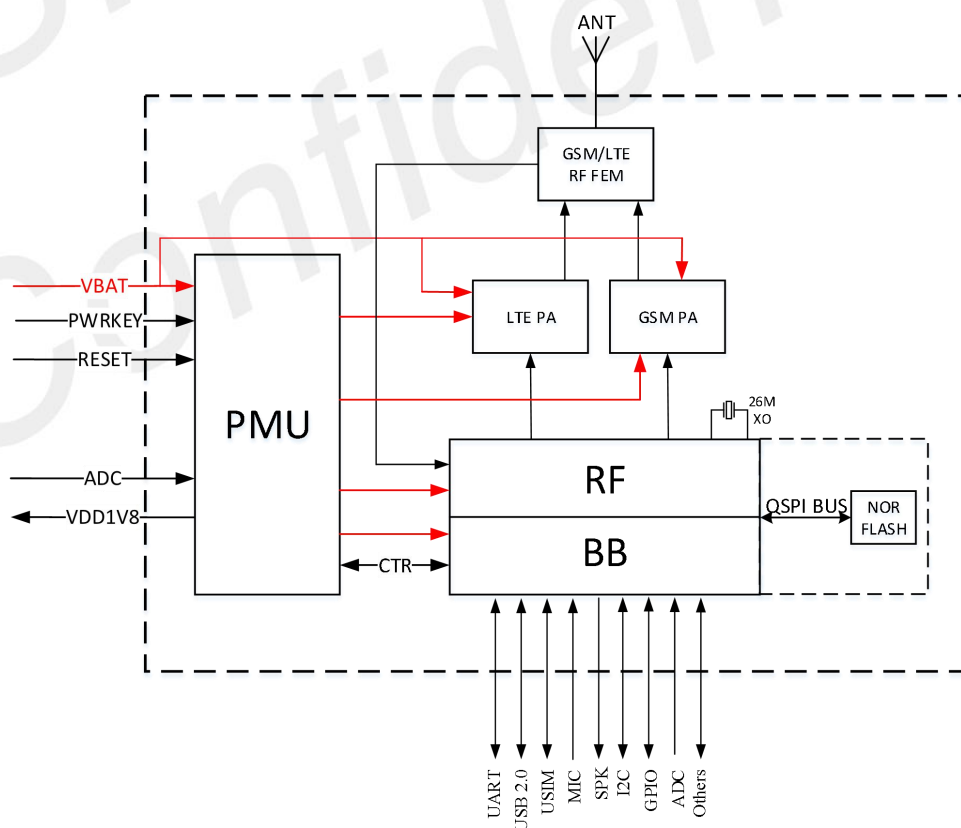


Figure 1: Block diagram

## 1.4 Functional Overview

**Table 2: General features**

Feature	Implementation
Power supply	VBAT: 3.4V ~4.2V, Recommended VBAT: 3.8V
Power consumption	Current consumption in sleep mode: <2mA
BAND	Refer to Table 1
TX power	GSM/GPRS power level: -- EGSM900: 4 (33dBm ±2dB) -- DCS1800: 1 (30dBm ±2dB) EDGE power level: -- EGSM900: E2 (27dBm ±3dB) -- DCS1800 : E1 (26dBm+3dB/-4dB) LTE power level: 3 (23dBm±2.7dB)
Data transmission throughput	GPRS Multiple time slot level 12 EDGE Multiple time slot level 12 FDD-LTE category 1 : 10 Mbps (DL),5 Mbps (UL)
Antenna interface	GSM/LTE antenna interface
Short Message (SMS)	MT,MO, CB, Text , PDU mode Short Message (SMS) storage device: USIM Card, CB does not support saving in SIM Card Support CS domain and PS domain SMS
USIM Card interface	Support 1.8V/3V USIM card
USIM application toolkit	Support SAT class3, GSM 11.14 Release 99 Support USAT
Phonebook management	Support phonebook types : SM/FD/ON/AP/SDN
Audio feature	Support one analog MIC, one analog audio output interface
UART interface	<ul style="list-style-type: none"> <li>●Main serial port</li> </ul> Baud rate support from 300bps to 3.6Mbps AT command and data can be sent through serial port Support RTS/CTS Hardware flow control <ul style="list-style-type: none"> <li>● UART3</li> </ul> one ordinary two-wire serial port The default baud rate is 115200bps. <ul style="list-style-type: none"> <li>●Debug serial port</li> </ul> Support debug usage
USB interface	USB 2.0 compliant, host mode not supported. This interface can be used for AT command sending, data transmission, software debugging and upgrading.
Firmware upgrade	Firmware upgrade over USB interface
Physical characteristics	Dimension: 19.6*19.6*2.4mm Weight: 1.9g±0.1

Temperature range

Operation temperature:  $-30^{\circ}\text{C} \sim +80^{\circ}\text{C}$   
Extended operation temperature:  $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}^*$   
Storage temperature:  $-45^{\circ}\text{C} \sim +90^{\circ}\text{C}$

**NOTE**

Module is able to make and receive voice calls, data calls, SMS and make GPRS/LTE traffic in  $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ . The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extended operating temperature range.

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## 2 Package Information

### 2.1 Pin Assignment Overview

A7682E provides 85 pins interface.

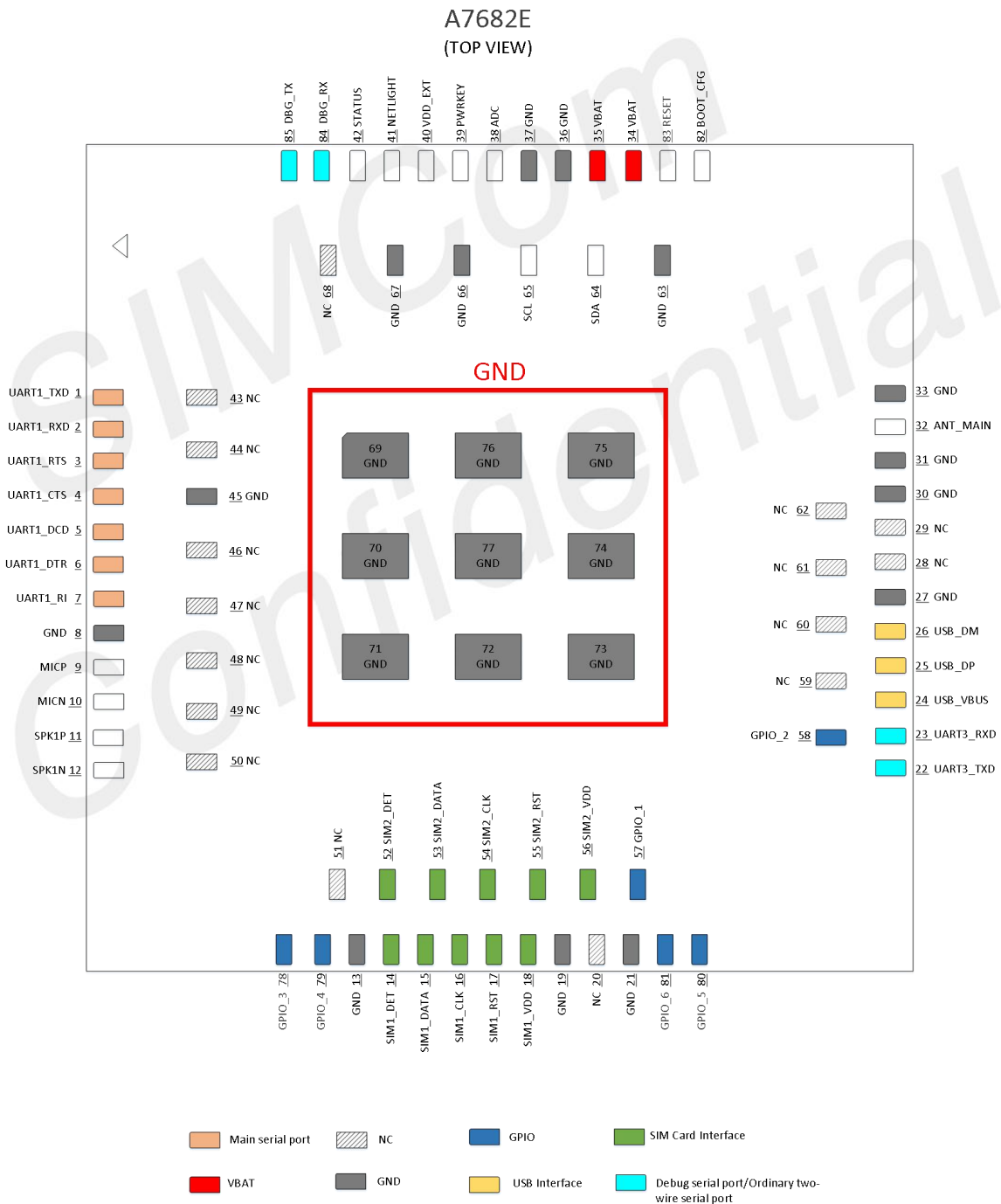


Figure 2: Module pin diagram (Top view)

Table 3: Pin Description

Pin No.	Pin name	Pin No.	Pin name
1	UART1_TXD	2	UART1_RXD
3	UART1_RTS	4	UART1_CTS
5	UART1_DCD	6	UART1_DTR
7	UART1_RI	8	GND
9	MICP	10	MICN
11	SPK1P	12	SPK1N
13	GND	14	SIM1_DET
15	SIM1_DATA	16	SIM1_CLK
17	SIM1_RST	18	SIM1_VDD
19	GND	20	NC
21	GND	22	UART3_TXD
23	UART3_RXD	24	USB_VBUS
25	USB_DP	26	USB_DM
27	GND	28	NC
29	NC	30	GND
31	GND	32	RF_ANT
33	GND	34	VBAT
35	VBAT	36	GND
37	GND	38	ADC
39	PWRKEY	40	VDD_EXT
41	NETLIGHT	42	STATUS
43	NC	44	NC
45	GND	46	NC
47	NC	48	NC
49	NC	50	NC
51	NC	52	SIM2_DET
53	SIM2_DATA	54	SIM2_CLK
55	SIM2_RST	56	SIM2_VDD
57	GPIO1	58	GPIO2
59	NC	60	NC
61	NC	62	NC
63	GND	64	SDA
65	SCL	66	GND
67	GND	68	NC
69	GND	70	GND
71	GND	72	GND
73	GND	74	GND

75	GND	76	GND
77	GND	78	GPIO3
79	GPIO4	80	GPIO5
81	GPIO6	82	BOOT_CFG●
83	RESET	84	DBG_RXD
85	DBG_TXD		

### NOTE

'BOOT\_CFG' Pin cannot be pulled down before the module powered up, otherwise it will affect the normal start-up of the module.

## 2.2 Pin Description

Table 4: IO parameters definition

Pin type	Description
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
I/O	Input/output
DI	Digital input
DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down
OD	Open Drain

Table 5: 1.8V IO electrical parameters definition

Power domain	Parameter	Description	Min	Typ.	Max
	VCC=1.8V				
	VIH	High level input	$VCC * 0.7$	1.8V	$VCC+0.2$
	VIL	Low level input	-0.3V	0V	$VCC * 0.3$
	Rpu	Pull up resistor	55 K $\Omega$	79 K $\Omega$	121K $\Omega$

	Rpd	Pull down resistor	51KΩ	87 KΩ	169KΩ
1.8V	VCC=1.8V Typical				
	IIL	Input leakage current	-	-	10uA
	Input DC Operating Conditions (VCC = 1.8 V Typical)				
	VOH	Output high level range	VCC-0.2	-	-
	VOL	Output low level range	-	-	0.2V
	Iol	Low-level output current Vpad=0.2V	-	-	13mA
	Ioh	High-level output current Vpad=VCC-0.2V	-	-	11mA

**Table 6: 3.3V IO electrical parameters definition**

Power domain	Parameter	Description	Min	Typ.	Max
3.3V(SIM)	VCC=3.3V				
	VIH	High level input	2V	-	VCC+0.3
	VIL	Low level input	-0.3V	0V	0.8V
	Rpu	Pull up resistor	26K	47K	72K
	Rpd	Pull down resistor	27K	54K	267K
	VCC=3.3V Typical				
	IIL	Input leakage current	-	-	10uA
	Input DC Operating Conditions (VCC = 3.3V Typical)				
	VOH	Output high level range	2.4V	-	-
	VOL	Output low level range	-	-	0.4V
	Iol	Low-level output current Vpad=0.4V	-	-	7mA
Ioh	High-level output current Vpad=VCC-0.5 V	-	-	7mA	

**Table 7: Pin description**

Pin name	Pin No.	Pin parameter		Description	Note
		Power	Type		



domain					
<b>Power supply</b>					
VBAT	34,35	-	PI	A7682E input voltage ranges from 3.4V to 4.2V, and the peak current value can reach 2A.	
VDD_EXT	40	-	PO	1.8V power output, output current up to 50 mA. It can provide power for level conversion circuits, but not for high-power loads.	If unused, keep it open.
GND	8,13,19,21,27,30,31,33,36,37,45,63,66,67,69,70,71,72,73,74,75,76,77	-	-	Ground	
<b>System Control</b>					
PWRKEY	39	-	DI,PU	Power ON/OFF input, active low. VIH: 0.7*VBAT VIL: 0.5V	PWRKEY has been internally pulled-up to VBAT with 50KΩ resistor, default high.
RESET	83	-	DI,PU	System reset control input, active low. VIH: 0.7*VBAT VIL: 0.5V	RESET has been pulled-up to VBAT with 50KΩ (typical) resistor, default high.
<b>SIM interface</b>					
SIM1_DET	14	1.8V	I/O,PD	SIM1 card hot swap detection	
SIM1_DATA	15	1.8/3.0 V	I/O,PU	SIM1 bus data, this pin has been pull-up with 4.7KΩ resistor to SIM1_VDD.	
SIM1_RST	17	1.8/3.0 V	I/O,PU	SIM1 bus reset output.	
SIM1_CLK	16	1.8/3.0 V	I/O,PU	SIM1 bus clock output.	
SIM1_VDD	18	1.8/3.0 V	PO	SIM card power supply output, Supports 1.8v/3.0v output according to the card type, Its output current is up to 50mA.	
SIM2_DET	52	1.8V	I/O,PD	SIM2 card hot swap detection	
SIM2_DATA	53	1.8/3.0 V	I/O,PU	SIM2 bus data, this pin has been pull-up with 4.7KΩ resistor to SIM2_VDD.	
SIM2_RST	55	1.8/3.0 V	I/O,PU	USIM2 bus reset output.	

SIM2_CLK	54	1.8/3.0 V	I/O,PU	USIM2 bus clock output.	
SIM2_VDD	56	1.8/3.0 V	PO	USIM card power supply output, Supports 1.8v/3.0v output according to the card type, Its output current is up to 50mA.	
<b>USB interface</b>					
USB_VBUS	24	-	AI	Valid USB detection input, active High Vmin=3.0V, Vmax=5.2V, Vnorm=5V	
USB_DM	26	-	I/O	Negative line of the differential, bi-directional USB signal.	
USB_DP	25	-	I/O	Positive line of the differential, bi-directional USB signal.	
<b>Full function UART interface</b>					
UART1_TXD	1	1.8V	DOH	Data output	If unused, keep it open.
UART1_RXD	2	1.8V	DI	Data input	
UART1_RTS	3	1.8V	DI	RTS input	
UART1_CTS	4	1.8V	DO	CTS output	
UART1_DCD	5	1.8V	DO	Carrier detection	
UART1_DTR	6	1.8V	DI	DTE Ready	
UART1_RI	7	1.8V	DO	Ring indicator	
<b>Debug UART</b>					
DBG_TXD	85	1.8V	DOH	CP_UART output	Default used as debug port.
DBG_RXD	84	1.8V	DI	CP_UART input	
<b>UART 3</b>					
UART3_TXD	22	1.8V	DOH	UART3 output	
UART3_RXD	23	1.8V	DI	UART3 input	
<b>I2C interface</b>					
SCL	65	1.8V	DO	I2C clock output	If unused, keep it open. If you need to use it, please use VDD_EXT (40 PIN of the module) for pull-up
SDA	64	1.8V	I/O	I2C data I/O	
<b>Analog audio interface</b>					
MICP	9	1.8V	AIO	Audio microphone positive input	If unused, keep it open.
MICN	10	1.8V	AIO	Audio microphone negative input	
SPK1P	11	1.8V	AIO	Audio output positive	
SPK1N	12	1.8V	AIO	Audio output negative	
<b>GPIO</b>					

GPIO1	57	1.8V	IO,PU	General purple I/O	If unused, keep it open.
GPIO2	58	1.8V	IO,PD	General purple I/O	If unused, keep it open.
GPIO3	78	1.8V	IO,PD	General purple I/O	If unused, keep it open.
GPIO4	79	1.8V	IO,PU	General purple I/O	If unused, keep it open.
GPIO5	80	1.8V	IO,PU	General purple I/O	If unused, keep it open.
GPIO6	81	1.8V	IO,PU	General purple I/O	If unused, keep it open.
<b>ANT interface</b>					
RF_ANT	32	-	AIO	Main ANT interface	
<b>Other pins</b>					
ADC	38	-	AI	General Purpose ADC	If unused, keep it open.
NETLIGHT	41	1.8V	DO	Network registration status indicator (LED). For more detail, please refer the chapter 3.9.	
STATUS	42	1.8V	DO	Power on status indicator	
BOOT_CFG	82	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, A7682E will access in USB download mode.	Do place 2 test points for debug. Do not pull down BOOT_CFG during normal power up!

## NOTE

- Please reserve test points for BOOT\_CFG, VDD\_EXT, DBG\_TXD and DBG\_RXD.
- If there is no USB connector, please reserve test points for USB\_VBUS, USB\_DP and USB\_DM for firmware upgrade.

## 2.3 Mechanical Information

The following figure shows the package outline drawing of A7682E module.

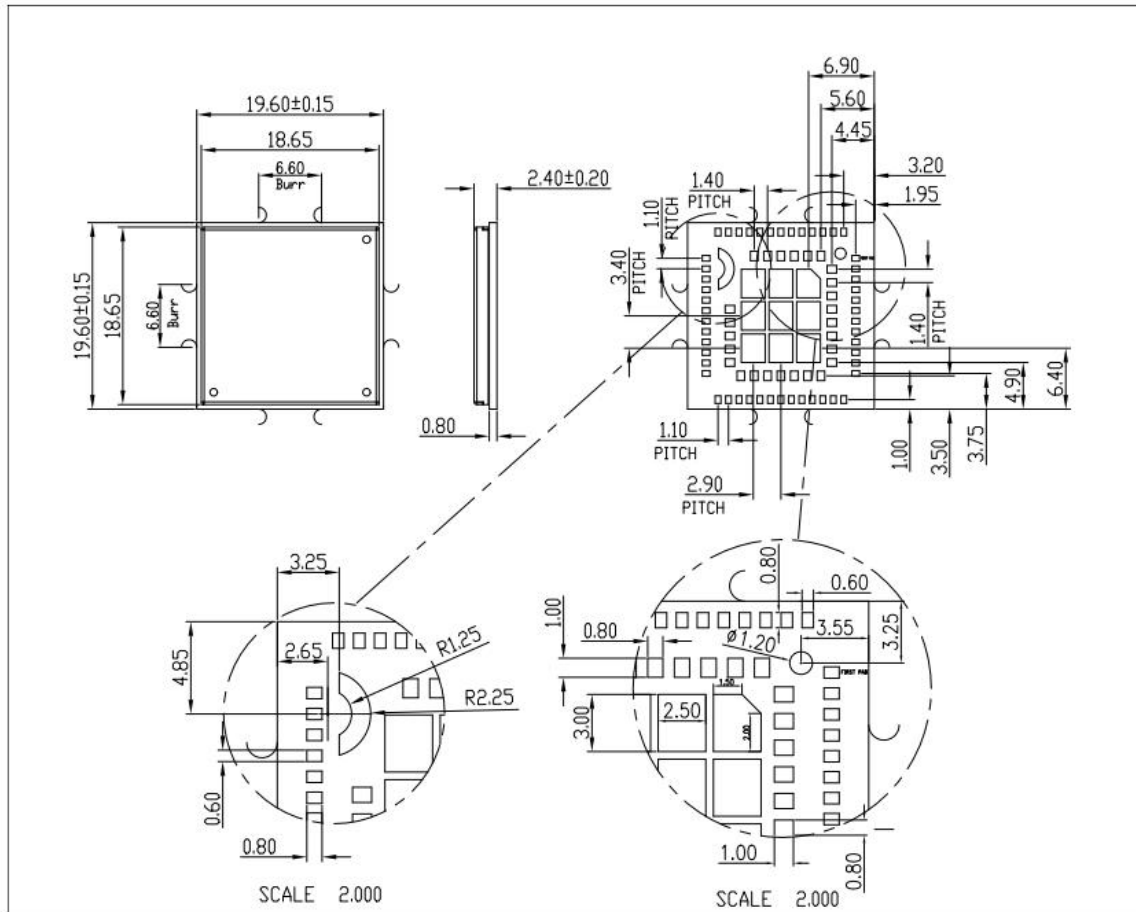


Figure 3: Dimension drawing (Unit: mm)

### NOTE

The side length is 19.60 ± 0.15mm, excluding burr area.

## 2.4 Recommend PCB Footprint Dimension

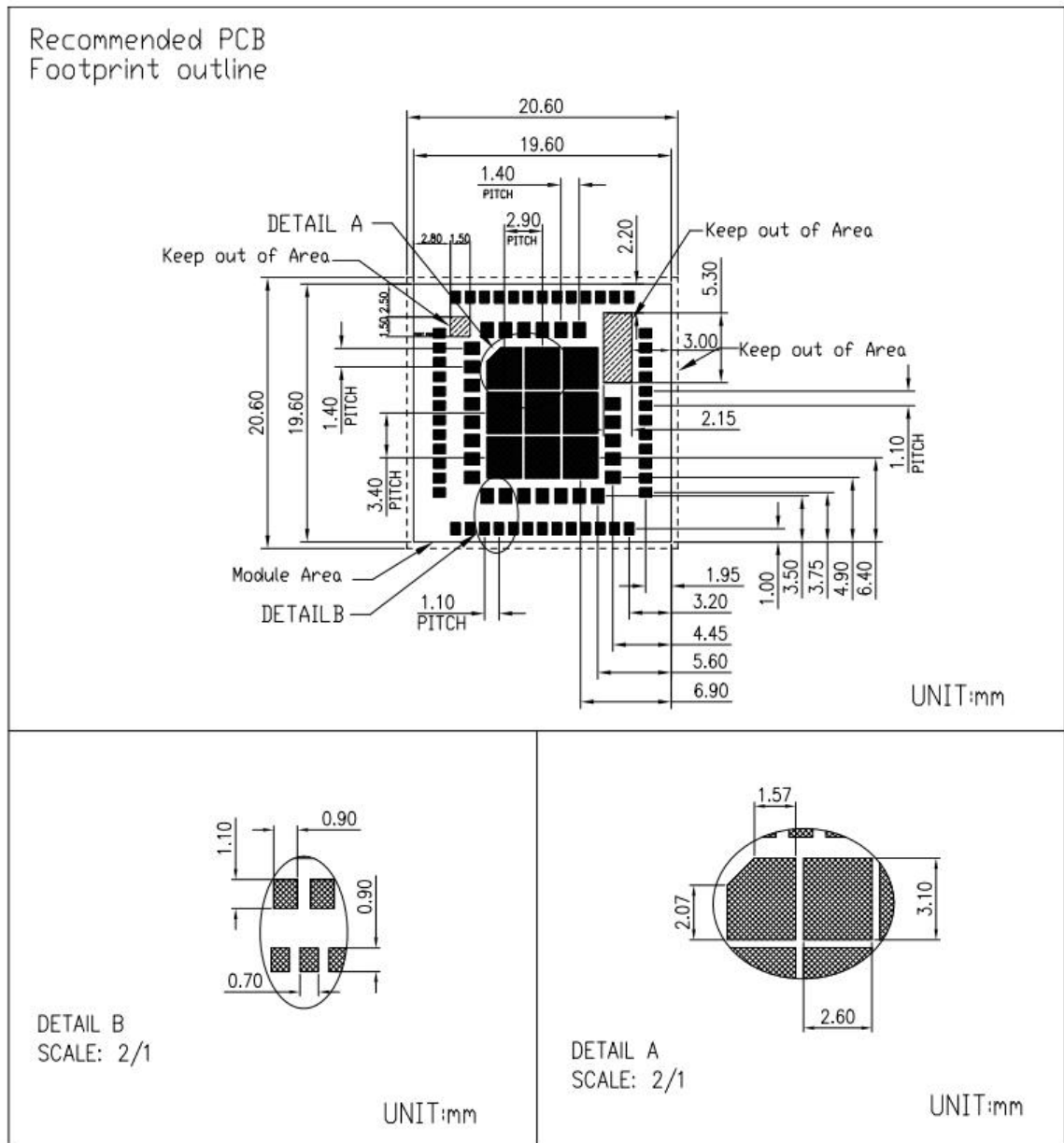


Figure 4: Recommend PCB footprint Dimension (Unit: mm)

## 2.5 Recommend Stencil Size

Recommend stencil thickness  $\geq 0.12\text{mm}$  and  $\leq 0.15\text{mm}$ .

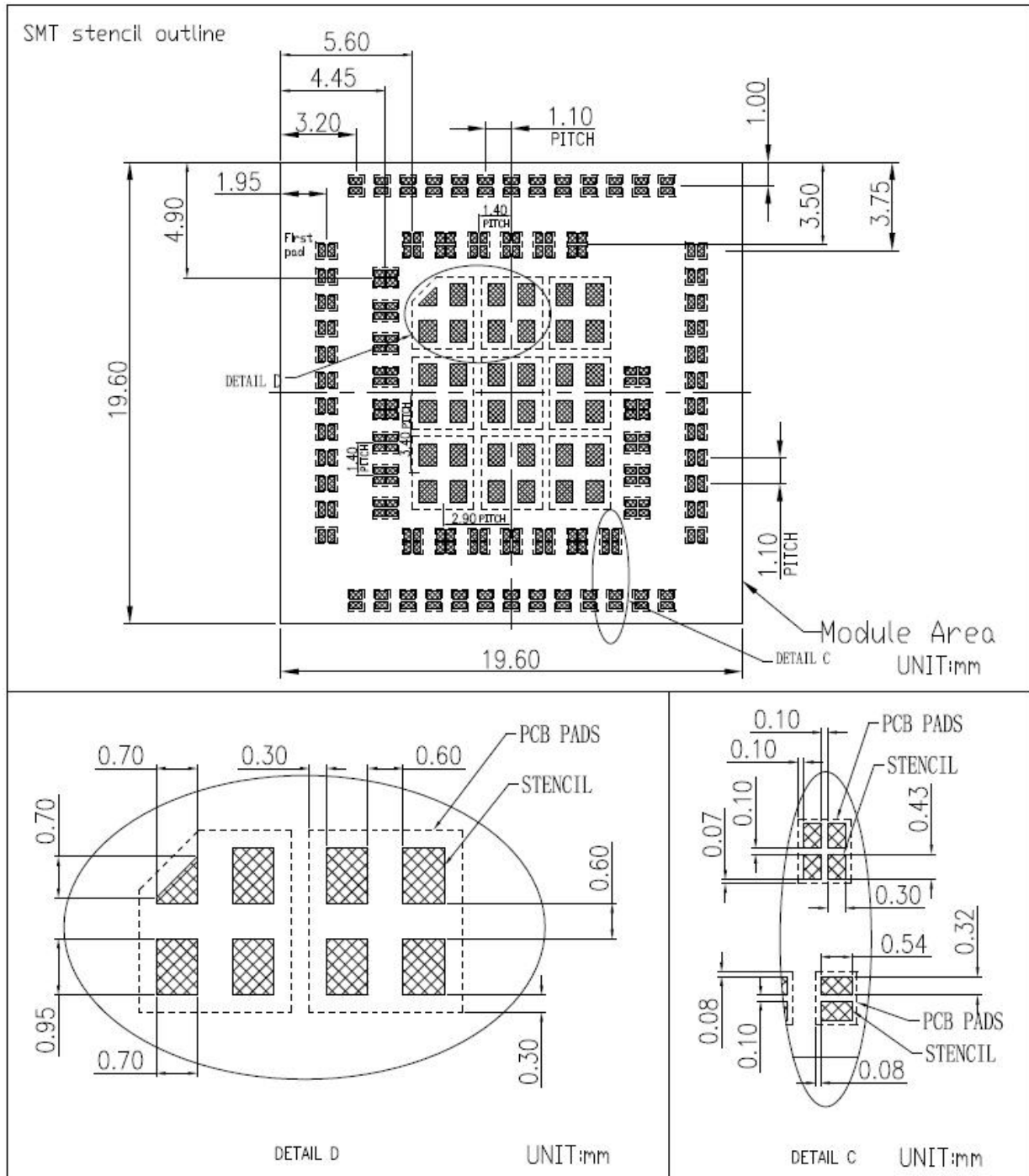


Figure 5: Recommend stencil dimension (Unit: mm)

## 3 Interface Application

### 3.1 Power Supply

A7682E offers two power supply PINs (34, 35) as VBAT power input PIN. A7682E use these PINs supply the internal RF and baseband circuit.

When the module is at the maximum power in GSM TX mode, the peak current can reach 2A (peak current), which results in a large voltage drop on VBAT. In order to ensure that the voltage drop is less than 300mV, the power supply capacity of external power supply must be no less than 2A.

The following figure shows the VBAT voltage drop.

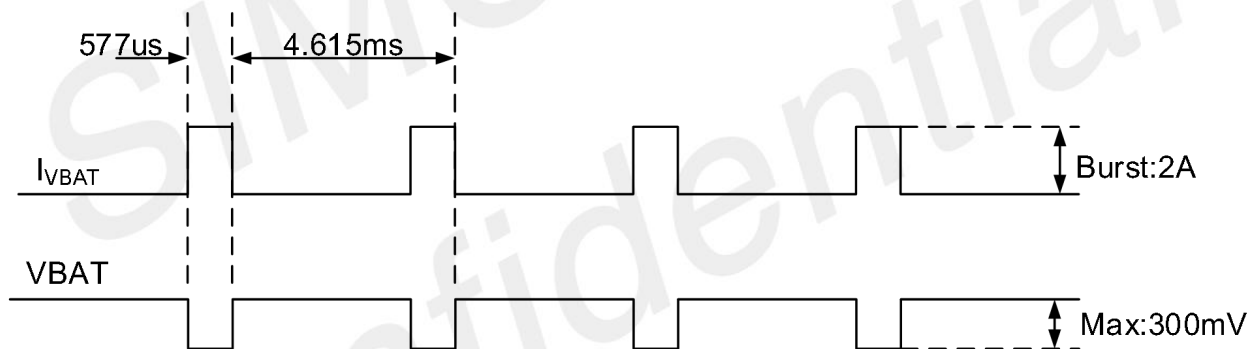


Figure 6: Burst current cause VBAT drop

#### NOTE

Test condition: VBAT power supply 3.8V, SIMCom TE board is used for test, add 330μF tantalum capacitor to VBAT power supply terminal.

Table 8: VBAT Pin electrical parameters

Parameter	Description	Min	Typ.	Max	Unit
VBAT	Module supply voltage	3.4	3.8	4.2	V
$I_{VBAT(peak)}$	Module consumption peak current	-	2	-	A
$I_{VBAT(average)}$	Module average consumption current (normal	Refer to table 35			

	mode)				
$I_{VBAT(sleep)}$	Module average consumption current (sleep mode)				
$I_{VBAT(power-off)}$	Module average consumption current (off leakage current)	-	30	-	$\mu A$

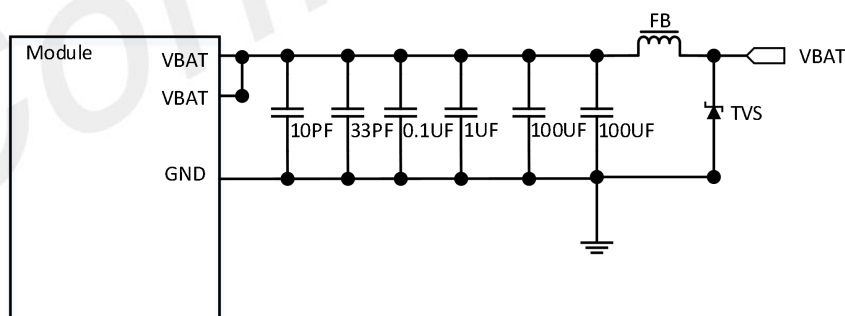
### 3.1.1 Power Supply Reference Design

In the user's design, make sure that the voltage on the VBAT pins will never drop below 3.4V even when the module current consumption reaches 2A. If the voltage drops below 3.4V, the RF performance of the module will be affected. It is recommended to select an LDO or DC-DC chip with an enable pin, and the enable pin is controlled by the MCU.

#### NOTE

When the power supply can provide a peak current of 2A, the total capacity of the external power supply capacitance is recommended to be no less than 300 $\mu f$ . If the peak current of 2A cannot be provided, the total capacity of the external capacitance is recommended to be no less than 600 $\mu f$  to ensure that the voltage drop on the VBAT pin at any time is not more than 300mV.

It is recommended to place four 0.1/ $1\mu F$  , 33/10pF ceramic capacitors near VBAT to improve RF performance and system stability. At the same time, it is recommended that the VBAT layout routing width from the power supply on the PCB to the module be at least 3mm. Reference design recommendations are as follows:



**Figure 7: VBAT input reference circuit**

If the VBAT input contains high-frequency interference, it is recommended to add magnetic beads for filtering. The recommended types of magnetic beads are BLM21PG300SN1D and MPZ2012S221A.

In addition, in order to prevent the damage of A7682E caused by surge and overvoltage, it is recommended to parallel one TVS on the VBAT pin of the module.



**Table 9: Recommended TVS diode list**

No.	Manufacturer	Part Number	$V_{RWM}$	Package
1	JCET	ESDBW5V0A1	5V	DFN1006-2L
2	WAYON	WS05DPF-B	5V	DFN1006-2L
3	WILL	ESD5611N	5V	DFN1006-2L
4	WILL	ESD56151W05	5V	SOD-323

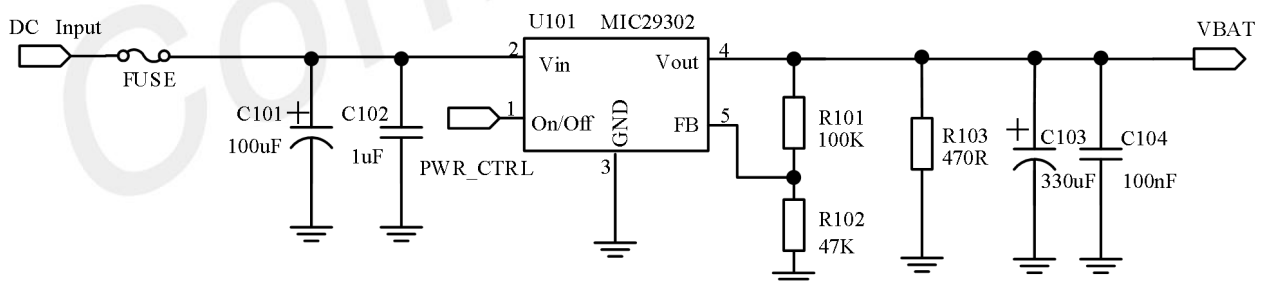
**NOTE**

When selecting TVS, pay attention to the clamping voltage for surge protection, the clamping voltage should not be higher than 10V for 100V surge input.

**3.1.2 Recommended Power Supply Circuit**

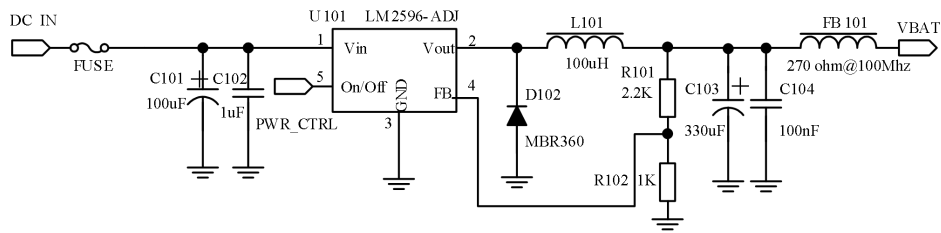
The MCU must have the function to power off the module, but the module can not be shut down or restarted normally. Only when the module is abnormal and cannot be shut down or restarted normally can the module be powered off. It is recommended that a switching mode power supply or a linear regulator power supply is used. DC-DC chip is recommended for input power greater than 9V; LDO power supply is recommended for input less than 9V.

The following figure shows the linear regulator reference circuit:



**Figure 8: Recommended circuit for linear power supply**

The following figure shows the DC-DC regulator reference circuit:



**Figure 9: Recommended circuits for switching power supply**

### 3.1.3 Voltage Monitor

AT command 'AT+CBC' can be used to monitor VBAT voltage.

AT command 'AT+CVALARM' can be used to set high/low voltage alarm, When the actual voltage exceeds the preset range, a warning message will be reported through the AT port.

AT command 'AT+CPMVT' can be used to set high/low voltage power off, When the actual voltage exceeds the preset range, the module will shut down automatically.

#### NOTE

Voltage monitoring function is being debugged, Overvoltage alarm and overvoltage shutdown are off by default. For details of at commands, please refer to document [1].

## 3.2 Power On/ Off and Reset

### 3.2.1 Module Power on

Customer can power on the module by pulling down the PWRKEY pin. This pin has been pulled up inside the module to VBAT.

It is recommended that when using the module, adding TVS diode at the module pin can effectively enhance the ESD performance.

The recommended circuit is as follows:

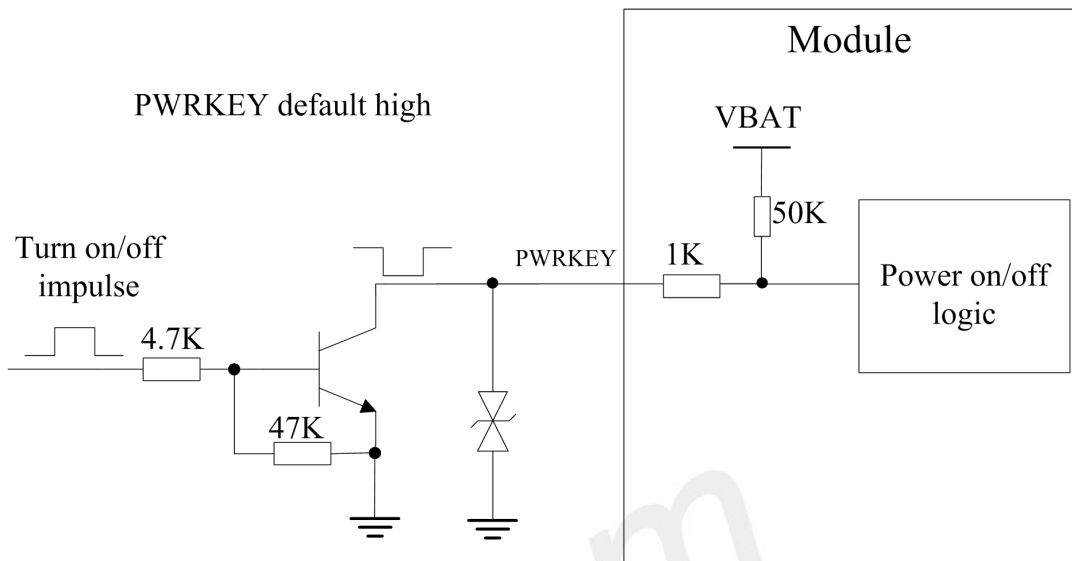


Figure 10: Power on/off reference circuit

**NOTE**

Do not parallel capacitors which the value is exceed 100nF on PWRKEY or RESET pin. It will cause module power on automatically when VBAT powered.  
It is forbidden to pull down both RESET key and PWRKEY to power on the module at the same time.

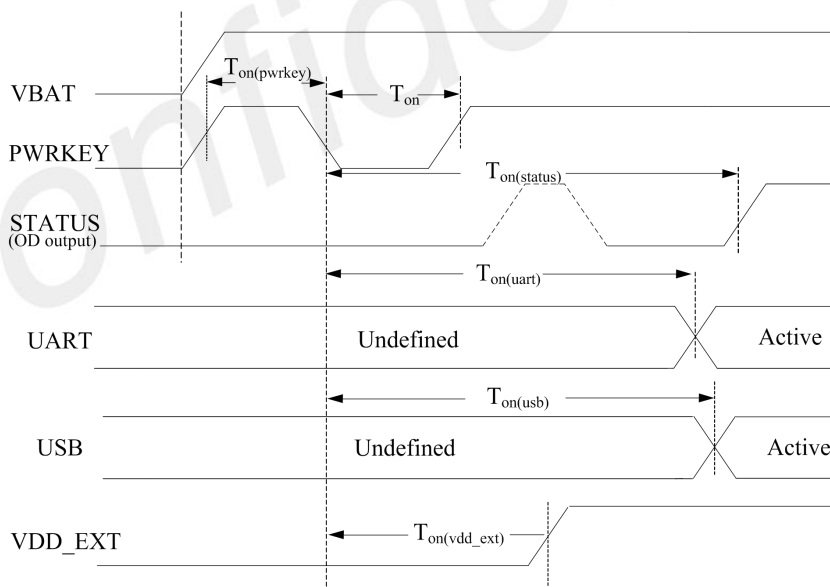


Figure 11: PWRKEY power on sequence

Table 10: Power on sequence parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{on(pwrkey)}$	The time from power on to pwrkey can be pulled down (the module can be normal)	-	30	-	ms
$T_{on}$	Power on low level pulse width	-	50	-	ms
$T_{on(status)}$	Power on time (according to Status interface)	-	7	-	s
$T_{on(uart)}$	Power on time (according to UART interface)	-	8	-	s
$T_{on(usb)}$	Power on time (according to USB interface)	-	9	-	s
$V_{IH}$	PWRKEY input high voltage level	$0.7 \cdot V_{BAT}$	-	$V_{BAT}$	
$V_{IL}$	PWRKEY input low voltage level	0	0	0.5V	

When the module is working, cutting off the power of the module will damage the flash. It is recommended to turn off the module through AT command or PWRKEY before disconnecting the power supply. When using the AT command to shut down, please ensure that the PWRKEY is at a high level; otherwise, the module will automatically power on again after the module completes the shutdown.

When the module is powered on, when the status pin is not externally connected with USB, press pwrkey, status will have a short pull-up pulse, and the module is powered on to complete the pull-up; When connecting the external USB, press pwrkey, the status status is always low, and the module is powered up and pulled up.

### 3.2.2 Module Power off

A7682E has the following shutdown methods:

- Power off by pulling the PWRKEY# pin down to a low level.
- Power off Module by AT command 'AT+CPOF'.
- Over-voltage or under-voltage automatic power off, 'AT+CPMVT' set voltage range
- Over-temperature or under-temperature automatic power off.

It is strongly recommended that the customer use PWRKEY or 'AT+CPOF' to shut down, and then power off VBAT (especially when the module does not need to work). In addition, the customer cannot shut down VBAT by disconnecting it, which may cause damage to FLASH.

#### NOTE

when the temperature exceeds the range of  $-30 \sim +80$  °C, A7682E will report warning information through AT port. When the temperature exceeds the range of  $-40 \sim +85$  °C, A7682E will shut down automatically. For a detailed description of 'AT+CPOF' and 'AT+CPMVT', please refer to document [1].

PWRKEY can be used to power off the module, power off sequence see the following figure:

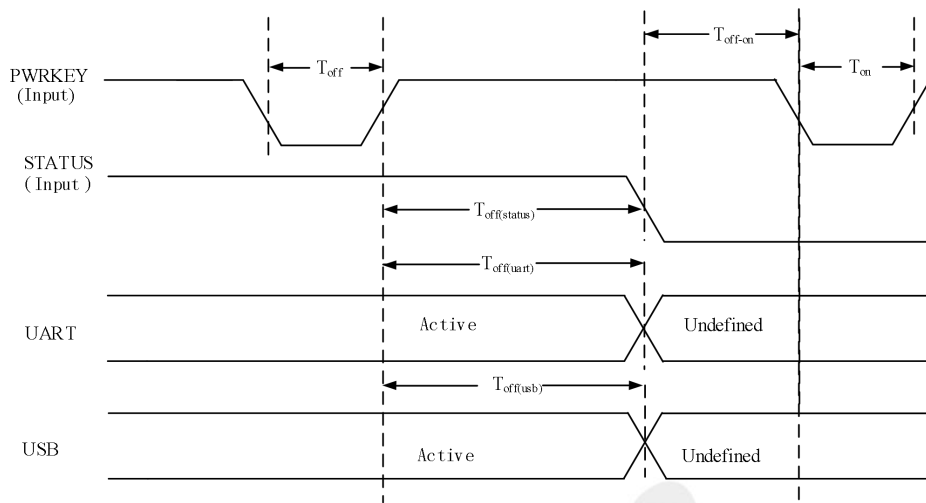


Figure 12: PWRKEY power off sequence

Table 11: Power off sequence parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{off}$	Power off low level pulse width	2.5	-	-	s
$T_{off(status)}$	Power off time(according to status interface)	-	2	-	s
$T_{off(uart)}$	Power off time(according to UART interface)	-	2	-	s
$T_{off(usb)}$	Power off time(according to USB interface)	-	2	-	s
$T_{off-on}$	Power off - power on buffer time	2	-	-	s

### 3.2.3 Module Reset

A7682E can restart the module by pulling down the reset pin of the module. Reset pin also has the function of power on when PMU first time be given a valid supply voltage (active low, but this key has no shutdown function). After first time power on, some register of this pin will be written then it will lose this function, so it is recommended to use PWRKEY to power on the module and RESET key only used as reset function.

A 50K  $\Omega$  resistor is used to pull-up to VBAT inside the module, so it is no need to add pull-up resistor outside. The recommended circuit is showed as follows:

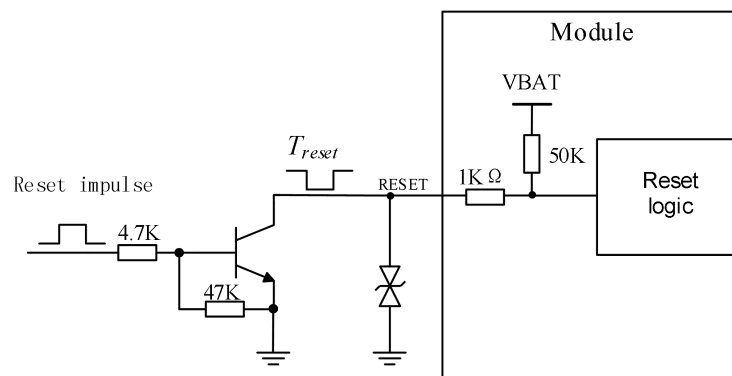


Figure 13: Reference reset circuit

Table 12: RESET electric parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
T <sub>reset</sub>	Restart low level pulse width	2	2.5	-	S
V <sub>IH</sub>	RESET pin input high voltage	0.7*VBAT	-	VBAT	V
V <sub>IL</sub>	RESET pin input low voltage	0	0	0.3*VBAT	V

**NOTE**

It is recommended to use the reset pin only in case of emergency, such as the module is not responding. The reset time is recommended to be 2.5s.

### 3.3 UART

A7682E provides three serial ports, the main communication serial port UART, one ordinary two-wire serial port, and the UART\_LOG dedicate to printing log. Module is DCE (Data Communication Equipment) equipment.

When using the full function serial port, you can refer to the following connection mode:

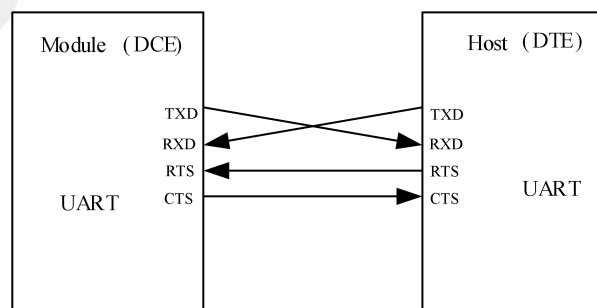
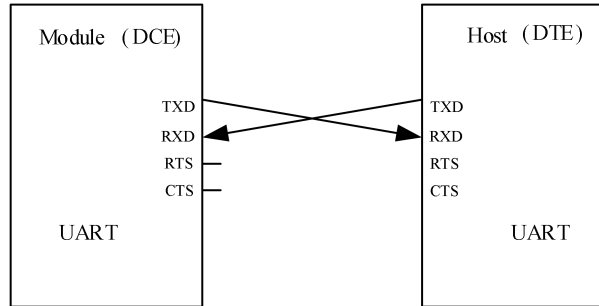


Figure 14: Serial port connection diagram (full function mode)

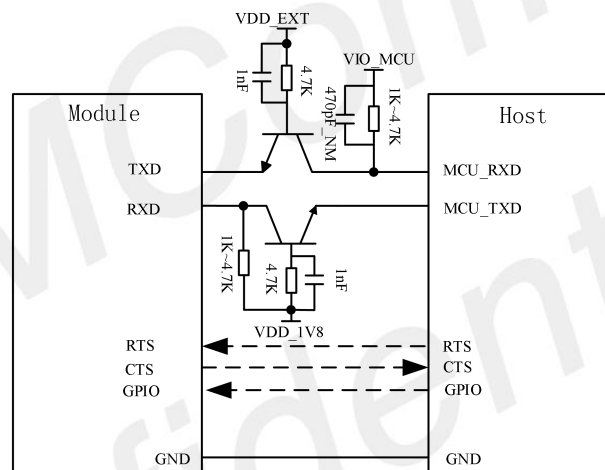
When using 2-wire serial port, please refer to the following connection mode:



**Figure 15: Serial port connection diagram (NULL mode)**

The following figure shows the use of triode for level shifter circuits. The circuit with dotted line can refer to the circuit with solid line TXD and RXD, and attention shall be paid to the direction of signal.

The recommended triode model is MMBT3904.



**Figure 16: Triode level conversion circuit**

**NOTE**

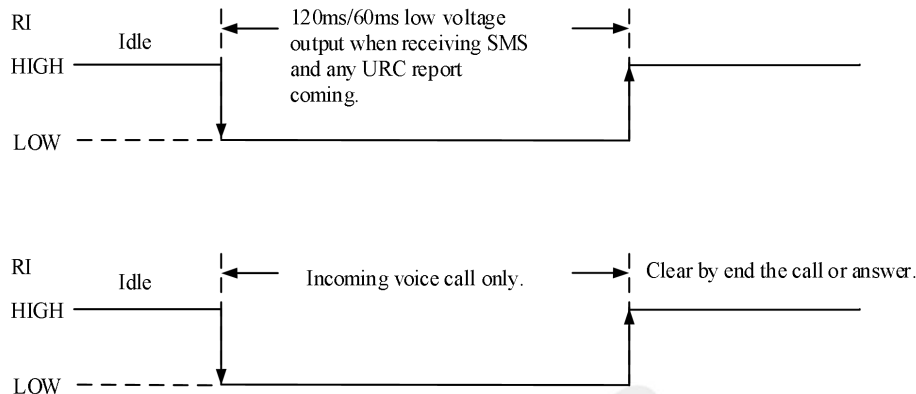
1. A7682E supports the following baud rates: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, 1842000, 3686400. The default baud rate is 115200bps.

2. The parasitic capacitance of the transistor will affect the edge of the high-speed digital signal. It is not recommended to use this circuit when the signal speed is higher than 115200bps.

**3.3.1 RI/DTR description**

The RI pin can be used as an interrupt to wake up the host. Normally, it maintains a high voltage output. When a short message or URC report is received, RI outputs a low voltage for 120ms (SMS)/60ms (URC), and then returns to a high voltage state; RI will output low voltage. When receiving a telephone call as the

called party, RI outputs low voltage, and then it will remain low voltage until the host accepts the call using the "ATA" command, or the caller stops calling RI will resume outputting high level.



**Figure 17: Level change on RI (SMS, URC, Incoming call)**

DTR can be used as the sleep wake-up pin of the A7682E module. When the A7682E module enters the sleep mode, pull down DTR to wake up the A7682E module.

When the user sets 'AT+CSCLK=1' and pulls up the DTR pin, the module will enter the sleep mode. The serial port function cannot communicate. When the A7682E module enters sleep mode, pull DTR low to wake up.

In the mode of setting "AT+CSCLK=0", pull up the DTR pin, the normal communication of the serial port function will not be affected.

### 3.4 USB Interface

A7682E contains a USB interface compliant with the USB2.0 specification as a peripheral, but does not support USB charging function and does not support USB HOST mode.

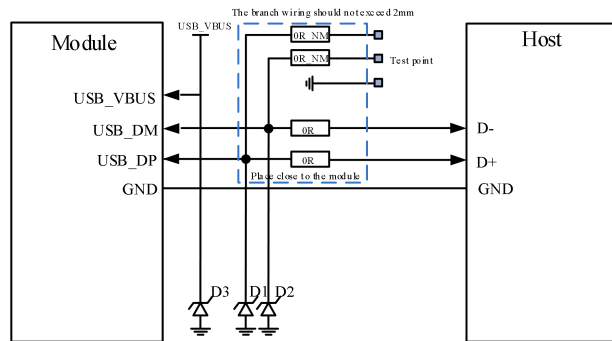
Support high speed (480Mbps) and full speed (12Mbps). The interface can be used for AT command sending, data transmission, software debugging and upgrading. Map out ttyUSB1-ttyUSB2 under Linux or android system (refer to Linux or android debugging document for details).

USB is the main debugging port and software upgrade interface. It is recommended that customers reserve USB test points during design. If a main control chip is connected, 0R resistors must be reserved for switching external test points during design, as shown in the figure below.



### 3.4.1 USB Reference Design

A7682E can be used as a USB slave device. The recommended connection circuit diagram is as follows:



**Figure 18: USB circuit diagram**

Customers should pay attention to the selection of the D3 device when using it. It is recommended to choose an anti-static and anti-surge two-in-one device. A TVS tube can be placed. The recommended model is ESD5681N07.

#### NOTE

1. The USB data cable must be strictly routed in  $90\Omega \pm 10\%$  differential. The TVS devices D1 and D2 on the data line must be selected with equivalent capacitance less than 1pF. The TVS device should be placed near the USB connector or test point, recommended models ESD73011N and WS05DUCFM.
2. The detection of USB2.0 speed is determined automatically by the USB protocol. The customer does not need to pull up the DP external, otherwise it may affect the device USB enumeration.

### 3.4.2 BOOT\_CFG Interface

A7682E provides one forced download boot interface 'BOOT\_CFG'.

**Table 13: BOOT\_CFG description**

Pin number	Pin name	I/O	Description	Power domain	Default state	Remark
82	BOOT_CFG	DI	Force download boot port	1.8V	B-PU	

If the module upgrade fails to boot, you can force upgrade through the BOOT\_CFG port.

Before the module is powered on, pull the BOOT\_CFG pin to GND, then apply VBAT power to the module, and press RESET to enter the download mode. After entering the download mode, you need to release BOOT\_CFG and remove the pull-down.

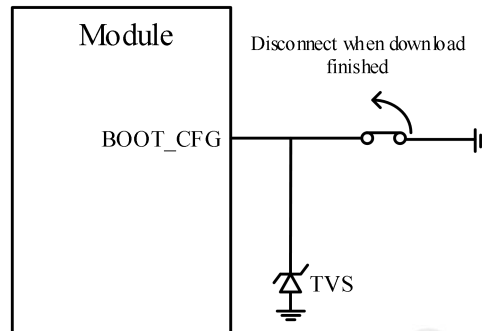


Figure 19: Reference BOOT\_CFG circuit

Customers will see the download port in the device manager port of the Windows system.



Figure 20: Force-download port

**NOTE**

BOOT\_CFG only has the function of forcing download and booting before booting (it cannot be pulled down).

### 3.5 sUSIM Interface

A7682E supports both 1.8V and 3.0V USIM Cards. The interface power of the USIM card is provided by the voltage regulator inside the module, and the normal voltage value is 3V or 1.8V.

Table 14: USIM electronic characteristic in 1.8V mode (USIM\_VDD=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	Power supply voltage output to USIM card	1.62	1.8	1.98	V

V <sub>IH</sub>	High-level input voltage	0.7*USIM_VDD	-	USIM_VDD +0.4	V
V <sub>IL</sub>	Low-level input voltage	-0.4	0	0.25*USIM_VDD	V
V <sub>OH</sub>	High-level output voltage	USIM_VDD -0.4	-	USIM_VDD	V
V <sub>OL</sub>	Low-level output voltage	0	0	0.2	V

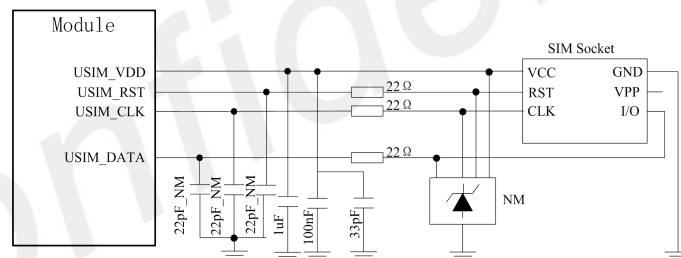
**Table 15: USIM electronic characteristic in 3.0V mode (USIM\_VDD=3V)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	Power supply voltage output to USIM card	2.7	3	3.3	V
V <sub>IH</sub>	High-level input voltage	0.7*USIM_VDD	-	USIM_VDD +0.4	V
V <sub>IL</sub>	Low-level input voltage	-0.4	0	0.25*USIM_VDD	V
V <sub>OH</sub>	High-level output voltage	USIM_VDD -0.45	-	USIM_VDD	V
V <sub>OL</sub>	Low-level output voltage	0	0	0.3	V

### 3.5.1 USIM Application Guide

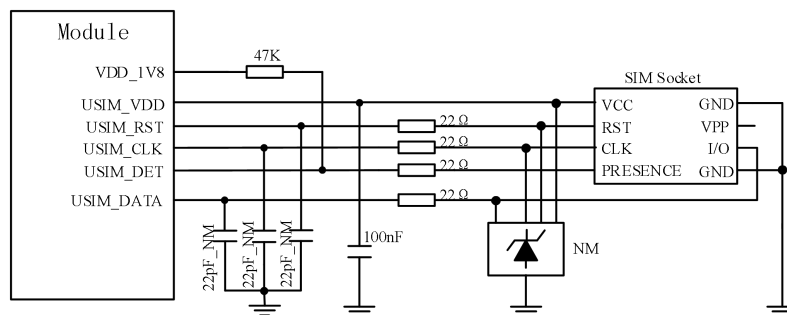
It is recommended to use an ESD protection component such as ESDA6V1W5 produced by ST ([www.st.com](http://www.st.com)) or SMF15C produced by ON SEMI ([www.onsemi.com](http://www.onsemi.com)). Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

The following figure shows the 6-pin SIM card holder reference circuit.



**Figure 21: USIM interface reference circuit (6PIN)**

The following figure shows the 8-pin SIM card holder reference circuit.



**Figure 22: USIM interface reference circuit (8PIN)**

## NOTE

USIM\_DATA has been pulled up with a 4.7K $\Omega$  resistor to USIM\_VDD in module. A 100nF capacitor on USIM\_VDD is used to reduce interference. For more details of AT commands about USIM, please refer to document [1].

Because the SIM card circuit is susceptible to interference, causing the card not to be recognized or dropped, please follow the following principles when designing:

- During the PCB layout stage, keep the USIM card holder away from the main antenna.
- The USIM card wiring should be kept away from RF lines, VBAT and high-speed signal lines as much as possible, and the USIM card wiring should not be too long.
- The GND of the USIM card holder and the GND of the module maintain good connectivity, so that the GNDs of the two are equal in potential.
- To prevent USIM\_CLK from interfering with other signals, it is recommended to protect USIM\_CLK separately.
- It is recommended to place a 220nF capacitor on the USIM\_VDD signal line close to the USIM card socket.
- It is recommended to place a 3.3V TVS close to the USIM card socket to enhance the ESD protection performance. The parasitic capacitance of TVS should not be greater than 50pF.
- Connecting a 22 $\Omega$  resistor in series between the USIM card socket and the module can enhance the ESD protection performance.
- In order to make the wiring smooth, it is recommended to use a single-channel TVS, placed close to each pin of the card socket.
- The USIM\_CLK signal is very important. Customers should ensure that the rising edge and falling edge time of the USIM\_CLK signal are less than 40ns, otherwise, abnormal card recognition may occur.

### 3.5.2 Recommend USIM Card Holder

It is recommended to use the 6-pin USIM socket such as C707 10M006 512 produced by Amphenol. User can visit <http://www.amphenol.com> for more information about the holder.

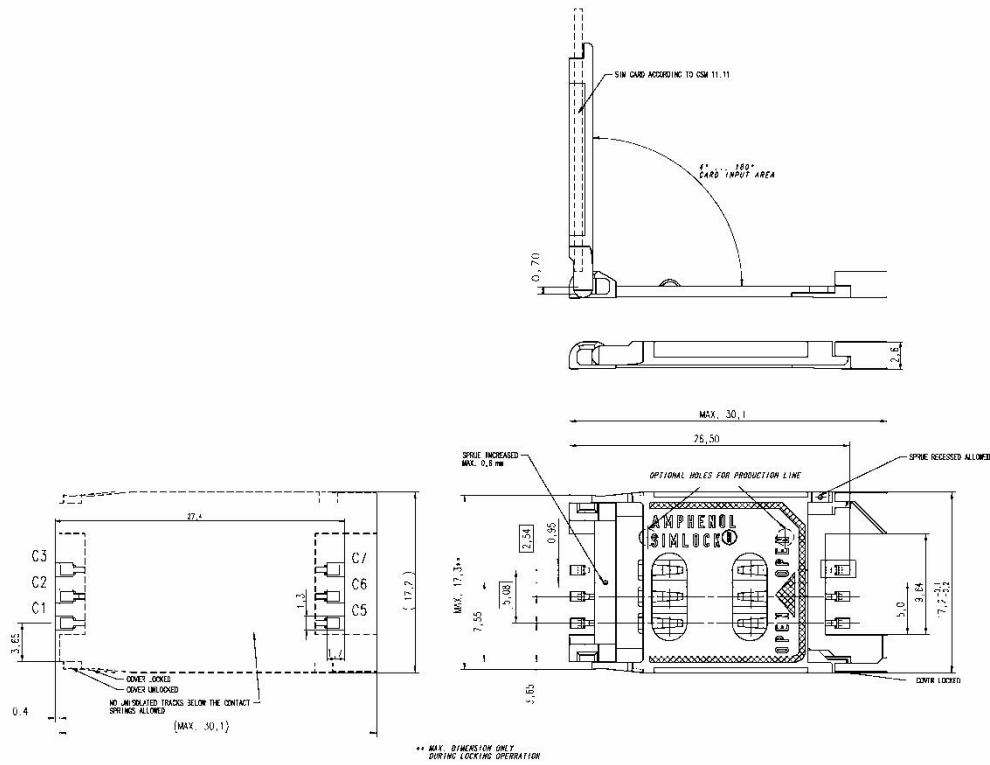


Figure 23: Amphenol C707 10M006 512 USIM card socket

Table 16: Amphenol USIM socket pin description

Pin	Signal	Description
C1	USIM_VDD	USIM Card Power supply.
C2	USIM_RST	USIM Card Reset.
C3	USIM_CLK	USIM Card Clock.
C5	GND	Connect to GND.
C6	VPP	NC
C7	USIM_DATA	USIM Card data I/O.

**NOTE**

When customers design in-vehicle products, please choose a more reliable SIM card holder with push-push structure.

### 3.6 Analog audio interface

A7682E integrates audio codec and audio front-end, provides 1 set of MIC analog audio interface, 1 set of SPK analog audio interface. Customers can connect the phone handle for voice calls.

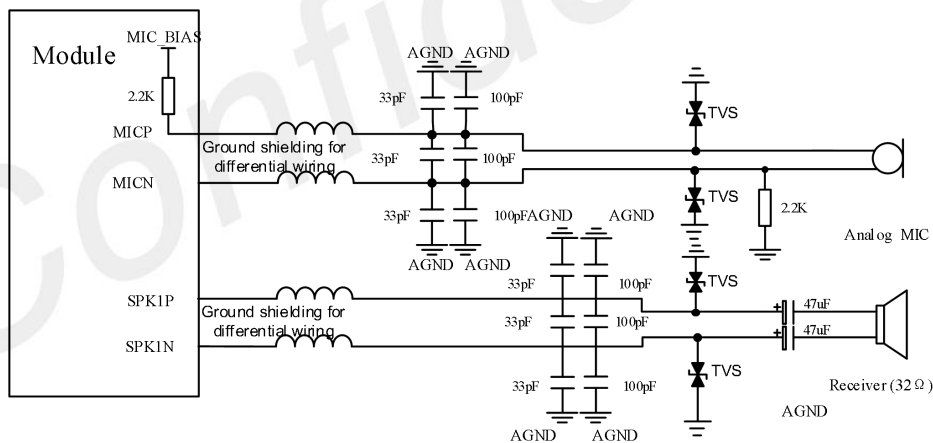
- ADC: 90dB SNR@20~20KHz
- DAC: 95dB SNR@20~20KHz
- Class-AB: THD<-85dB@32-ohm Load
- SPK1P SPK1N Support earpiece output

**Table 17: Analog MIC input ADC parameter table**

parameter	conditions	DR (Typical)	THD+N ( Typical )	Maximum power
ADC	RL=10K	101dBA	-96dB(@vout -2dBv)	1.59Vp
Class-AB	Mono,32Ω Difference	100dBA	-90dB(0.00316%) (@20mW output)	37mW

#### 3.6.1 Analog Audio Reference Design

The recommended circuit for analog audio is shown below:



**Figure 24: Analog audio interface reference circuit**

### 3.7 GPIO Interface

A7682E module provides 6 GPIOs.

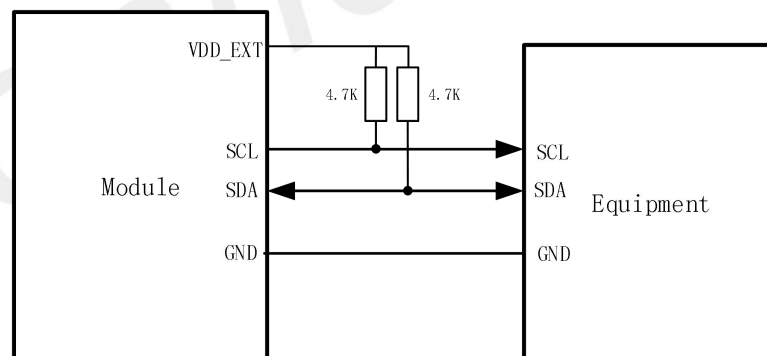
**Table 18: GPIO Resource List**

Pin No.	Pin name	AT command operation number	GPIO	Pin typ.	Power domain	Default function	Pad Edge wakeup
57	GPIO1	GPIO1		IO,PD	1.8V	GPIO	Yes
58	GPIO2	GPIO2		IO,PD	1.8V	GPIO	Yes
78	GPIO3	GPIO3		IO,PD	1.8V	GPIO	Yes
79	GPIO4	GPIO4		IO,PD	1.8V	GPIO	Yes
80	GPIO5	GPIO5		IO,PD	1.8V	GPIO	Yes
81	GPIO6	GPIO6		IO,PD	1.8V	GPIO	Yes

### 3.8 I2C Bus

The module provides a sets of I2C interface, supports standard speed clock rate 100Kbps, support high speed clock rate 400Kbps, its operation voltage is 1.8V.

I2C is open-drain output, and the reference circuit is as follows:



**Figure 25: I2C reference circuit**

#### NOTE

The SCL and SDA pins have no internal pull-up resistors, and the reserved pull-up power must be VDD\_EXT output by the module.

### 3.9 Network status

The NETLIGHT pin is used to control network status LED, its reference circuit is shown in the following figure.

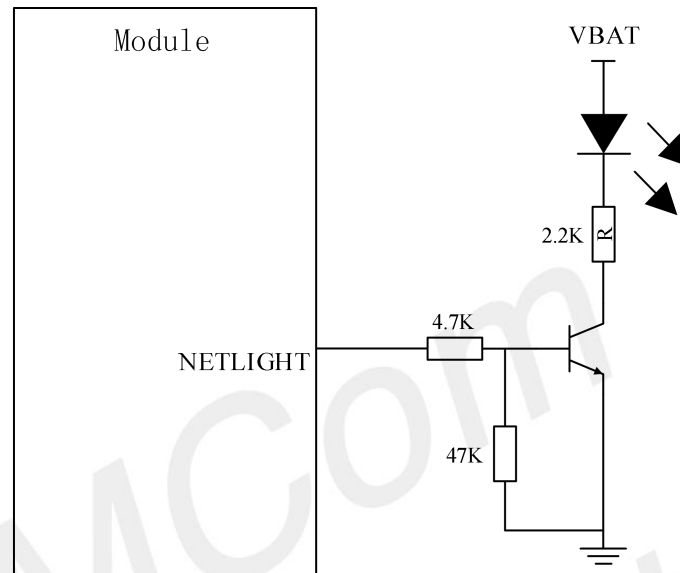


Figure 26: NETLIGHT reference circuit

#### NOTE

The value of the resistor named 'R' depends on the LED characteristic.

The NETLIGHT signal is used to control the LED lights that indicate the status of the network. The working status of this pin is shown in the table below.

Table 19: 2G mode NETLIGHT pin status

NETLIGHT pin status	Module status
Always On	Searching Network
200ms ON, 200ms OFF	Data Transmit
800ms ON, 800ms OFF	Registered network
OFF	Power off / AT+CSCLK=1, and DTR is pulled high.



**Table 20: LTE mode NETLIGHT pin status**

NETLIGHT pin status	Module status
Always On	Searching Network
200ms ON, 200ms OFF	Data Transmit/Registered
OFF	Power off / AT+CSCLK=1, and DTR is pulled high.

## 3.10 Other interface

### 3.10.1 ADC

The A7682E module provides 1 ADC, and its electrical characteristics are as follows:

**Table 21: ADC electronic characteristics**

Characteristics	Min.	Typ.	Max.	Unit
Resolution	–	9	–	bits
Input Range	0	–	1.8	V

#### NOTE

The function of using "AT+CADC" to read the voltage value of the ADC pin is under debugging. For more information, please refer to document [1].

### 3.10.2 LDO

A7682E module provides one power output: VDD\_EXT.

VDD\_EXT is the module's system IO power supply, which can only provide a current capacity of 50mA. It cannot be used as a high current drive source.

**Table 22: VDD\_EXT Electrical characteristics**

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>VDD_EXT</sub>	Output voltage	-	1.8	-	V
I <sub>o</sub>	Output current	-	-	50	mA

**NOTE**

This power supply is the system power supply. If the damage will affect the system startup, it is recommended that customers add TVS protection. The recommended model is ESD56051N.

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## 4 RF Specifications

### 4.1 GSM/LTE

Table 23: Conducted emission power

Frequency	power	Minimum power
EGSM900(GMSK)	33dBm $\pm$ 2dB	5dBm $\pm$ 5dB
DCS1800(GMSK)	30dBm $\pm$ 2dB	0dBm $\pm$ 5dB
EGSM900 (8-PSK)	27dBm $\pm$ 3dB	5dBm $\pm$ 5dB
DCS1800 (8-PSK)	26dBm +3/-4dB	0dBm $\pm$ 5dB
LTE-FDD B1	23dBm +/-2.7dB	<-40dBm
LTE-FDD B3	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B7	23dBm +/-2.7dB	<-40dBm
LTE-FDD B8	23dBm +/-2.7dB	<-40dBm
LTE-FDD B20	23dBm +/-2.7dB	<-40dBm

Table 24: GSM Operating bands

Frequency	DL	UL
EGSM900	925~960MHz	880~915 MHz
DCS1800	1805~1880 MHz	1710~1785 MHz

Table 25: E-UTRA operating bands

E-UTRA BAND	UL	DL	Duplex Mode
1	1920 ~1980 MHz	2110 ~2170 MHz	FDD
3	1710 ~1785 MHz	1805 ~1880 MHz	FDD
5	824~849 MHz	869~894MHz	FDD
7	2500~2570MHz	2620~2690MHz	FDD
8	880 ~915 MHz	925 ~960 MHz	FDD
20	832~862MHz	791~ 821MHz	FDD

Table 26: Conducted receive sensitivity

Frequency	Sensitivity ( TYP )	Sensitivity ( MAX )
EGSM900	< -109dBm	3GPP
DCS1800	< -108dBm	3GPP
LTE FDD	See table 28.	3GPP

Table 27: Reference sensitivity (QPSK)

E-UTRA band	3GPP Standard (unit:dBm)						Measured 10 MHz	Duplex Mode
	1.4 MHz	3MHz	5MHz	10MHz	15 MHz	20 MHz		
1			-100	-97	-95.2	-94	-97	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	-96	FDD
5	-103.2	-100.2	-98	-95			-99	FDD
7			-98	-95	-93.2	-92	-96.5	FDD
8	-102.2	-99.2	-97	-94			-99	FDD
20			-97	-94	-91.2	-90	-96.5	FDD

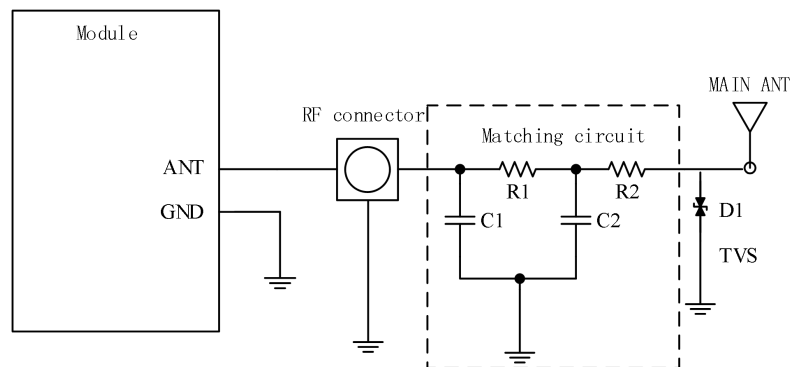
## 4.2 GSM/ LTE Antenna Reference Design

For better overall performance, it is recommended that the antenna design refer to the index requirements in the following table.

Table 28: GSM/LTE antenna requirements

Parameter	Requirement
operating band	See table 25 and table 26
Direction	omnidirectional
Gain	> -3dBi (Avg)
Input impedance	50 ohm
Efficiency	> 50 %
Maximum input power	50W
VSWR	< 2
Isolation	>20dB
PCB insertion loss(<1GHz)	<0.5dB
PCB insertion loss(1GHz~2.2GHz)	<1dB
PCB insertion loss(2.3GHz~2.7GHz)	<1.5dB

### 4.3 Antenna reference design



**Figure 27: Passive antenna connection circuit**

In above figure, the component R1/R2/C1/C2 is reserved for antenna matching, the value of components can only be got after the antenna tuning, usually provided by the antenna factory. Among them, R1 and R2 paste 0Ω, C1 and C2 do not paste by default. The component D1 is a Bidirectional ESD Protection device, which is suggested to add to protection circuit, the recommended Part Numbers of the TVS are listed in the following table:

**Table 29: TVS recommended part list**

Package	Part	Vendor
0201	CE0201S05G01R	SOCAY
0402	PESD0402-03	PRISEMI

### 4.4 PCB layout

Users should pay attention to the impedance design of PCB layout from the module ANT port to the antenna connector, and the length of the PCB trace should be within 20 mm, and far away from interference signals such as power & clock. It is recommended to reserve RF Switch Connector for conduction test. The reference model of RF Switch Connector is: ECT 818011998.

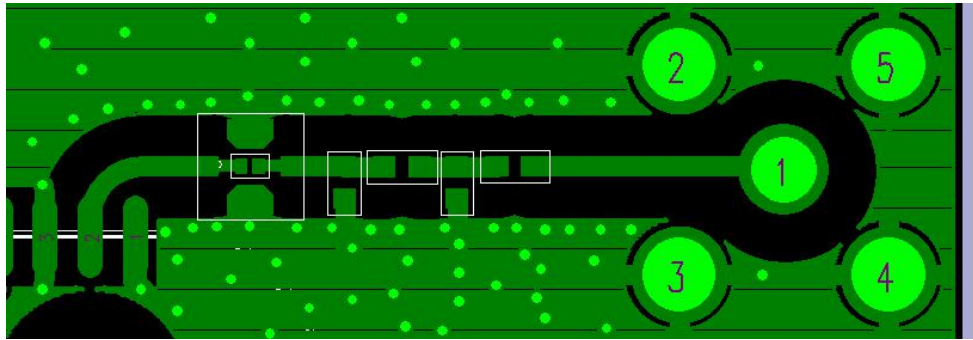


Figure 28: Reference PCB layout

## 5 Electrical Specifications

### 5.1 Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of A7682E are listed in the following table, exceeding these limits may cause permanent damage to the module.

Table 30: Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	-0.5	-	4.8	V
Voltage at VBUS	-0.5	-	5.4	V
Voltage at digital pins (GPIO, I2C, UART)	-0.3	-	2.0	V
Voltage at digital pins (USIM)	-0.3	-	2.0	V
	-0.3	-	3.9	V
Voltage at PWRKEY、RESET	-0.3	-	4.8	V

### 5.2 Operating conditions

Table 31: Recommended operating ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	3.4	3.8	4.2	V

Voltage at VBUS	3.0	5.0	5.2	V
-----------------	-----	-----	-----	---

**Table 32: 1.8V Digital I/O characteristics\***

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	High-level input voltage	VCC*0.7	1.8	VCC+0.2	V
V <sub>IL</sub>	Low-level input voltage	-0.3	0	VCC*0.3	V
V <sub>OH</sub>	High-level output voltage	VCC-0.2	-	-	V
V <sub>OL</sub>	Low-level output voltage	0	-	0.2	V
I <sub>OH</sub>	High-level output current(no pull down resistor)	-	-	13	mA
I <sub>OL</sub>	Low-level output current(no pull up resistor)	-	-	13	mA
I <sub>IH</sub>	Input high leakage current (no pull down resistor)	-	-	10	uA
I <sub>IL</sub>	Input low leakage current(no pull up resistor)	-10	-	-	uA

**NOTE**

These parameters are for digital interface pins, such as GPIO , I2C, UART.

**Table 33: Operating temperature**

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature	-30	25	80	°C
Extended operation temperature	-40	25	85	°C
Storage temperature	-45	25	+90	°C

**NOTE**

The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

## 5.3 Operating Mode

### 5.3.1 Operating Mode Definition

The table below summarizes the various operating modes of A7682E product.

**Table 34: Operating mode Definition**

Mode		Function
Normal operation	GSM/ LTE Sleep	In this case, the current consumption of module will be reduced to the minimal level and the module can still receive paging message and SMS.
	GSM /LTE Idle	Software is active. Module is registered to the network, and the module is ready to communicate.
	GSM / LTE Talk	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings .
	GSM /LTE Standby	Module is ready for data transmission, but no data is currently sent or received. In this case, power consumption depends on network settings.
	GPRS/EDGE/LTE Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g. power control level); uplink/downlink data rates, and the network configuration (e.g. multi-slot configuration).
Minimum functionality mode		AT command 'AT+CFUN=0' can be used to set the module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the module will not work and the USIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode		AT command 'AT+CFUN=4' or pulling down the FLIGHTMODE pin can be used to set the module to flight mode without removing the power supply. In this mode, the RF part of the module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Power off		Module will go into power off mode by sending the AT command 'AT+CPOF' or pull down the PWRKEY pin, normally. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are is not accessible.



### 5.3.2 Sleep mode

In sleep mode, the current consumption of module will be reduced to the minimal level, and module can still receive paging message and SMS.

Several hardware and software conditions must be satisfied together in order to let A7682E enter into sleep mode:

- UART condition
- USB condition
- Software condition

For more information about sleep mode, please refer to document [24].

### 5.3.3 Minimum functionality mode and Flight mode

The command "AT+CFUN=<fun>" can set the module to this mode. This command provides three options for setting different functions.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If A7682E has been set to minimum functionality mode, the RF function and USIM card function will be closed. In this case, the serial port and USB are still accessible, but RF function and USIM card and some AT commands will be unavailable.

If A7682E has been set to flight mode, the RF function will be closed. In this case, the serial port and USB are still accessible, but RF function and some AT commands will be unavailable.

When A7682E is in minimum functionality or flight mode, it can return to full functionality by the AT command 'AT+CFUN=1'.

For detailed information about the "AT+CFUN" command, please refer to the document [1].

## 5.4 Current Consumption

The current consumption is listed in the table below.

**Table 35: Current consumption on VBAT Pins (VBAT=3.8V)**

#### GSM sleep/idle mode

GSM/GPRS supply current (without USB connection)	Sleep mode @ BS_PA_MFRMS=2	Typical: 3mA
	Idle mode @ BS_PA_MFRMS=2	Typical: 16mA

#### LTE sleep/idle mode

LTE supply current (without USB connection)	Sleep mode Typical: 2mA Idle mode Typical: 12mA
<b>GSM Talk</b>	
EGSM 900	@ power level #5 Typical: 264mA
DCS1800	@ power level #0 Typical: 193mA
<b>GPRS data</b>	
EGSM 900 ( 1 Rx,4 Tx)	@ power level #5 Typical: 582mA
DCS1800 ( 1 Rx,4 Tx)	@ power level #0 Typical: 398mA
EGSM 900 ( 3 Rx,2 Tx)	@ power level #5 Typical: 450mA
DCS1800 ( 3 Rx,2 Tx)	@ power level #0 Typical: 315mA
<b>EDGE data</b>	
EGSM 900 ( 1 Rx,4 Tx)	@ power level #8 Typical: 316mA
DCS1800 ( 1 Rx,4 Tx)	@ power level #2 Typical: 307mA
EGSM 900 ( 3 Rx,2 Tx)	@ power level #8 Typical: 244mA
DCS1800 ( 3 Rx,2 Tx)	@ power level #2 Typical: 206mA
<b>LTE data</b>	
LTE-FDD B1	@5MHz 23.0dBm Typical: 693mA @10MHz 23.0dBm Typical: 694mA
LTE-FDD B3	@5MHz 23.0dBm Typical: 566mA @10MHz 23.0dBm Typical: 587mA
LTE-FDD B5	@5MHz 23.0dBm Typical: 534mA @10MHz 23.0dBm Typical: 554mA
LTE-FDD B7	@5MHz 23.0dBm Typical: 832mA @10MHz 23.0dBm Typical: 837mA
LTE-FDD B8	@5MHz 23.0dBm Typical: 588mA @10MHz 23.0dBm Typical: 417mA
LTE-FDD B20	@5MHz 23.0dBm Typical: 541mA @10MHz 23.0dBm Typical: 588mA

## 5.5 ESD Notes

A7682E is an electrostatic sensitive device. Users must pay attention to electrostatic protection when producing, assembling and operating the module. The electrostatic performance parameters of the module are as follows:

**Table 36: The ESD performance measurement table (Temperature: 25°C, Humidity: 45%)**

Part	Contact discharge	Air discharge
VBAT,GND	+/-6K	+/-12K
Antenna port	+/-5K	+/-10K
USB	+/-6K	+/-12K

Other PADS

+/-1K

+/-2K

**NOTE**

Test condition is module pasted on SIMcom Development board (With ESD components).

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## 6 SMT Production Guide

### 6.1 Top and Bottom View of A7682E

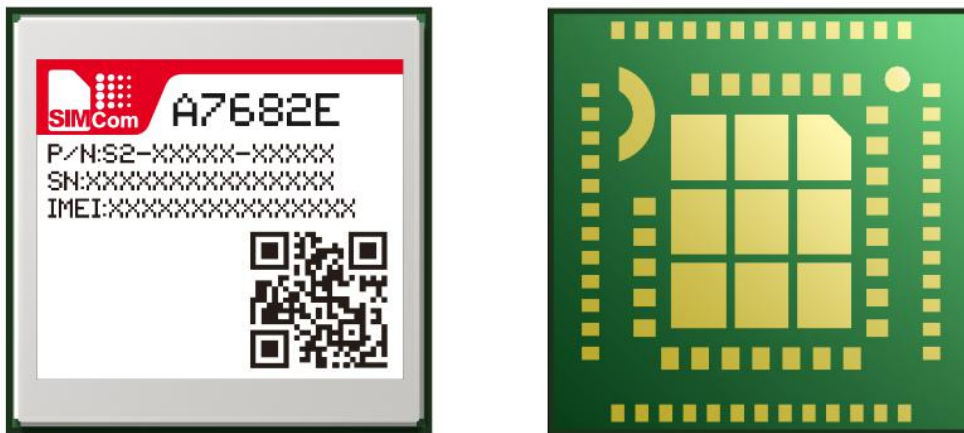


Figure 29: Top and bottom view of A7682E

#### NOTE

The above is the design effect diagram of the module for reference. The actual appearance is subject to the actual product.

## 6.2 Label Information

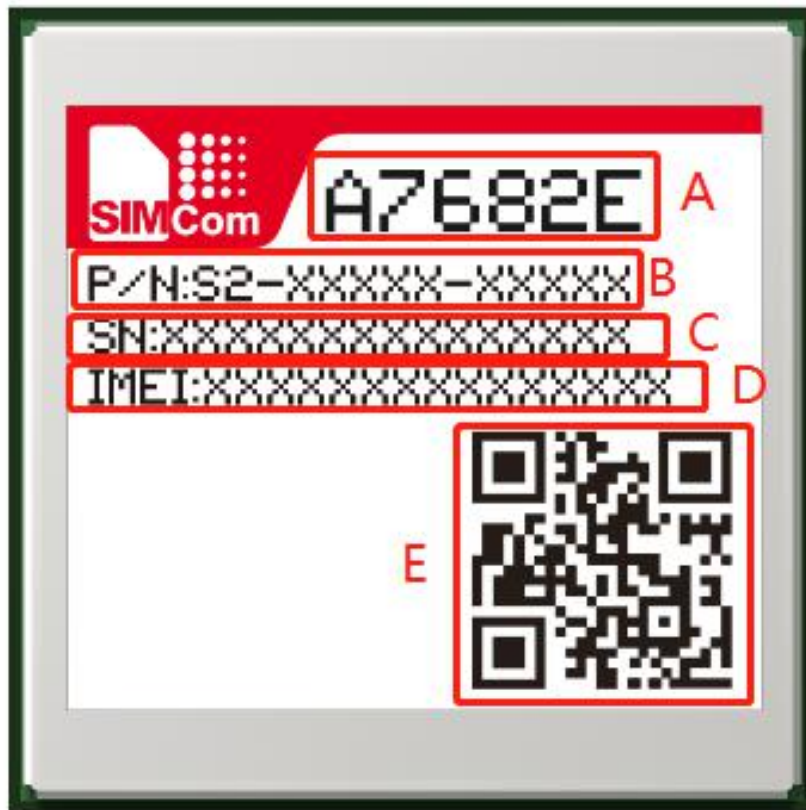


Figure 30: Label information

Table 37: The description of label information

No.	Description
A	Project name
B	Product code
C	Serial number
D	Module IMEI number
E	QR code

### 6.3 Typical SMT Reflow Profile

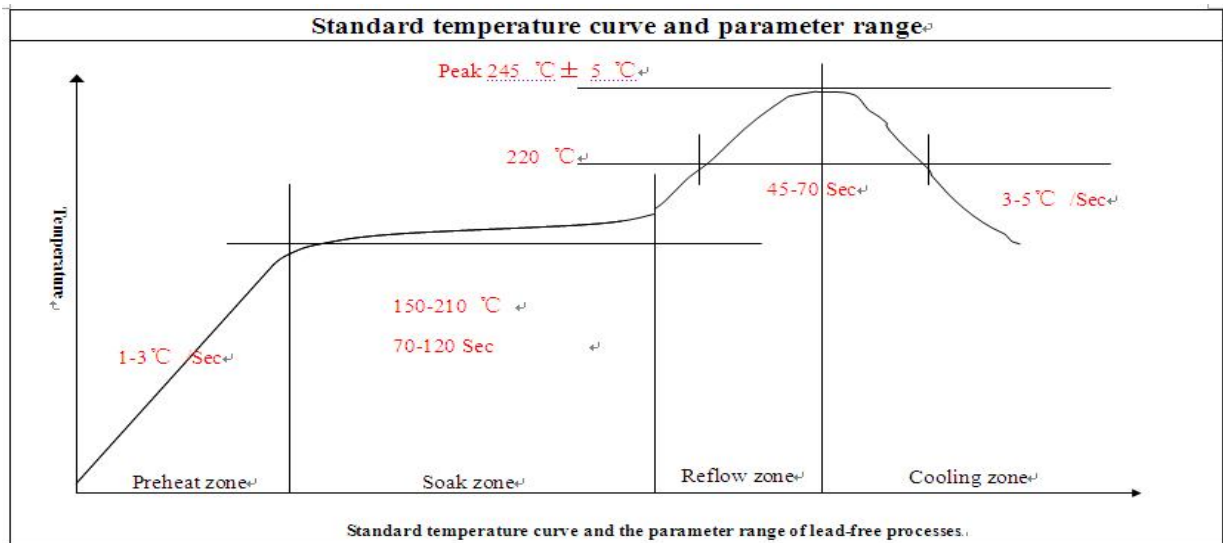


Figure 31: The ramp-soak-spike reflow profile of A7682E

**NOTE**

For more details about secondary SMT, please refer to the document [21].

### 6.4 Moisture Sensitivity Level (MSL)

A7682E is qualified to Moisture Sensitivity Level (MSL) 3 in accordance with JEDEC J-STD-033.

In the following two cases, the A7682E module should be fully baked before reflow soldering, otherwise the module may cause permanent damage during the reflow soldering process.

After unpacking or vacuum packaging is damaged and leaks, the A7682E module needs to be SMT patched within 168 hours under environmental conditions of temperature <30 degrees and relative humidity <60%. If the above conditions are not met, bake is required.

If the vacuum packaging is not opened, but the shelf life has expired, baking is also required.

Bake conditions: users should bake modules for 192 hours in drying equipment (<5% RH) at 40+5/-0°C, or 72 hours at 85+5/-5°C. (If using a tray, please pay attention to whether the tray is resistant to thermal deformation).

**Table 38: Moisture Sensitivity Level and Floor Life**

Moisture Sensitivity Level (MSL)	Floor Life (out of bag) at factory ambient $\leq 30^{\circ}\text{C}/60\% \text{RH}$ or as stated
1	Unlimited at $\leq 30^{\circ}\text{C}/85\% \text{RH}$
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.

**NOTE**

IPC / JEDEC J-STD-033 standard must be followed for production and storage.

## 7 Packaging

A7682E support tray packaging.

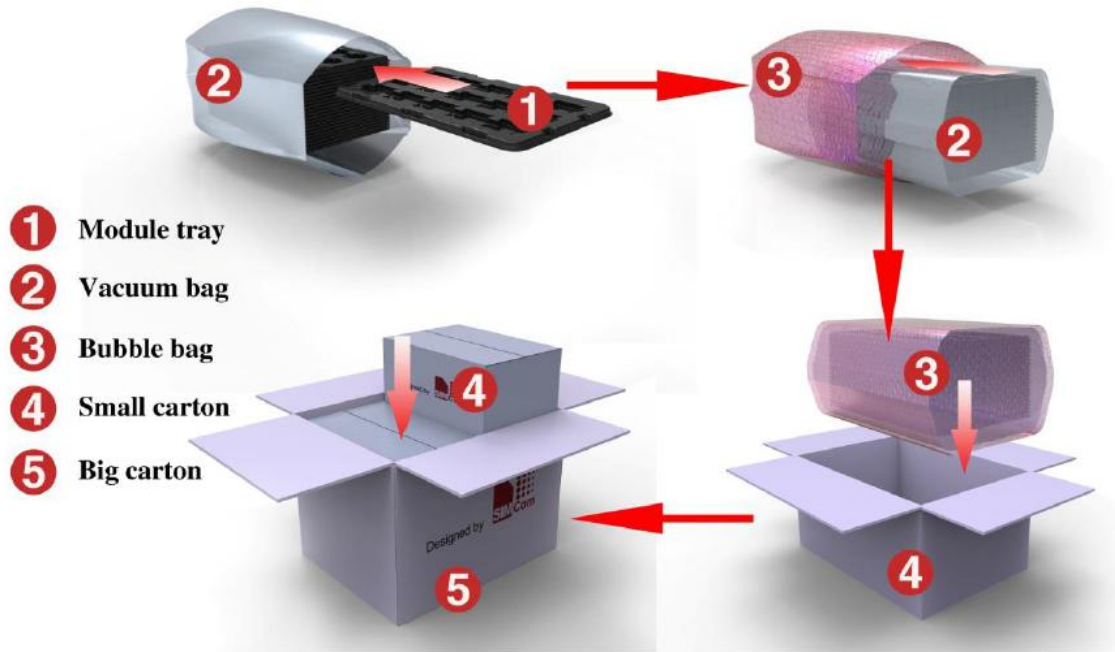


Figure 32: packaging diagram

Module tray drawing:

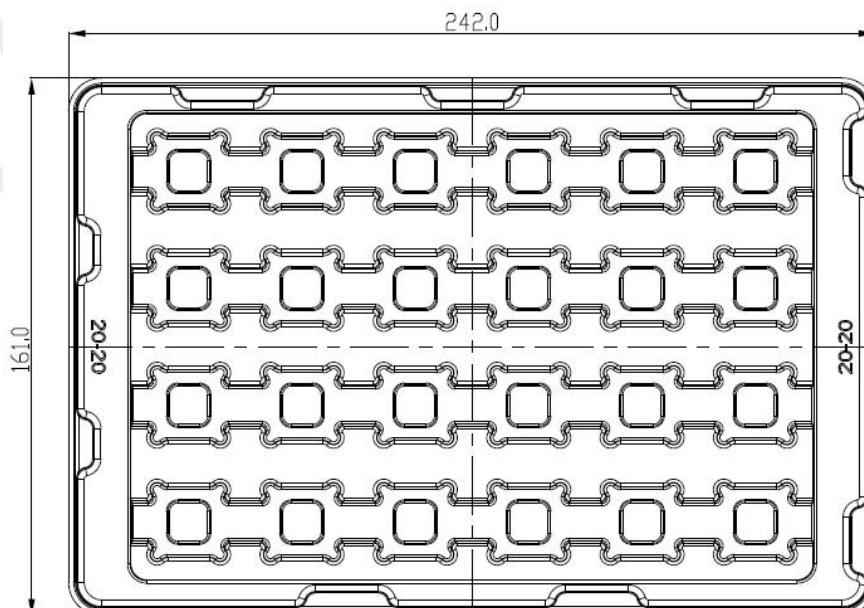




Figure 33: Tray drawing

Table 39: Tray size

Length ( ±3mm )	Width ( ±3mm )	number
242.0	161.0	24

Small carton drawing:

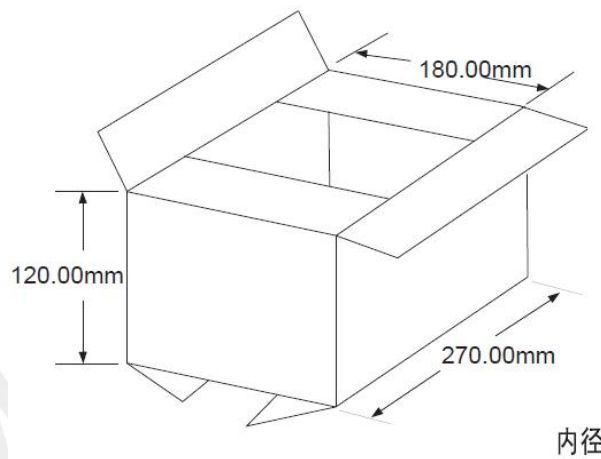


Figure 34: Small carton drawing

Table 40: Small Carton size

Length ( ±10mm )	Width ( ±10mm )	Height ( ±10mm )	number
270	180	120	24*20=480

Big carton drawing:

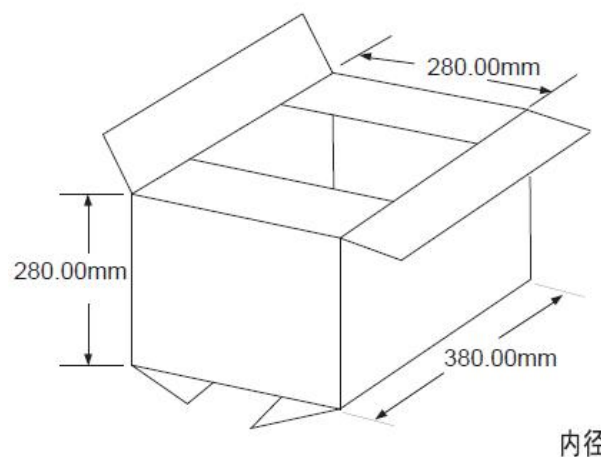


Figure 35: Big carton drawing

Table 41: Big Carton size

Length ( ±10mm )	Width ( ±10mm )	Height ( ±10mm )	number
380	280	280	480*4=1920

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## 8 Appendix

### 8.1 Coding Schemes and Maximum Net Data Rates over Air Interface

Table 42: Coding Schemes and Maximum Net Data Rates over Air Interface

Multi slot definition (GPRS/EDGE)			
Slot class	DL slot number	UL slot number	Active slot number
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
GPRS coding scheme	Max data rate (4 slots)		Modulation type
CS 1 = 9.05 kb/s / time slot	36.2 kb/s		GMSK
CS 2 = 13.4 kb/s / time slot	53.6 kb/s		GMSK
CS 3 = 15.6 kb/s / time slot	62.4 kb/s		GMSK
CS 4 = 21.4 kb/s / time slot	85.6 kb/s		GMSK
EDGE coding scheme	Max data rate (4 slots)		Modulation type
MCS 1 = 8.8 kb/s/ time slot	35.2 kb/s		GMSK
MCS 2 = 11.2 kb/s/ time slot	44.8 kb/s		GMSK
MCS 3 = 14.8 kb/s/ time slot	59.2 kb/s		GMSK
MCS 4 = 17.6 kb/s/ time slot	70.4 kb/s		GMSK
MCS 5 = 22.4 kb/s/ time slot	89.6 kb/s		8PSK
MCS 6 = 29.6 kb/s/ time slot	118.4 kb/s		8PSK
MCS 7 = 44.8 kb/s/ time slot	179.2 kb/s		8PSK
MCS 8 = 54.4 kb/s/ time slot	217.6 kb/s		8PSK
MCS 9 = 59.2 kb/s/ time slot	236.8 kb/s		8PSK
HSDPA device category	Max data rate (peak)		Modulation type

Category 1	1.2Mbps	16QAM,QPSK
Category 2	1.2Mbps	16QAM,QPSK
Category 3	1.8Mbps	16QAM,QPSK
Category 4	1.8Mbps	16QAM,QPSK
Category 5	3.6Mbps	16QAM,QPSK
Category 6	3.6Mbps	16QAM,QPSK
Category 7	7.2Mbps	16QAM,QPSK
Category 8	7.2Mbps	16QAM,QPSK
Category 9	10.2Mbps	16QAM,QPSK
Category 10	14.4Mbps	16QAM,QPSK
Category 11	0.9Mbps	QPSK
Category 12	1.8Mbps	QPSK
Category 13	17.6Mbps	64QAM
Category 14	21.1Mbps	64QAM
Category 15	23.4Mbps	16QAM
Category 16	28Mbps	16QAM
Category 17	23.4Mbps	64QAM
Category 18	28Mbps	64QAM
Category 19	35.5Mbps	64QAM
Category 20	42Mbps	64QAM
Category 21	23.4Mbps	16QAM
Category 22	28Mbps	16QAM
Category 23	35.5Mbps	64QAM
Category 24	42.2Mbps	64QAM
<b>HSUPA device category</b>	<b>Max data rate (peak)</b>	<b>Modulation type</b>
Category 1	0.96Mbps	QPSK
Category 2	1.92Mbps	QPSK
Category 3	1.92Mbps	QPSK
Category 4	3.84Mbps	QPSK
Category 5	3.84Mbps	QPSK
Category 6	5.76Mbps	QPSK
<b>LTE-FDD device category (Downlink)</b>	<b>Max data rate (peak)</b>	<b>Modulation type</b>
Category 1	10Mbps	QPSK/16QAM/64QAM
Category 2	50Mbps	QPSK/16QAM/64QAM
Category 3	100Mbps	QPSK/16QAM/64QAM
Category 4	150Mbps	QPSK/16QAM/64QAM
<b>LTE-FDD device category (Uplink)</b>	<b>Max data rate (peak)</b>	<b>Modulation type</b>
Category 1	5Mbps	QPSK/16QAM
Category 2	25Mbps	QPSK/16QAM

Category 3	50Mbps	QPSK/16QAM
Category 4	50Mbps	QPSK/16QAM

## 8.2 Related Documents

**Table 43: Related Documents**

NO.	Title	Description
[1]	A7600 Series_AT Command Manual_V1.00.04	AT Command Manual
[2]	ITU-T Draft new recommendation V.25ter	Serial asynchronous automatic dialing and control
[3]	GSM 07.07	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[4]	GSM 07.10	Support GSM 07.10 multiplexing protocol
[5]	GSM 07.05	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[6]	GSM 11.14	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[7]	GSM 11.11	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[8]	GSM 03.38	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[9]	GSM 11.10	Digital cellular telecommunications system (Phase 2) ; Mobile Station (MS) conformance specification ; Part 1: Conformance specification
[10]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[11]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[12]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[13]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[14]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[15]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[16]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for

		IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment
[17]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[18]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[19]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[20]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
[21]	Module secondary-SMT-UGD-V1.xx	Module secondary SMT Guidelines
[22]	A7600Series_UART_Application Note_V1.xx	This document describes how to use UART interface of SIMCom modules.
[23]	Antenna design guidelines for diversity receiver system	Antenna design guidelines for diversity receiver system
[24]	A7600 Series_SleepMode_Application Note_V1.xx	Sleep Mode Application Note

### 8.3 Terms and Abbreviations


**Table 44: Terms and Abbreviations**






Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated

MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
<b>PB abbreviation</b>	
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

## 8.4 Safety Caution

Table 45: Safety Caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.

	<p>Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.</p>
	<p>Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.</p>
	<p>Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.</p>
	<p>Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.</p>
	<p>GSM cellular terminals or mobiles operate over radio frequency signals and cellular networks and cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.</p> <p>Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call.</p> <p>Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.</p>