SiT1552

Smallest (1.2mm^2), Smallest (1.2mm2), Ultra-Low Power, 32.768 kHz

Features

- 32.768 kHz ±5, ±10, ±20 ppm frequency stability options over temp
- World's smallest TCXO in a 1.5 x 0.8 mm CSP
- Operating temperature ranges:
  - 0°C to +70°C
  - -40°C to +85°C
- Ultra-low power: <1 µA
- Vdd supply range: 1.5V to 3.63V
- Improved stability reduces system power with fewer network timekeeping updates
- Internal filtering eliminates external Vdd bypass cap and saves space
- Pb-free, RoHS and REACH compliant

Applications

- Smart Meters (AMR)
- Health and Wellness Monitors
- Pulse-per-Second (pps) Timekeeping
- RTC Reference Clock

TempFlat MEMS™

INSTANT SAMPLES | SEARCH INVENTORY | GREEN SOLUTIONS | LIFETIME WARRANTY

Electrical Specifications

Table 1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Frequency Stability Over Temperature[1] (without Initial Offset[2])	F_stab	-5.0		5.0	ppm	Stability part number code = E
		-10		10		Stability part number code = F
		-20		20		Stability part number code = 1
Frequency Stability Over Temperature (with Initial Offset[2])	F_stab	-10		10	ppm	Stability part number code = E
		-13		13		Stability part number code = F
		-22		22		Stability part number code = 1
Frequency Stability vs Voltage	F_vdd	-0.75		0.75	ppm	1.8V ±10%
		-1.5		1.5	ppm	1.5V – 3.63V
First Year Frequency Aging	F_aging	-1.0		1.0	ppm	T_A = 25°C, Vdd = 3.3V
Jitter Performance (T_A = over temp)						
Long Term Jitter				2.5	μs_{pp}	81920 cycles (2.5 sec), 100 samples
Period Jitter			35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5V – 3.63V
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.5		3.63	V	T_A = -40°C to +85°C
Core Supply Current[3]	Idd		0.99		µA	T_A = 25°C, Vdd = 1.8V, LVCMOS Output configuration, No Load
				1.52		T_A = -40°C to +85°C, Vdd = 1.5V – 3.63V, No Load
Power-Supply Ramp	t_Vdd_Ramp			100	ms	Vdd Ramp-Up 0 to 90% Vdd, T_A = -40°C to +85°C
Start-up Time at Power-up	t_start		180	300	ms	T_A = -40°C +60°C, valid output
				350		T_A = +60°C to +70°C, valid output
				380		T_A = +70°C to +85°C, valid output

Notes:

1. No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and ±20% load variation. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
2. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled Calculating Load Current.

Table 1. Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Temperature Range						
Commercial Temperature	Op_Temp	0		70	°C	
Industrial Temperature		-40		85	°C	
LVCMOS Output						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90% (Vdd), 15 pF Load
				50		10-90% (Vdd), 5 pF Load, Vdd ≥ 1.62V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V – 3.63V. I_{OH} = -1 µA, 15 pF Load
Output Voltage Low	VOL			10%	V	Vdd: 1.5V – 3.63V. I_{OL} = 1 µA, 15 pF Load

Table 2. Pin Configuration

CSP Pin	Symbol	I/O	Functionality
1, 4	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground. The GND pins can be connected together, as long as both GND pins are connected ground.
2	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The SIT1552 oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
3	Vdd	Power Supply	Connect to power supply 1.5V ≤ Vdd ≤ 3.63V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see Power-Supply Noise Immunity section in the detailed description. Contact SiTime for applications that require a wider operating supply voltage range.

CSP Package (Top View)

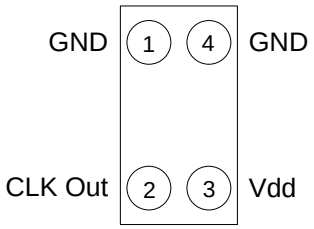


Figure 1. Pin Assignments

System Block Diagram

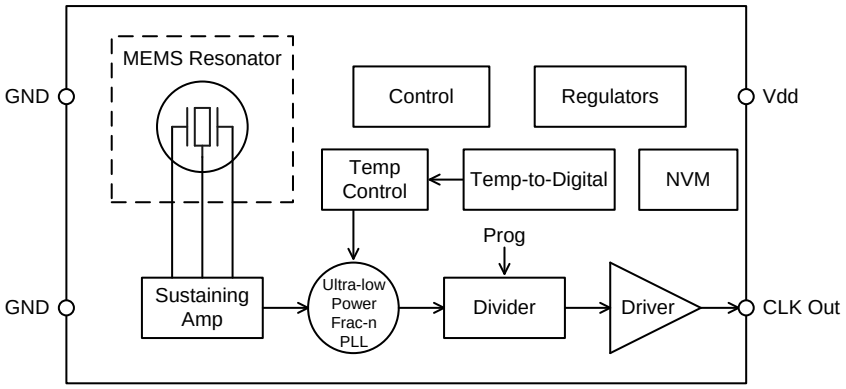


Figure 2. SiT1552 Block Diagram

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD22- C101	750	V
Machine Model (MM) ESD Protection	JESD22- A115	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	*g*
Mechanical Vibration Resistance	Mil 883, Method 2007	70	*g*
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

Description

The SiT1552 is an ultra-small and ultra-low power 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical core supply current is only 1 µA.

SiTime's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

TCXO Frequency Stability

The SiT1552 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C2 temperature coefficient, the SiT1552 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range. Contact SiTime for applications that require a wider supply voltage range >3.63V, or lower operating frequency below 32 kHz.

When measuring the SiT1552 output frequency with a frequency counter, it is important to make sure the counter's gate time is >100 ms. The slow frequency of a 32kHz clock will give false readings with faster gate times.

Power Supply Noise Immunity

In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor to keep the footprint as small as possible. Internal power supply filtering is designed to reject more than ±150 mV noise and frequency components from low frequency to more than 10 MHz.

Start-up and Steady-State Supply Current

The SiT1552 TCXO starts-up to a valid output frequency within 300 ms (180 mstyp). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 – 20 ms (to within 90% of Vdd).

During initial power-up, the SiT1552 power-cycles internal blocks, as shown in the power-supply start-up and steady state plot in the Typical Operating Curves section. Power-up and initialization is typically 200 ms, and during that time, the peak supply current reaches 28 µA as the internal capacitors are charged, then sequentially drops to its 990 nA steady-state current. During steady-state operation, the internal temperature compensation circuit turns on every 350 ms for a duration of approximately 10 ms.

Calculating Load Current

No Load Supply Current

When calculating no-load power for the SIT1552, the core and output driver components need to be added. Since the output voltage swing can be programmed to minimize load current, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) = Idd Core + Idd Output Driver

Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 990nA (typ)
- Voutpp = 1.8V
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA
- Supply Current = 990nA + 206nA = 1.2µA

Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below.

Total Current = Idd Core + Idd Output Driver + Load Current

Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 990n
- Load Capacitance = 10pF
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA
- Load Current: (10pF)(1.8V)(32768Hz) = 590nA
- Total Current = 990nA + 206nA + 590nA = 1.79µA

Typical Operating Curves

(T_A = 25°C, Vdd = 1.8V, unless otherwise stated)

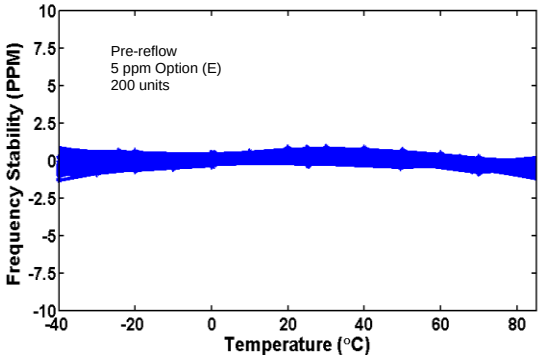


Figure 3. Frequency Stability Over Temperature (Pre-Reflow)

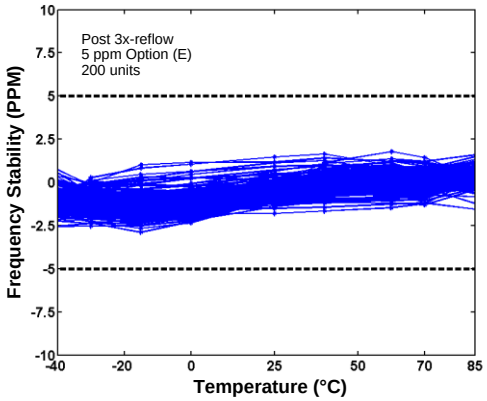


Figure 4. Frequency Stability Over Temperature (Post-Reflow)

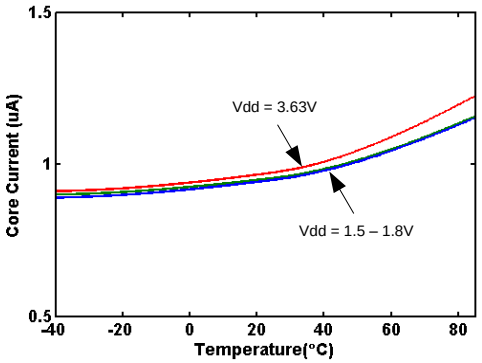


Figure 5. Core Current Over Temperature

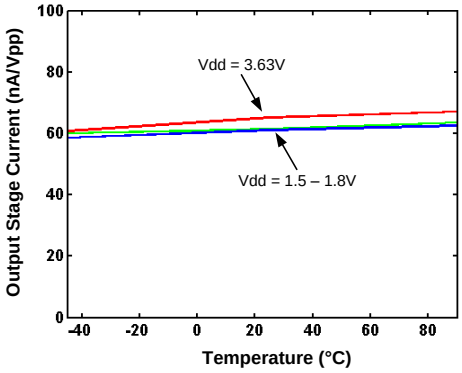


Figure 6. Output Stage Current Over Temperature

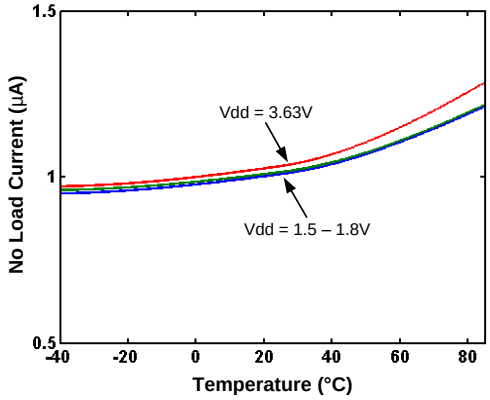


Figure 7. Total Supply Current Over Temperature, LVCMOS (Core + LVCMOS Output Driver, No Load)

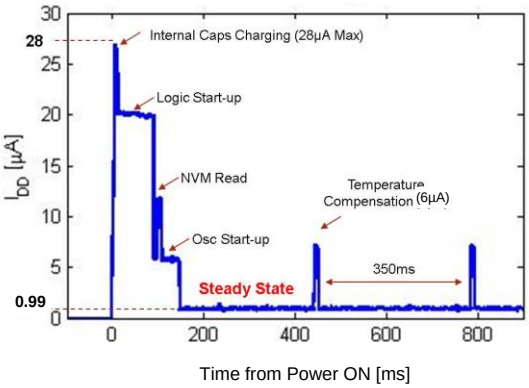


Figure 8. Start-up and Steady-State Current Profile

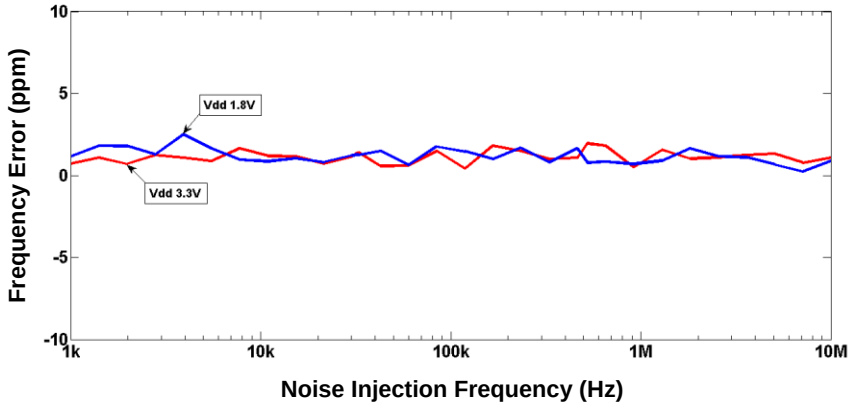


Figure 9. Power Supply Noise Rejection (±150mV Noise)

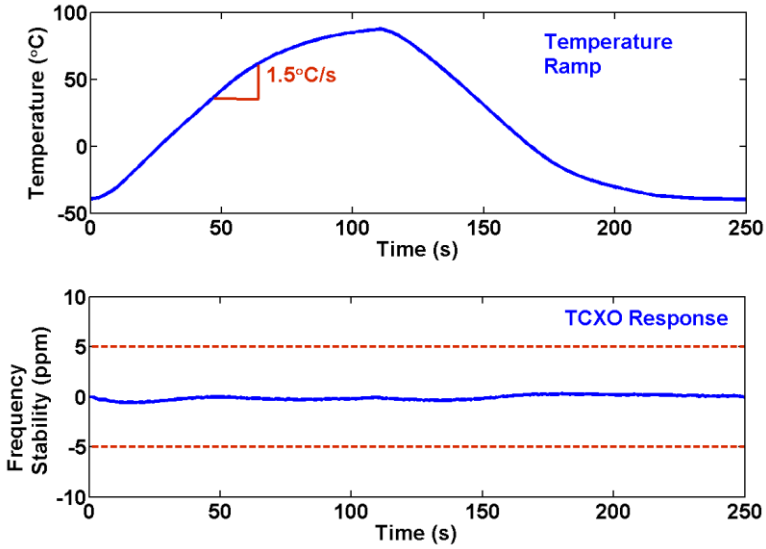


Figure 10. Temperature Ramp Response

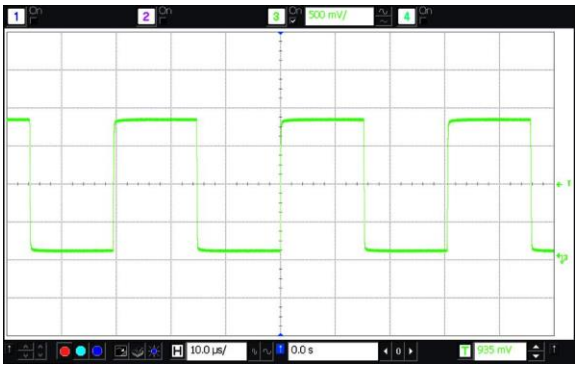
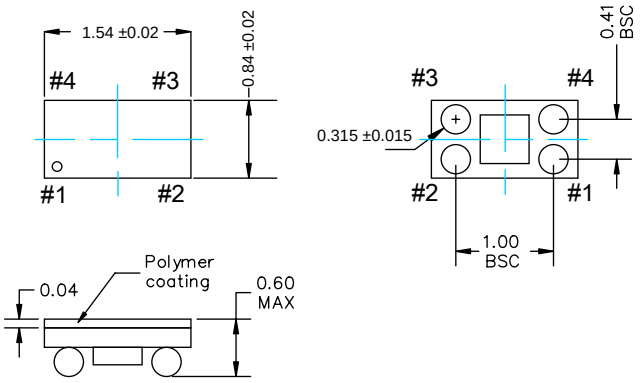
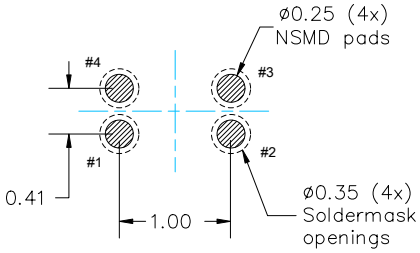


Figure 11. LVCMOS Output Waveform
(Vswing = 1.8V, SIT1552AI-JE-DCC-32.768, 10 pF Load)

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)	Recommended Landing Pattern (Unit: mm)
1.55 x 0.85 mm CSP 	 (soldermask openings shown with dashed line around NSMD pad) **Recommend 4-mil (0.1mm) stencil thickness**

Manufacturing Guidelines

1) No Ultrasonic Cleaning: Do not subject the SiT1552 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.
2) Do not apply underfill to the SiT1552. The device will not meet the frequency stability specification if underfill is applied.
3) Reflow profile, per JESD22-A113D.
4) For additional manufacturing guidelines and marking/tape-reel instructions, refer to: SiTime Manufacturing Notes.

Ordering Information

Part number characters in blue represent the customer specific options. The other characters in the part number are fixed.

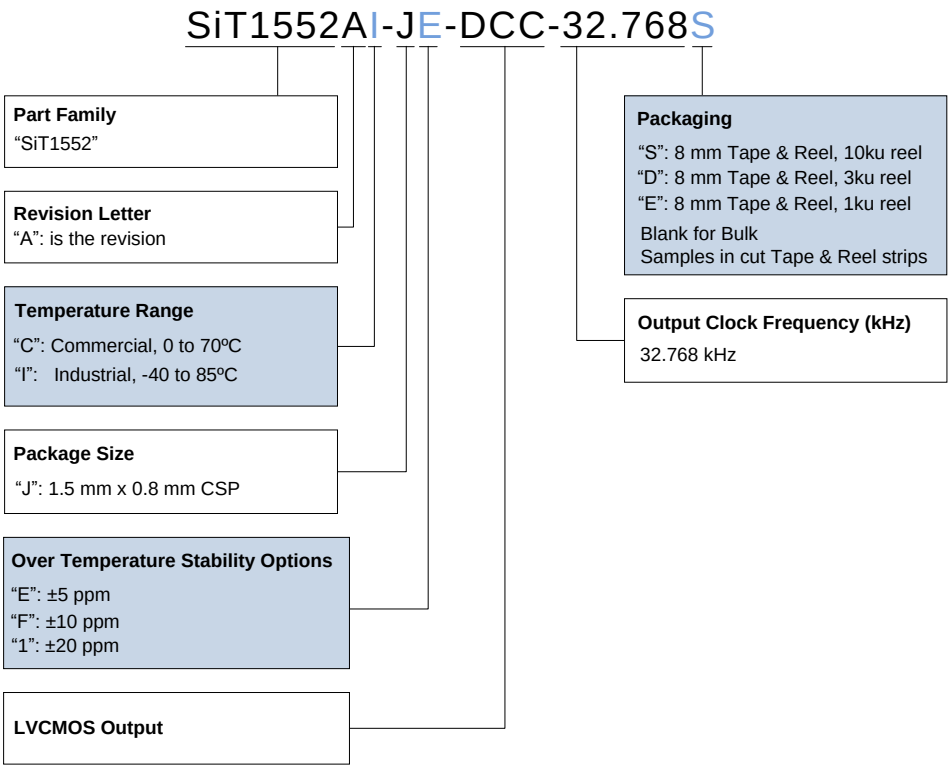


Table 4. Revision History

Version	Release Date	Change Summary
1.0	09/17/2014	Rev 0.9 Preliminary to Rev 1.0 Production Release Updated start-up time specification Added typical operating plots Removed SOT23 and 2012 SMD package options Added “no underfill” in frequency stability specification condition Added Manufacturing Guidelines section
1.1	10/14/2014	Improved Start-up Time at Power-up spec Added 5 pF LVCMOS rise/fall time spec
1.2	11/10/2014	Updated 5 pF LVCMOS rise/fall time spec
1.3	11/12/2015	Removed NanoDrive from EC Table and Ordering Info Updated logo and company address
1.31	01/18/2018	Updated SPL, page layout changes

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439