ALM2402-Q1 Dual Op-amp with High Current Output

1 Features

- High Output Current Drive: 400 mA Continuous (Per Channel)
  - Op-amp With Discrete Power Boost Buffer Replacement
- Wide Supply Range for Both Supplies (up to 16 V)
- Over Temperature Shutdown
- Current Limit
- Shutdown Pin for Low Iq Applications
- Stable with Large Capacitive Loads (up to 3 µF)
- Zero Crossover Distortion
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM Classification Level H2 (DRR)
  - Device CDM Classification Level C5 (DRR)
- Low Offset Voltage: 1 mV (typ)
- Internal RF/EMI Filter
- Available in 3.00 mm x 3.00 mm 12 Pin WSON (DRR) With Thermal Pad

2 Applications

- Large Capacitive Loads
  - Cable Shields
  - Reference Buffers
  - Power-FET/IGBT Gates
  - Super Caps
- Tracking LDO
- Inductive Loads
  - Resolvers
  - Bipolar DC & Servo Motors
  - Solenoids & Valves

3 Description

The ALM2402-Q1 is a dual high voltage, high current op-amp with protection features that are optimal for driving low impedances and/or high ESR capacitive loads. ALM2402-Q1 operates with single or split power supplies from 5.0 V to 16 V and can output up to 400 mA DC.

Each op-amp includes over-temperature flag/shut-down. It also includes separate supply pins for each output stage that allow the user to apply a lower voltage on the output to limit the Voh and henceforth the on-chip power dissipation.

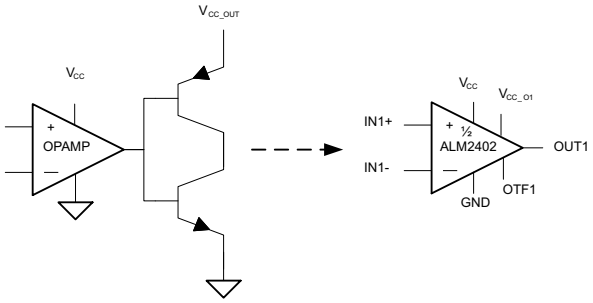
The ALM2402 is packaged in a 12 pin leadless DRR package and 14 pin leaded HTSSOP (preview). Both include a thermally conductive power pad that facilitates heat sinking. The very low thermal impedance of these packages enable optimal current drive with minimal die temperature increase. Providing customers with the ability to drive high currents in harsh temperature conditions. Maximum power dissipation can be determined in the figure below.

Device Information(1)

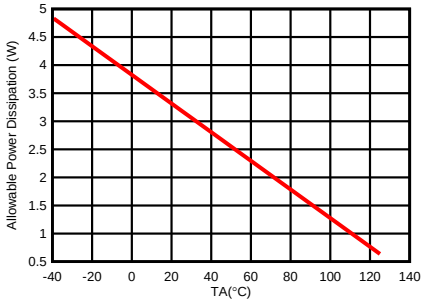
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ALM2402-Q1	SON (12)	3.00 mm x 3.00 mm
	HTSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



Maximum Power Dissipation vs Temperature



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2015) to Revision D — **Page**

- Added package corresponding to ESD level ... 1
- Removed HTSSOP preview status ... 3
- Added thermal metrics for PWP ... 4
- Added CDM value for PWP ... 4

Changes from Revision B (May 2015) to Revision C — **Page**

- Changed DRR to industry standard SON. ... 1
- Changed document wording to remove the word "guarantee." ... 11
- Updated Resolver Application Graphic. ... 15

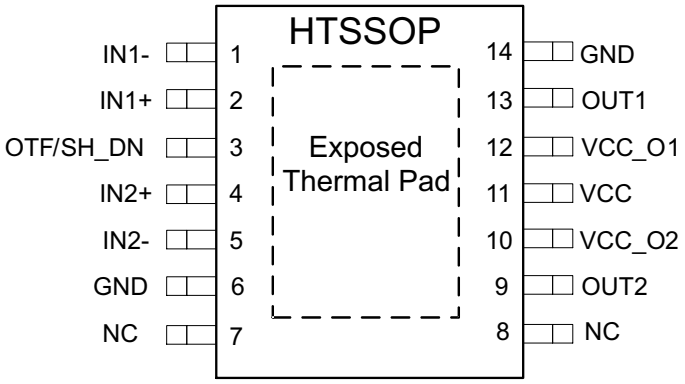
Changes from Revision A (April 2015) to Revision B — **Page**

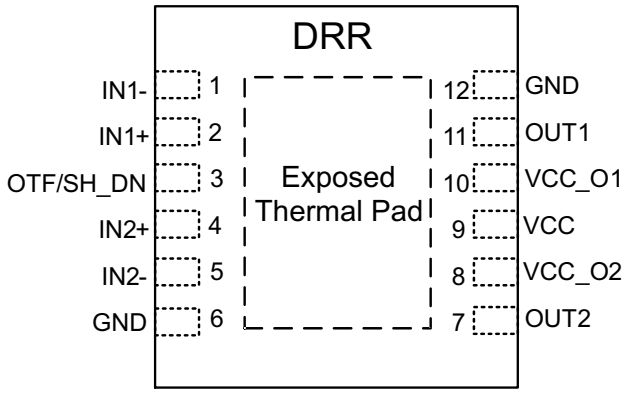
- Fixed HBM Classification typo from "Level 2" to "Level H2" ... 1

Changes from Original (February 2015) to Revision A — **Page**

- Initial release of full version document. ... 1

6 Pin Configuration and Functions





It is recommended to connect the Exposed Pad to ground for best thermal performance. Must not be connected to any other pin than ground. However, it can be left floating.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DDR	PWP		
	NO.	NO.		
IN(X)+	2, 4	2, 4	Input	non-inverting op amp input terminal
IN(X)-	1, 5	1, 5	Input	inverting op amp input terminal
OUT(X)	11, 7	13, 9	Output	Op amp output
OTF/SH_DN	3	3	Input/output	Over temperature flag and Shutdown (see Table 1 for truth table)
VCC_O(X)	8, 10	10, 12	Input	Output stage supply pin
VCC	9	11	Input	Gain stage supply pin
GND	6, 12	14	Input	Ground pin (Both ground pins must be used and connected together on board)
NC	N/A	7, 8	N/A	No Internal Connection (do no connect)

7 Specifications

7.1 Absolute Maximum Ratings(1)

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	-0.3	18	V
$V_{CC\_(OX)}$	Output supply voltage(2)	-0.3	18	V
$V_{OUT(X)}$	Opamp voltage(2)	-0.3	18	V
$V_{IN(X)}$	Positive and negative input to GND voltage (2)	-0.3	18	V
I_{OTF}	Over Temperature Flag pin maximum Current		20	mA
V_{OTF}	Over Temperature Flag pin maximum Voltage	0	7	V
I_{SC}	Continuous output short current per opamp		Internally Limited Figure 6	mA
T_A	Operating free-air temperature range	–40	125	°C
T_J	Operating virtual junction temperature(3)	-40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND/substrate terminal, unless otherwise noted.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

7.2 Thermal Information

THERMAL METRIC(1)		ALM2402Q1		UNIT
		DRR (SON)	PWP (HTSSOP)	
		12 Pins	14 Pins	
θ_{JA}	Junction-to-ambient thermal resistance	39.2	46.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34.5	33.0	°C/W
θ_{JB}	Junction-to-board thermal resistance	15.0	27.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.2	27.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	4.2	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	DRR	±750	
			PWP	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.4 Recommended Operating Conditions

T_A= 25°C

		MIN	MAX	UNIT
T_J	Junction Temperature	-40	150	°C
T_A	Ambient Temperature	-40	125	
I_{OUT}(1)	Continuous output current (sourcing)		400	mA
	Continuous output current (sinking)		400	
V_{IH_OTF}	OTF input high voltage (Opamp "On" or full operation state)	1.0		V
V_{IL_OTF}	OTF input low voltage (Opamp "Off" or shutdown state)		0.35	
$V_{IN(X)}$	Positive and negative input to GND voltage	0	7	
V_{OTF}	Over Temperature Flag pin maximum Voltage	2	5	
V_{CC}	Input Vcc	4.5	16	
$V_{CC\_O(X)}$	Output Vcc	3	16	

(1) Current Limit must taken into consideration when choosing maximum output current

7.5 Electrical Characteristics

V_{OTF} = 5 V, V_{CC} = V_{CC_O1} = V_{CC_O2} = 5 V and 12 V; T_A = –40°C to 125°C; Typical Values at T_A = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage (1)	V_{ICM} = Vcc/2, R_L = 10 kΩ			1	15	mV
I_{IB}	Input Bias Current (1)	V_{ICM} = Vcc/2			1.5	100	nA
I_{IOS}	Input Offset Current (1)	V_{ICM} = Vcc/2				30	nA
V_{ICM}	Input Common Mode Range (1)	V_{CC} = 5.0		0.2		Vcc-1.2	V
		V_{CC} = 12.0 V		0.2		7	
I_{CC}	Total Supply Current (both amplifiers)(1)	I_O = 0 A			5	15	mA
		V_{OTF} = 0V			0.5(2)		
Vo	Positive Output Swing	V_{CC} = $V_{CC\_O(X)}$ = 5.0 V; V_{ICM} = Vcc/2; V_{ID} = 100 mV	I_{SINK} = 200 mA	4.7	4.87		V
			I_{SINK} = 100 mA	4.85	4.94		
	Negative Output Swing	V_{CC} = $V_{CC\_O(X)}$ = 5.0 V; V_{ICM} = Vcc/2; V_{ID} = 100 mV	I_{SOURCE} = 200 mA		200	425	mV
			I_{SOURCE} = 100 mA		100	200	
OTF	Over Temp. Fault and Shutdown(3)			157	165	175	°C
V_{OL_OTF}	Over Temp. Fault low voltage	Rpullup = 2.5 kΩ, Vpullup = 5.0 V				450	mV
I_{LIMIT}	Short to Supply Limit (low-side limit)(4)				550		mA
	Short to Ground Limit (high-side limit)(1)(4)				750		
PSRR	Power Supply Rejection Ratio(1)	V_{CC} = 5.0 V to 12 V, R_L = 10 kΩ, V_{ICM} = Vcc/2, V_O = Vcc/2		65	90		dB
CMRR	Common Mode Rejection Ratio(1)	V_{ICM} = V_{ICM}(min) to V_{ICM}(max), R_L = 10 kΩ, V_O = Vcc/2		45	90		dB
A_{VD}	DC Voltage Gain(1)	RL = 10 kΩ, V_{ICM} = Vcc/2, V_O = 0.3 V to Vcc-1.5		70	90		dB

(1) Tested and verified in closed loop negative feedback configuration.
(2) Verified by design.
(3) Please see refer to *Absolute Maximum Ratings* table for maximum junction temperature recommendations.
(4) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay.

7.6 AC Characteristics

T_J= –40°C to 125°C; Typical Values at T_A = T_J = 25°C; V_{CC} = V_{CC_O1} = V_{CC_O2} = 5.0 V and 12 V; V_{ICM}=V_{CC}/2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GBW	Gain Bandwidth	C_L=15 pF R_L=10 kΩ		600		KHz
PM	Phase Margin	C_L=200 nF R_L= 50 Ω		50		°
GM	Gain Margin	C_L=200 nF R_L= 50 Ω		17		dB
SR	Slew Rate	G = +1; C_L=50 pF; 3 V step		0.17		V/us
THD + N	Total Harmonic Distortion + Noise	A_V = 2 V/V, R_L = 100 Ω, Vo = 8 Vpp, Vcc = 12 V, F = 1 kHz, V_{ICM} = Vcc/2		-80		dB
e_n	Input Voltage Noise Density	Vcc = 5 V, F = 1kHz, V_{ICM} = Vcc/2		110		nV/√HZ

7.7 Typical Characteristics

T_A= 25°C and V_{CC} = $V_{CC\_O(X)}$

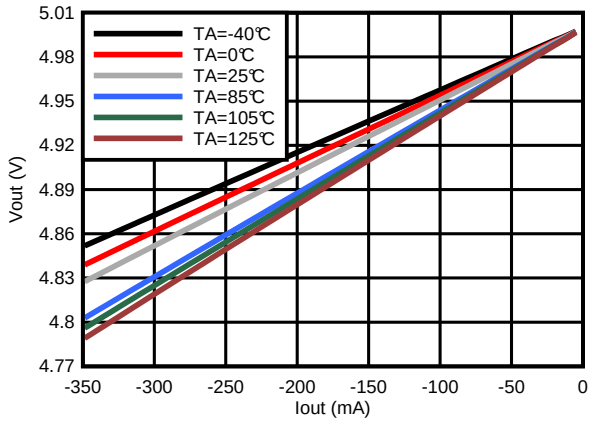


Figure 1. VOH at VCC = 5 V

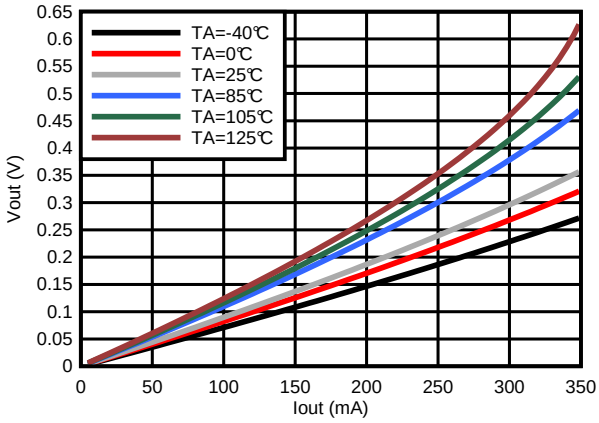


Figure 2. VOL at VCC = 5 V

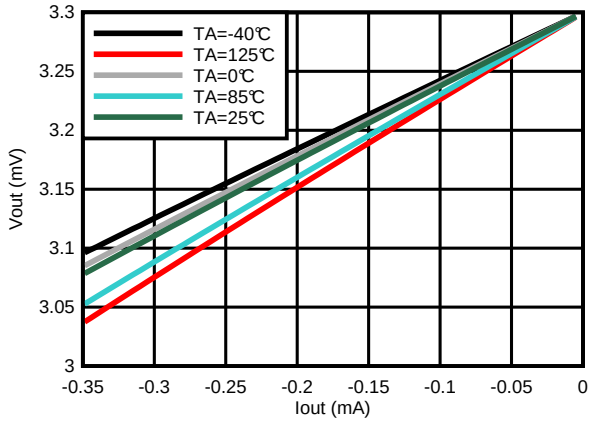


Figure 3. VOH at VCC = 3.3 V

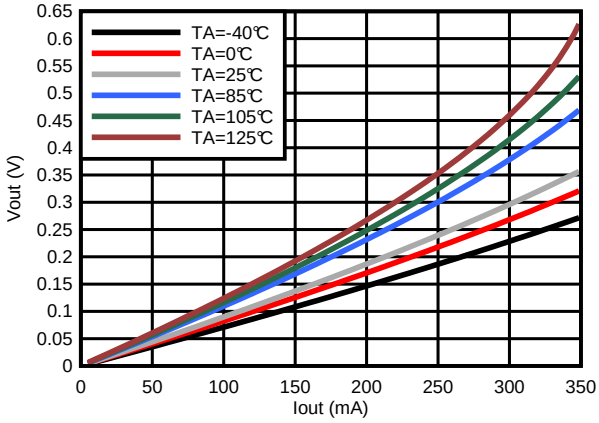


Figure 4. VOL at VCC = 3.3 V

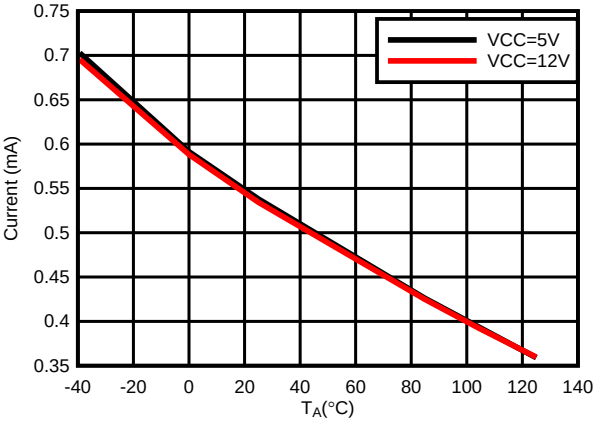


Figure 5. Short to Supply Current Limit vs. Temperature

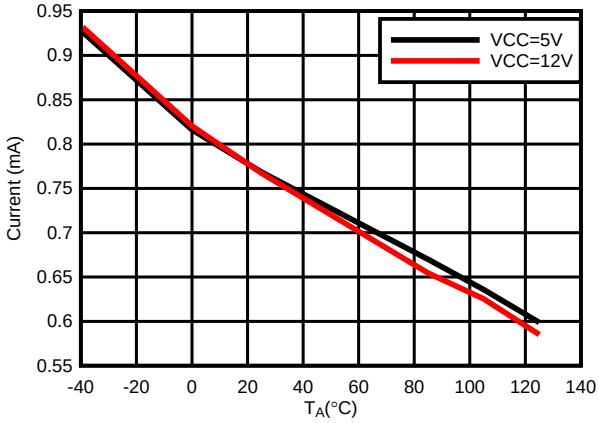


Figure 6. Short to Groung Current Limit vs. Temperature

Typical Characteristics (continued)

T_A= 25°C and V_{CC} = $V_{CC\_O(X)}$

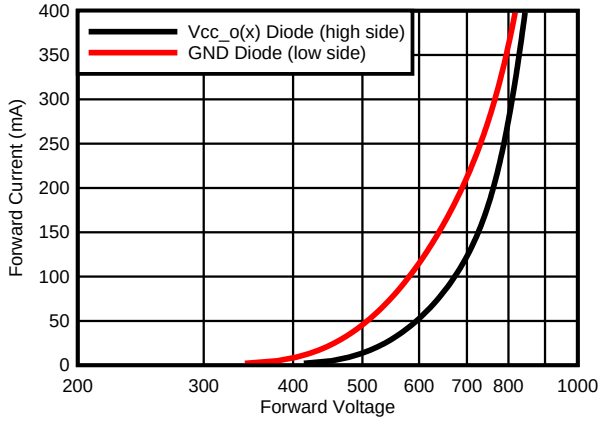


Figure 7. PMOS (High Side) and NMOS (Low Side) Output Diode Forward Voltage

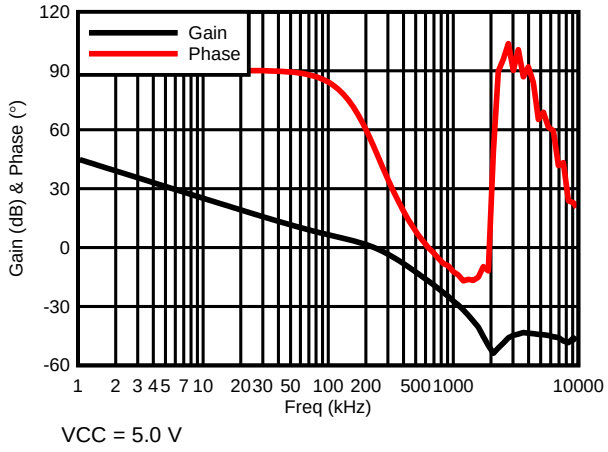


Figure 8. Gain and Phase (CL = 200 nF and RL = 50 Ω)

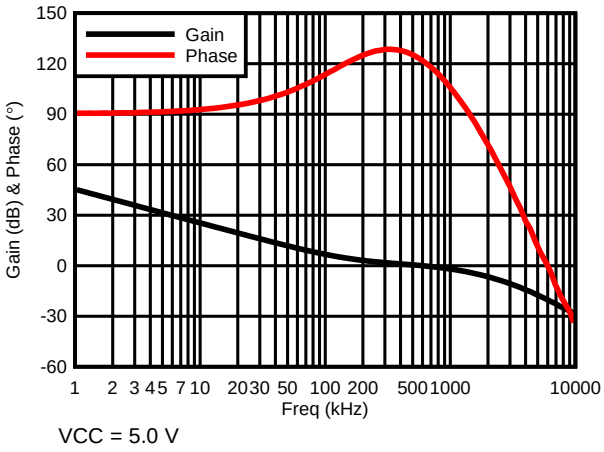


Figure 9. Gain and Phase (CL = 50 pF and RL = 10 kΩ)

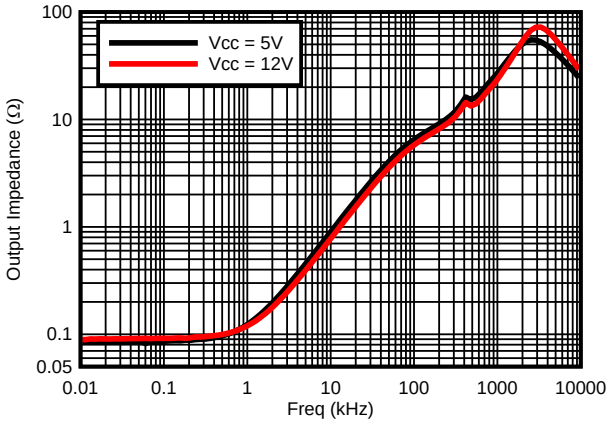


Figure 10. Output Impedance vs. Frequency

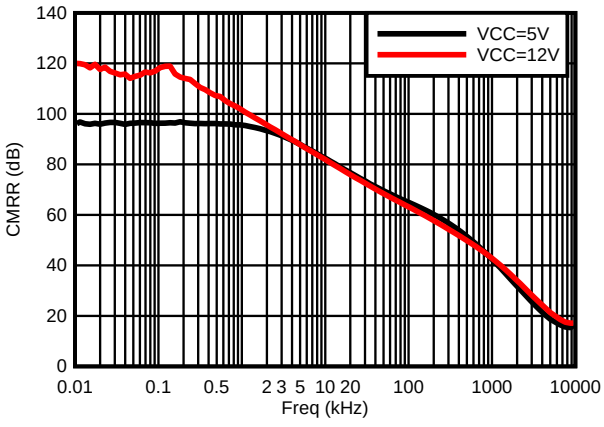


Figure 11. CMRR vs. Frequency

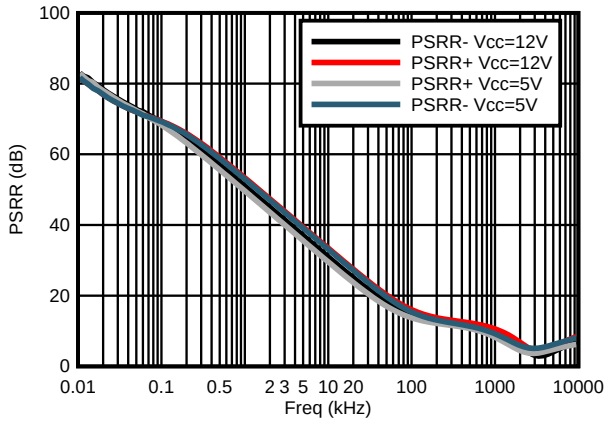


Figure 12. PSRR vs. Frequency

Typical Characteristics (continued)

T_A= 25°C and V_{CC} = $V_{CC\_O(X)}$

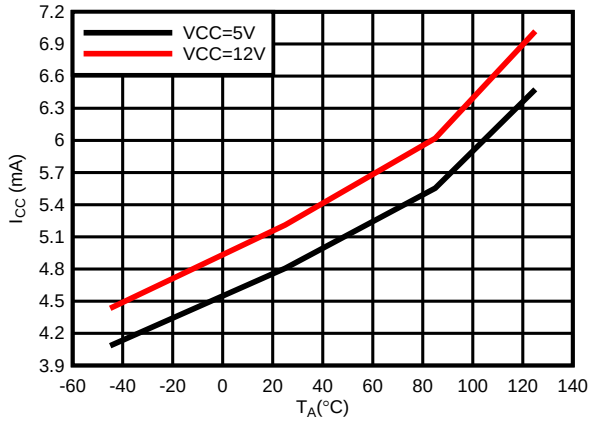


Figure 13. I_{CC} vs. Temperature

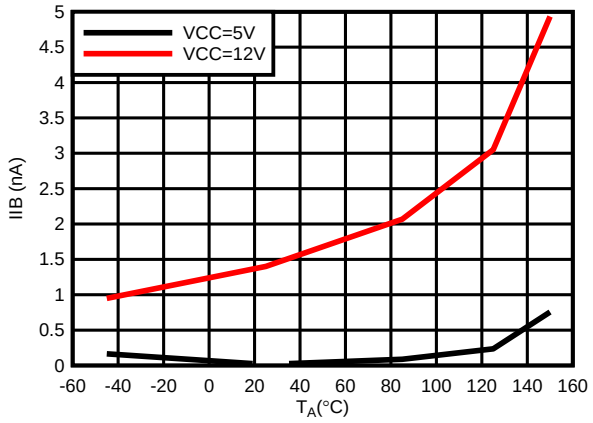
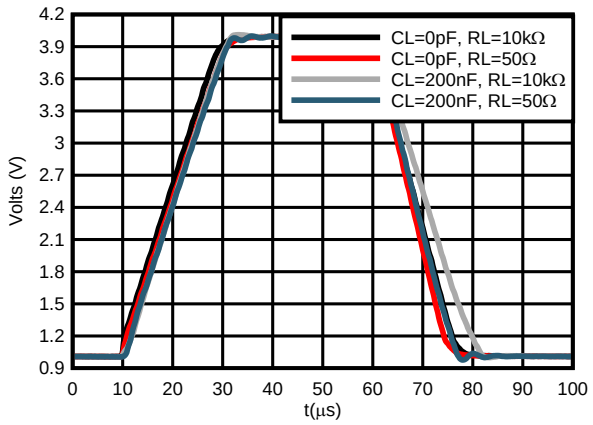
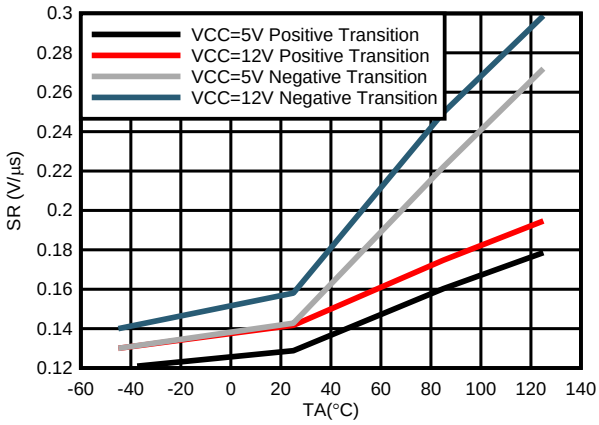


Figure 14. Input Bias Current vs. Temperature



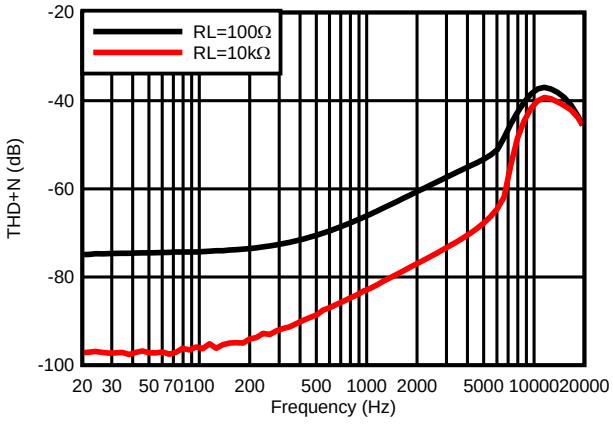
VCC = 5.0 V

Figure 15. Slew Rate



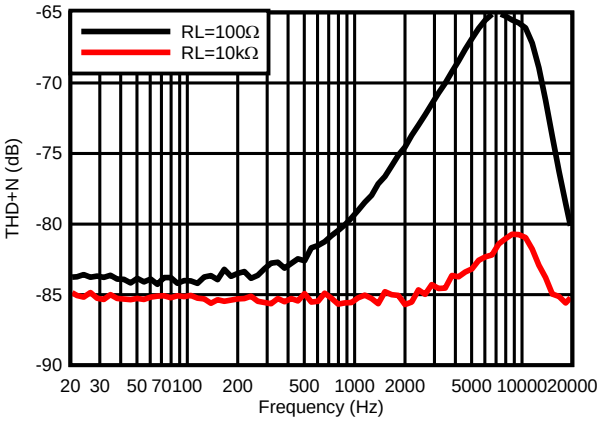
VCC =5.0 V

Figure 16. Slew Rate vs. Temperature



Av = 2V/V Vo = 8Vpp

Figure 17. THD + Noise (Vcc = 12 V)

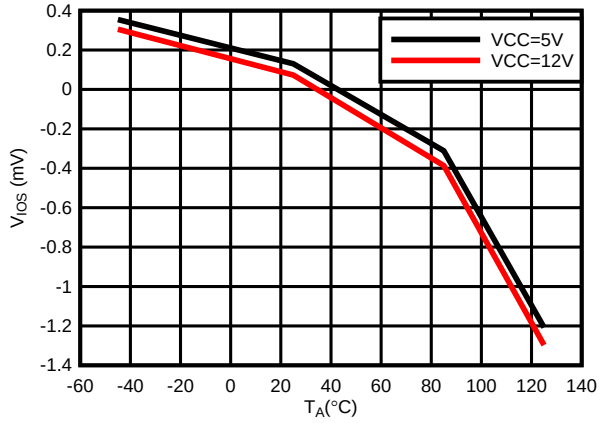


Av = 1V/V Vo = 1Vpp

Figure 18. THD + Noise (Vcc = 5 V)

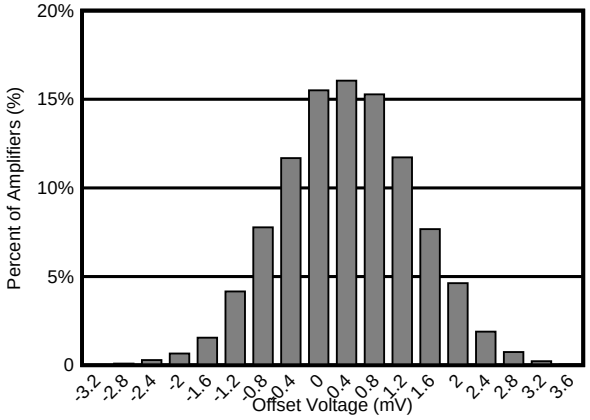
Typical Characteristics (continued)

T_A= 25°C and V_{CC} = $V_{CC\_O(X)}$



Vcm = Vcc/2

Figure 19. Input Offset vs. Temperature



Vcc =12 V and 5 V Vcm = Vcc/2

Figure 20. Offset Voltage Production Distribution

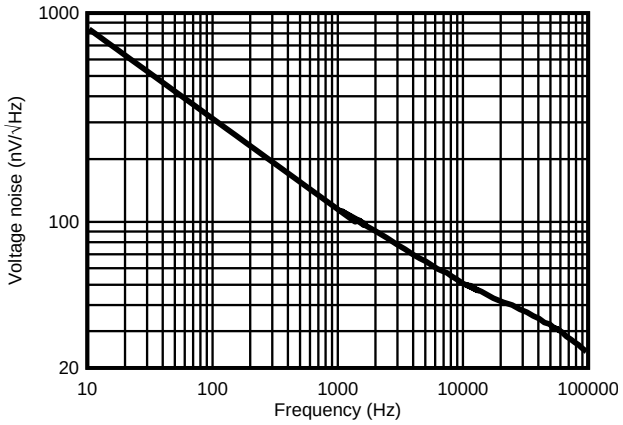


Figure 21. . Input Voltage Noise Spectral Density vs. Frequency

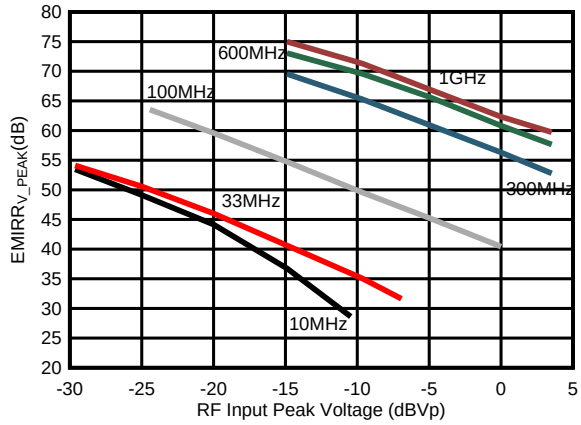


Figure 22. EMIRR vs. Power

8 Detailed Description

8.1 Overview

ALM2402Q1 is a dual power opamp with features and performance that makes it preferable in many applications. Its high voltage tolerance, low offset and drift are ideal in sensing applications. While its current limiting and over temperature detection allows it to be very robust in applications that drive analog signal off of the PCB and on to wires that are susceptible to faults from the outside world.

This device is optimal for applications that require high amounts of power. Its rail to rail output, enabled by the low Rdson PMOS and NMOS transistors, keeps the power dissipation low. The small 3.00 mm x 3.00 mm DRR package with its thermal pad and low θ_{JA} also allows users to deliver high currents to loads.

Other key features this device offers is its separate output driver supply (for external high-side current limit adjustability), wide stability range (with good phase margin up to 1 µF) and shutdown capability (for applications that need low Icc).

8.2 Functional Block Diagram

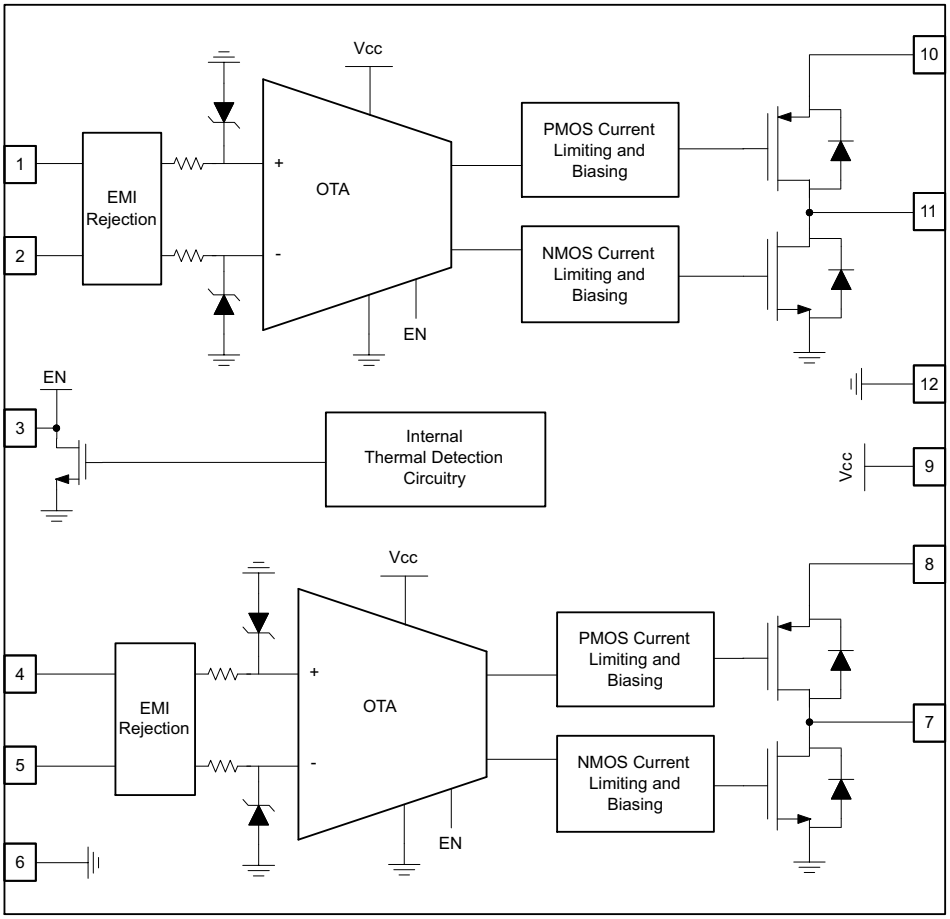


Figure 23. Functional Block Diagram

8.3 Feature Description

8.3.1 OTF/SH_DN

The OTF/SH_DN pin is a bidirectional pin that will allow the user to put both opamps in to a low Iq state (< 500 µA) when forced low or below V_{IL_OTF}. Due to this pin being bidirectional and it's Enable/Disable functionality, it must be pulled high or above V_{IH_OTF} through a pull-up resistor in order for the opamp to function properly or within the specifications, see *Electrical Characteristics*.

When the junction temperature of ALM2402Q1 crosses the limits specified in *Electrical Characteristics*, the OTF/SH_DN pin will go low to alert the application that the both output have turned off due to an over temperature event. Also, the OTF pin will go low if VCC_O1 and VCC_O2 are 0 V.

When OTF/SH_DN is pulled low and the opamps are shutdown, the opamps will be in open-loop even when there is negative feedback applied. This is due to the loss of open loop gain in the opamps when the biasing is disabled. Please see *Open Loop and Closed Loop* for more detail on open and close loop considerations.

8.3.2 Supply Voltage

ALM2402Q1 uses three power rails. VCC powers the opamp signal path (OTA) and protection circuitry and VCC_O1 and VCC_O2 power the output high side driver. Each supply can operate at separate voltages levels (higher or lower). The min and max values listed in *Electrical Characteristics* table are voltages that will enable ALM2402Q1 to properly function at or near the specification listed in *Electrical Characteristics* table. The specifications listed in this table are verified by design for 5 V and 12 V.

8.3.3 Current Limit and Short Circuit Protection

Each opamp in ALM2402Q1 has seperate internal current limiting for the PMOS (high-side) and NMOS (low-side) output transistors. If the output is shorted to ground then the PMOS (high-side) current limit is activated and will limit the current to 750 mA nominally (see *Electrical Characteristics*) or to values shown in Figure 6 over temperature. If the output is shorted to supply then the NMOS (low-side) current limit is activated and will limit the current to 550 mA nominally (see *Electrical Characteristics*) or to values shown in Figure 5 over temperature. The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures.

A programmable current limit for short to ground scenarios can be achieved by adding resistance between VCC_O(X) and the supply (or battery).

When current is limited, the safe limits for the die temperature (see *Recommended Operating Conditions* and *Absolute Maximum Ratings*) must be taken in to account. With too much power dissipation, the die temperature can surpass the thermal shutdown limits and the opamp will shutdown and reactivate once the die has fallen below thermal limits. However, it is not recommended to continuously operate the device in thermal hysteresis for long periods of time (see *Absolute Maximum Ratings*).

8.3.4 Input Common Mode Range and Overvoltage Clamps

ALM2402Q1's input common mode range is between 0.2 V and VCC-1.2 V (see *Electrical Characteristics*). Staying withing this range will allow the opamps to perform and operate within the specification listed in *Electrical Characteristics*. Operating beyond these limits can cause distortion and non-linearities.

In order for the inputs to tolerate high voltages in the event of a short to supply, zener diodes have been added (see Figure 24). The current into this zener is limited via internal resistors. When operating near or above the zener voltage (7 V), the additional voltage gain error caused by the mismatch in internal resistors must be taken in to account. In unity gain, the opamp will force both gate voltages to be equal to the zener voltage on the positive input pin and ideally both zeners will sink the same amount of current and force the output voltage to be equal to Vin. In reality, R_N and R_P and V_Z between both zener diodes do not perfectly match and have some % difference between their values. This leads to the output being $Vo = Vin \times (\Delta R + \Delta V_Z)$.

Feature Description (continued)

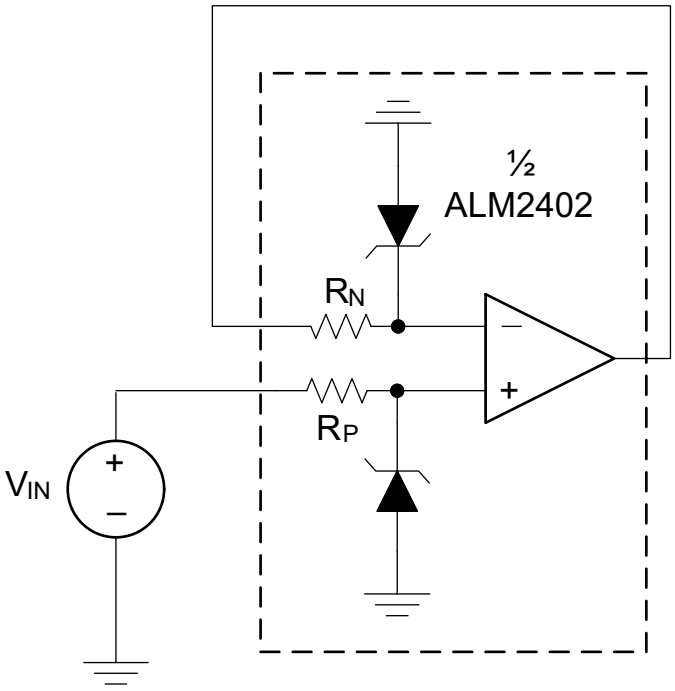


Figure 24. Schematic Including Input Clamps

8.3.5 Thermal Shutdown

If the die temperature exceeds safe limits, all outputs will be disabled, and the OTF/SH_DN pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume. The OTF/SH_DN pin will be released after operation has resumed.

When operating the die at a high temperature, the opamp will toggle on and off between the thermal shutdown hysteresis. In this event the safe limits for the die temperature (see *Recommended Operating Conditions* and *Thermal Information*) must be taken in to account. It is not recommended to continuously operate the device in thermal hysteresis for long periods of time (see *Recommended Operating Conditions*).

8.3.6 Output Stage

Designed as a high voltage, high current operational amplifier, the ALM2402Q1 device delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; refer to the graphs in *Typical Characteristics* section.

Each output transistor has internal reverse diodes between drain and source that will conduct if the output is forced higher than the supply or lower than ground (reverse current flow). Users may choose to use these as fly-back protection in inductive load driving applications. Figure 7 show I-V characteristics of both diodes. It is recommended to limit the use of these diodes to pulsed operation to minimize junction temperature overheating due to ($V_F \times I_F$). Internal current limiting circuitry will not operate when current is flown in the reverse direction and the reverse diodes are active.

Feature Description (continued)

8.3.7 EMI Susceptibility and Input Filtering

Op-amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op-amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op-amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The ALM2402Q1 device incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 990 MHz. The EMI rejection ratio (EMIRR) metric allows op-amps to be directly compared by the EMI immunity. Figure 22 shows the results of this testing on the ALM2402Q1 device. Detailed information can also be found in the application report, EMI Rejection Ratio of Operational Amplifiers (SBOA128), available for download from www.ti.com.

8.4 Device Functional Modes

8.4.1 Open Loop and Closed Loop

Due to its very high open loop DC gain, the ALM2402Q1 will function as a comparator in open loop for most applications. As noted in *Electrical Characteristics* table, the majority of electrical characteristics are verified in negative feedback, closed loop configurations. Certain DC electrical characteristics, like offset, may have a higher drift across temperature and lifetime when continuously operated in open loop over the lifetime of the device.

8.4.2 Shutdown

When the OTF/SH_DN pin is left floating or is grounded, the op amp will shutdown to a low Iq state and will not operate. The op amp outputs will go to a high impedance state. See the *OTF/SH_DN* section for more detailed information on OTF/SH_DN pin.

Table 1. Shutdown Truth Table

	Logic State	Opamp State
OTF/SH_DN	High (> VIH_OTF see *Recommended Operating Conditions*)	Operating
	Low (< VIL_OTF see *Recommended Operating Conditions*)	Shutdown (low Iq state)

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ALM2402Q1 is a dual power op amp with performance and protection features that are optimal for many applications. As it is an op amp, there are many general design consideration that must taken into account. Below will describe what to consider for most closed loop applications and gives a specific example of ALM2402Q1 being used in a motor drive application.

9.1.1 Capacitive Load and Stability

The ALM2402Q1 device is designed to be used in applications where driving a capacitive load is required. As with all op-amps, specific instances can occur where the ALM2402Q1 device can become unstable. The particular op-amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op-amp in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated

Application Information (continued)

at a higher noise gain. The capacitive load, in conjunction with the op-amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the ALM2402Q1 device remains stable with a pure capacitive load up to approximately 3 µF. The equivalent series resistance (ESR) of some very large capacitors (CL greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor, typically 100 mΩ to 10 Ω, in series with the output (R_S), as shown in Figure 25. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads.

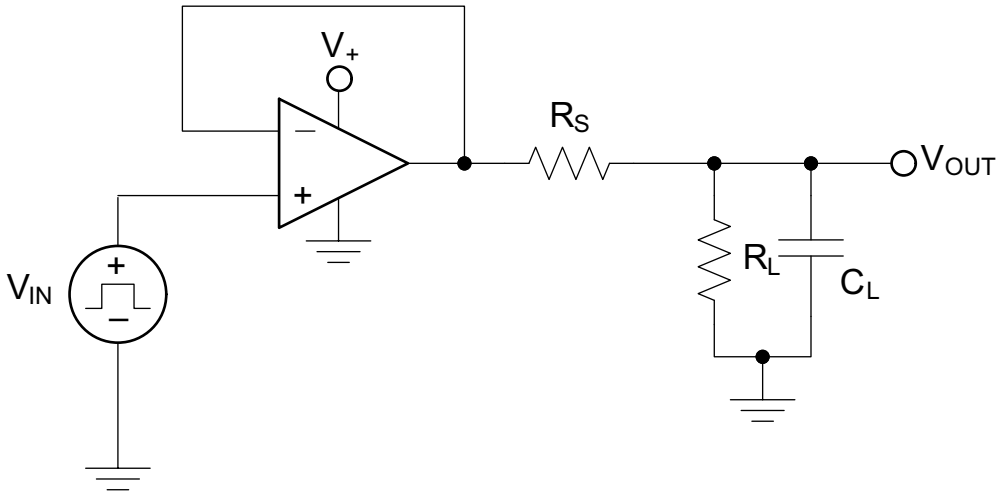


Figure 25. Capacitive Load Drive

Below are application curves displaying the step response of the above configuration with CL = 2.2 µF, R_L = 10 MΩ and R_L = 100 Ω. Displaying the ALM2402Q1's good stability performance with big capacitive loads.

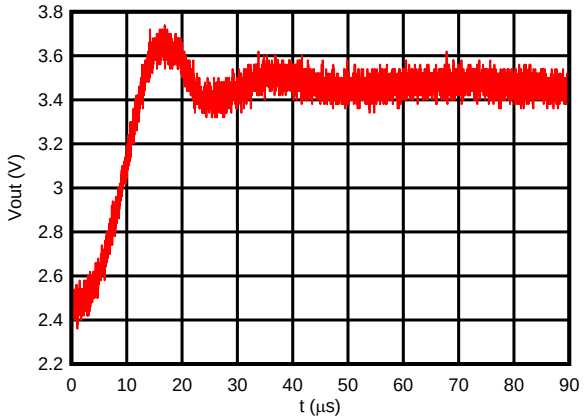


Figure 26. Output Pulse Response (CL = 2.2 µF and R_L = 10 MΩ)

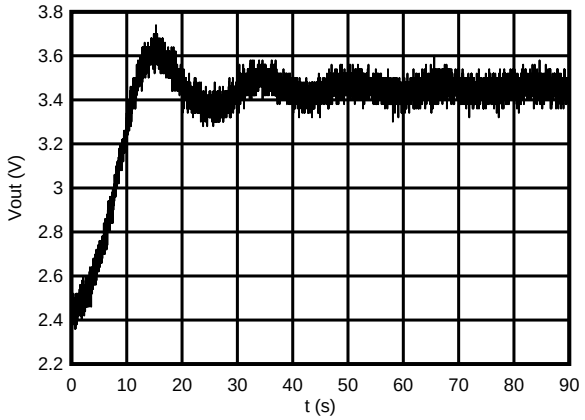


Figure 27. Output Pulse Response (CL = 2.2 µF and R_L = 100 Ω)

9.2 Typical Application

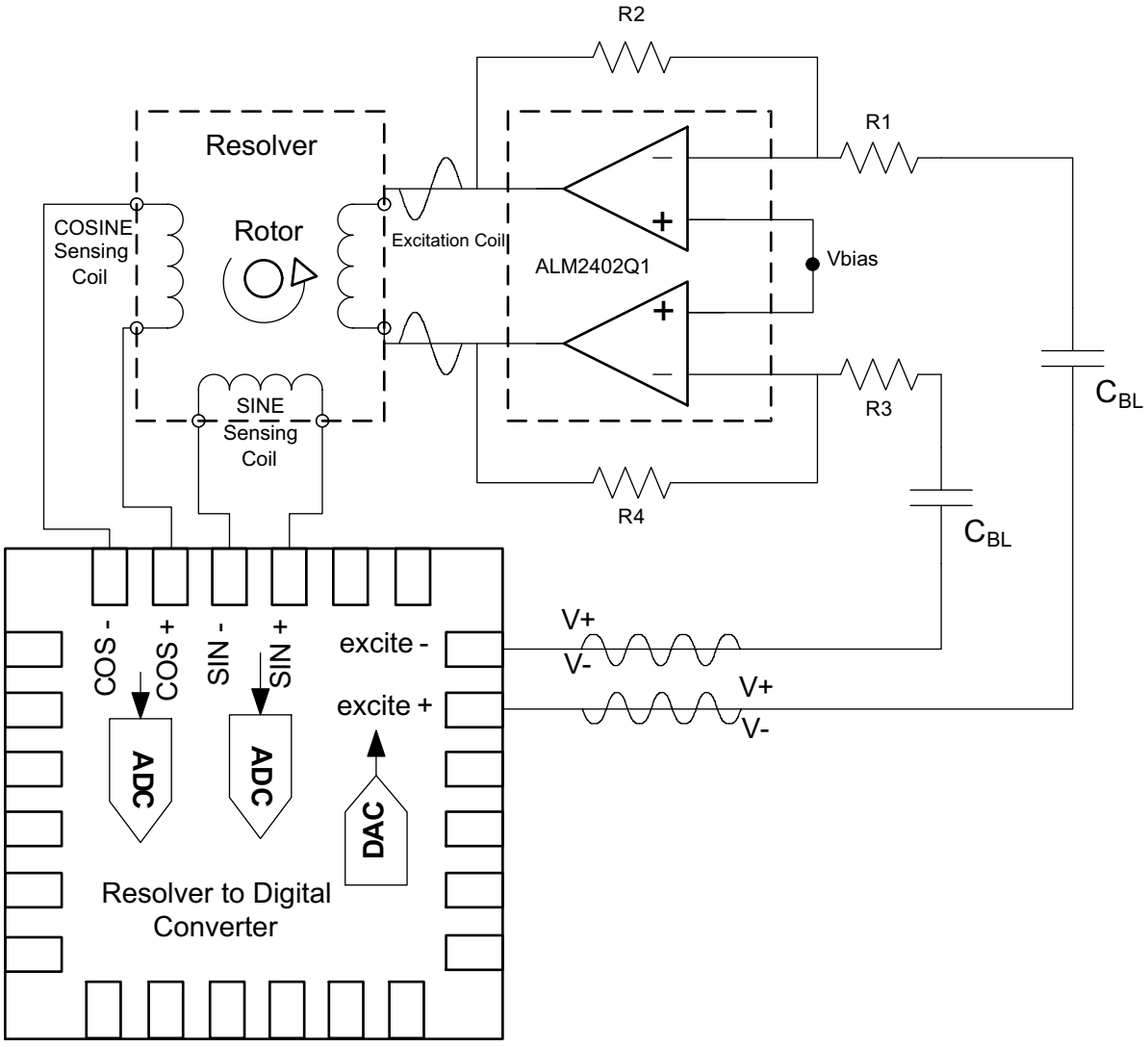


Figure 28. ALM2402Q1 in Resolver Application

High power AC and BLDC motor drive applications need angular and position feedback in order to efficiently and accurately drive the motor. Position feedback can be achieved by using optical encoders, hall sensors or resolvers. Resolvers are the go to choice when environmental or longevity requirements are challenging and extensive.

A resolver acts like a transformer with one primary coil and two secondary coils. The primary coil, or excitation coil, is located on the rotor of the resolver. As the rotor of the resolver spins, the excitation coil induces a current into the sine and cosine sensing coils. These coils are oriented 90 degrees from one another and produce a vector position read by the resolver to digital converter chip.

Resolver excitation coils can have a very low DC resistance (< 100 Ω), causing need for a sink and a source of up to 200 mA from the excitation driver. The ALM2402Q1 can source and sink this current while providing current limiting and thermal shutdown protection. Incorporating these protections in a resolver design can increase the life of the end product.

The fundamental design steps and ALM2402Q1 benefits shown in this application example can be applied to other inductive load applications like DC and servo motors. For more information on other applications that ALM2402Q1 offers a solution for, see (SLVA696), which is available for download from www.ti.com.

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Ambient Temperature Range	–40°C to 125°C
Available Supply Voltages	12 V, 5 V, 3.3 V
EMC Capacitance (CL)	100 nF
Excitation Input Voltage Range	2 Vrms - 7 Vrms
Excitation Frequency	10 kHz

9.2.2 Detailed Design Procedure

When using ALM2402Q1 in a resolver application, determine:

- Resolver Excitation Input Impedance or Resistance and Inductance: Z_O= 50 + j188; (R = 50 Ω and L = 3 mH)
- Resolver Transformation Ration (V_{EXC}/V_{SINCOS}): 0.5 V/V at 10 kHz
- Package and θ_{JA} : DRR, 39.2°C/W
- Opamp Maximum Junction Temperature: 150ºC
- Opamp Bandwidth: 600 kHz

9.2.2.1 Resolver Excitation Input (Opamp Output)

Like a transformer, a resolver needs an alternating current input to function properly. The resolver recieves alternating current from the primary coil (excitation input) and creates a multiple of it on the secondary sides (SIN, COS ports). When determining how to generate this alternating current, it is important to understand an opamp's ability or limitations. For the excitation input, the resolver input impedance, stability RMS voltage and desired frequency must be taken in to account.

9.2.2.1.1 Excitation Voltage

For this example, the resolver impedance is specified between 2 Vrms and 7 Vrms up 20 kHz maximum frequency. Since the resolver attenuation is ~0.5 V/V and most data acquisition microelectronics run off of 5 V supply voltages, An excitation input of 6 Vpp (or 2.12 Vrms) will be chosen to give the output readout circuitry enough headroom to measure the secondary side outputs (~3 Vpp).

The excitation coil can be driven by a single-ended op amp output with the other side of the coil grounded or differentially as shown in Figure 28. Differential drive offers higher peak to peak voltage (double) on to the excitation coil, while not using up as much output voltage headroom from the op amp. Leading to lower distortion on the output signal.

Another consideration for excitation is op amp power dissipation. As described in *Power Dissipation and Thermal Reliability*, power dissipation from the op amp can be lowered by driving the output peak voltages close to the supply and ground voltages. With ALM2402Q1's very low V_{OH}/V_{OL}, this can be easily accomplished. See Figure 1 for V_{OH}/V_{OL} values with respect to output current and the *Output Stage* section for further description of the rail-rail output stage.

9.2.2.1.2 Excitation Frequency

The excitation frequency is chosen based on the desired secondary side output signal resolution. As shown in Figure 34, the excitation signal is similar to a sampling pulse in ADCs, with the real information being in the envelope created by the rotor. With a GBW of 600 kHz, ALM2402Q1 has more than enough open loop gain at 10 kHz to create negligible closed loop gain error.

Along with GBW, ALM2402Q1 has optimal THD and SR performance (see *Typical Characteristics*) to achieve 6 Vpp (or 3 Vpp from each op amp). The signal integrity can also be observed in the *Typical Characteristics* section.

9.2.2.1.3 Excitation Impedance

Knowledge of the primary side impedance is very important when choosing an op amp for this application. As shown below in Figure 29, the excitation coil looks like an inductance in series with a resistance. Many time these values aren't given and must by calculated from the Cartesian or polar form, as it is given as a function of frequency or phase angle. This calculation is a trivial task.

Once the coil resistance is determined, the maximum or peak-peak current needed from ALM2402Q1 can be determined by below:

$$I_{OUT} = \frac{V_{PP}}{R_{EXC}} \quad (1)$$

In this example the peak-peak output current equates to ~120 mA. Each op amp will handle the peak current, with one sinking max and the other sourcing. Knowledge of the op amp current is very important when determining ALM2402Q1's power dissipation. Which is discussed in the *Power Dissipation and Thermal Reliability* section.

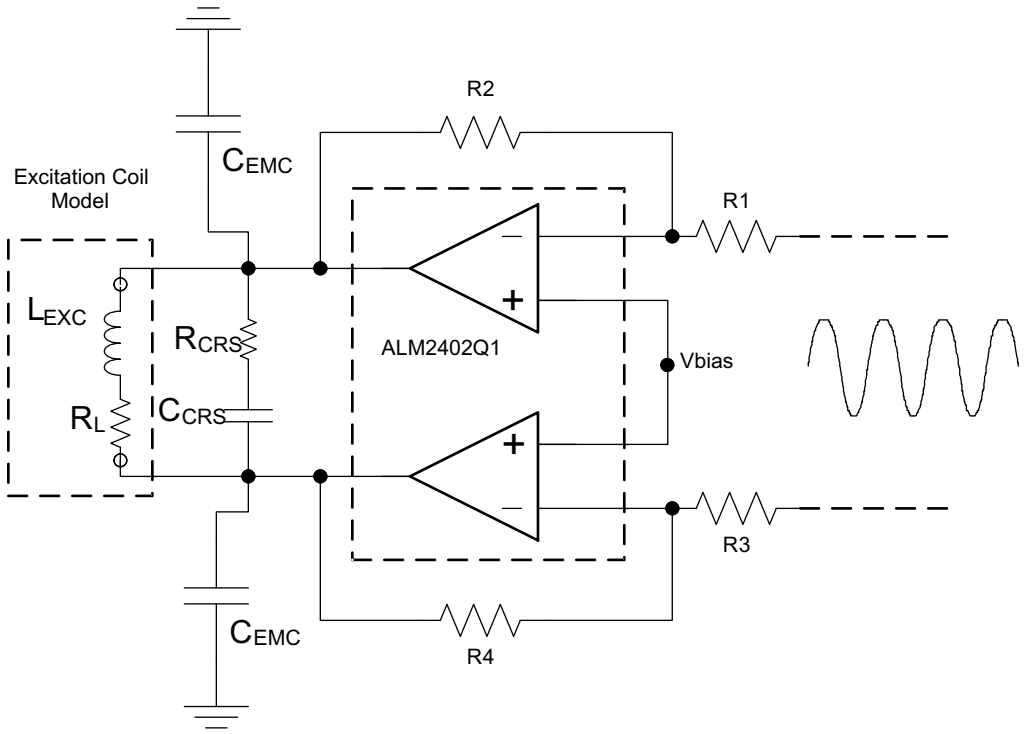


Figure 29. Excitation Coil Implementation

The primary side of a resolver is inductive, but that typically is not all the op amps driving the coils. As shown in Figure 29, many times designers will add a resistor in series with a capacitor to eliminate crossover distortion. Which happens due to the biasing of BJTs in the discrete implementation. With ALM2402Q1's rail-rail output, this is rarely needed. This can be seen in the waveforms shown in the *Typical Characteristics* section.

It is also common practice to add EMC capacitors to the op amp outputs to help shield other devices on the PCB from the radiation created by the motor and resolver. When choosing C_{EMC}, it is important to take the op amp's stability in to account. Since the ALM2402Q1 has a phase margin at and above 200 nF, no stability issues will be present for many typical C_{EMC} values.

9.2.2.2 Resolver Output

As mentioned in the *Excitation Frequency* section, the excitation signal is similar to a sampling pulse in ADCs, with the real information being in the envelope created by the rotor. The equations below show the behavior of the sin and cos outputs. Whereby the excitation signal is attenuated and enveloped by the voltage created from the electromagnetic response of the rotating rotor. The resolver analog output to digital converter will filter out the excitation signal and process the sine and cosine angles produced by the rotor. Hence, signal integrity or the sine and cosine envelope is most important in resolver design and some trade-offs in signal integrity of the excitation signal can be made for cost or convenience. Many times users can use a square wave or sawtooth signal to accomplish excitation, as opposed to a sine wave.

$$V_{EXC} = V_{PP} \times \sin(2\pi ft) \tag{2}$$

$$V_{SIN} = T_R \times V_{PP} \times \sin(2\pi ft) \times \sin(\theta) \tag{3}$$

$$V_{COS} = T_R \times V_{PP} \times \sin(2\pi ft) \times \cos(\theta) \tag{4}$$

9.2.2.3 Power Dissipation and Thermal Reliability

Very critical aspects to many industrial and automotive applications are operating temperature and power dissipation. Resolvers are typically chosen over other position feedback techniques due to their sustainability and accuracy in harsh conditions and very high temperatures.

Along with the resolver, the electronics used in this system must be able to withstand these conditions. ALM2402Q1 is Q100 qualified and is able to operate at temperatures up to 125°C. To ensure that this device can withstand these temperatures, the internal power dissipation must be determined.

The total power dissipation from ALM2402Q1 in this application is the sum of the power from the input supply and output supplies.

$$P_D = P_{SS} + (P_{SSO} - P_L) \tag{5}$$

(Input Supply Power; Output Supply Power; Load Power)

As shown in the equation below. P_{SS} is a function of the internal supply and operating current of both op amps (I_{CC}). With this op amp being CMOS, the ICC will not increase proportionally to the load like a BJT based design. It will stay close to the average value listed in *Electrical Characteristics*.

$$P_D = V_{CC} \times I_{CC} + \left(V_{CCO(X)} - V_{OUT}(RMS)\right) \times I_{OUT}(RMS)$$

For more information on this and calculating and measuring power dissipation with complex loads, please refer to (SBOA022), available for download from www.ti.com (6)

$$P_D = 12\ V \times 5\ mA + \left(12\ V - \frac{3\ V}{\sqrt{2}}\right) \times \frac{60\ mA}{\sqrt{2}} = 480\ mW \tag{7}$$

As shown inFigure 30, the load current will flow out of one op amp, through the load and in to the other. Each opamp shares the same load at 180° phase difference. The PMOS and NMOS output transistors are resistive when driven near supply and ground. Operating the output voltage at a high percentage of the supply voltage will greatly limit the chip power dissipation. The *Typical Characteristics* section gives more information on the expected voltage drop, that can be used to determine the limits of V_{OUT}.

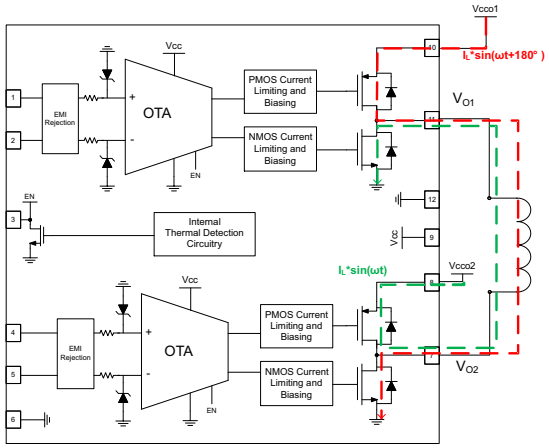


Figure 30. ALM2402Q1 Current Flow

After the total power dissipation is determined, the junction temperature at the worst expected ampient temperature case must be determined. This can be determined by Equation 9 below or from Figure 31.

$$T_{J(MAX)} = P_D \times \theta_{JA} + T_{A(MAX)} \tag{8}$$

$$T_{J(MAX)} = 480\ mW \times 39.2\ \frac{°C}{W} + 125°C = 143.8°C$$

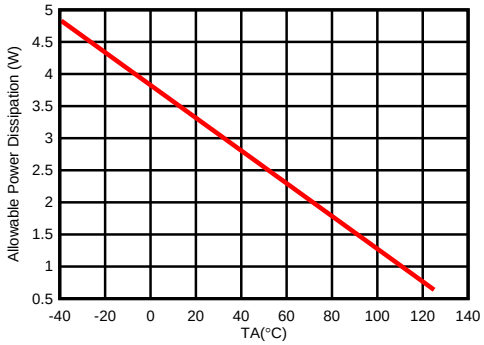
Where:

$T_{J(MAX)}$ is the target maximum junction temperature. → 150°C

T_A is the operating ambient temperature. → 125°C

θ_{JA} is the package junction to ambient thermal resistance. → 39.2°C/W (9)

For this example, the maximum junction temperature equates to ~144ºC which is in the safe operating region, below the maximum junction temperature of 150°C. It is required to limit ALM2402Q1's die junction temperature to less than 150°C. Please see *Absolute Maximum Ratings* table for further detail.



Maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Figure 31. Maximum Power Dissipation vs Temperature (DRR)

9.2.2.3.1 Improving Package Thermal Performance

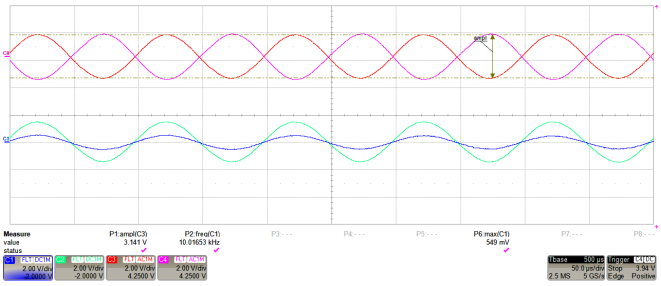
θ_{JA} value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

9.2.3 Application Curves

Below is test data with ALM2402Q1 exciting TE Connectivity (V23401-D1001-B102) Hollow Shaft Resolver.

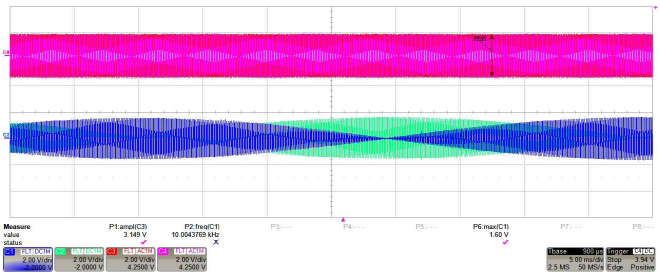
Table 3. Waveform Legend

Waveform Color	Description
Green	SINE output
Blue	COSINE output
Red	Excitation positive terminal inputs (referenced to ground)
Purple	Excitation negative terminal inputs (referenced to ground)



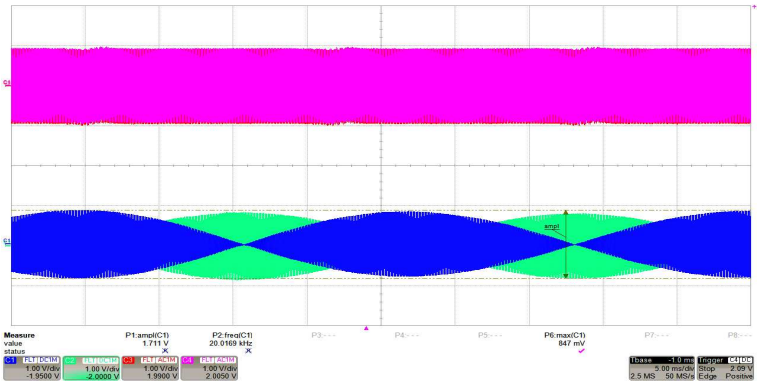
The peak-peak excitation voltage is the difference between the green and blue voltages

Figure 32. Resolver Excitation V_{EXC} ≈ 6 V_{pp} 10 kHz



The peak-peak excitation voltage is the difference between the green and blue voltages

Figure 33. Resolver Excitation V_{EXC} ≈ 6 V_{pp} at 10 kHz (ZOOM)



The peak-peak excitation voltage is the difference between the green and blue voltages

Figure 34. Resolver Excitation V_{EXC} ≈ 4 V_{pp} at 20 kHz

10 Power Supply Recommendations

The ALM2402Q1 device is recommended for continuous operation from 4.5 V to 16 V (±2.25 V to ±8.0 V) for Vcc and 3.0 V to 16V (±1.5 V to ±8.0 V) for Vcc_o(x); many specifications apply from –40°C to 125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 18 V can permanently damage the device (see *Absolute maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

11.2 Layout Example

This layout does not verify optimum thermal impedance performance. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

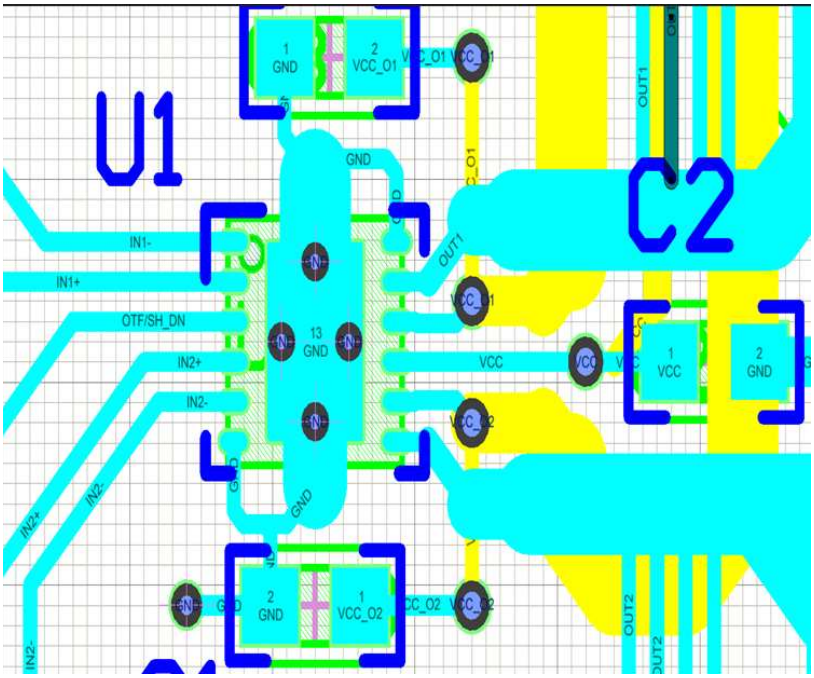


Figure 35. ALM2402Q1 Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ALM2402QDRRRQ1	ACTIVE	SON	DRR	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALM24Q	Samples
ALM2402QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ALM24Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

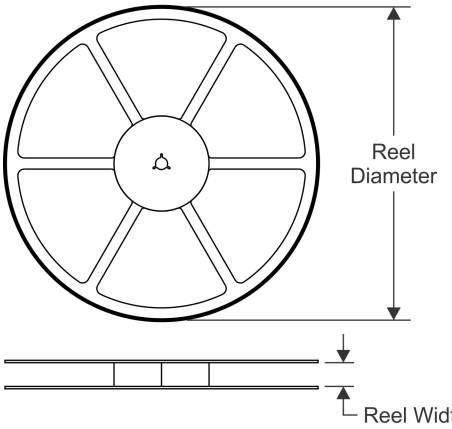
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

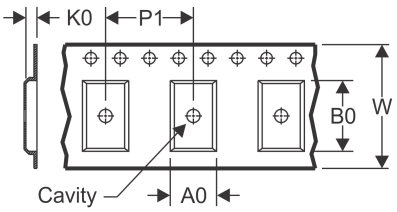
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

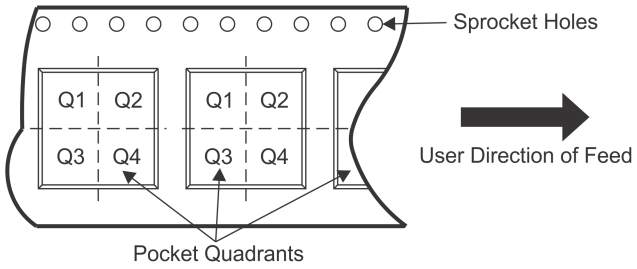


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

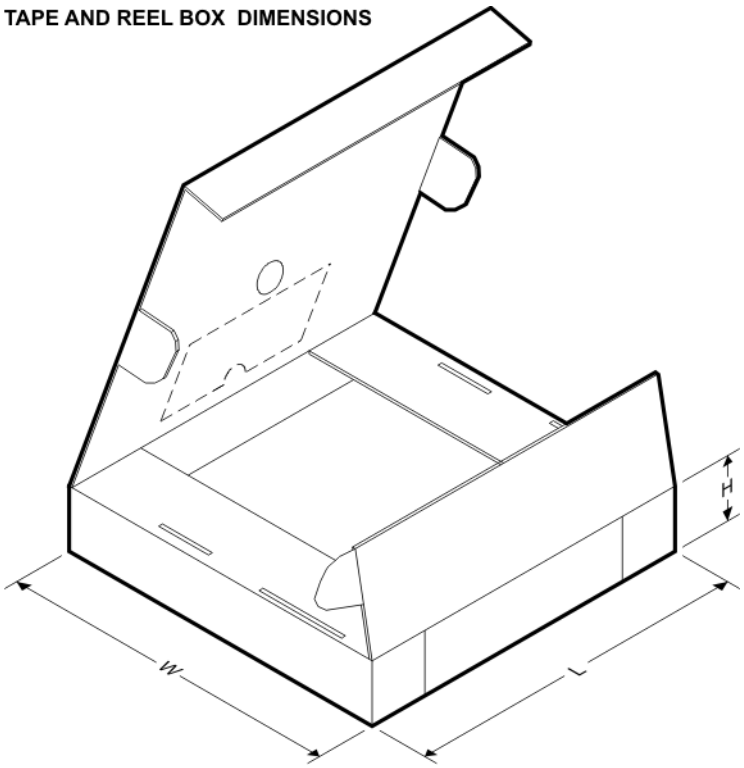
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ALM2402QDRRRQ1	SON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ALM2402QPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

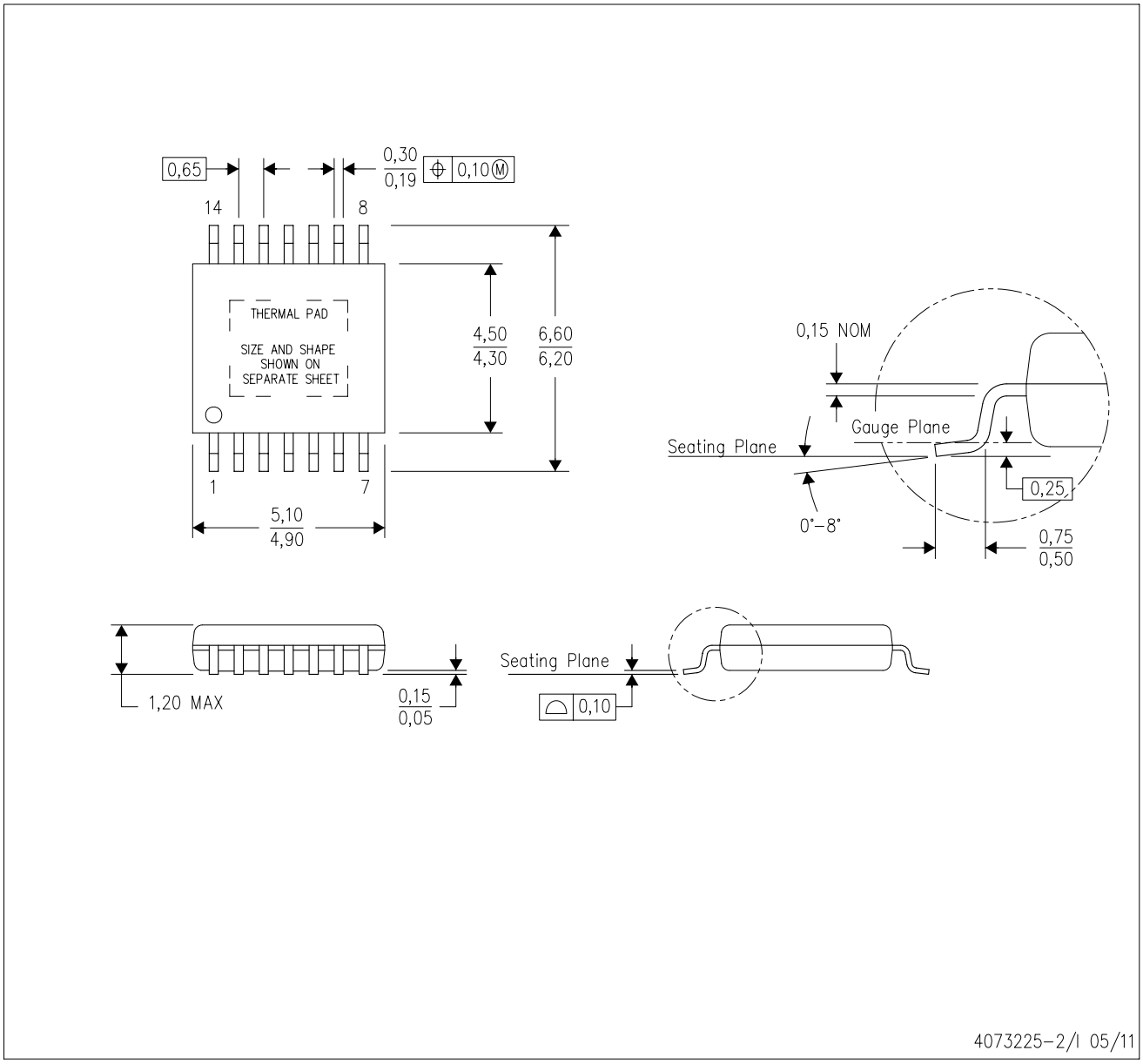
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

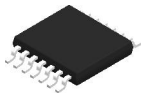
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ALM2402QDRRRQ1	SON	DRR	12	3000	367.0	367.0	35.0
ALM2402QPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

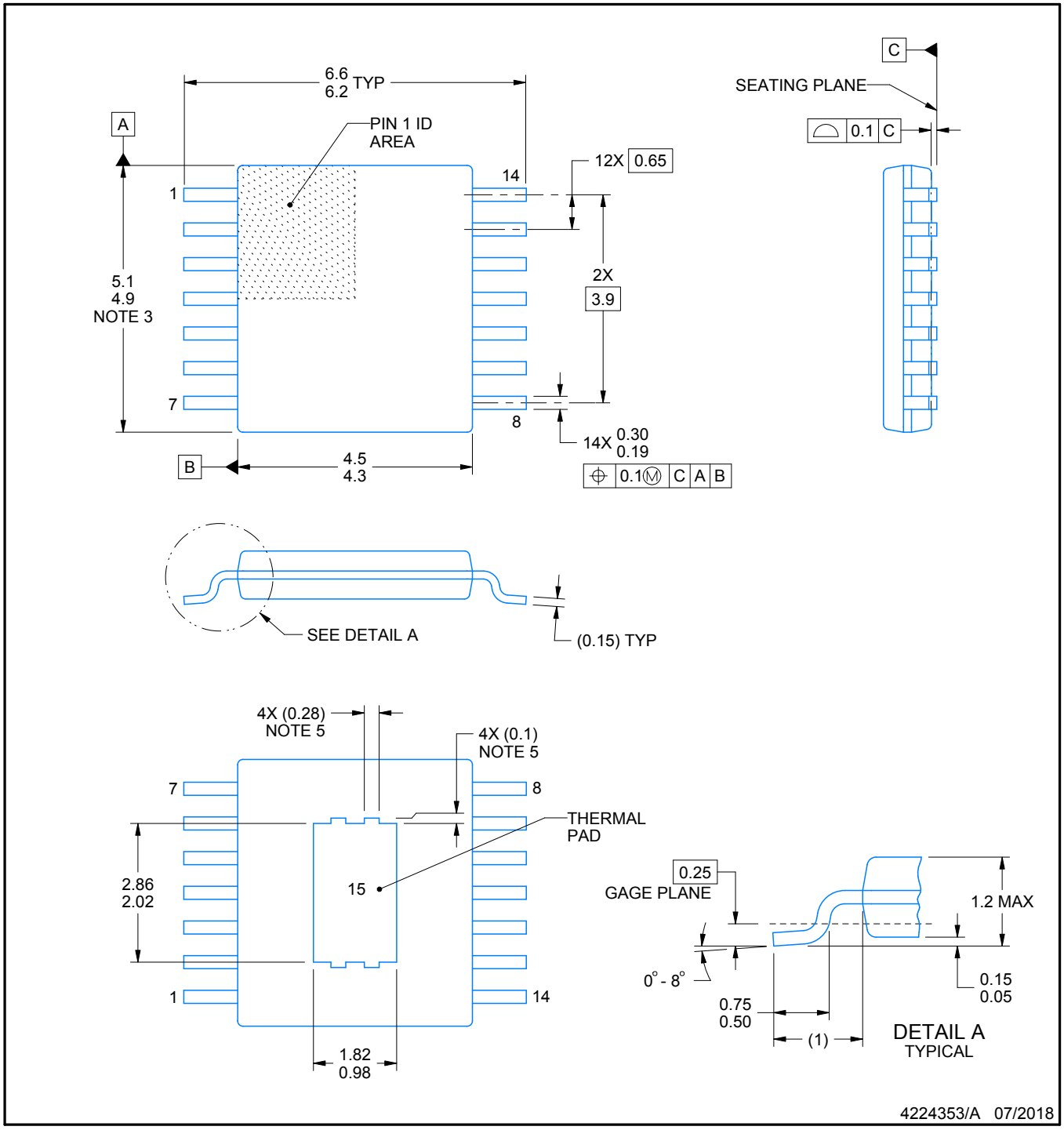


PACKAGE OUTLINE

PWP0014H

PowerPAD™ TSSOP - 1.2 mm max height

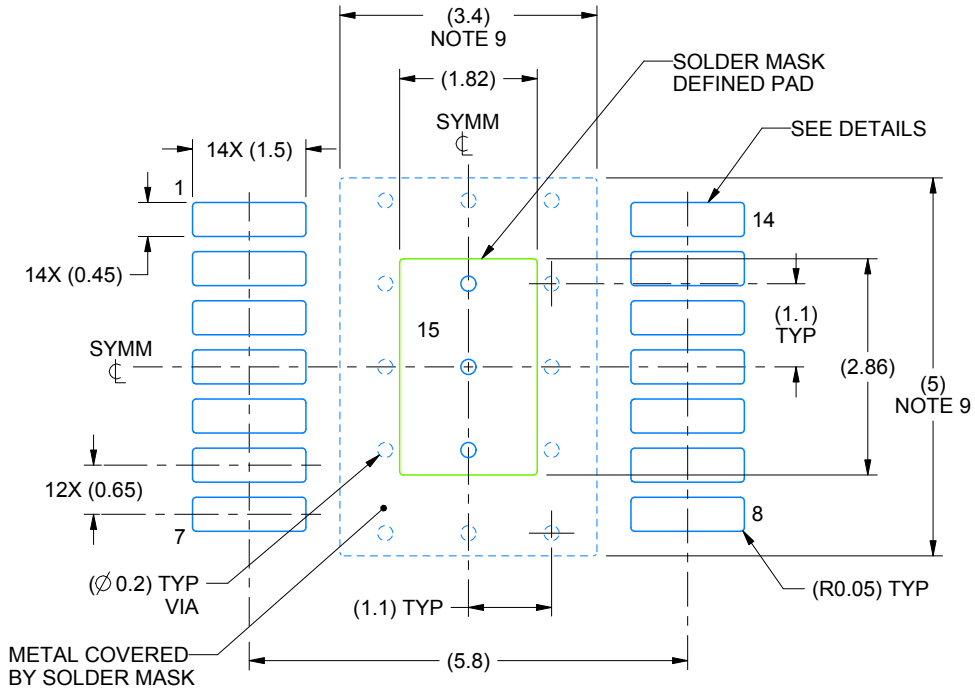
PLASTIC SMALL OUTLINE



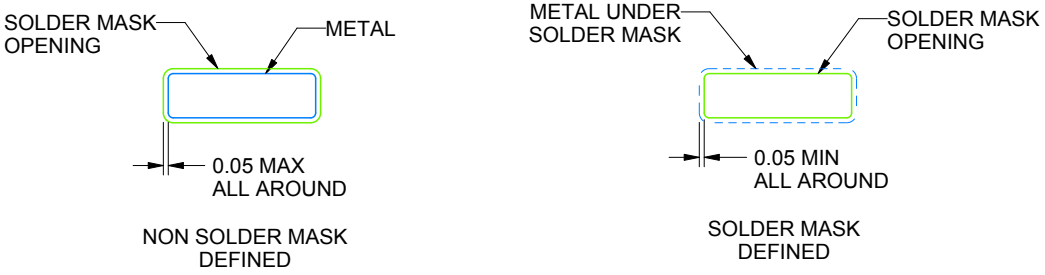
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

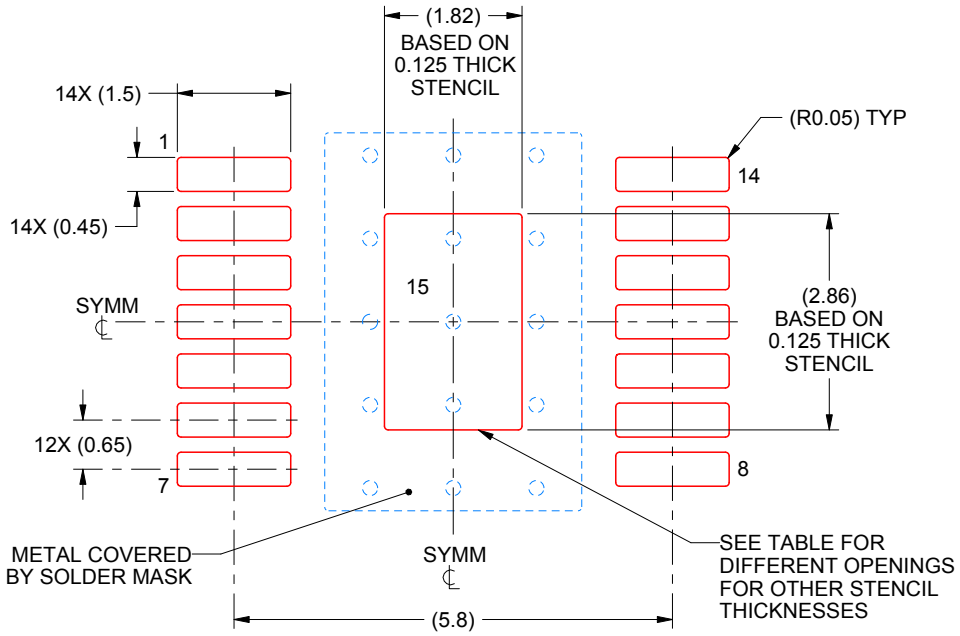


SOLDER MASK DETAILS
PADS 1-14

/A 07/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.03 X 3.20
0.125	1.86 X 2.86 (SHOWN)
0.15	1.66 X 2.61
0.175	1.54 X 2.42

4224353/A 07/2018

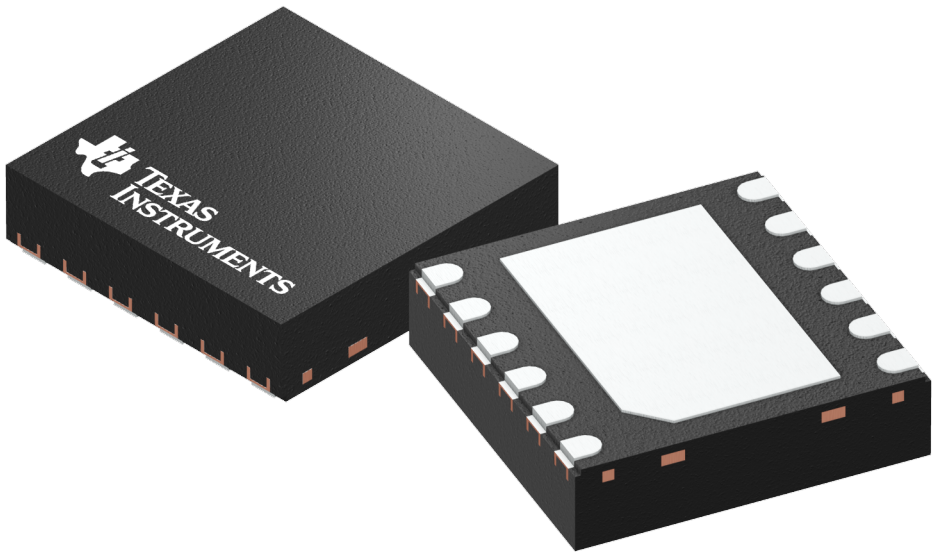
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRR 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

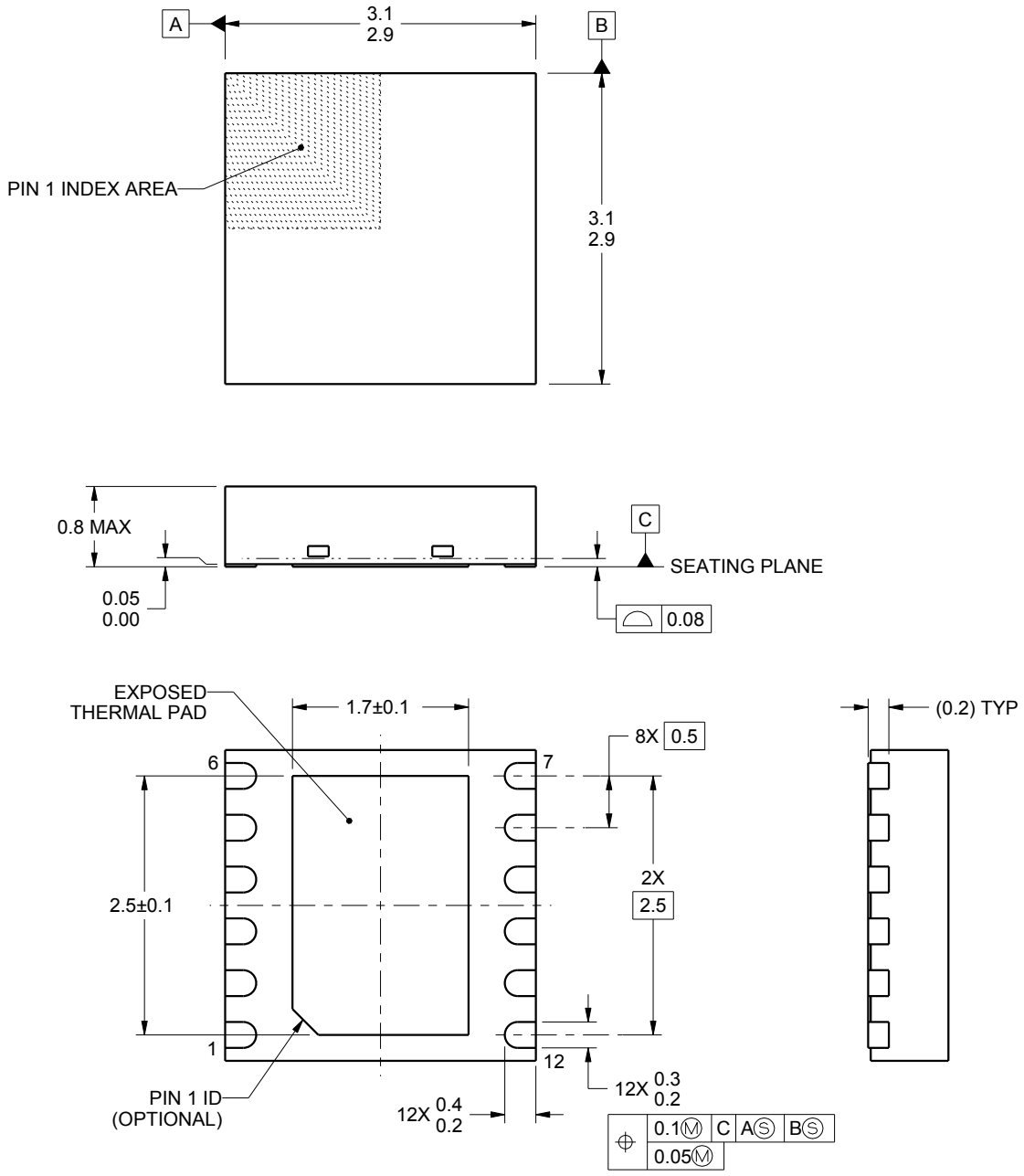
4223490/A

PACKAGE OUTLINE

DRR0012A

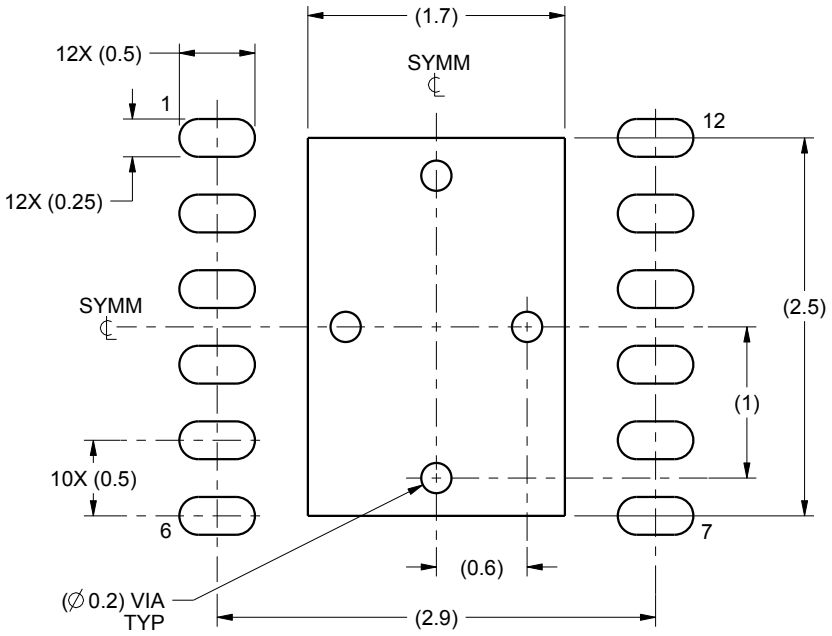
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

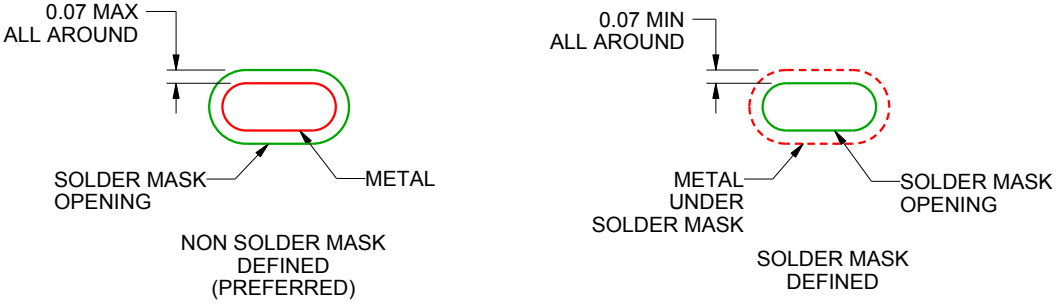


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

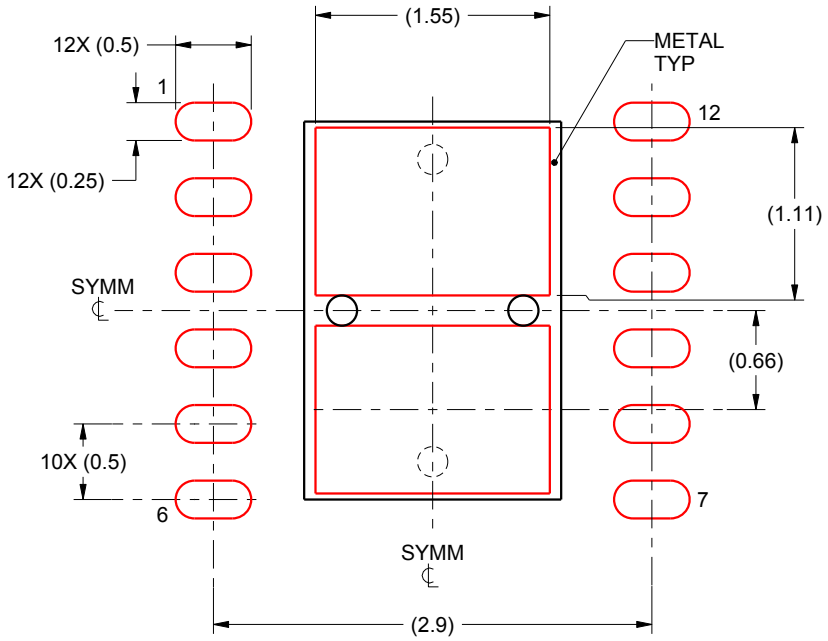


SOLDER MASK DETAILS

4221617/A 09/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4221617/A 09/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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