Robust, Industrial, Low Power 10BASE-T1L Ethernet MAC-PHY

Preliminary Technical Data

ADIN1110

FEATURES

- 10BASE-T1L IEEE® Std 802.3cg-2019™ compliant
- Supports 1.0 V pk-pk & 2.4 V pk-pk transmit levels
- Auto-Negotiation capability
- Supports intrinsic safety applications
  - External termination resistors
  - Separate Rx/Tx pins
- Integrated MAC with SPI interface
  - SPI interface supporting 10Mb/sec full duplex
  - Supports Open Alliance 10BASE-T1x MAC-PHY Serial Interface
  - MDIO memory map accessible via SPI
  - On Chip FIFOs: 20kB receive, 8kB transmit
    - Cut-through or Store & forward operation
    - Rx high & low priority queues
  - IEEE 1588 timestamp support
  - Statistics counters
  - 16 MAC addresses supported for frame filtering
- Unmanaged configuration using pin strapping including:
  - Master/Slave selection
  - Transmit amplitude
- 25 MHz crystal oscillator/25 MHz external clock input
- Single supply 1.8 V/3.3 V operation (mode dependent)
- Cable Reach
  - 1700 meters+ with 1.0 V pk-pk
  - 1700 meters+ with 2.4 V pk-pk
- Low power consumption – Dual supply 42 mW typ
- Link LED
- Small package 40-lead (6 mm x 6 mm) LFCSP
- Wide temperature range -40°C to 105°C

APPLICATIONS

- Process Control
- Factory Automation
- Building Automation

GENERAL DESCRIPTION

The ADIN1110 is a low power single port 10BASE-T1L MAC-PHY designed for industrial Ethernet applications. It integrates an Ethernet PHY core with a MAC and all the associated analog circuitry, input and output clock buffering.

The device operates from a single power supply rail of 1.8 V or 3.3 V.

Programmable transmit levels, external termination resistors and independent Rx/Tx pins make the ADIN1110 suited to intrinsic safety applications.

The ADIN1110 has an integrated voltage supply monitoring and power on reset circuitry to improve system level robustness.

The device has a 4-wire SPI interface for communication between the MAC and host processor.

The ADIN1110 is available in a 6 mm x 6 mm 40-ld package.

Table 1. Related Products.

Product No.	Description
ADIN1100	Robust, Industrial, Low Power 10BASE-T1L Ethernet PHY in 40-lead (6 mm x 6 mm) LFCSP

Rev. PrA

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FUNCTIONAL BLOCK DIAGRAM

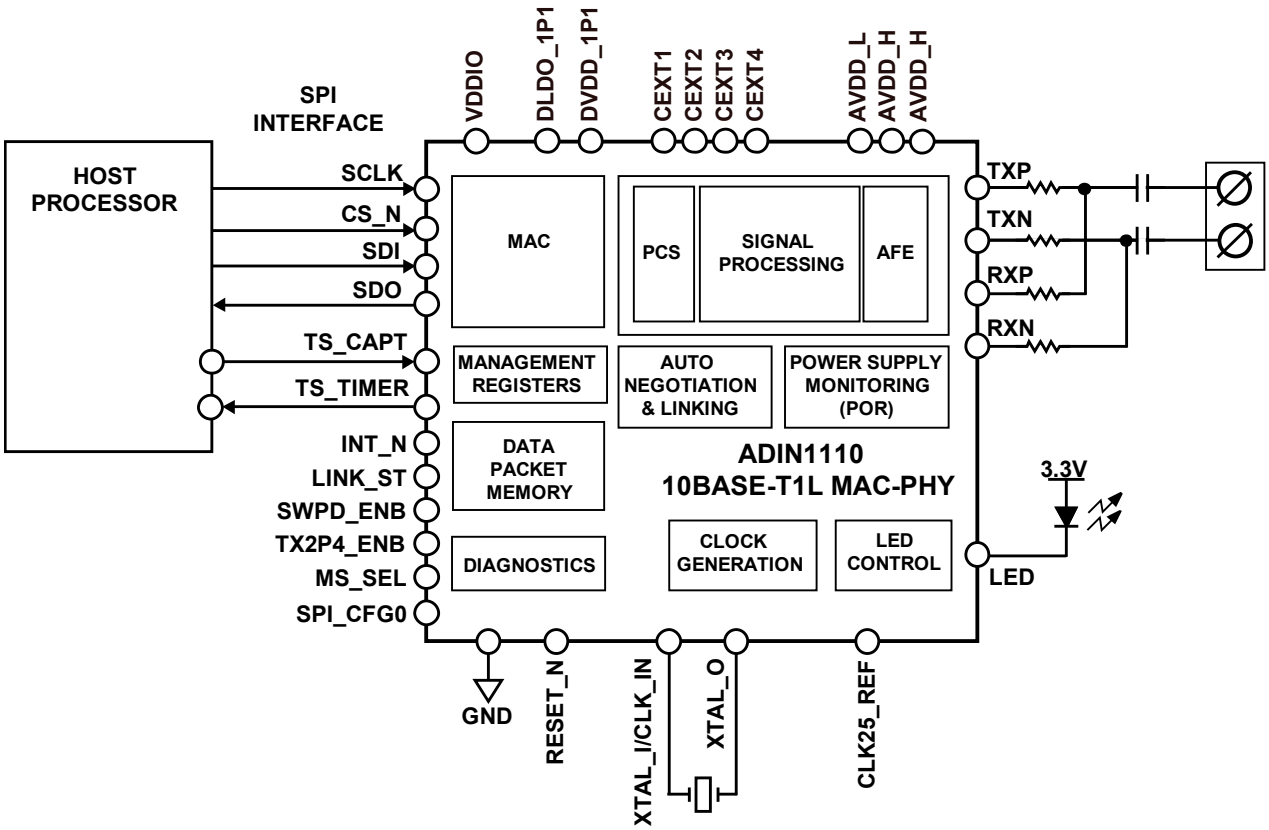

Figure 1.

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SPECIFICATIONS

AVDD_H= AVDD_L = VDDIO = 3.3 V; DVDD_1P1 supplied from Internal LDO (DVDD_1P1 = DLDO_1P1); All specifications at −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltage Range					
AVDD_H	3.13	3.3	3.46	V	2.4 V pk-pk or 1.0 V pk-pk Transmit Level
AVDD_L	1.71	1.8/3.3	3.46	V	
AVDD_H, AVDD_L	1.71	1.8	3.46	V	1.0 V pk-pk Transmit Level
DVDD_1P1	1.0	1.1	1.2	V	
VDDIO	1.71	1.8/2.5 /3.3	3.46	V	
1.0 V pk-pk Transmit Level (Single Supply)					AVDD_H=AVDD_L = VDDIO = 1.8 V DVDD_1P1 = DLDO_1P1
Supply Current, AIDD		28		mA	
Power Consumption		50		mW	100% data throughput, full activity
1.0 V pk-pk Transmit Level (Dual Supply)					AVDD_H = AVDD_L = VDDIO = 1.8 V DVDD_1P1 = External 1.1 V
Supply Current, AIDD		16		mA	
Supply Current, DIDD		12		mA	
Power Consumption		42		mW	100% data throughput, full activity
2.4 V pk-pk Transmit Level (Single Supply)					AVDD_H = AVDD_L = VDDIO = 3.3 V DVDD_1P1 = DLDO_1P1
Supply Current, AIDD		36		mA	
Power Consumption		119		mW	100% data throughput, full activity
2.4 V pk-pk Transmit Level (Dual Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V DVDD_1P1 = DLDO_1P1
Supply Current, AIDD		16.5		mA	
Supply Current, IDDIO		18		mA	
Power Consumption		87		mW	100% data throughput, full activity
2.4 V pk-pk Transmit Level (Triple Supply)					AVDD_H = 3.3 V, AVDD_L = VDDIO = 1.8 V, DVDD_1P1 = External 1.1 V
Supply Current, AIDD		16.5		mA	
Supply Current, IDDIO		6		mA	
Supply Current, DIDD		12		mA	
Power Consumption		78		mW	100% data throughput, full activity
DIGITAL INPUTS/OUTPUTS					Applies to SPI interface pins, SWPD_ENB, TX2P4_ENB, TS_TIMER/MS_SEL, TS_CAPT, INT_N, LINK_ST, RESET_N and LED
VDDIO = 3.3 V					
Input Low Voltage (V_{IL})			0.8	V	
Input High Voltage (V_{IH})	2.0			V	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) (min) = 4 mA
Output High Voltage (V_{OH})	2.4			V	Output high current (I_{OH}) (min) = 4 mA
VDDIO = 2.5 V					
V_{IL}			0.7	V	
V_{IH}	1.7			V	
V_{OL}			0.4	V	I_{OL} (min) = 4 mA
V_{OH}	2.0			V	I_{OH} (min) = 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VDDIO = 1.8 V					
V_{IL}			0.3 × VDDIO	V	
V_{IH}	0.7 × VDDIO			V	
V_{OL}			0.2 × VDDIO	V	I_{OL} (min) = 4 mA
V_{OH}	0.8 × VDDIO			V	I_{OH} (min) = 4 mA
RESET_N deglitch time	0.3	0.5	1	µs	
LED OUTPUT					
Output Drive Current	8			mA	VDDIO = 3.3 V
	6			mA	VDDIO = 2.5 V
	4			mA	VDDIO = 1.8 V
CLOCKS					
External Crystal (XTAL)					Requirements for external crystal used on XTAL_I pin and XTAL_O pin
Crystal Frequency		25		MHz	
Crystal Frequency Tolerance	−30		+30	ppm	
Crystal Drive Level		<200		µW	
Crystal ESR			60	Ω	
XTAL_I, XTAL_O Cin,eq		1.5		pF	Equivalent parallel differential input capacitance looking into XTAL pins
Crystal Load Capacitance (C_L) [1]		10	18	pF	Including PCB trace capacitance and XTAL_I, XTAL_O $C_{in,eq}$
XTAL_I Jitter		2	TBD	ps	Absolute rms jitter, frequency range 1 kHz to 12.5 MHz
Start-up Time			2	ms	Crystal Oscillator Only
Clock Input (CLK_IN)					
Clock Input Frequency		25		MHz	Requirements for external clock applied to XTAL_I pin, MII mode
		50		MHz	RMII mode
Clock Input Voltage Range	0.8		2.5	Vp-p	AC-coupled sine or square wave at XTAL_I pin
Clock Input Duty Cycle	45		55	%	
XTAL_I $Z_{in,eq}$					
R_P		6		kΩ	R_p||C_p
C_P		3		pF	
Jitter			TBD	ps rms	
CLK25_REF clock output					
CLK25_REF Frequency		25		MHz	
VOH		1.05		V	Load 10pF
VOL		0		V	Load 10pF
CLK25_REF Duty Cycle	45		55	%	Load 10pF
CLK25_REF Frequency Tolerance	−50		+50	ppm	

[1] Where load capacitance (C_L) = ((C1 × C2)/(C1 + C2) + C_{STRAY}), where C_{STRAY} is the stray capacitance including routing and package parasitics.

TIMING CHARACTERISTICS

POWER-UP TIMING

Table 3. Power Up Timing

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramp time			40	ms
t1	Minimum time interval to internal power good [1]	20		43	ms
t2	Hardware configuration latch time	6	8	14	µs
t3	Management interface active			50	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

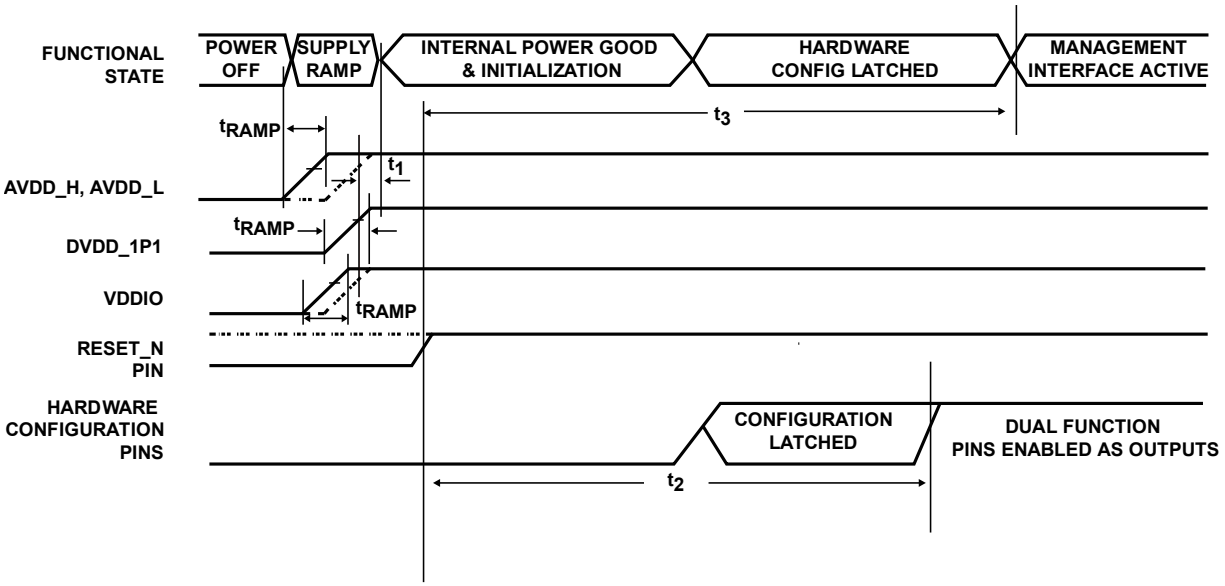


Figure 2. Power-Up Timing

SPI SERIAL INTERFACE

Table 4.

Parameter[1]	Description	Min	Typ	Max	Unit
t_1	SCLK cycle time (generic SPI protocol)	42			ns min
t_1	SCLK cycle time (Open-Alliance SPI protocol)	50			ns min
t_2	SCLK high time	17			ns min
t_3	SCLK low time	17			ns min
t_4	CS_N falling edge to SCLK falling edge setup time	21			ns min
t_5	Last SCLK falling edge to CS_N rising edge	21			ns min
t_6	CS_N high time	42			ns min
t_7	Data setup time	5			ns min
t_8	Data hold time	5			ns min
t_9	RESET_N pulse width	10			µs min
t_{10}	SCLK rising edge to SDO valid			15	ns max
t_{11}	SCLK rising edge to SDO tristate	12			ns min

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of VDDIO) and timed from a voltage level of 1.2 V. t_R is rise time. t_F is fall time.

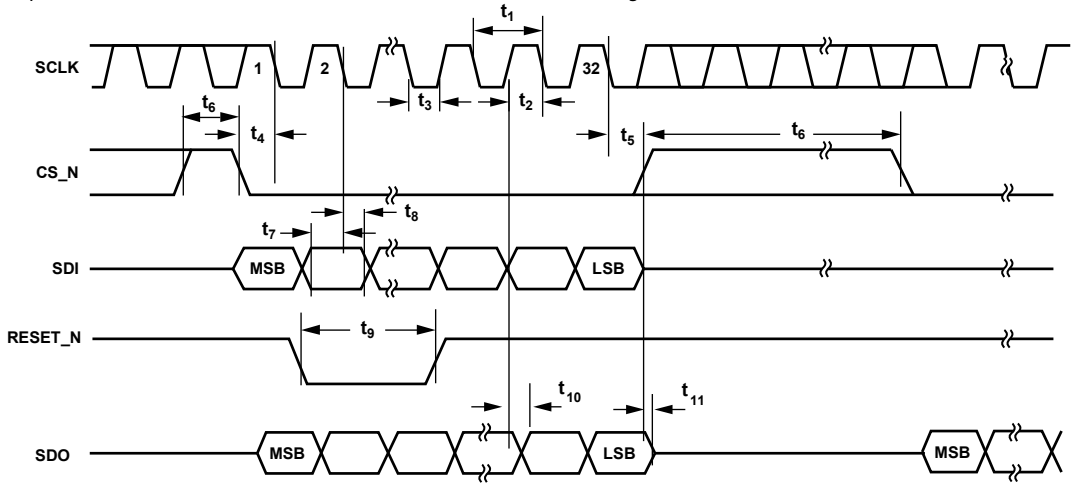


Figure 3. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VDDIO to GND	−0.3 V to +4 V
DVDD_1P1, DLDO_1P1 to GND	−0.3 V to +1.35 V
AVDD_H, AVDD_L to GND	−0.3 V to +4 V
SPI Interface, INT_N to GND	−0.3 V to VDDIO + 0.3 V
TXN, TXP, RXN, RXP to GND	−0.3 V to AVDD + 0.3 V
LED, RESET_N, LINK_ST to GND	−0.3 V to VDDIO + 0.3 V
XTAL_I/CLK_IN to GND	−0.3 V to 2.75 V
XTAL_O, CLK25_REF to GND	−0.3 V to 1.35 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD	
Human Body Model (HBM)	
TXN, TXP, RXN, RXP Pins	4kV
All Other pins	2 kV
Machine Model (MM)	200V
Field Induced Charged Device Model (FICDM)	1.25 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

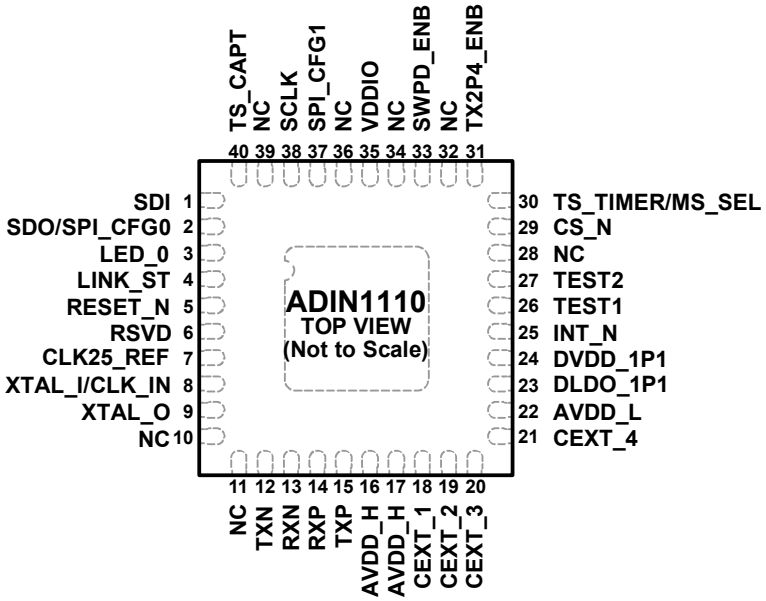
Package Type	θ_{JA}	Unit
CP-40-29	TBD	°C/W

Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS AND TO GND.

Figure 4.

Table 7. Pin Function Descriptions (hardware pin configuration groupings are subject to change)

Pin No.	Mnemonic[1]	Description
CLOCK INTERFACE		
8	XTAL_I/CLK_IN	Input for crystal/single ended 25MHz reference clock.
9	XTAL_O	Crystal output. If using a single ended reference clock on XTAL_I/CLK_IN, leave XTAL_O open circuit. See the External Clock Input section.
7	CLK25_REF	Analog reference clock output. The 25 MHz reference clock from the crystal oscillator is available on the CLK25_REF pin.
SPI INTERFACE		
38	SCLK	Serial Clock Input, data is clocked into the shift register on each falling edge.
29	CS_N	Active low Chip Select. See the MDIO PHY Address Determination section for a description of how the CS_N pin value latched on power-up or reset can affect the MDIO PHY address.
1	SDI	Serial Data Input, data is clocked in on the SDI pin on each falling edge.
2	SDO/SPI_CFG0[2]	SDO: Serial Data Output, data is clocked out on the SDO pin on each rising edge.
		SPI_CFG0: Configure the part to use an 8-bit CRC on the SPI host interface. See Table 11.
37	SPI_CFG1	Reserved for more SPI configurations on final product, may need a 4.7kΩ pull-up resistor to VDDIO.
25	INT_N	Management interface interrupt pin output. Open drain, active low output. A low on INT_N indicates an unmasked management interrupt. This pin requires a 1.5 kΩ pull-up resistor to VDDIO.
TIME STAMP SUPPORT		
40	TS_CAPT	Time stamp capture, input to ADIN1110. See 802.1AS Support section. If not using the time stamp function, this pin can be left floating as there is an internal pull down resistor present.
30	TS_TIMER/MS_SEL[2]	TS_TIMER: Time Stamp Timer output. See 802.1AS Support section.
		MS_SEL: Master/Slave Selection. Set high for prefer master selection, low for prefer slave selection. See Table 9.

Pin No.	Mnemonic[1]	Description
RESET		
5	RESET_N	Active low input. Hold low for >10 µs. RESET_N does not require a pull-up resistor as there is an internal pull-up already in place.
MEDIA DEPENDENT INTERFACE (MDI)		
15	TXP	Transmit Positive pin.
12	TXN	Transmit Negative pin.
14	RXP	Receive Positive pin.
13	RXN	Receive Negative pin.
CONFIGURATION/STATUS		
4	LINK_ST	Link Status output to indicate whether a valid link has been established. LINK_ST is active high.
3	LED_0	Programmable LED indicator for general purpose LED. The LED is active low. By default, LED is disabled. This is subject to change. A common configuration is for the LED to turn on when a link is established. See the LED Link section.
33	SWPD_ENB[2]	Software Powerdown Configuration. Set low to configure PHY to enter Software Powerdown mode after power-up/reset. See Table 8.
31	TX2P4_ENB[2]	Transmit Level Amplitude hardware configuration pin. Set high for 1.0 V pk-pk transmit amplitude only, set low to support both 1.0 V pk-pk and 2.4 V pk-pk transmit amplitude. See Table 10.
LDOs, REFERENCE		
18	CEXT_1	External decoupling for reference used in analog circuit. Connect a 4.7 µF cap to ground as close as possible to this pin.
19	CEXT_2	External decoupling for LDO circuit. Connect a 0.1 µF cap to ground as close as possible to this pin.
20	CEXT_3	External decoupling for LDO circuit. Connect a 1 µF cap to ground as close as possible to this pin.
21	CEXT_4	External decoupling for LDO circuit. Connect a 1 µF cap to ground as close as possible to this pin.
POWER AND GROUND PINS		
16, 17	AVDD_H	Analog supply voltage for the various analog circuits in the device. This supply rail can be supplied by 1.8 V to 3.3 V depending on the transmit level configuration. If AVDD_H is 3.3 V both 1.0 V pk-pk and 2.4V pk-pk transmit operating modes are supported. If AVDD_H is 1.8 V only 1.0 V pk-pk transmit operating mode is supported. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
22	AVDD_L	Analog supply voltage for the internal LDOs. This supply rail can be supplied by 1.8V to 3.3 V. It could be connected direct to the AVDD_H rail in long reach applications or to an alternative lower voltage rail when the device is configured with dual supplies for lower power consumption. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to this pin.
35	VDDIO	3.3V/2.5V/1.8V digital power for SPI interface. Connect 0.1 µF and 0.01µF capacitors to GND as close as possible to the pin.
24	DVDD_1P1	Input pin for 1.1 V DVDD_1P1 supply rail. When using the internal LDO, connect this pin directly to the DLDO_1P1 pin. Alternatively, an external 1.1 V rail can be provided to the pin for greater power efficiency. Connect 0.1 µF capacitor to GND as close as possible to the pin.
23	DLDO_1P1	Digital Core 1.1 V power supply output pin. Connect 0.68 µF capacitor to GND as close as possible to the pin. When using the internal LDO, connect this pin directly to the DVDD_1P1 pin.
6	RSVD	Reserved. On first samples this pin must be connected to GND through a 10kΩ pull-down resistor. This pin will be 2nd LED output on final product.
	EP	Exposed Pad. This is the GND paddle and it must be connected to GND. The LFCSP package has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND. A 4 × 4 array of thermal vias beneath the exposed GND pad is also recommended.
OTHER PINS		
10, 11, 28, 32, 34, 36, 39	NC	No connect. These pins must be left open-circuit.

Pin No.	Mnemonic[1]	Description
26	TEST1	This pin requires a 1.5 kΩ pull-up resistor to VDDIO.
27	TEST2	This pin must be left open-circuit.

[1] Where a pin is shared between a functional signal and a hardware pin configuration, the hardware pin configuration signal is listed last and the pin will be referred to using the functional signal(s) name throughout the datasheet.

[2] All of the hardware configuration pins have internal pull-down resistors. The default mode of operation without any external resistors connected to these pins is captured in Table 7. If an alternative mode of operation is required, 4.7 kΩ pull-up resistors should be used.

THEORY OF OPERATION

The ADIN1110 is a low power single port 10 Mb/s Ethernet MAC-PHY, integrating a PHY core and MAC with all the associated common analog circuitry, input and output clock buffering, the SPI interface and sub-system registers as well as the control logic to manage the reset and clock control and hardware pin configuration. The ADIN1110 is available in a 40-ld LFCSP package.

POWER SUPPLY DOMAINS

The ADIN1110 has three power supply domains and requires a minimum of one supply rail.

- AVDD_H is the analog power supply input for the analog front end (AFE) circuitry in the ADIN1110.
- AVDD_L is the analog supply voltage for the internal LDOs. It can be connected to the AVDD_H rail when in single supply mode, or to an alternative lower voltage rail when the device is configured with dual supplies for lower power consumption.
- DVDD_1P1 is the 1.1 V digital core power supply input, it can operate from an internal 1.1 V LDO coming from the DLDO_1P1 pin to the DVDD_1P1 pin. Alternatively, DVDD_1P1 can be driven from an external 1.1 V supply for greater power efficiency.
- VDDIO enables the SPI interface voltage supply to be configured independently of the other circuitry on the ADIN1110. It can be connected directly to the AVDD_L rail.

In a single supply application, connect AVDD_H = AVDD_L = VDDIO and use the internal 1.1 V LDO for DVDD_1P1. The appropriate supply voltage used will depend on the end application and cable length. For long reach/trunk applications the higher transmit amplitude of 2.4 V pk-pk requires AVDD_H = 3.3 V whereas spur applications can use a lower transmit amplitude of 1.0 V pk-pk with an AVDD_H = 1.8 V.

MAC

The MAC included in the ADIN1110 supports 16 different MAC addresses. It also has one low priority RX FIFO, one high priority RX FIFO and one TX FIFO. These FIFOs can ship data in store and forward mode when using the generic SPI protocol and in either store and forward or cut-through mode when using the Open-Alliance protocol.

A generic and Open-Alliance version of the SPI protocol are available. The data is transferred over the SPI interface half duplex using the generic SPI protocol and full duplex using the Open-Alliance SPI protocol. See the Register Summary section.

Interrupt (INT_N)

The ADIN1110 is capable of generating an interrupt to a host processor using the INT_N pin in response to a variety of user-selectable conditions. The following conditions can be selected to generate an interrupt:

- Link status change
- Port 1 Rx FIFO contains data
- Tx Ready
- Timestamp Captured
- Operation Error Detected
- PHY related interrupts

When an interrupt occurs, the system can poll the MAC Status register (STATUS) to determine the origin of the interrupt.

AUTO-NEGOTIATION

The ADIN1110 uses Auto-Negotiation capability in accordance with IEEE 802.3 Clause 98, providing a mechanism for exchanging information between PHYs to allow link partners to agree to a common mode of operation. During the Auto-Negotiation process, the PHY advertises its own capabilities and compares to those received from the link partner. The concluded operating mode is the transmit amplitude mode and master/slave preference common across the two devices.

In the event of the link being dropped, the Auto-Negotiation process restarts automatically. Auto-Negotiation can be restarted by request through a write to the Auto-Negotiation restart bit (AN_RESTART) in the Auto-Negotiation control register (AN_CONTROL, device address 0x07, register address 0x0200, bit 9).

The Auto-Negotiation process takes some time to complete, depending on the number of pages exchanged, but is always the fastest way to bring up a link. Clause 98 of the IEEE 802.3 standard details the timers related to Auto-Negotiation.

Note, Auto-Negotiation is enabled by default for the ADIN1110 and it is strongly recommended that Auto-Negotiation is always enabled.

Transmit Amplitude Resolution

Auto-Negotiation is used to resolve the transmit amplitude resolution. The PHY can be configured to support both 1.0 V pk-pk and 2.4 V pk-pk transmit levels or to operate with 1.0 V pk-pk transmit level only through the hardware configuration (see Table 10). This configuration can also be done in software using the 10BASE-T1L high level transmit operating mode ability (AN_ADV_B10L_TX_LVL_HI_ABL) and 10BASE-T1L high level transmit operating mode request (AN_ADV_B10L_TX_LVL_HI_REQ) register bits (device address 0x07, register address 0x0204, bits 13 and 12 respectively).

To operate at 2.4 V pk-pk transmit level, both the local and remote PHYs must advertise that they are capable of operating at 2.4 V and at least one PHY must request 2.4 V pk-pk transmit level operation.

If it is required to only operate the PHY at 1.0 V pk-pk transmit level operation, then AN_ADV_B10L_TX_LVL_HI_ABL should be 0, so that 2.4 V pk-pk transmit level operation is not

advertised. In this case Auto-Negotiation can only resolve to 1.0 V pk-pk transmit level operation, irrespective of what setting the remote PHY advertises.

Master/Slave Resolution

Auto-Negotiation is also used to resolve master or slave status. The PHY can be configured to prefer slave or prefer master through the hardware configuration (see Table 9). If Auto-Negotiation is disabled, the MS_SEL hardware configuration pin sets the default master/slave selection. Note that the recommended use of the ADIN1110 is with Auto-Negotiation enabled.

During Auto-Negotiation, when prefer slave is selected, and the remote end is prefer or forced Master, the local PHY will be set to slave (and remote to master). When the remote end is prefer or forced slave, the local PHY will be set to master (and remote to slave).

MDI INTERFACE

The Media Dependent Interface (MDI) connects the ADIN1110 to the Ethernet network via a twisted wire pair.

The ADIN1110 requires an external hybrid between the separate TXN/P and RXN/P pins and the twisted wire pair. This external hybrid allows the system to have full-duplex communication, by removing the local transmit signal from the combined signal on the cable, leaving just the desired receive signal.

The ADIN1110 hybrid requires a specific topology and values for correct operation. The topology and values for the components can be seen in Figure 5.

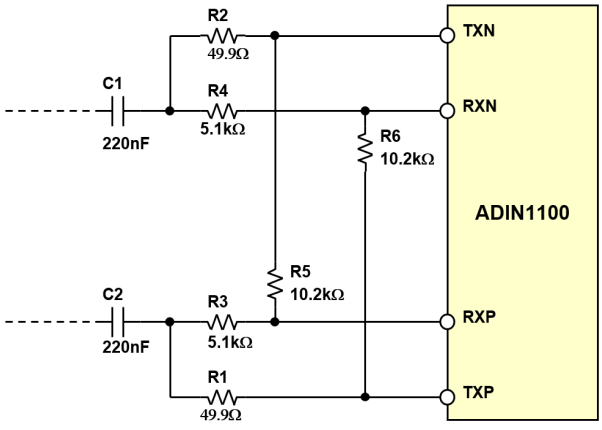


Figure 5. Recommended hybrid for the ADIN1110.

The size, power and voltage rating of these components should be considered in the context of other system requirements, for example, requirements of intrinsic safety.

RESET OPERATION

The ADIN1110 supports a number of resets - power-on reset, hardware reset, and multiple software reset types (full chip software reset, PHY subsystem reset and MAC only reset). All of these put the ADIN1110, including the PHY core and MAC into a known state. Whenever the MAC is reset, the SPI output pins are driven to a low state.

Power-On Reset

The ADIN1110 includes power monitoring circuitry to monitor all of the supplies. At power-up the ADIN1110 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value and the power is considered good.

Brown out protection is provided by monitoring the supplies to detect if one or more of the supplies drops below a minimum falling threshold value and holding the part in hardware reset until the power is good again.

Hardware Reset

A hardware reset is initiated by the power-on reset circuitry or by asserting the RESET_N pin low. The pin should be brought low for a minimum of 10 µs. De-glitch circuitry is included on this pin to reject pulses of a maximum of 1 µs.

When the RESET_N pin is de-asserted, all the I/O pins are held in tristate mode and the hardware configuration pins are latched, and then the I/O pins are configured for their functional mode. Once all the external and internal supplies are valid and stable, the crystal oscillator circuit is enabled, and after some time for the crystal start-up and stabilization, the PLL is enabled. After approximately 50 ms (max) from the de-assertion of RESET_N, all the internal clocks are valid, the internal logic is released from reset and all the management interface registers are accessible so that the device can be programmed.

Software Reset

A full chip software reset can be initiated by writing the required pair of keys to the SPI software reset register (SOFT_RST - Table 38) to reset the MAC and PHY.

If a transmission was taking place when the SPI software reset was initiated, the frame transmission will stop abruptly and a runt or a frame with a bad CRC may be transmitted. Once the MAC-PHY is reset, the ADIN1110 will be ready to bring up links.

When this software reset is initiated, a full initialization of the chip, almost equivalent to a hardware reset, is done. The I/O pins are held in tristate mode and the hardware configuration pins are latched, and then the I/O pins are configured for their functional mode. The crystal oscillator circuit is enabled, and after some time for the crystal start-up and stabilization, the PLL is enabled. Approximately 10 ms (max) after writing the SOFT_RST keys, the internal logic is released from reset and all the management interface registers are accessible.

MAC Subsystem Reset

A MAC subsystem reset can be initiated by writing the key 0x4F1C followed by the key 0xC1F4 to the software reset (SPI register address 0x14). When this bit is set, a reset sequence is provided to the MAC without dropping the existing links. The

reset is applied for about 1.2 µs. The MAC subsystem reset interrupts any Tx/Rx packet exchange between the MAC and the PHY but does not drop any existing link nor prevents a link being established. PHY management registers are not initialized.

The PHY needs to be out of software powerdown (Device address 0x1E, register address: 0x8812).

PHY Subsystem Reset

The PHY subsystem is the part of the ADIN1110 that incorporates the 10BASE-T1L PHY transceiver analog and digital circuits. A PHY subsystem reset can be initiated by setting the PHY subsystem reset register bit (CRSM_PHY_SUBSYS_RST, device address 0x1E, register address 0x8814, bit 0). When this bit is set, the PHY subsystem is reset. The reset is applied for about 1.2 µs and then this bit self clears. All of the PHY digital circuitry is reset and any existing link will drop. The management registers are not initialized by this reset, and access to all the management registers is available during the PHY subsystem reset. This is a short reset and can be used to put the part into a known state while retaining any software initialization of the part.

STATUS LED

LED Link

The ADIN1110 provides a configurable status LED. The LED can be used to indicate link status. By default, the LED is disabled (default behaviour is subject to change) and can be enabled by setting the LED enable bit (LED_EN) within the LED control register (LED_CNTRL, device address 0x1E, register address 0x8C81, bit 0).

Link Status Pin

In addition to the LED pin, there is also a LINK_ST pin. This pin is asserted when the link status bit (AN_LINK_STATUS, device address 0x07, register address 0x0201, bit 2) is asserted and indicates that the link is established. The LINK_ST pin is active high.

POWERDOWN MODES

The ADIN1110 supports a number of powerdown modes - hardware powerdown and software powerdown. The lowest power mode is hardware powerdown where the part is turned fully off and the registers are not accessible.

Hardware Powerdown Mode

Hardware powerdown is a useful mode when operation of the ADIN1110 is not required and power is to be minimized. The ADIN1110 enters hardware powerdown mode when the RESET_N pin is asserted and held low. In this mode, all analog and digital circuits are disabled, the clocks are gated off, all the I/O pins are held in tristate mode and the only power is the leakage power of the circuits. The management registers are not accessible in this mode.

Software Powerdown Mode

Software powerdown mode is a useful mode when the part is being configured by software before links are brought up. The ADIN1110 can be configured to enter software powerdown mode after reset using the RX_DV/SWPD_ENB pin. The ADIN1110 can also be instructed to enter software powerdown mode by setting the software powerdown bit (CRSM_SFT_PD, device address 0x1E, register address 0x8812, bit 0).

The software powerdown status bit (CRSM_SFT_PD_RDY, device address 0x1E, register address 0x8818, bit 1) indicates that the part is in the software powerdown state. In software powerdown mode, the analog and digital circuits are in a low power state, the PLL is active and can provide output clocks if configured to do so. Any signal or energy on the MDI pins are ignored and no link will be brought up. The management interface registers are accessible, and the part can be configured using software. The ADIN1110 exits software powerdown mode when the CRSM_SFT_PD bit is cleared. At this point the MAC-PHY will start Auto-Negotiation and attempt to bring up a link after Auto-Negotiation completes successfully.

HARDWARE CONFIGURATION PINS

The ADIN1110 can operate in unmanaged or managed applications. In unmanaged applications, it is possible to configure the desired operation of the MAC-PHY from hardware configuration pins without any software intervention. After coming out of reset, it will immediately start to attempt to bring up a link. Note for an unmanaged application, the MAC-PHY should not be hardware configured to enter software powerdown.

In managed applications, software is available to configure the MAC-PHY via the management interface. In this case, the user can configure the MAC-PHY to enter software powerdown after reset, software can then intervene to configure the device as required and bring the device out of software powerdown to allow linking to be established.

Hardware configuration pins are often shared with functional pins and the voltage level on the pin is sensed and latched upon exiting from a reset. All hardware configuration pins are 2-level sense using a pull-down or pull-up resistor.

HARDWARE CONFIGURATION PIN FUNCTIONS

The following functions are configurable from the ADIN1110 hardware pins:

- Software powerdown mode after reset
- Transmit amplitude configuration
- Master/Slave selection
- 8-bit SPI CRC

All of these pins have internal pull-down resistors, so the default mode of operation without any external resistors connected to these pins is captured in Table 7. If an alternative mode of operation is required, 4.7 kΩ pull-up resistors should be used.

Table 8. Default Hardware Configuration Modes

Hardware Configuration Pin Function	Default Mode
Software PD Mode after Reset	PHY in Software PD after reset
Master/Slave selection	Prefer Slave
Transmit Amplitude	1.0 V pk-pk / 2.4 V pk-pk
8-bit SPI CRC	Enabled

Software Powerdown after Reset

If the ADIN1110 is configured so that it does not enter software powerdown mode after reset, then once it exits reset, the ADIN1110 will start Auto-Negotiation and try to bring up a link after Auto-Negotiation completes successfully. If the ADIN1110 is configured so that it enters software powerdown mode after reset, the ADIN1110 will wait in software powerdown mode until it is configured over the SPI interface at which point, the PHY configuration can be set to exit software powerdown by software.

Table 9. Software Powerdown (Hardware Configuration)

Software Powerdown Configuration	SWPD_ENB
PHY in Software PD after reset	0
PHY not in Software PD	1

Master/Slave Preference

The MS_SEL hardware configuration pin is shared with the TS_TIMER pin and configures the default master/slave selection. If MS_SEL is pulled low during power-up/reset the part is configured by default to prefer slave (this is the case if no external pull-up resistor is connected to MS_SEL pin due to the presence of the internal pull-down resistor). If MS_SEL is pulled high during power-up/reset the part is configured by default to prefer master.

If Auto-Negotiation is disabled, this pin sets the default master/slave selection. Note, Auto-Negotiation is enabled by default for the ADIN1110 and it is strongly recommended that Auto-Negotiation is always enabled.

During Auto-Negotiation when prefer slave is selected, and the remote end is prefer or forced master, the local PHY will be set to slave (and remote to master). When the remote end is prefer or forced slave, the local PHY will be set to master (and remote to slave).

Table 10. Master/Slave Selection (Hardware Configuration)

Master/Slave Selection	MS_SEL
Prefer Slave selection	0
Prefer Master selection	1

Transmit Amplitude

The TX2P4_ENB hardware configuration pin allows the user to configure the required transmit amplitude mode for the intended application. If TX2P4_ENB is pulled low, the ADIN1110 is configured by default to support both 1.0 V pk-pk and 2.4 V pk-pk transmit levels, to be decided by Auto-Negotiation. If TX2P4_ENB is pulled high, the ADIN1110 is configured to disable 2.4 V pk-pk transmit operating mode by default and operate with 1.0 V pk-pk transmit level only. Note that if the TX2P4_ENB pin is strapped high (1.0 V pk-pk only), the associated register cannot be changed through the SPI interface, i.e. 2.4 V pk-pk operation is not possible if the ADIN1110 has been hardware pin-configured for 1.0 V pk-pk only.

The 1.0 V pk-pk transmit operating mode supports the spur use case and can operate at a lower AVDD_H supply voltage of 1.8 V. This supports intrinsic safe applications

The higher transmit operating mode of 2.4 V pk-pk supports trunk applications and requires a higher AVDD_H supply voltage of 3.3 V. This mode can be used for longer cable lengths in Industrial Ethernet environments with high noise levels.

Table 11. Transmit Amplitude Configuration (Hardware Configuration)

Transmit Amplitude Selection	TX2P4_ENB
1.0 V/ 2.4 V pk-pk	0
1.0 V pk-pk	1

8-Bit SPI CRC

When using the generic SPI protocol, it is possible to end SPI transactions with a CRC byte. This 8-bit CRC byte provides up to 3-bit error detection using the polynomial $x^8 + x^2 + x + 1$ seeded with 0x0. The 8-bit CRC will not be used for data transaction as ethernet frames already have their own 32-bit CRC. SPI CRC must be disabled when using the Open-Alliance protocol.

Table 12. Generic SPI Protocol 8-bit CRC (Hardware Configuration)

8-Bit CRC configuration	SPI_CFG0
Use 8-bit CRC on host SPI	0
Do not use 8-bit CRC on host SPI	1

BRINGING UP 10BASE-T1L LINKS

UNMANAGED PHY OPERATION

For an unmanaged PHY or lightly managed PHY application where there is no software management of the PHY, the hardware configuration pins determine the operating mode. The TX2P4_ENB pin configures the PHY to advertise the support of both 1.0 V pk-pk and 2.4 V pk-pk transmit level operation or to only advertise support of 1.0 V pk-pk transmit level operation. The MS_SEL pin is used to configure the PHY to advertise prefer slave or prefer master. The SWPD_ENB pin should be asserted at power-up and reset so that the PHY does not enter software powerdown mode when it exits reset. Once it exits reset, the ADIN1110 will start Auto-Negotiation and try to bring up a link after Auto-Negotiation completes successfully.

A lightly managed PHY may use the hardware configuration pins to determine the operation of the PHY and to bring up a 10BASE-T1L link. And afterwards software can monitor the operation of the PHY.

MANAGED PHY OPERATION

In a managed PHY application, software is used to configure the PHY operation using the management interface, the hardware configuration pins may be used to set the default values of the registers used to control the transmit amplitude and master/slave setting. The SWPD_ENB pin should be de-asserted at power-up and reset so that the PHY enters software powerdown mode when it exits reset. The PHY will stay in software powerdown mode until the software has configured the PHY and takes it out of software powerdown mode so that it can start Auto-Negotiation and try to bring up a link.

Power-up and Reset Complete

A typical way for software to verify that the part has completed the power-up and reset sequence and is available for normal operation is to verify that the SPI access to the MAC is working. This can be done either reading the SPI Protocol Control Register (SPI_PC, SPI address 0x00) and checking that the value read is 0x106; or writing and reading back the SPI Scratch Registers (SCRATCHn, SPI Address: 0xDC to 0xDF).

Once checked that the SPI access to the MAC is working, the following step is to check that PHY has initialized correctly. This can be done reading the management register that has the IEEE OUI, model and revision numbers. The value of this register is unique to each PHY vendor and is a non-zero value. If the part has not completed the power-up, the value read will not be correct. In legacy BASE-T PHYs this would be at MI register addresses 2 and 3.

In the ADIN1110 these can also be read at register addresses 2 and 3, but at Clause 45 device address 0x1E. The vendor specific MMD 1 device identifier high register (MMD1_DEV_ID1, device address 0x1E, register address 0x0002, bits [15:0]) has a value of 0x0283 and is the Organizationally Unique Identifier (OUI) bits[3:18]. The vendor specific MMD 1 device identifier low register contains the Organizationally Unique Identifier. bits[19:24] (MMD1_DEV_ID2_OUI, device address 0x1E, register address 0x0003, bits 15:10), the model number (MMD1_MODEL_NUM, bits 9:4) and the revision number (MMD1_REV_NUM, bits 3:0). For the ADIN1110:

- MMD1_DEV_ID1 = 0x0283;
- MMD1_DEV_ID2_OUI = 0x2F
- MMD1_MODEL_NUM = 0x9
- MMD1_REV_NUM = 0x0.

When a valid read of the IEEE OUI is done, the system ready bit (CRSM_SYS_RDY, device address 0x1E, register address 0x8818, bit 0) can also be read to verify that the start-up sequence is complete and the system is ready for normal operation.

The software powerdown status bit (CRSM_SFT_PD_RDY, device address 0x1E, register address 0x8818, bit 1) can be read to check if the part is in the software powerdown state. This is configured by the SWPD_ENB hardware configuration pin.

Configuring the Part for Linking

After power-up or reset, the ADIN1110 should be configured for the desired operation for linking. The ADIN1110 may already be configured as required by the hardware configuration pins, but greater control is available using the management registers.

The Auto-Negotiation process is used to agree the operating mode between a local and remote PHY. For example, Auto-Negotiation is used to agree which PHY operates as master and which as slave and is also used to agree the transmit level.

Auto-Negotiation is enabled by default for the ADIN1110 and it is strongly recommended that Auto-Negotiation is always kept enabled. Auto-Negotiation is defined by the IEEE standard and includes a number of mechanisms to ensure robust linking operation between PHYs and is the fastest way to bring up a link.

Advertisement of Transmit Level Operating Mode

If the 10BASE-T1L high voltage Tx ability read only register bit (B10L_TX_LVL_HI_ABLE, device address 0x01, register address 0x08F7, bit 12) is 1 and there is a 3.3 V supply provided on the AVDD_H pin, the ADIN1110 can support transmit level operation at either 1.0 V pk-pk or 2.4 V pk-pk. The higher transmit level can support longer reach but has high power consumption. The ADIN1110 can support 1.0 V pk-pk transmit level operation with a 1.8 V supply on the AVDD_H pin at very low power consumption. The 1.0 V pk-pk transmit level operation is required for intrinsically safe operation.

The ADIN1110 can either be configured to advertise support of both 1.0 V pk-pk and 2.4 V pk-pk transmit level operation (if B10L_TX_LVL_HI_ABLE = 1) or to advertise support of only 1.0 V pk-pk transmit level operation. This is set using the

10BASE-T1L high level transmit operating mode ability bit within the BASE-T1 Auto-Negotiation advertisement register (AN_ADV_B10L_TX_LVL_HI_ABL, device address 0x07, register address 0x0204, bit 13):
0 = support 1.0 V pk-pk transmit level only;

1 = support both 1.0 V pk-pk and 2.4 V pk-pk transmit level.

The ADIN1110 can also be configured to advertise a request for 2.4 V pk-pk transmit level operation (if B10L_TX_LVL_HI_ABLE = 1). This is set using the 10BASE-T1L high level transmit operating mode request bit (AN_ADV_B10L_TX_LVL_HI_REQ, device address 0x07, register address 0x0204, bit 12):
0 = request 1.0 V pk-pk transmit level;

1 = request 2.4 V pk-pk transmit level.

The link partner advertised transmit level ability can be read in the link partner 10BASE-T1L high level transmit operating mode ability register bit (AN_LP_ADV_B10L_TX_LVL_HI_ABL, device address 0x07, register address 0x0207, bit 13). The link partner advertised transmit level request can be read in the link partner 10BASE-T1L high level transmit operating mode request register bit (AN_LP_ADV_B10L_TX_LVL_HI_REQ, device address 0x07, register address 0x0207, bit 12). These bits are updated during the Auto-Negotiation process and are valid when the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set.

If either the local or remote PHY advertises that it is not capable of transmitting in the high level (2.4 V pk-pk) transmit operating mode or if neither the local nor remote PHY advertises a request for high level (2.4 V pk-pk) transmit operating mode, then the result will be operation at 1.0 V pk-pk transmit level.

If both the local and remote PHY advertises that they are capable of transmitting in the high level (2.4 V pk-pk) transmit operating mode and if either the local or remote PHY advertises a request for high level (2.4 V pk-pk) transmit operating mode, then the result will be operation at 2.4 V pk-pk transmit level.

Hence, a PHY can ensure it must operate at 1.0 V pk-pk transmit level. But it can only request operation at 2.4 V pk-pk transmit level.

Table 13. Determination of Transmit Level by Auto-Negotiation

HI_ABL[1]	HI_REQ[1]	LP_HI_ABL[1]	LP_HI_REQ[1]	Transmit Level
0	X	0	X	1.0 V pk-pk
1	X	0	X	1.0 V pk-pk
0	X	1	X	1.0 V pk-pk
1	0	1	0	1.0 V pk-pk
1	0	1	1	2.4 V pk-pk
1	1	1	0	2.4 V pk-pk
1	1	1	1	2.4 V pk-pk

[1]HI_ABL, HI_REQ, LP_HI_ABL and LP_HI_REQ refer to the advertisement bits AN_LP_ADV_B10L_TX_LVL_HI_ABL, AN_LP_ADV_B10L_TX_LVL_HI_REQ, AN_ADV_B10L_TX_LVL_HI_ABL and AN_ADV_B10L_TX_LVL_HI_REQ respectively.

Advertisement of Master/Slave

The 10BASE-T1L standard uses what is known as a master/slave clock scheme. This is commonly used in full-duplex transceiver standards using echo cancellation. One PHY is designated as the master and the other PHY as the slave. Auto-Negotiation is used to agree which PHY is the master and which is the slave and it generally doesn't matter which is which.

The ADIN1110 has an internal pull-down resistor on the MS_SEL pin and this results in a default setting of configuring the PHY to advertise prefer slave. The recommendation is to either use the default setting of advertise prefer slave or to use a setting of advertise prefer master.

If it is mandatory for the PHY to operate as master, then an advertise forced mater configuration should be used. However, this should be used with caution, as if remote end is also forced master, there is a configuration fault and Auto-Negotiation will fail and the link will not come up.

The force master/slave configuration register bit (AN_ADV_FORCE_MS, device address 0x07, register address 0x0202, bit 12) is used to configure the PHY to advertise its master/slave configuration as a preference or as a forced value, as follows:
0 = master/slave configuration is a preferred mode;
1 = master/slave configuration is a forced mode.

The master/slave configuration register bit (AN_ADV_MST, device address 0x07, register address 0x0203, bit 4) is used to configure the PHY to advertise its master/slave configuration, as follows:
0 = slave;
1 = master.

The link partner advertised master/slave setting can be read in the link partner force master/slave configuration register bit (AN_LP_ADV_FORCE_MS, device address 0x07, register address 0x0205, bit 12) and the link partner master/slave configuration register bit (AN_LP_ADV_MST, device address 0x07, register address 0x0206, bit 4). These bits are updated

during the Auto-Negotiation process and are valid when the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set.

When the local and remote PHY have the same preferred configuration, e.g. both slave or both master; a random process is used to determine which is master and which is slave. When one PHY has a forced configuration, its master/slave configuration is given priority over a PHY with a preferred setting where both PHYs have the same master/slave configuration. If both PHYs have a forced configuration and the same master/slave configuration, there is a configuration fault and Auto-Negotiation will fail.

Table 14. Determination of Master/Slave by Auto-Negotiation

Local		Remote		Local	Remote
Force[1]	MST[1]	Force[1]	MST[1]	M/S Resolution	
0	0	0	0	Master/Slave	Slave/Master
0	0	0	1	Slave	Master
0	1	0	0	Master	Slave
0	1	0	1	Master/Slave	Slave/Master
0	X	1	0	Master	Slave
0	X	1	1	Slave	Master
1	0	0	X	Slave	Master
1	1	0	X	Master	Slave
1	0	1	0	Config Fault	Config Fault
1	0	1	1	Slave	Master
1	1	1	0	Master	Slave
1	1	1	1	Config Fault	Config Fault

[1] Where Force and MST refer to the advertisement bits AN_ADV_FORCE_MS, AN_ADV_MST, AN_LP_ADV_FORCE_MS and AN_LP_ADV_MST.

The resolution of master/slave can be read using the master/slave resolution result register bits (AN_MS_CONFIG_RSLTN, device address 0x07, register address 0x8001, bits 6:5). This indicates if the PHY is configured as a slave or a master or if there was a configuration fault. These bits are updated during the Auto-Negotiation process and are valid when the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set.

Successful Completion of Auto-Negotiation

When Auto-Negotiation has completed, the Auto-Negotiation complete indication register bit (AN_LINK_GOOD, device address 0x07, register address 0x8001, bit 0) is set. This bit indicates completion of the Auto-Negotiation transmission, and that the enabled PHY technology is either bringing up its link, or that it has brought up its link.

When Auto-Negotiation has completed and the link is up the Auto-Negotiation complete register bit (AN_COMPLETE, device address 0x07, register address 0x0201, bit 5) is set. When this bit is read as one, it means that the Auto-Negotiation process has been completed, the PHY link is up, and that the contents of the AN_ADV_ABILITY and AN_LP_ADV_ABILITY register bits are valid.

Link Status

The status of the link can be determined by reading the link status register bit (AN_LINK_STATUS, device address 0x07, register address 0x0201, bit 2). This bit latches low. When read as one, this bit indicates that a valid link has been established. If this bit reads zero, it means that the link has failed since the last time it was read. If the value of this bit is read as zero, it needs to be read a second time to determine the link status at this time (see Latch Low Registers section).

In the event of the link being dropped, the Auto-Negotiation process restarts automatically. Auto-Negotiation can be restarted by request through a write to the Auto-Negotiation restart bit (AN_RESTART) in the Auto-Negotiation control register (AN_CONTROL, device address 0x07, register address 0x0200, bit 9).

ON-CHIP DIAGNOSTICS

LOOPBACK MODES

The PHY core within the MAC-PHY provides several loopback modes: PMA loopback, PCS loopback, MAC interface loopback and MAC interface remote loopback. These loopback modes test and verify various functional blocks within the PHY. The use of frame generator and frame checkers allow completely self-contained in-circuit testing of the digital and analog data paths within the PHY core. A loopback can also be established that includes the MAC portion of the ADIN1110, i.e. not limited to just the PHY core, by implementing the necessary software within the host processor.

PMA Loopback

For PMA loopback, leave the MDI pins open-circuit, thereby transmitting into an unterminated connector/cable. For the most accurate results leave the cable disconnected. The PHY can then operate by receiving the reflection from its own transmission. This loopback is intended as an implementation of IEEE Std 802.3cg subclause 146.5.6 PMA Local Loopback. Note that for 10BASE-T1L PMA local loopback, the device needs to be configured in the forced link configuration mode (Auto-Negotiation disabled). Setting the B10L_LB_PMA_LOC_EN bit (B10L_PMA_CNTRL register, device address 0x01, register address 0x08F6) enables PMA loopback.

PCS Loopback

PCS loopback mode loops the Tx data back to the Rx within the PCS block at the input stage of the PHY digital block. Setting the B10L_LB_PCS_EN bit (B10L_PCS_CNTRL register, device address 0x03, register address 0x08E6) enables PCS loopback.

When the PCS loopback mode is enabled, no signal is transmitted to the MDI pins.

MAC Interface Loopback

MAC interface loopback mode loops the data received on the MAC interface TXD pins back to the RXD pins. Setting the MAC_IF_LB_EN bit (MAC_IF_LOOPBACK register, device address 0x1E, register address 0x803D) enables MAC interface loopback. Note that if the MAC_IF_LB_TX_SUP_EN bit, within the same register, is set, which is its default state, then transmission of the signal is suppressed to the MDI pins.

MAC Interface Remote Loopback

MAC interface remote loopback requires a link up with a remote PHY and enables looping of the data received from the remote PHY back to the remote PHY. This linking allows a remote PHY to verify a complete link by ensuring that the PHY receives the proper data. Setting the MAC_IF_REM_LB_EN bit (MAC_IF_LOOPBACK register, device address 0x1E, register address 0x803D) enables MAC interface remote loopback. Note that if the MAC_IF_REM_LB_RX_SUP_EN bit, within the same register, is set, which is its default state, then the data received by the PHY is suppressed and not sent to the MAC.

Host Processor Loopback

Outside of loopback modes associated with the PHY core within the ADIN1110, the host processor can be utilized to create a full MAC loopback, whereby whatever frame is received from the MAC is transmitted back to the MAC as depicted on the left-hand side of Figure 5.

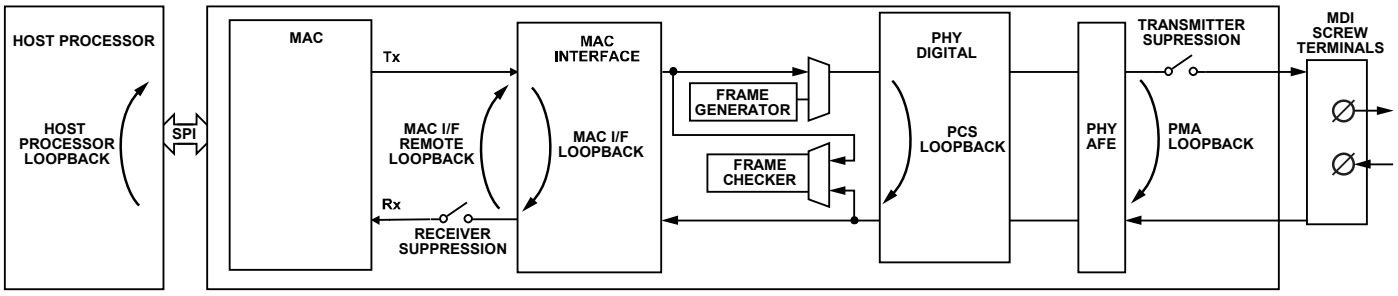


Figure 6. ADIN1110 Loopback Modes

FRAME GENERATOR AND CHECKER

The ADIN1110 can be configured to generate frames and to check received frames (see Figure 6). The frame generator and checker can be used independently to just generate frames or just check frames or can be used together to simultaneously generate frames and check frames. If frames are looped back at the remote end, the frame checker can be used to check frames generated by the ADIN1110.

When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC. To use the frame generator, the diagnostic clock must also be enabled (CRSM_DIAG_CLK_EN, device address 0x1E, register address 0x882C, bit 0).

The frame generator control registers configure the type of frames to be sent (random data, all 1s, etc.), the frame length, and the number of frames to be generated.

The generation of the requested frames starts by enabling the frame generator (set the FG_EN bit, device address 0x1E, register address 0x8015, bit 0). When the generation of the frames is completed, the frame generator done bit is set (FG_DONE, device address 0x1E, register address 0x801E, bit 0).

The frame checker is enabled using the frame checker enable bit (FC_EN, device address 0x1E, register address 0x8001, bit 0). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY, which is configured using the frame checker transmit select bit (FC_TX_SEL, device address 0x1E, register address 0x8005, bit 0). The frame checker reports the number of frames received, cyclic redundancy check (CRC) errors, and various other frame errors. The frame checker frame counter register and frame checker error counter register count these events.

The frame checker counts the number of CRC errors and these are reported in the receive error counter register (RX_ERR_CNT, device address 0x1E, register address 0x8008). To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched when the receive error counter register is read. Therefore, when using the frame checker, read the receive error counter first, and then read all other frame counters and error counters. A latched copy of the receive frame counter register is available in the FC_FRM_CNT_H register and FC_FRM_CNT_L register (device address 0x1E, register addresses 0x8009 and 0x800A respectively).

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frames errors, and undersized frame errors. In addition to the received frames, the frame checker counts frames with an odd number of nibbles in the frame, and counts packets with an odd number of nibbles in the preamble. The frame checker also counts the number of false carrier events, which is a count of the number of times the bad start of stream delimiter (BAD SSD) state is entered.

Frame Generator and Checker used with Remote Loopback with two MAC-PHYs

Using two MAC-PHY devices, the user can configure a convenient self-contained validation of the PHY core to PHY core connection, or indeed can exercise the full signal chain by utilizing the host processor to perform the loopback at the remote end. Figure 6 shows an overview of how each MAC-PHY is configured. An external cable is connected between both devices, and MAC-PHY 1 is generating frames using the frame generator. When limiting the test to just the PHY core portions of the ADIN1110, MAC-PHY 2 has MAC interface remote loopback enabled (MAC_IF_REM_LB_EN). The frames issued by MAC-PHY 1 are sent through the cable, through the PHY 2 signal chain returned by PHY 2 MAC interface remote loopback, back again through the cable, and checked by the MAC-PHY 1 frame checker. Alternatively, the frames from MAC-PHY 1 can be sent all the way to the remote device's host processor and looped back from there, through the MAC and PHY blocks within MAC-PHY 2 and back to MAC-PHY 1.

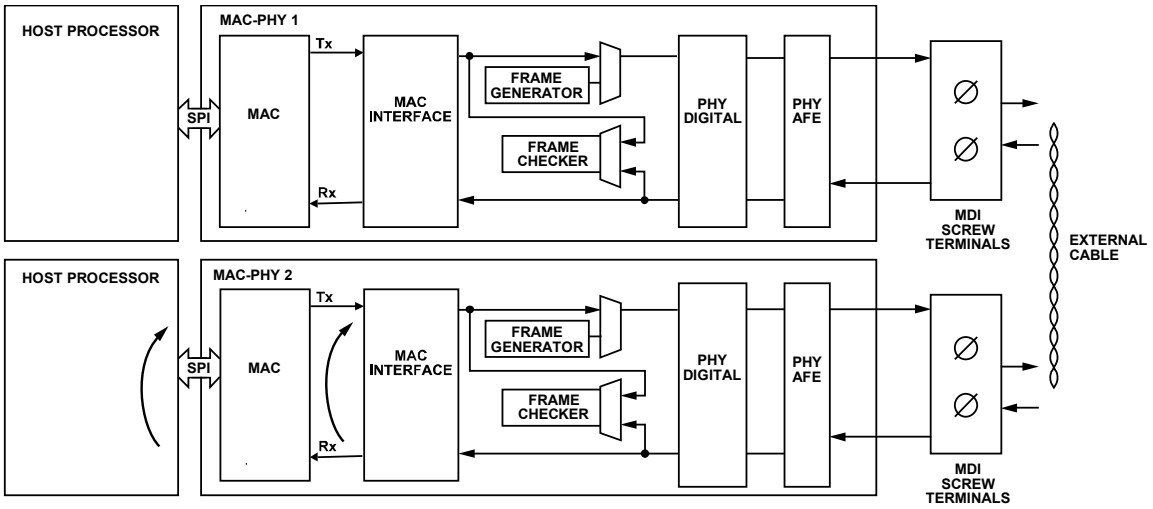


Figure 7. Remote Loopback used across two PHYs for Self-Check Purposes

TEST MODES

The ADIN1100 provides several test modes that allow testing of the transmitter waveform, distortion, jitter and droop. These test modes change only the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.

The ADIN1100 has three different test modes:

1. Test mode 1. This is a transmitter output voltage and timing jitter test mode. When this mode is selected, the ADIN1100 repeatedly transmits the data symbol sequence (+1, –1).
2. Test mode 2. This is a transmitter output droop test mode. In this mode, the ADIN1100 transmits ten "+1" symbols followed by ten "-1" symbols. This sequence is repeated indefinitely.
3. Test mode 3. Normal operation in idle mode test mode. When this test mode is selected, the ADIN1100 transmits as in non-test operation and in the master data mode, with data set to normal inter-frame idle signals.

Accessing the test modes

In order to set the ADIN1100 into the test mode configuration, the device needs to be in software power-down mode (CRSM_SFT_PD, device address 0x1E, register address 0x8812, bit 0). The power-down status of the ADIN1100 can be checked reading the Software Power-down Status bit (CRSM_SFT_PD_RDY, device address 0x1E, register address 0x8818, bit 1).

Once the ADIN2111 is in software power-down mode, the autonegotiation needs to be disabled. This can be done by clearing the Autonegotiation Enable bit (AN_EN, device address 0x07, register address 0x0200, bit 12).

With the autonegotiation disabled, the following step is to force the autonegotiation configuration. This is done by writing to the Autonegotiation Forced Mode bit (AN_FRC_MODE_EN, device address 0x07, register address 0x8000, bit 0).

The desired test mode can now be selected by writing the appropriate value to the 10BASE-T1L Test Mode Control register (B10L_TEST_MODE_CNTRL, device address 0x01, 0x08F8), and exiting the device from power-down by clearing the Software Power-down bit (CRSM_SFT_PD, device address 0x1E, register address 0x8812, bit 0).

APPLICATIONS INFORMATION

SYSTEM LEVEL POWER MANAGEMENT

Transmit Level = 1.0 V pk-pk

For shorter reach applications supporting cable lengths up to 400 m, signal amplitude requirements tend to be lower, the transmit mode of 1.0 V pk-pk can be used.

For applications where it is required that the ADIN1110 operates in a 1.0 V pk-pk transmit operating mode, the TX2P4_ENB pin must be tied high via a 4.7 kΩ resistor (see Figure 7). This configuration forces the ADIN1100 to operate at only 1.0 V pk-pk transmit operating mode and enables the operation of the ADIN1110 from a signal supply voltage, operating at a lower voltage rail (e.g. 1.8 V), allowing the user to minimize power dissipation in the system. When this mode is selected, the CEXT_1 and CEXT_4 capacitors are not required.

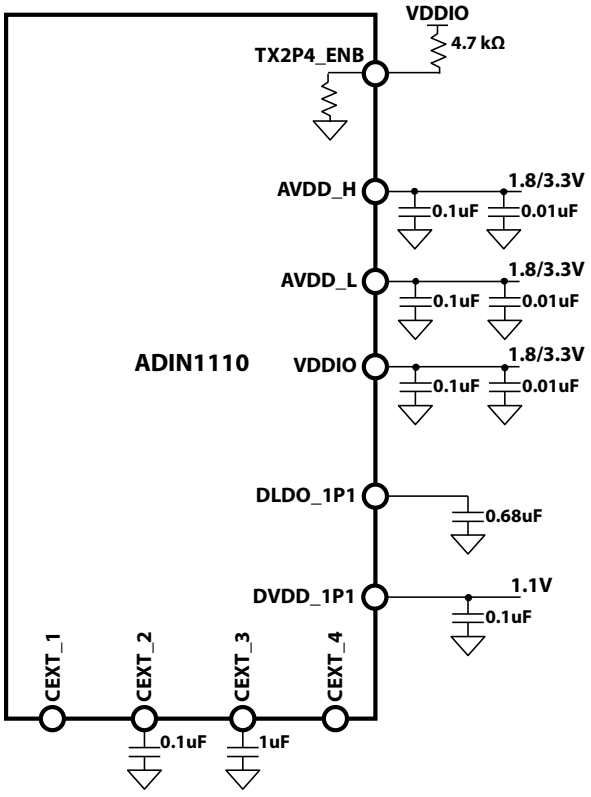


Figure 8. Supplies and capacitors for 1.0V pk-pk transmit mode

Transmit Level = 2.4 V pk-pk

For longer reach applications, a higher signal amplitude of 2.4 V pk-pk is required. The ADIN1110 is designed to operate with long reach cables up to 1000 m in this mode, requiring a higher AVDD_H supply voltage of 3.3 V.

For the ADIN1110 to be able to operate in 2.4 V pk-pk, the TX2P4_ENB pin must be tied low (no external connection required to achieve this due to the presence of an internal pull-down resistor). This mode of operation still allows the 1.0 V pk-pk operating mode to be selected via MDIO or via autonegotiation.

Figure 8 shows an overview of the proposed power configuration. For single supply operation, the same rail can be used to supply the ADIN1110 AVDD_H, AVDD_L and VDDIO supply rails. The DVDD_1P1 1.1 V rail can be derived internally or alternatively provided by an external 1.1 V rail. Note that this configuration requires that AVDD_H is 3.3 V even if the link is established at 1.0 V pk-pk transmit operating mode via MDIO or autonegotiation. The CEXT_1 capacitor can be reduced to 2.2 µF in this configuration as long as it does not go below 2 µF over temperature, voltage, etc.

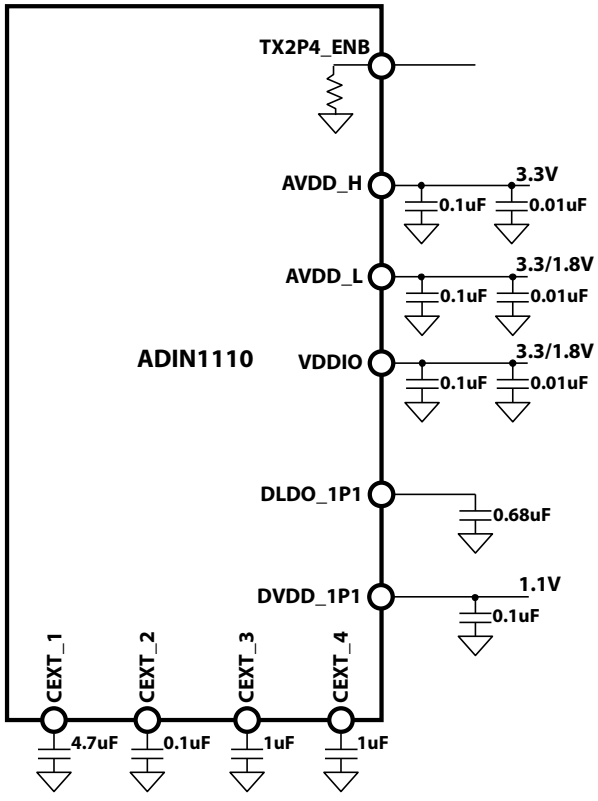


Figure 9. Supplies and capacitors for 2.4/1.0 V pk-pk transmit mode

COMPONENT RECOMMENDATIONS

Crystal

The typical connection for an external crystal (XTAL) is shown in Figure 9. To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1110 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

The crystal specification defines C_L. Assuming the following:

- $C_{PCB1} \approx C_{PCB2} \approx C_{PCB}$
- $C_{X1} \approx C_{X2} \approx C_X$

Then, $C_X = 2 \times C_L - C_{PCB} - 3$ pF

Choose precision capacitors for C_X with low appreciable temperature coefficient to minimize frequency errors. Ensure good ground connections on C_{X1}, C_{X2}, the package ground of the quartz resonator and the ground paddle of the ADIN1110 package.

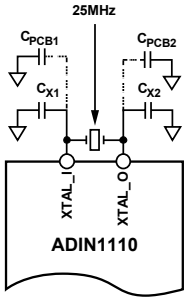


Figure 10. Crystal Oscillator Connection

External Clock Input

If using a single-ended reference clock on XTAL_I/CLK_IN, leave XTAL_O open-circuit. This clock must be an ac-coupled 0.8 V - 2.5 V pk-pk sine or (filtered) square wave signal. This also applies when connecting CLK25_REF output clock from one 10BASE-T1L device to the XTAL_I/CLK_IN input of another 10BASE-T1L device.

If $V_{S\,pk\text{-}pk} < 2.5\ V_{pk\text{-}pk}$

- C_2 is not required
- C_1 = 1nF

If $V_{S\,pk\text{-}pk} \geq 2.5\ V_{pk\text{-}pk}$

- C_2 = 10 pF
- $C_1 = 2.5\ (13\text{pF} + C_{PCB}) / (V_{S\,pk\text{-}pk} - 2.5)$

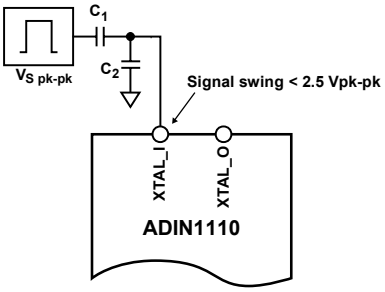


Figure 11. External Clock Connection

802.1AS SUPPORT

Typically, any device operating in an 802.1AS network executes the following operations periodically:

- Generate Peer Delay Request and handle response
- Receive Peer Delay Request and generate response
- Receive Synchronization Frame (Slave Clock)
- Transmit Synchronization Frame (Master Clock)

These features require that the MAC is capable of timestamping specific incoming and outgoing frames.

In order to assist with these features, the ADIN1110 MAC provides the following hardware:

- Internal free-running counter
- Syntonized counter
- Waveform generation on TS_TIMER output

Internal Free-running Counter

The ADIN1110 has an internal free-running counter running at 25 MHz. This counter provides an accuracy of 40 ns and a period of approximately 170 s; this ensures that the clock doesn't wrap during any of the necessary operations, for example, between receipt of peer delay request and transmission of the response.

To enable the free-running counter, the TS_EN (TS_CFG register, SPI address 0xA0) bitfield must be set to 1.

When the free-running counter is enabled, the ADIN1110 captures the timestamp for all received frames and it is appended before each data frame received. The timestamps of transmitted frames are captured when requested. (See Timestamp Capture for more details).

The value of the free-running counter can be captured using the input capture signal (TS_CAPT), capturing the value of the counter in the TS_FREECNT_CAPT_UPR and TS_FREECNT_CAPT_LWR.

Syntonized Counter

The syntonized counter is a 64-bit counter in which the lower 32-bits represent seconds with 1LSB = 1 ns. When the lower 32-bits reach 1 second, they clear and the upper 32-bits increment representing seconds. This counter increments by 80 ns steps and therefore, the 4 LSBs are always 0.

To enable the syntonized counter, the TS_EN (TS_CFG register, SPI address 0xA0) bitfield must be set to 1.

The value of the syntonized counter can be captured using the TS_CAPT signal, capturing the value of the counter in the registers TS_EXT_CAPT0 to TS_EXT_CAPT3.

Waveform Generation on TS_TIMER Output

The ADIN1110 can generate an output signal (TS_TIMER) which uses two counters to generate repeating waveforms driven by the syntonized time. These two counters, TS_TIMER_HI (SPI register addresses 0xA1 and 0xA2) and TS_TIMER_LO (SPI register addresses 0xA3 and 0xA4) specify the high and low period of the TS_TIMER signal, and need to be programmed with multiples of 80, as they are driven by the syntonized time.

As it is frequent that the required period of TS_TIMER cannot be programmed as a multiple of 80, the quantization error correction register (TS_TIMER_QE_CORR, SPI register address 0xA5) can be programmed with a value between 0 and 79 in order to compensate for the TS_TIMER quantization error.

It is possible to specify a time with respect to the 64-bit syntonized timer to start the generation of the TS_TIMER output. With the register TS_TIMER_START (SPI addresses 0xA6 and 0xA7) can be programmed with any value multiple of 80 which is compared with the nanoseconds portion of the syntonized counter to generate a one-shot start.

The sequence to enable the TS_TIMER output is as follows:

1. If required, change the default value of the TS_TIMER output from 0 to 1 writing to the TS_TIMER_DEF bitfield (SPI address 0xA0, bit 2).
2. Write to TS_TIMER_HI and TS_TIMER_LO registers the values required for the high and low times for the TS_TIMER output.
3. Write to the TS_TIMER_QE_CORR register the value required for the quantization error correction.
4. Write a start time to the TS_TIMER_START registers. When the nanoseconds part of the syntonized counter matches this value, TS_TIMER starts toggling.

The TS_TIMER output can be stopped by writing 1 to the TS_TIMER_STOP bitfield (SPI address 0xA0, bit 3). When the TS_TIMER output is stopped, the output goes back to the default value specified in TS_TIMER_DEF.

REGISTER SUMMARY

The ADIN1110 register interface is via a 4-wire SPI interface consisting of the following pins: SCLK, CS_N, SDI and SDO/SPI_CFG0.

The possible access permissions of the registers are:

- R/W: read/write
- R: read only
- W write only
- R/W1C: read/write-1-to-clear

The ADIN1110 also allows to access the PHY registers via an SPI to MDIO master bridge. See SPI Access to the PHY Registers section.

These registers have some additional access permissions:

- R LL: read only, latch low
- R LH: read only, latch high
- R/W SC: read/write, self-clear

SPI PROTOCOL

The SPI protocol is illustrated in Table 14 to Table 17. The protocol used is determined by the 2nd bit received on the SPI interface, called the PROT bit. The register map is organized as a 16-bit map, and all accesses are in multiples of 16-bit words. Both single and burst access in multiples of 16-bit words are supported. The MSB of the data is transmitted first.

- CD: Control/Data transaction. Always 1.
- PROT: Protocol. Always 1.
- RW: Read/Write
  - 0: Read
  - 1: Write
- TA: Turn around.

Burst writes and reads must be in multiples of 2bytes - odd sized frames must have an extra byte appended to the frame on SDI/SDO. However, TX_FSIZE is still written with the original frame size + 2 bytes for the frame header (Figure 11). For example, to transmit a 65-byte frame which is prepended with a 2-byte header, 67 is written to TX_FSIZE but 68 bytes are transferred over SDI – the last byte is not used.

Table 15. Control Write Transaction

	MSB					**LSB**
	D31	**D30**	**D29**	**D[28:16]**	**D[15:8]**	**D[7:0]**
SDI:	CD	PROT	R/W	ADDR[12:0]	DATA[15:8]	DATA[7:0]

Table 16. Control Read Transaction

	MSB						**LSB**
	D23	**D22**	**D21**	**D[20:8]**	**D[7:0]**		
SDI:	CD	PROT	R/W	ADDR[12:0]	TA[7:0]		
						D[15:8]	**D[7:0]**
SDO:						DATA[15:8]	DATA[7:0]

Table 17. Burst Write Transaction (Control or Data)

	MSB									**LSB**
	D63	**D62**	**D61**	**D[60:48]**	**D[47:40]**	**D[39:32]**	**D[31:24]**	**D[23:16]**	**D[15:8]**	**D[7:0]**
SDI:	CD	PROT	R/W	ADDR[12:0]	DATA0[15:8]	DATA0[7:0]	DATA1[15:8]	DATA1[7:0]	DATA2[15:8]	DATA2[7:0]

Table 18. Burst Read Transaction (Control or Data)

	MSB									**LSB**
	D23	**D22**	**D21**	**D[20:8]**	**D[7:0]**					
SDI:	CD	PROT	R/W	ADDR[12:0]	TA[7:0]					
						D[47:40]	**D[39:32]**	**D[31:24]**	**D[23:16]**	**D[15:8]**	**D[7:0]**
SDO:						DATA0 [15:8]	DATA0 [7:0]	DATA1 [15:8]	DATA1 [7:0]	DATA2 [15:8]	DATA2 [7:0]

It is possible to enable a CRC on the SPI protocol via a hardware configuration pin on power up. This 8-bit CRC uses the polynomial $x^8 + x^2 + x + 1$ seeded with 0x0 and provides up to 3-bit error detection. The 8-bit CRC is not used for data transactions – writes to the P1_RX (SPI address 0x07) and TX (SPI address 0x0E) registers – because ethernet frames already have a 32-bit CRC.

The generic SPI protocol is half-duplex, therefore, it is not possible to write frame data into the MAC_TX register and read from the MAC_RX register at the same time. Because of this, the SPI SCLK frequency needs to be 24 MHz to achieve full-duplex transmissions on ethernet at 10 Mb/s.

MAC Frame - Transmit and Receive

The 2-byte frame header seen in Table 18 is appended to all transmitted and received frames. This always precedes the frame data (see Figure 11).

Timestamp Capture

On receive, if TIME_STAMP_PRESET is asserted, an additional 4-byte timestamp is provided after the 2-byte header in Table 18 and before the data frame. This timestamp can then be stored or discarded by software when reading the Rx FIFO.

On transmit, if EGRESS_CAPTURE is different to 2'b00, the ADIN1110 then captures the timestamp of the transmitted frame into the respective TS_EGRESS_* register.

In order to capture timestamps, the free-running counter must be enabled by setting the TS_EN (TS_CFG register, SPI address 0xA0) to 1.

Tx Frame over SPI

The space in the transmit FIFO can be checked by reading the Tx FIFO Space register (TX_SPACE, SPI address 0x0F). Ensure there is sufficient space for the frame. Include 4 bytes of overhead as the device will internally append additional information to the frame memory.

The size of the frame to be transmitted, including the 2-byte MAC frame header in Table 18 has to be written to the MAC TX frame size register (TX_FSIZE, SPI address 0x0D). A frame is then transmitted by appending the 2-byte MAC frame header and writing the frame to the MAC transmit register (TX, SPI address 0x0E) in one or more SPI transactions.

The MAC defaults to operating in store and forward mode, so the frame will be transmitted via the PHY once the full frame has been stored in the Tx FIFO.

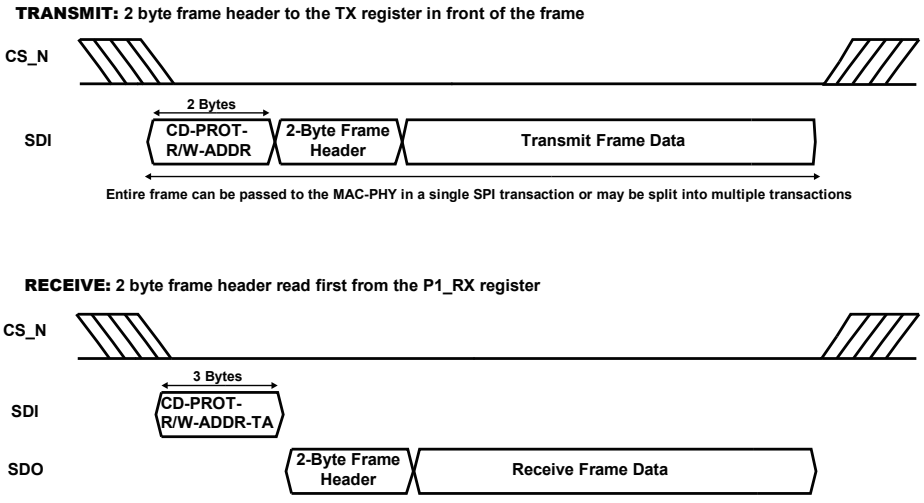


Figure 12. MAC Frame- Transmit & Receive

Table 19. Frame Header

D[15:11]	D10	D9	D8	D[7:6]	D[5:3]	D2	D[1:0]
Reserved	Priority	CRC_APPEND	Reserved	EGRESS_CAPTURE	Reserved	TIME_STAMP_PRESENT	Reserved

- Priority: Indicates which priority queue the frame was received from. Not used on transmit; set 0 in transmitted frames.
- CRC_APPEND: On transmit, append a CRC to the frame. Not used on receive; will always be 0 in received frames.
- EGRESS_CAPTURE: Capture an egress timestamp into the host readable egress time registers:
  - 00 → No action
  - 01 → Capture in the pair of TS_EGRESS_A_LWR and TS_EGRESS_UPR registers. The TSE_CAPTD_A bit field in TSE_STATUS register asserts when captured.
  - 10 → Capture in the pair of TS_EGRESS_B_LWR and TS_EGRESS_UPR registers. The TSE_CAPTD_B bit field in TSE_STATUS register asserts when captured.
  - 11 → Capture in the pair of TS_EGRESS_C_LWR and TS_EGRESS_UPR registers. T The TSE_CAPTD_C bit field in TSE_STATUS register asserts when captured.

- TIME_STAMP_PRESENT: On receive, the first 4 bytes of data contain the timestamp for the frame. Not used on transmit; set to 0 in transmitted frames
- Reserved: Always set to 0

.

Rx Frame over SPI

When a frame is completely received into one of the Rx FIFOs, a corresponding bit field (P1_RX_RDY in the STATUS register, SPI address 0x01) asserts, which, in turn, generates an interrupt if not masked.

The size of the received frame can then be read in the MAC Rx frame size register (P1_RX_FSIZE, SPI address 0x06), once the size of the frame has been read, the frame can be read from the MAC receive register (P1_RX, SPI address 0x07). Note that once the contents of a full frame have been read, no more contents can be read until P1_RX_FSIZE is read again.

If the P1_RX_RDY bit field in the STATUS register is still asserted after the frame has been read, then another frame is waiting to be read. P1_RX_RDY returns to 0 when the receive FIFO is empty.

Frame Filtering on Receive

By default, the device filters all frames received. To receive frames, the Address Filtering Table has to be setup, or the default operation for all received frames can be changed.

The device can be configured to filter up to 16 different MAC addresses based on the Destination MAC address (DA).

To receive frames with a particular DA, that DA has to be programmed to one of the 16 ADDR_FILT* registers. Each register is 16-bit wide, so for example, to program a DA of 0800 005A 646B to ADDR_FILT[0] write:

1. 0x0800 to ADDR_FILT_UPR[0]
2. 0x005A to ADDR_FILT_MID[0]
3. 0x6468 to ADDR_FILT_LWR[0]

To forward frames with this DA to the host, set the TO_HOST bit field within the ADDR_RULE[0] register to 1; and to apply this rule, set the APPLY2PORT1 bit to 1.

Frames that do not match any of the 16 ADDR_FILT* registers are dropped by default. If the P1_FWD_UNK2HOST bit field within the HOST_CFG register is set to 1, then all frames that do not match a DA are forwarded to the host. The filtering algorithm can be seen in Figure 13.

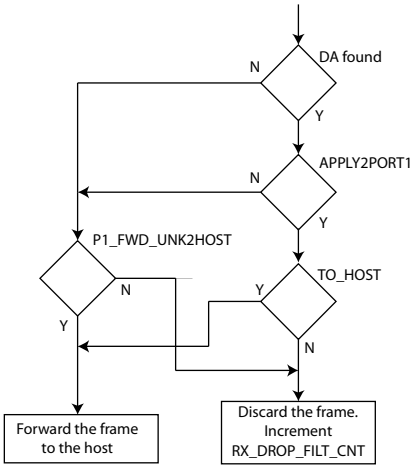


Figure 13. Filtering algorithm.

Frames received with a bad CRC or with RX_ER asserted from the PHY, as well as runt and jabber frames, are dropped and counted.

Rx Priority Queues

There are two different FIFOs on receive, a high priority FIFO and a low priority FIFO.

By default, the low priority FIFO is configured to 12 kbytes, and the high priority FIFO is configured to 8 kbytes.

In the default configuration, frames are always returned from the high priority FIFO first. This configuration can be changed by setting the RX_LOW_PRI_1ST bit field within the HOST_CFG register to 1.

Statistics Counters

There are fourteen 16-bit counters on the receive port that increment on each frame transmit and receive. They roll over to 0 when the max value of 65535 is reached and they are not cleared on reading. Therefore, the counters must be read every 4 seconds to ensure that the counters do not roll over the last value read by the host.

Table 20. Statistics counters

Name	Description
P1_RX_FRM_CNT	Rx frame count
P1_RX_UCAST_CNT	Rx unicast frame count
P1_RX_MCAST_CNT	Rx multicast frame count
P1_RX_BCAST_CNT	Rx broadcast frame count
P1_RX_CRC_ERR_CNT	Rx CRC errored frame count
P1_RX_ALGN_ERR_CNT	Rx alignment error count
P1_RX_PHY_ERR_CNT	Rx PHY error count
P1_RX_LS_ERR_CNT	Rx long/short frame error count
P1_TX_FRM_CNT	Tx frame count
P1_TX_UCAST_CNT	Tx unicast frame count
P1_TX_MCAST_CNT	Tx multicast frame count
P1_TX_BCAST_CNT	Tx broadcast frame count
P1_RX_DROP_FULL_CNT	Rx frames dropped due to FIFO full
P1_RX_DROP_FILT_CNT	Rx frames dropped due to filtering

Rx Drop FIFO Full Counter

Before the first byte of a received frame is written into the appropriate Rx FIFO, the space in the FIFO is checked. If there is not space for at least 256 bytes, the frame is dropped and the P1_RX_DROP_FULL_CNT counter increments. If there is space for at least 256 bytes in the FIFO, the logic commences writing the frame to the Rx FIFO. If the received frame exceeds 256 bytes and the Rx FIFO fills, the frame is then dropped and the P1_RX_DROP_FULL_CNT counter increments.

Frame Rx/Tx Errors

All received errored frames are by default dropped and counted. Received errored frames do not generate interrupts, they are simply dropped and counted, and the software must monitor the statistics counters.

The following errors are reported in the ERR_STATUS register and result in the INT_N pin asserting unless the error is masked using the ERR_STATUS_MASK register.

SRAM ECC error

When writing a frame to the FIFO, the size of the frame is inserted in a 16-bit word at the front of the frame and written to the FIFO. A 5-bit ECC code is placed alongside the size field.

When this location is read from SRAM, the ECC is checked. If a double bit error is detected, the bit fields RX_ECC_ERR or TX_ECC_ERR of the ERR_STATUS register assert. If a double bit error is detected on reading a frame header from the Tx FIFO, the frame is not transmitted.

In response to an ECC error the FIFOs must be cleared using the FIFO_CLR register. All frames in the FIFOs will be lost, transmission will stop, and a bad CRC will be appended to the frame that was being transmitted. The next frame received will be written to a FIFO.

SPI Error

If a CRC error is detected when writing to a register, the SPI_ERR bitfield of the ERR_STATUS register asserts.

If the software cannot determine which transaction caused an SPI error, then the configuration state of the device may be unknown. In this scenario it is recommended to reset the MAC.

Tx FIFO Overflow error

This error occurs if the host attempts to write to the Tx FIFO but there is not enough space. Software should check the space available in the Tx FIFO before attempting to write to it.. See Tx FIFO Space Register (TX_SPACE, SPI address 0x0F).

If this error occurs, the frame is automatically dumped, and the software has no other requirement than to clear the TX_OVF_ERR status bit. Note that frames dropped because of a Tx FIFO overflow are not counted in the statistics counters.

NVM Error

The host software must reset the part if a non-correctable Non-Volatile Memory error is detected. The NVM will be read again on exiting reset; if an NVM error is detected, the MAC-PHY will not complete initialization.

SPI ACCESS TO THE PHY REGISTERS

Table 21. MDIO_CMD

D15	D[14:13]	D12	D[11:10]	D[9:5]	D[4:0]
MRDY	MCMD	MCLAUSE45	MSPEED	PADDR	DADDR

The ADIN1110 allows to access the PHY registers via an SPI to MDIO master bridge. The sequence to write into a PHY register is:

1. Set the PHY address to the required value in the PADDR bit field of the MDIO_CMD register (see Table 20 and the MDIO PHY Address Determination section below).
2. Write the device address to the DADDR bitfield of the MDIO_CMD register.
3. Write the register address to the MDIO_ADDR register.
4. Write the data to the MDIO_WDATA register.
5. Set the MCMD field in the MDIO_CMD register to WRITE. The MCLAUSE45 bit field of the MDIO_CMD register must be set to 1.

6. Poll the MRDY bit in the MDIO_CMD register until it asserts.

To read a PHY register the sequence is as follows:

1. Set the PHY address to the required value in the PADDR bit field of the MDIO_CMD register (see Table 20 and the MDIO PHY Address Determination section below).
2. Write the device address to the DADDR bitfield of the MDIO_CMD register.
3. Write the register address to the MDIO_ADDR register.
4. Set the MCMD bit in the MDIO_CMD register to READ. The MCLAUSE45 bit field of the MDIO_CMD register must be set to 1.
5. Poll the MRDY bit in the MDIO_CMD register until it asserts.
6. Read the data from the MDIO_RDATA register.

The SPI to MDIO bridge only supports an MDC speed of 2.5 MHz.

MDIO PHY Address Determination

Currently the MDIO PHY address used to access the PHY registers (PADDR) is determined by the CS_N pin value latched on power-up or reset. Reading from a PHY register while using an incorrect MDIO PHY address will return a value of 0xFFFF.

Before accessing PHY registers it is important to determine the MDIO PHY address to use. This can be achieved as follows:

1. Read from CRSM_IRQ_STATUS using MDIO PHY address 0.
2. If the value returned is not 0xFFFF, go to step 5.
3. Read from CRSM_IRQ_STATUS using MDIO PHY address 1.
4. If the value returned is not 0xFFFF, go to step 5.
5. Use the new found valid MDIO PHY address for further PHY register accesses.

Note that the MDIO PHY address may change again following a reset of the device, which may not be initiated by the host but triggered by a hardware condition (e.g. brown-out). Depending on application requirements, the above sequence can be performed before a batch of PHY register accesses. Alternatively, the host may choose to use the ADIN1110 interrupt to get notified when a hardware reset occurs by unmasking the following bits - P1_PHY_INT in the STATUS register and CRSM_HRD_RST_IRQ_LH in the CRSM_IRQ_STATUS register using the STATUS_MASK and CRSM_IRQ_MASK registers respectively.

PHY Registers Contents

The PHY registers provide access to control and status information in the management registers.

The registers are made up of four device address groupings (see Table 21) based on the MDIO Manageable Device (MMD). Within each device address space, IEEE standard registers are located in register addresses between 0x0000 and 0x7FFF and vendor specific registers are located in register addresses from 0x8000 to 0xFFFF.

Table 22. Register Groupings

Device Address	MMD Name
0x01	PMA/PMD (Physical Medium Attachment/Physical Medium Dependent)
0x03	PCS (Physical Coding Sublayer)
0x07	Auto-Negotiation
0x1E	Vendor Specific 1

This allows access to up to 32 PHYs consisting of up to 32 MMDs through a single MDIO interface.

The default value of some of the registers are determined by the value of the hardware configuration pins, which are read just after the RESET_N pin is de-asserted. In these cases, the reset value in the register table is listed as pin dependent. This allows the default operation of the ADIN1110 to be configured without having to write to it over the SPI interface. This is useful in unmanaged applications, where the desired operation of the PHY is configured from the hardware configuration pins without any software intervention. For unmanaged applications, do not configure the PHY to enter software power-down after reset to ensure that the PHY immediately attempts to bring up links as configured by the other hardware configuration pins. In managed applications, software is available to configure the PHY via the management interface. In this case, it is possible to use the hardware configuration pins to configure the PHY to enter software power-down mode after reset, such that the PHY can be configured before linking is attempted.

Recommended Register Operation

Many of the PHY registers in the ADIN1110 are defined in the IEEE Standard 802.3 and the exact behavior of these registers follows the standard. This behavior may not always be obvious and is described here including the recommended operation and use of the registers.

Latch Low Registers

The IEEE Standard 802.3-2018 requires certain MDIO accessible registers to exhibit latch low behavior. The idea is to allow software that only intermittently reads these registers to detect conditions that may be transitory or short lived. For example, the AN_LINK_STATUS bit, is required to latch low. When the device exits from a reset or powerdown state, the latching condition is not active and the value of the AN_LINK_STATUS bit reflects the current status of the link. However, if the link comes up and subsequently drops, then the latching condition becomes active. In this case the AN_LINK_STATUS bit reads as 1'b0 even if the link has come back up again in the interim. The latching condition is only cleared once the AN_LINK_STATUS bit is read. This ensures

that software has had the opportunity to observe that the link dropped.

One implication of the latch low behavior described above is that, if software wishes to determine the current status of the link, it must perform two reads of the AN_LINK_STATUS bit back-to-back. The first read is needed to clear any active latching condition.

Another implication is that it is important that software take account of the interaction between MDIO accessible bits that share a register address. For example, the AN_PAGE_RX and AN_LINK_STATUS bits reside at the same register address. As a result, reading the AN_PAGE_RX bit will clear any active latching condition associated with the AN_LINK_STATUS bit.

IEEE Duplicated Registers

The IEEE Standard 802.3-2018 covers a very wide range of standards and speeds from 10 Mb/s to 40 Gb/s and higher and includes a very large number of clauses. There are registers associated with many clauses and different PHYs may include different clauses and combinations of clauses. Hence, registers for common functions like software reset, software powerdown, loopback, etc. tend to be implemented in multiple clauses.

In the ADIN1110, the physical implementation of these registers is in a single location, but they may be accessed at multiple addresses. For example, the Software Reset bit, can be read or written in all the following IEEE MMD locations and vendor specific register locations:

- PMA_SFT_RST (device address 0x01, register address 0x0000, bit 15)
- B10L_PMA_SFT_RST (device address 0x01, register address 0x08F6, bit 15)
- PCS_SFT_RST (device address 0x3, register address 0x0000, bit 15)
- B10L_PCS_SFT_RST (device address 0x03, register address 0x08E6, bit 15)
- CRSM_SFT_RST (device address 0x1E, register address 0x8810, bit 15)

Note, in this example these are the PMA/PMD, PCS, Auto-Negotiation and Vendor Specific MMD 1 device address locations (per Table 21).

Having multiple address locations for the same register makes the use of the part more complex than necessary, in particular in relation to registers that have latch low or self-clear access permissions. Unfortunately, this is an unavoidable consequence of the IEEE standard.

The ADIN1110 datasheet only calls out a single recommended address location for each of these IEEE registers. This is done to simplify the operation and use of the part. In general, the registers introduced in the 802.3cg (10BASE-T1L) section of the standard are recommended over older (equivalent) registers. Often registers in a vendor specific address are recommended, in particular where a register brings a number of useful IEEE register bits into a single register address. The ADIN1110 will correctly respond to register accesses to all the IEEE register address locations covered by the 10BASE-T1L standard once the start-up is complete after power on reset, hardware reset or software reset.

Read Modify Write Operation

It is strongly recommended that all register write operations should be performed as read modify write operations. If this is not followed, it is possible that the value of register bits are inadvertently changed.

SPI REGISTER DETAILS

Table 23. SPI Register Summary

Address	Name	Description	Reset	Access
0x00	SPI_PC	SPI Protocol Control Register.	0x0106	R/W
0x01	STATUS	MAC Status Register.	0x0000	R/W
0x02	STATUS_MASK	Mask Bits for Driving the Interrupt Pin Register.	0x0020	R/W
0x03	TSE_STATUS	Egress Timestamp Status Register.	0x0000	R/W
0x04	ERR_STATUS	Error Status Register.	0x0000	R/W
0x05	ERR_STATUS_MASK	Error Status Mask Register.	0x0000	R/W
0x06	P1_RX_FSIZE	P1 MAC Rx Frame Size Register.	0x0000	R
0x07	P1_RX	P1 MAC Receive Register.	0x0000	R
0x0C	RX_THRESH	MAC Rx Threshold Register.	0x0010	R/W
0x0D	TX_FSIZE	MAC Tx Frame Size Register.	0x0000	R/W
0x0E	TX	MAC Transmit Register.	0x0000	W
0x0F	TX_SPACE	Tx FIFO Space Register.	0x0FFF	R
0x10	TX_THRESH	Transmit Threshold Register.	0x0004	R/W
0x11	HOST_CFG	MAC Configuration Register.	0x0000	R/W
0x13	FIFO_CLR	MAC FIFO Clear Register.	0x0000	W
0x14	SOFT_RST	Software Reset Register.	0x0000	W
0x15	MDIO_CMD	MDIO Command and Address Register.	0x8000	R/W
0x16	MDIO_ADDR	MDIO Clause 45 Address Register.	0x0000	R/W
0x17	MDIO_WDATA	MDIO Write Data Register.	0x0000	R/W
0x18	MDIO_RDATA	MDIO Read Data Register.	0x0000	R
0x1A	FIFO_SIZE	FIFO Sizes Register.	0x0075	R/W
0x40 to 0x7C by 4	ADDR_FILT_UPRn	MAC Address DA Filter Upper 16 Bits Registers.	0x0000	R/W
0x41 to 0x7D by 4	ADDR_FILT_MIDn	MAC Address DA Filter Middle 16 Bits Registers.	0x0000	R/W
0x42 to 0x7E by 4	ADDR_FILT_LWRn	MAC Address DA Filter Lower 16 Bits Registers.	0x0000	R/W
0x43 to 0x7F by 4	ADDR_RULEn	MAC DA Filter Table Rule Registers.	0x0000	R/W
0x80	P1_RX_FRM_CNT	P1 Rx Frame Count Register.	0x0000	R
0x81	P1_RX_BCAST_CNT	P1 Rx Broadcast Frame Count Register.	0x0000	R
0x82	P1_RX_MCAST_CNT	P1 Rx Multicast Frame Count Register.	0x0000	R
0x83	P1_RX_UCAST_CNT	P1 Rx Unicast Frame Count Register.	0x0000	R
0x84	P1_RX_CRC_ERR_CNT	P1 Rx CRC Errored Frame Count Register.	0x0000	R
0x85	P1_RX_ALGN_ERR_CNT	P1 Rx Align Error Count Register.	0x0000	R
0x86	P1_RX_LS_ERR_CNT	P1 Rx Long/Short Frame Error Count Register.	0x0000	R
0x87	P1_RX_PHY_ERR_CNT	P1 Rx PHY Error Count Register.	0x0000	R
0x88	P1_TX_FRM_CNT	P1 Tx Frame Count Register.	0x0000	R
0x89	P1_TX_BCAST_CNT	P1 Tx Broadcast Frame Count Register.	0x0000	R
0x8A	P1_TX_MCAST_CNT	P1 Tx Multicast Frame Count Register.	0x0000	R
0x8B	P1_TX_UCAST_CNT	P1 Tx Unicast Frame Count Register.	0x0000	R
0x8C	P1_RX_DROP_FULL_CNT	P1 Rx Frames Dropped Due to FIFO Full Register.	0x0000	R
0x8D	P1_RX_DROP_FILT_CNT	P1 Rx Frames Dropped Due to Filtering Register.	0x0000	R
0x90	P1_TX_IFG	P1 Transmit Inter Frame Gap Register.	0x000B	R/W
0x95	P1_RX_IFG	P1 Receive Inter Frame Gap Register.	0x000A	R/W
0x96	P1_RX_MAX_LEN	P1 Max Receive Frame Length Register.	0x0618	R/W
0x97	P1_RX_MIN_LEN	P1 Min Receive Frame Length Register.	0x0040	R/W
0x98	TS_ADDEND_LWR	Timestamp Accumulator Addend Register.	0x0000	R/W
0x99	TS_ADDEND_UPR	Timestamp Accumulator Addend Register.	0x8000	R/W
0x9A	TS_1SEC_CMP_LWR	Timer Update Compare Register.	0xCA00	R/W

Address	Name	Description	Reset	Access
0x9B	TS_1SEC_CMP_UPR	Timer Update Compare Register.	0x3B9A	R/W
0x9C	TS_SEC_CNT_LWR	Seconds Counter Lower Register.	0x0000	R/W
0x9D	TS_SEC_CNT_UPR	Seconds Counter Upper Register.	0x0000	R/W
0x9E	TS_NS_CNT_LWR	Nanoseconds Counter Register.	0x0000	R/W
0x9F	TS_NS_CNT_UPR	Nanoseconds Counter Register.	0x0000	R/W
0xA0	TS_CFG	Timer Configuration Register.	0x0000	R/W
0xA1	TS_TIMER_HI_LWR	High Period for TS_TIMER Register.	0x0000	R/W
0xA2	TS_TIMER_HI_UPR	High Period for TS_TIMER Register.	0x0000	R/W
0xA3	TS_TIMER_LO_LWR	Low Period for TS_TIMER Register.	0x0000	R/W
0xA4	TS_TIMER_LO_UPR	Low Period for TS_TIMER Register.	0x0000	R/W
0xA5	TS_TIMER_QE_CORR	Quantization Error Correction Register.	0x0000	R/W
0xA6	TS_TIMER_START_LWR	TS_TIMER Counter Start Time Lower Register.	0x0000	R/W
0xA7	TS_TIMER_START_UPR	TS_TIMER Counter Start Time Upper Register.	0x0000	R/W
0xA8	TS_EXT_CAPT0	TS_CAPT Pin Timestamp Register 0.	0x0000	R
0xA9	TS_EXT_CAPT1	TS_CAPT Pin Timestamp Register 1.	0x0000	R
0xAA	TS_EXT_CAPT2	TS_CAPT Pin Timestamp Register 2.	0x0000	R
0xAB	TS_EXT_CAPT3	TS_CAPT Pin Timestamp Register 3.	0x0000	R
0xAC	TS_FREECNT_CAPT_LWR	TS_CAPT Free Running Counter Register Lower.	0x0000	R
0xAD	TS_FREECNT_CAPT_UPR	TS_CAPT Free Running Counter Upper Register.	0x0000	R
0xAE	TS_EGRESS_A_LWR	Captured Egress Timestamp A Lower Register.	0x0000	R
0xAF	TS_EGRESS_A_UPR	Captured Egress Timestamp A Upper Register.	0x0000	R
0xB0	TS_EGRESS_B_LWR	Captured Egress Timestamp B Lower Register.	0x0000	R
0xB1	TS_EGRESS_B_UPR	Captured Egress Timestamp B Upper Register.	0x0000	R
0xB2	TS_EGRESS_C_LWR	Captured Egress Timestamp C Lower Register.	0x0000	R
0xB3	TS_EGRESS_C_UPR	Captured Egress Timestamp C Upper Register.	0x0000	R
0xB4	P1_LO_RFC	P1 Rx Low Priority FIFO Frame Count Register.	0x0000	R
0xB5	P1_HI_RFC	P1 Rx High Priority FIFO Frame Count Register.	0x0000	R
0xB6	TFC	Tx FIFO Frame Count Register.	0x0000	R
0xB7	TXSIZE	Tx FIFO Valid Half Words Register.	0x0000	R
0xB8	P1_LO_RXSIZE	P1 Low Priority Rx FIFO Valid Half Words Register.	0x0000	R
0xB9	P1_HI_RXSIZE	P1 High Priority Rx FIFO Valid Half Words Register.	0x0000	R
0xDC to 0xDF by 1	SCRATCHn	Scratch Registers.	0x0000	R/W

SPI Protocol Control Register

Address: 0x00, Reset: 0x0106, Name: SPI_PC

Table 24. Bit Descriptions for SPI_PC

Bits	Bit Name	Description	Reset	Access
[15:8]	VER	SPI Version Field. Protocol Version Information.	0x1	R
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	CPS	Chunk Payload Selector (N). Chunk Payload Size is 2^N. N = 3 minimum & 6 maximum. Default is 64 bytes. This field should be set on device configuration before frame transmission from the host starts and before enabling receiving frames into the Rx FIFOs. This field cannot be modified while transmitting a frame from the host or while sending a received frame to the host. This bitfield is only relevant for the Open-Alliance SPI protocol. 011: Chunk size is 8 byte. 100: Chunk size is 16 byte. 101: Chunk size is 32 byte. 110: Chunk size is 64 byte.	0x6	R/W

MAC Status Register

Address: 0x01, Reset: 0x0000, Name: STATUS

Table 25. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	P1_PHY_INT	PHY Interrupt for Port 1. Host software must read the MDIO Interrupt Status registers (PHY_SUBSYS_IRQ_STATUS or CRSM_IRQ_STATUS) to determine the source of the interrupt.	0x0	R
6	OP_ERR	Operation Error Detected. See the ERR_STATUS Register.	0x0	R
5	RESERVED	Reserved.	0x0	R/W1C
4	TSE_CAPTD	Timestamp Captured. See the TSE_STATUS register for further details.	0x0	R
3	TX_RDY	Tx Ready. If TX_RDY_ON_EMPTY is 0 then TX_RDY asserts when frame transmission completes. If TX_RDY_ON_EMPTY is 1 then TX_RDY asserts when the Tx FIFO is empty and frame transmission completes. This bit is cleared by writing 1 to this field.	0x0	R/W1C
2	P1_RX_RDY	Port 1 Rx FIFO Contains Data. In store and forward this field indicates that there are 1 or more frames in Port 1 Rx FIFO. In cut-through this field indicates that the receive threshold (RX_THRESH) has been reached or the EOF byte of a frame has been received. If there are frames in both the Rx high and low priority FIFOs, then the frame from the high priority FIFO will be read first by default. This default operation can be changed using the field HOST_CFG.RX_LOW_PRI_1ST.	0x0	R
1	LINK_CHANGE	Link Status Changed. Indicates that the link status has changed.	0x0	R/W1C
0	P1_LINK_STATUS	Port 1 Link Status. This bit does not generate an interrupt event. 0: Link Down. 1: Link up.	0x0	R

Mask Bits for Driving the Interrupt Pin Register

Address: 0x02, Reset: 0x0020, Name: STATUS_MASK

Table 26. Bit Descriptions for STATUS_MASK

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	P1_PHY_INT_MASK	Mask Bit for P1_PHY_INT.	0x0	R/W
[6:5]	RESERVED	Reserved.	0x1	R
4	TSE_CAPTD_MASK	Mask Bit for TSE_CAPTD.	0x0	R/W
3	TX_RDY_MASK	Mask Bit for TX_RDY.	0x0	R/W
2	P1_RX_RDY_MASK	Mask Bit for P1_RX_RDY.	0x0	R/W
1	LINK_CHANGE_MASK	Mask Bit for LINK_CHANGE.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Egress Timestamp Status Register

Address: 0x03, Reset: 0x0000, Name: TSE_STATUS

Table 27. Bit Descriptions for TSE_STATUS

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
2	TSE_CAPTD_C	Timestamp Captured on Egress C.	0x0	R/W1C
1	TSE_CAPTD_B	Timestamp Captured on Egress B.	0x0	R/W1C
0	TSE_CAPTD_A	Timestamp Captured on Egress A.	0x0	R/W1C

Error Status Register

Address: 0x04, Reset: 0x0000, Name: ERR_STATUS

Table 28. Bit Descriptions for ERR_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W1C
14	RD_ACC_ERR	Read Access Error. Memory read access error. May assert if the SPI frequency is higher than the specified value for the SPI protocol.	0x0	R/W1C
[13:6]	RESERVED	Reserved.	0x0	R
5	P1_RX_IFG_ERR	Port 1 Rx MAC Inter Frame Gap Error. If the IFG is too short, then the frame will be dropped on receive. It is not counted. The threshold used for measuring the IFG on receive can be set in the P1_RX_IFG register.	0x0	R/W1C
4	TX_UNR_ERR	Host Tx FIFO Underrun Error. This error can only assert when cut-through from the host is enabled. The host software should ensure this bit never asserts by writing frame data to the MAC at a rate greater than 10Mbps. If an underrun error occurs transmit of the current packet will stop. The host Tx FIFO must then be cleared using FIFO_CLR.TXF_CLR.	0x0	R/W1C
3	TX_OVF_ERR	Host Tx FIFO Overflow. The host software should ensure this bit will never assert by checking the space available in the Tx FIFO before writing to the Tx FIFO. If using the Open-Alliance SPI Data protocol, then the space in the Tx FIFO is indicated in the TXC field in the Rx footer. If using the generic SPI protocol, then the TX_SPACE register indicates the remaining space in the Tx FIFO. If the Host Tx FIFO overflows, then the frame being written is dumped and software must resend the entire frame. Writes to the FIFO will commence at the next SOF. There is always room for more than one frame in the Tx FIFO as it is 4k bytes (or greater) in size therefore a frame being transmitted will not be interrupted by an overflow on the write side of the FIFO.	0x0	R/W1C
2	SPI_ERR	Detected an Error on an SPI Transaction. When using the generic SPI Protocol, this field indicates that a CRC error was detected. When using the Open-Alliance SPI Data or Control Protocol it indicates that a parity error was detected on a Tx Header or a data mismatch on a control frame write.	0x0	R/W1C
1	TX_ECC_ERR	ECC Error on Reading the Frame Size from a Tx FIFO. If an uncorrectable ECC error is detected on a read of the size field from the Tx FIFO, then in response to this the Tx FIFOs must be cleared by the host. Frame transmission will stop until the Tx FIFOs are cleared.	0x0	R/W1C
0	RX_ECC_ERR	ECC Error on Reading the Frame Size from an Rx FIFO. If an ECC error is detected on a reading the frame size field from an Rx FIFO, then in response to this all the Rx FIFOs must be cleared/reset by the host software. The frame associated with the ECC error and subsequent frames will not be forwarded to the host.	0x0	R/W1C

Error Status Mask Register

Address: 0x05, Reset: 0x0000, Name: ERR_STATUS_MASK

Table 29. Bit Descriptions for ERR_STATUS_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	RD_ACC_ERR_MASK	Mask Bit for RD_ACC_ERR.	0x0	R/W
[13:6]	RESERVED	Reserved.	0x0	R
5	P1_RX_IFG_ERR_MASK	Mask Bit for P1_RX_IFG_ERR.	0x0	R/W
4	TX_UNR_ERR_MASK	Mask Bit for TXF_UNR_ERR.	0x0	R/W
3	TX_OVF_ERR_MASK	Mask Bit for TXF_OVF_ERR.	0x0	R/W
2	SPI_ERR_MASK	Mask Bit for SPI_ERR.	0x0	R/W
1	TX_ECC_ERR_MASK	Mask Bit for TX_ECC_ERR.	0x0	R/W
0	RX_ECC_ERR_MASK	Mask Bit for RX_ECC_ERR.	0x0	R/W

P1 MAC Rx Frame Size Register

Address: 0x06, Reset: 0x0000, Name: P1_RX_FSIZE

Table 30. Bit Descriptions for P1_RX_FSIZE

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
[10:0]	P1_RX_FRM_SIZE	Receive Frame Size. The size of the frame at the head of the Rx FIFO in bytes. The size includes the appended header. This register is only relevant for the generic SPI protocol. This register must be read before reading a frame from a receive FIFO via P1_RX.	0x0	R

P1 MAC Receive Register

Address: 0x07, Reset: 0x0000, Name: P1_RX

The receive FIFO is read via this register.

It is possible to burst read data from the Rx FIFO over SPI.

Table 31. Bit Descriptions for P1_RX

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RDR	Receive Data Register. Reading this register returns the two bytes at the top of the receive FIFO and pops the two bytes from the FIFO. The upper 8 bits contain the 1st byte, the lower 8 bits contain the 2nd byte. If the frame contains an uneven number of bytes then the last byte will be in RDR[15:8]. This register is only relevant when using the generic SPI protocol and when all of the data from a frame is read out, no further data is returned from the P1 Rx FIFOs until the P1_RX_FRM_SIZE register is read first.	0x0	R

MAC Rx Threshold Register

Address: 0x0C, Reset: 0x0010, Name: RX_THRESH

When cut-through on receive is enable this bit determines the threshold in words at which P*_RX_RDY asserts.

Table 32. Bit Descriptions for RX_THRESH

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
[6:0]	RX_THRESH	Receive Threshold in Cut-through. When cut-through on Rx is enabled (RX_CUT_THRU_EN=1), this field is used to set a receive threshold in half words (16 bit). When this threshold is reached P*_RX_RDY asserts. This field is not used when store and forward is enabled. This field must be set to greater than or equal to the chunk size (see CPS). i.e. RX_THRESH >= (2^{CPS})/2. The maximum value for this field is 32 half words The minimum value for this field is 4 half words - corresponding to a chunk size of 8 bytes. This register is only relevant when using the Open-Alliance SPI protocol.	0x10	R/W

MAC Tx Frame Size Register

Address: 0x0D, Reset: 0x0000, Name: TX_FSIZE

Table 33. Bit Descriptions for TX_FSIZE

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
[10:0]	TX_FRM_SIZE	Transmit Frame Size. This field indicates the size of the frame that will be written to the transmit FIFO in bytes when using the generic SPI protocol. The size should include the 2-byte frame header. This is used on the SPI side of the Tx FIFO to determine when the full frame has been written. When the full frame byte count is reached subsequent writes to the TX register will be ignored until TX_FSIZE is written again. This field is only relevant when using the generic SPI protocol.	0x0	R/W

MAC Transmit Register

Address: 0x0E, Reset: 0x0000, Name: TX

The transmit FIFO is written via this register.

Table 34. Bit Descriptions for TX

Bits	Bit Name	Description	Reset	Access
[15:0]	TDR	Transmit Data Register. Writing to this register adds 2 bytes to the Tx FIFO. Note that the last word of a frame may only contain 1 byte of data (in the upper 8 bits). The hardware will use TX_FSIZE to determine if there is one or two bytes valid in the last SPI write of a frame. This register is only relevant when using the generic SPI protocol.	0x0	W

Tx FIFO Space Register

Address: 0x0F, Reset: 0x0FFF, Name: TX_SPACE

Table 35. Bit Descriptions for TX_SPACE

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
[13:0]	TX_SPACE	Transmit FIFO Space Available in Half Words (16 Bits). This is used by the host software to determine if there is space in the Tx FIFO for a frame. Note that the software can queue 2 frames for transmission and simply wait for a TX_RDY interrupt or it can fill the Tx FIFO with multiple frames and use TX_SPACE to determine if there is space for the next frame.	0xFFF	R

Transmit Threshold Register

Address: 0x10, Reset: 0x0004, Name: TX_THRESH

Table 36. Bit Descriptions for TX_THRESH

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	TX_THRESH	Transmit Start Threshold in Cut-through. When cut-through on Tx is enabled (TX_CUT_THRU_EN=1), this field is used to set the threshold in half words (16 bits) at which frame transmission will start. The range of valid values for this field is 1 to 26 half words. This register is only relevant when using the Open-Alliance SPI protocol.	0x4	R/W

MAC Configuration Register

Address: 0x11, Reset: 0x0000, Name: HOST_CFG

Table 37. Bit Descriptions for HOST_CFG

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	P1_FWD_UNK2HOST	Forward Frames Not Matching Any MAC Address to the Host. Determines the default rule for forwarding unknown frames. Frames with an unknown destination address are placed in the low priority FIFO.	0x0	R/W
4	RESERVED	Reserved.	0x0	R/W
3	TX_RDY_ON_EMPTY	Assert TX_RDY When the Tx FIFO is Empty. By default, TX_RDY asserts when a frame has been transmitted. If this bit is set, then TX_RDY will assert when the Tx FIFO is empty.	0x0	R/W
2	RX_LOW_PRI_1ST	Receive Low Priority Frames First. This bit can be used to select between the High and Low Priority queues on the Rx FIFO when there are frames in both FIFOs. If this bit is 0 then frames from the high priority FIFO are returned first. If this bit is 1 the then frames from the low priority queue are returned first.	0x0	R/W
1	HTX_CUT_THRU_EN	Enable Cut-through on Host Transmit. When cut-through on Tx is enabled the host must ensure that data is provided to the device at a rate of > 10 Mbps to ensure frame transmission does not under-run. Cut-through must be enabled on device configuration before receiving of frames is enabled. i.e. Enable cut-through before setting P*_FWD_UNK2HOST or P*_FWD_UNK2P* or writing to the ADDR_FILT_* registers. This bitfield is only relevant when using the Open-Alliance SPI protocol.	0x0	R/W
0	HRX_CUT_THRU_EN	Enable Cut-through on Host Receive. Cut-through must be enabled on device configuration before receiving of frames is enabled. i.e. Enable cut-through before setting P*_FWD_UNK2HOST or P*_FWD_UNK2P* or writing to the ADDR_FILT_* registers. This bitfield is only relevant when using the Open-Alliance SPI protocol.	0x0	R/W

MAC FIFO Clear Register

Address: 0x13, Reset: 0x0000, Name: FIFO_CLR

Table 38. Bit Descriptions for FIFO_CLR

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	MAC_TXF_CLR	Clear the Host Transmit FIFO. If a frame is currently being transmitted, then transmission will stop and a bad CRC will be appended to the frame. Use this field if TX_UNR_ERR asserts to clear the Host transmit FIFO. Use this field when an uncorrectable ECC error is detected on a read from a Tx FIFO.	0x0	W
0	MAC_RXF_CLR	Clear the Receive FIFOs. Writes to the Rx FIFO will resume at the start of the next frame. Use when an uncorrectable ECC error is detected on a read from an Rx FIFO.	0x0	W

Software Reset Register

Address: 0x14, Reset: 0x0000, Name: SOFT_RST

Table 39. Bit Descriptions for SOFT_RST

Bits	Bit Name	Description	Reset	Access
[15:0]	RST_KEY	Software Reset. Write a pair of keys in order and back to back on the SPI to trigger a reset. 0x4F1C: Key1 to Reset the MAC Logic Only. 0xC1F4: Key 2 to Reset the MAC Logic Only. 0x503D: Key 1 to Reset the MAC and PHY. 0xD305: Key 2 to Reset the MAC and PHY.	0x0	W

MDIO Command and Address Register

Address: 0x15, Reset: 0x8000, Name: MDIO_CMD

MDIO_CMD, MDIO_ADDR, MDIO_WDDATA and MDIO_RDATA provide a method to indirectly access the registers on the MDIO interface. Writing to this register will trigger an MDIO command. MDIO_ADDR and MDIO_WDATA (for writes) should be written before this register is written.

Table 40. Bit Descriptions for MDIO_CMD

Bits	Bit Name	Description	Reset	Access
15	MRDY	MDIO Ready. Poll this bit to determine when the MDIO command has completed. Writing to the MDIO_CMD register while MRDY is 0 will not trigger the start of another MDIO transaction.	0x1	R
[14:13]	MCMD	MDIO Command. 00: Write Command. 01: Read Command. 10: Incremental Read Command. 11: Not Valid.	0x0	R/W
12	MCLAUSE45	Enable Clause 45 Operation. This field must be set to 1 as Clause 45 must be used to access the PHY registers.	0x0	R/W
[11:10]	MSPEED	MDC Clock Speed. 00: 2.5 MHz.	0x0	R/W
[9:5]	PADDR	MDIO PHY Address.	0x0	R/W
[4:0]	DADDR	MDIO Device Address. This is the MDIO Clause 45 Device Address	0x0	R/W

MDIO Clause 45 Address Register

Address: 0x16, Reset: 0x0000, Name: MDIO_ADDR

Table 41. Bit Descriptions for MDIO_ADDR

Bits	Bit Name	Description	Reset	Access
[15:0]	MADDR	MDIO Register Address.	0x0	R/W

MDIO Write Data Register

Address: 0x17, Reset: 0x0000, Name: MDIO_WDATA

Table 42. Bit Descriptions for MDIO_WDATA

Bits	Bit Name	Description	Reset	Access
[15:0]	MWDATA	MDIO Write Data.	0x0	R/W

MDIO Read Data Register

Address: 0x18, Reset: 0x0000, Name: MDIO_RDATA

Table 43. Bit Descriptions for MDIO_RDATA

Bits	Bit Name	Description	Reset	Access
[15:0]	MRDATA	MDIO Read Data.	0x0	R

FIFO Sizes Register

Address: 0x1A, Reset: 0x0075, Name: FIFO_SIZE

Before modifying the FIFO sizes, frame reception and transmission must be stopped, and the FIFOs must be empty.

Configure ADDR_RULE to drop all frames and set P1_UNK2HOST to 0 to ensure all received frames are dropped.

Use RXF_CLR & TXF_CLR to reset the FIFOs. Then the FIFO sizes can be modified.

The total FIFO size must less than or equal to 28k bytes.

Table 44. Bit Descriptions for FIFO_SIZE

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R/W
[7:5]	P1_RX_HI_SIZE	Port 1 Rx High Priority FIFO Size. 000: 0K Bytes. 001: 4k Bytes. 010: 6k Bytes. 011: 8k Bytes. 100: 10k Bytes. 101: 12k Bytes. 110: 14k Bytes. 111: 16k Bytes.	0x3	R/W
[4:2]	P1_RX_LO_SIZE	Port 1 Rx Low Priority FIFO Size. 000: 0K Bytes. 001: 4k Bytes. 010: 6k Bytes. 011: 8k Bytes. 100: 10k Bytes. 101: 12k Bytes. 110: 14k Bytes. 111: 16k Bytes.	0x5	R/W
[1:0]	HTX_SIZE	Host Transmit FIFO Size. 00: 4k Bytes. 01: 8k Bytes. 10: 12k Bytes. 11: 16k Bytes.	0x1	R/W

MAC Address DA Filter Upper 16 Bits Registers

Address: 0x40 to 0x7C (Increments of 4), Reset: 0x0000, Name: ADDR_FILT_UPRn

The Upper 16 Bits of a MAC Address in the DA Filter Table.

When writing the ADDR* registers all 4 register locations must be written in order for a given table entry. They should be written in order with the ADDR_RULE register always written last.

For example, to write table entry 0 the registers should be written in this order:

1: ADDR_FILT_UPR[0]

2: ADDR_FILT_MID[0]

3: ADDR_FILT_LWR[0]

4: ADDR_RULE[0]

Table 45. Bit Descriptions for ADDR_FILT_UPRn

Bits	Bit Name	Description	Reset	Access
[15:0]	MAC_ADDR[47:32]	MAC Address.	0x0	R/W

MAC Address DA Filter Middle 16 Bits Registers

Address: 0x41 to 0x7D (Increments of 4), Reset: 0x0000, Name: ADDR_FILT_MIDn

The Middle 16 Bits of a MAC Address in the DA Filter Table.

When writing the ADDR* registers all 4 register locations must be written in order for a given table entry. They should be written in order with the ADDR_RULE register always written last.

For example, to write table entry 0 the registers should be written in this order:

1: ADDR_FILT_UPR[0]

2: ADDR_FILT_MID[0]

3: ADDR_FILT_LWR[0]

4: ADDR_RULE[0]

Table 46. Bit Descriptions for ADDR_FILT_MIDn

Bits	Bit Name	Description	Reset	Access
[15:0]	MAC_ADDR[31:16]	MAC Address.	0x0	R/W

MAC Address DA Filter Lower 16 Bits Registers

Address: 0x42 to 0x7E (Increments of 4), Reset: 0x0000, Name: ADDR_FILT_LWRn

The Lower 16 Bits of a MAC Address in the DA Filter Table.

When writing the ADDR* registers all 4 register locations must be written in order for a given table entry. They should be written in order with the ADDR_RULE register always written last.

For example, to write table entry 0 the registers should be written in this order:

1: ADDR_FILT_UPR[0]

2: ADDR_FILT_MID[0]

3: ADDR_FILT_LWR[0]

4: ADDR_RULE[0]

Table 47. Bit Descriptions for ADDR_FILT_LWRn

Bits	Bit Name	Description	Reset	Access
[15:0]	MAC_ADDR[15:0]	MAC Address.	0x0	R/W

MAC DA Filter Table Rule Registers

Address: 0x43 to 0x7F (Increments of 4), Reset: 0x0000, Name: ADDR_RULEn

The Rule for the Programmed MAC DA in the Filter Table.

When writing the ADDR* registers all 4 register locations must be written in order for a given table entry. They should be written in order with the ADDR_RULE register always written last.

For example, to write table entry 0 the registers should be written in this order:

1: ADDR_FILT_UPR[0]

2: ADDR_FILT_MID[0]

3: ADDR_FILT_LWR[0]

4: ADDR_RULE[0]

Table 48. Bit Descriptions for ADDR_RULEn

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W
14	APPLY2PORT1	Apply to Port 1. 0: Do Not Apply to Port 1. Do not apply this table entry/rule to frames received on port 1. 1: Apply to Port 1. Apply this table entry/rule to frames received on port 1.	0x0	R/W
[13:4]	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
3	HOST_PRI	Host Rx Port Priority. On the receive port to the host there are 2 FIFOs, low and high priority. This field determines which FIFO the frame is placed in. 0: Low priority 1: High priority Note that by default memory resources are provided for a high priority FIFO. However, if the memory assigned to the high priority FIFO is moved to another FIFO by writing to the FIFO_SIZE register then this field must not be set to 1.	0x0	R/W
[2:1]	RESERVED	Reserved.	0x0	R
0	TO_HOST	Forward Frames Matching This MAC Address to the Host. If APPLY2PORT1 is set to 1 and TO_HOST is 0 then frames matching the DA for this entry will be dropped.	0x0	R/W

P1 Rx Frame Count Register

Address: 0x80, Reset: 0x0000, Name: P1_RX_FRM_CNT

Table 49. Bit Descriptions for P1_RX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_FRM_CNT	Port 1 Rx Frame Count.	0x0	R

P1 Rx Broadcast Frame Count Register

Address: 0x81, Reset: 0x0000, Name: P1_RX_BCAST_CNT

Table 50. Bit Descriptions for P1_RX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_BCAST_CNT	Port 1 Rx Broadcast Frame Count.	0x0	R

P1 Rx Multicast Frame Count Register

Address: 0x82, Reset: 0x0000, Name: P1_RX_MCAST_CNT

Table 51. Bit Descriptions for P1_RX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_MCAST_CNT	Port 1 Rx Multicast Frame Count.	0x0	R

P1 Rx Unicast Frame Count Register

Address: 0x83, Reset: 0x0000, Name: P1_RX_UCAST_CNT

Table 52. Bit Descriptions for P1_RX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_UCAST_CNT	Port 1 Rx Unicast Frame Count.	0x0	R

P1 Rx CRC Errored Frame Count Register

Address: 0x84, Reset: 0x0000, Name: P1_RX_CRC_ERR_CNT

Table 53. Bit Descriptions for P1_RX_CRC_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_CRC_ERR_CNT	Port 1 Rx CRC Errored Frame Count.	0x0	R

P1 Rx Align Error Count Register

Address: 0x85, Reset: 0x0000, Name: P1_RX_ALGN_ERR_CNT

Table 54. Bit Descriptions for P1_RX_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_ALGN_ERR_CNT	Port 1 Rx Align Error Count.	0x0	R

P1 Rx Long/Short Frame Error Count Register

Address: 0x86, Reset: 0x0000, Name: P1_RX_LS_ERR_CNT

Table 55. Bit Descriptions for P1_RX_LS_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_LS_ERR_CNT	Port 1 Rx Long/Short Frame Error Count.	0x0	R

P1 Rx PHY Error Count Register

Address: 0x87, Reset: 0x0000, Name: P1_RX_PHY_ERR_CNT

Table 56. Bit Descriptions for P1_RX_PHY_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_PHY_ERR_CNT	Port 1 Rx PHY Error Count.	0x0	R

P1 Tx Frame Count Register

Address: 0x88, Reset: 0x0000, Name: P1_TX_FRM_CNT

Table 57. Bit Descriptions for P1_TX_FRM_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_TX_FRM_CNT	Port 1 Tx Frame Count.	0x0	R

P1 Tx Broadcast Frame Count Register

Address: 0x89, Reset: 0x0000, Name: P1_TX_BCAST_CNT

Table 58. Bit Descriptions for P1_TX_BCAST_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_TX_BCAST_CNT	Port 1 Tx Broadcast Frame Count.	0x0	R

P1 Tx Multicast Frame Count Register

Address: 0x8A, Reset: 0x0000, Name: P1_TX_MCAST_CNT

Table 59. Bit Descriptions for P1_TX_MCAST_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_TX_MCAST_CNT	Port 1 Tx Multicast Frame Count.	0x0	R

P1 Tx Unicast Frame Count Register

Address: 0x8B, Reset: 0x0000, Name: P1_TX_UCAST_CNT

Table 60. Bit Descriptions for P1_TX_UCAST_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_TX_UCAST_CNT	Port 1 Tx Unicast Frame Count.	0x0	R

P1 Rx Frames Dropped Due to FIFO Full Register

Address: 0x8C, Reset: 0x0000, Name: P1_RX_DROP_FULL_CNT

Table 61. Bit Descriptions for P1_RX_DROP_FULL_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_DROP_FULL_CNT	Port 1 Rx Frames Dropped Due to FIFO Full.	0x0	R

P1 Rx Frames Dropped Due to Filtering Register

Address: 0x8D, Reset: 0x0000, Name: P1_RX_DROP_FILT_CNT

Table 62. Bit Descriptions for P1_RX_DROP_FILT_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_RX_DROP_FILT_CNT	Port 1 Rx Frames Dropped Due to Filtering.	0x0	R

P1 Transmit Inter Frame Gap Register

Address: 0x90, Reset: 0x000B, Name: P1_TX_IFG

Table 63. Bit Descriptions for P1_TX_IFG

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	P1_TX_IFG	Inter Frame Gap. Generates an IFG of (P1_TX_IFG+1) x 8-bit times between frames on Tx.	0xB	R/W

P1 Receive Inter Frame Gap Register

Address: 0x95, Reset: 0x000A, Name: P1_RX_IFG

Table 64. Bit Descriptions for P1_RX_IFG

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	P1_RX_IFG	Inter Frame Gap. The receive MAC checks that the IFG is greater than P1_RX_IFG x 8-bit times. If the received IFG is too small the MAC will drop the received frame and assert ERR_STATUS.P1_RX_IFG_ERR.	0xA	R/W

P1 Max Receive Frame Length Register

Address: 0x96, Reset: 0x0618, Name: P1_RX_MAX_LEN

Max Receive Frame Length in Bytes.

Table 65. Bit Descriptions for P1_RX_MAX_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_MAX_FRM_LEN	Maximum Frame Length on Receive.	0x618	R/W

P1 Min Receive Frame Length Register

Address: 0x97, Reset: 0x0040, Name: P1_RX_MIN_LEN

Min Receive Frame Length in Bytes.

Table 66. Bit Descriptions for P1_RX_MIN_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	P1_MIN_FRM_LEN	Minimum Frame Length on Receive.	0x40	R/W

Timestamp Accumulator Addend Register

Address: 0x98, Reset: 0x0000, Name: TS_ADDEND_LWR

Table 67. Bit Descriptions for TS_ADDEND_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_ADDEND[15:0]	Timestamp Accumulator Addend. The TS_ADDEND_* registers must be written in the correct order, TS_ADDEND_LWR first followed by TS_ADDED_UPR. The values will be used on detecting the write to TS_ADDED_UPR.	0x0	R/W

Timestamp Accumulator Addend Register

Address: 0x99, Reset: 0x8000, Name: TS_ADDEND_UPR

Table 68. Bit Descriptions for TS_ADDEND_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_ADDEND[31:16]	Timestamp Accumulator Addend. The TS_ADDEND_* registers must be written in the correct order, TS_ADDEND_LWR first followed by TS_ADDED_UPR. The values will be used on detecting the write to TS_ADDED_UPR.	0x8000	R/W

Timer Update Compare Register

Address: 0x9A, Reset: 0xCA00, Name: TS_1SEC_CMP_LWR

Table 69. Bit Descriptions for TS_1SEC_CMP_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_1SEC_CMP[15:0]	Timestamp 1 Second Compare Value. The TS_1SEC_CMP_* registers must be written in the correct order, TS_1SEC_CMP_LWR first followed by TS_1SEC_CMP_UPR. The values will be used on detecting the write to TS_1SEC_CMP_UPR. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80.	0xCA00	R/W

Timer Update Compare Register

Address: 0x9B, Reset: 0x3B9A, Name: TS_1SEC_CMP_UPR

Table 70. Bit Descriptions for TS_1SEC_CMP_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_1SEC_CMP[31:16]	Timestamp 1 Second Compare Value. The TS_1SEC_CMP_* registers must be written in the correct order, TS_1SEC_CMP_LWR first followed by TS_1SEC_CMP_UPR. The values will be used on detecting the write to TS_1SEC_CMP_UPR. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80.	0x3B9A	R/W

Seconds Counter Lower Register

Address: 0x9C, Reset: 0x0000, Name: TS_SEC_CNT_LWR

Use This Register to Write to the Seconds Counter.

Table 71. Bit Descriptions for TS_SEC_CNT_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_SEC_CNT[15:0]	Write to the Seconds Counter.	0x0	R/W

Seconds Counter Upper Register

Address: 0x9D, Reset: 0x0000, Name: TS_SEC_CNT_UPR

Use This Register to Write to the Seconds Counter.

Table 72. Bit Descriptions for TS_SEC_CNT_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_SEC_CNT[31:16]	Write to the Seconds Counter.	0x0	R/W

Nanoseconds Counter Register

Address: 0x9E, Reset: 0x0000, Name: TS_NS_CNT_LWR

Use This Register to Write to the Nanoseconds Counter.

Table 73. Bit Descriptions for TS_NS_CNT_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_NS_CNT[15:0]	Write to the Nanoseconds Counter. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80.	0x0	R/W

Nanoseconds Counter Register

Address: 0x9F, Reset: 0x0000, Name: TS_NS_CNT_UPR

Use This Register to Write to the Nanoseconds Counter.

Table 74. Bit Descriptions for TS_NS_CNT_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_NS_CNT[31:16]	Write to the Nanoseconds Counter. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80.	0x0	R/W

Timer Configuration Register

Address: 0xA0, Reset: 0x0000, Name: TS_CFG

Table 75. Bit Descriptions for TS_CFG

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	TS_TIMER_STOP	Stop Toggling the TS_TIMER Output. Write 1 to this field to stop the TS_TIMER output toggling and return it to its default value. Write to the TS_TIMER_START registers to start the TS_TIMER output signal again.	0x0	W
2	TS_TIMER_DEF	The Default Value for the TS_TIMER Output. To change the default value of the TS_TIMER from 0 write 1 to this field before enabling the TS_TIMER (its enabled when TS_TSTART is written). Note that on writing 1 to this register the TS_TIMER output will immediately toggle from 0 to 1. Writing to this field will have no effect if the TS_TIMER has already been enabled.	0x0	R/W
1	TS_CLR	Clear the 1588 Timestamp Counters. Write to 1 to reset the timestamp counters to 0. This field automatically clears to 0 after it is written to 1. Four counters are cleared, the accumulator, the nanoseconds counter, the seconds counter and the "free running" counter.	0x0	W
0	TS_EN	Enable the 1588 Timestamp Counter. When 1, the timestamp counter is enabled, and timestamps are captured for all received frames. The counters are not cleared when TS_EN is 0, they simply freeze, so its recommended to write to use TS_CLR after disabling the counters to get them to a known state before starting again.	0x0	R/W

High Period for TS_TIMER Register

Address: 0xA1, Reset: 0x0000, Name: TS_TIMER_HI_LWR

Table 76. Bit Descriptions for TS_TIMER_HI_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_TIMER_HI[15:0]	TS_TIMER High Period. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80. The minimum value that can be written to this field is 80 decimal.	0x0	R/W

High Period for TS_TIMER Register

Address: 0xA2, Reset: 0x0000, Name: TS_TIMER_HI_UPR

Table 77. Bit Descriptions for TS_TIMER_HI_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_TIMER_HI[31:16]	TS_TIMER High Period. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80. The minimum value that can be written to this field is 80 decimal.	0x0	R/W

Low Period for TS_TIMER Register

Address: 0xA3, Reset: 0x0000, Name: TS_TIMER_LO_LWR

Table 78. Bit Descriptions for TS_TIMER_LO_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_TIMER_LO[15:0]	TS_TIMER Low Period. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80. The minimum value that can be written to this field is 80 decimal.	0x0	R/W

Low Period for TS_TIMER Register

Address: 0xA4, Reset: 0x0000, Name: TS_TIMER_LO_UPR

Table 79. Bit Descriptions for TS_TIMER_LO_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_TIMER_LO[31:16]	TS_TIMER Low Period. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80. The minimum value that can be written to this field is 80 decimal.	0x0	R/W

Quantization Error Correction Register

Address: 0xA5, Reset: 0x0000, Name: TS_TIMER_QE_CORR

Table 80. Bit Descriptions for TS_TIMER_QE_CORR

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	TS_TIMER_QE_CORR	TS_TIMER Quantization Error Correction Value. If the required TS_TIMER low and high periods are not directly divisible by 80 then program this field with a value between 0 and 79 to compensate for the TS_TIMER quantization error.	0x0	R/W

TS_TIMER Counter Start Time Lower Register

Address: 0xA6, Reset: 0x0000, Name: TS_TIMER_START_LWR

Point in Time at Which to Start the TS_TIMER Counter.

Table 81. Bit Descriptions for TS_TIMER_START_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_TSTART[15:0]	Point in Time at Which to Start the TS_TIMER Counter. Writing to this register will start the TS_TIMER output. After the TS_TIMER has started, writing to TS_CFG.TS_TIMER_STOP will stop the timer and return the TS_TIMER output to its default value. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80.	0x0	R/W

TS_TIMER Counter Start Time Upper Register

Address: 0xA7, Reset: 0x0000, Name: TS_TIMER_START_UPR

Point in Time at Which to Start the TS_TIMER Counter.

Table 82. Bit Descriptions for TS_TIMER_START_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_TSTART[31:16]	Point in Time at Which to Start the TS_TIMER Counter. Writing to this register will start the TS_TIMER output. After the TS_TIMER has started, writing to TS_CFG.TS_TIMER_STOP will stop the timer and return the TS_TIMER output to its default value. Note that this register must be programmed with a value that is divisible by 80 decimal. This is because the counters are driven by a 25MHz clock and increment in steps of 80.	0x0	R/W

TS_CAPT Pin Timestamp Register 0

Address: 0xA8, Reset: 0x0000, Name: TS_EXT_CAPT0

Timestamp Captured on the Assertion of the TS_CAPT Pin.

Table 83. Bit Descriptions for TS_EXT_CAPT0

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EXT_CAPTD[15:0]	Timestamp Captured on the Assertion of TS_CAPT Pin.	0x0	R

TS_CAPT Pin Timestamp Register 1

Address: 0xA9, Reset: 0x0000, Name: TS_EXT_CAPT1

Timestamp Captured on the Assertion of the TS_CAPT Pin.

Table 84. Bit Descriptions for TS_EXT_CAPT1

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EXT_CAPTD[31:16]	Timestamp Captured on the Assertion of TS_CAPT Pin.	0x0	R

TS_CAPT Pin Timestamp Register 2

Address: 0xAA, Reset: 0x0000, Name: TS_EXT_CAPT2

Timestamp Captured on the Assertion of the TS_CAPT Pin.

Table 85. Bit Descriptions for TS_EXT_CAPT2

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EXT_CAPTD[47:32]	Timestamp Captured on the Assertion of TS_CAPT Pin.	0x0	R

TS_CAPT Pin Timestamp Register 3

Address: 0xAB, Reset: 0x0000, Name: TS_EXT_CAPT3

Timestamp Captured on the Assertion of the TS_CAPT Pin.

Table 86. Bit Descriptions for TS_EXT_CAPT3

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EXT_CAPTD[63:48]	Timestamp Captured on the Assertion of TS_CAPT Pin.	0x0	R

TS_CAPT Free Running Counter Register Lower

Address: 0xAC, Reset: 0x0000, Name: TS_FREECNT_CAPT_LWR

Capture of the Free Running Counter When TS_CAPT Asserts.

Table 87. Bit Descriptions for TS_FREECNT_CAPT_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_CNT_CAPTD[15:0]	Captured Free Running Counter. This 32-bit counter is captured on the assertion of TS_CAPT pin as is TS_EXT_CAPT.	0x0	R

TS_CAPT Free Running Counter Upper Register

Address: 0xAD, Reset: 0x0000, Name: TS_FREECNT_CAPT_UPR

Table 88. Bit Descriptions for TS_FREECNT_CAPT_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_CNT_CAPTD[31:16]	Captured Free Running Counter. This 32-bit counter is captured on the assertion of TS_CAPT pin as is TS_EXT_CAPT.	0x0	R

Captured Egress Timestamp A Lower Register

Address: 0xAE, Reset: 0x0000, Name: TS_EGRESS_A_LWR

Table 89. Bit Descriptions for TS_EGRESS_A_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EGRESS_A[15:0]	Egress Timestamp A.	0x0	R

Captured Egress Timestamp A Upper Register

Address: 0xAF, Reset: 0x0000, Name: TS_EGRESS_A_UPR

Table 90. Bit Descriptions for TS_EGRESS_A_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EGRESS_A[31:16]	Egress Timestamp A.	0x0	R

Captured Egress Timestamp B Lower Register

Address: 0xB0, Reset: 0x0000, Name: TS_EGRESS_B_LWR

Table 91. Bit Descriptions for TS_EGRESS_B_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EGRESS_B[15:0]	Egress Timestamp B.	0x0	R

Captured Egress Timestamp B Upper Register

Address: 0xB1, Reset: 0x0000, Name: TS_EGRESS_B_UPR

Table 92. Bit Descriptions for TS_EGRESS_B_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EGRESS_B[31:16]	Egress Timestamp B.	0x0	R

Captured Egress Timestamp C Lower Register

Address: 0xB2, Reset: 0x0000, Name: TS_EGRESS_C_LWR

Table 93. Bit Descriptions for TS_EGRESS_C_LWR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EGRESS_C[15:0]	Egress Timestamp C.	0x0	R

Captured Egress Timestamp C Upper Register

Address: 0xB3, Reset: 0x0000, Name: TS_EGRESS_C_UPR

Table 94. Bit Descriptions for TS_EGRESS_C_UPR

Bits	Bit Name	Description	Reset	Access
[15:0]	TS_EGRESS_C[31:16]	Egress Timestamp C.	0x0	R

P1 Rx Low Priority FIFO Frame Count Register

Address: 0xB4, Reset: 0x0000, Name: P1_LO_RFC

The number of frames in the receive FIFO.

Table 95. Bit Descriptions for P1_LO_RFC

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
[8:0]	P1_LO_RFC	Receive Frame Count for the Low Priority FIFO. The number of frames in the Rx FIFO. Provided for debug purposes. In store and forward the host software will only need to know that there is at least one frame available - see P1_RX_RDY.	0x0	R

P1 Rx High Priority FIFO Frame Count Register

Address: 0xB5, Reset: 0x0000, Name: P1_HI_RFC

The number of frames in the receive FIFO.

Table 96. Bit Descriptions for P1_HI_RFC

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
[8:0]	P1_HI_RFC	Receive Frame Count for the High Priority FIFO. The number of frames in the Rx FIFO. Provided for debug purposes. In store and forward the host software will only need to know that there is at least one frame available - P1_RX_RDY.	0x0	R

Tx FIFO Frame Count Register

Address: 0xB6, Reset: 0x0000, Name: TFC

For debug only. Number of frames in the transmit FIFO.

Table 97. Bit Descriptions for TFC

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
[8:0]	TFC	Number of Frames in the Tx FIFO.	0x0	R

Tx FIFO Valid Half Words Register

Address: 0xB7, Reset: 0x0000, Name: TXSIZE

Number of Valid Half Words (16 Bit) in the Host Tx FIFO.

Table 98. Bit Descriptions for TXSIZE

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
[13:0]	TX_SIZE	Data in the Tx FIFO. Number of Half Words (16 Bit).	0x0	R

P1 Low Priority Rx FIFO Valid Half Words Register

Address: 0xB8, Reset: 0x0000, Name: P1_LO_RXSIZE

Number of Valid Half Words (16 Bit) in the low priority Rx FIFO.

Table 99. Bit Descriptions for P1_LO_RXSIZE

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
[13:0]	P1_LO_RXSIZE	Data in the Rx FIFO. Number of Half Words (16 Bit).	0x0	R

P1 High Priority Rx FIFO Valid Half Words Register

Address: 0xB9, Reset: 0x0000, Name: P1_HI_RXSIZE

Number of Valid Half Words (16 Bit) in the high priority Rx FIFO.

Table 100. Bit Descriptions for P1_HI_RXSIZE

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
[13:0]	P1_HI_RXSIZE	Data in the Rx FIFO. Number of Half Words (16 Bit).	0x0	R

Scratch Registers

Address: 0xDC to 0xDF (Increments of 1), Reset: 0x0000, Name: SCRATCHn

The user can freely use these registers for debug purposes.

Table 101. Bit Descriptions for SCRATCHn

Bits	Bit Name	Description	Reset	Access
[15:0]	SCRATCH_DATA	Scratch Data.	0x0	R/W

PHY REGISTER DETAILS

Table 102. MDIOMAP_SPEPHY Register Summary

Device Address	Register Address	Name	Description	Reset	Access
0x01	0x0012	PMA_PMD_BT1_ABILITY	BASE-T1 PMA/PMD Extended Ability Register.	0x0004	R
0x01	0x0834	PMA_PMD_BT1_CONTROL	BASE-T1 PMA/PMD Control Register.	0x8002	R/W
0x01	0x08F6	B10L_PMA_CNTRL	10BASE-T1L PMA Control Register.	0x0000	R/W
0x01	0x08F7	B10L_PMA_STAT	10BASE-T1L PMA Status Register.	0x2000	R
0x01	0x08F8	B10L_TEST_MODE_CNTRL	10BASE-T1L Test Mode Control Register.	0x0000	R/W
0x01	0x8302	B10L_PMA_LINK_STAT	10BASE-T1L PMA Link Status Register.	0x0000	R
0x03	0x08E6	B10L_PCS_CNTRL	10BASE-T1L PCS Control Register.	0x0000	R/W
0x07	0x0200	AN_CONTROL	BASE-T1 Autonegotiation Control Register.	0x1000	R/W
0x07	0x0201	AN_STATUS	BASE-T1 Autonegotiation Status Register.	0x0008	R
0x07	0x0202	AN_ADV_ABILITY_L	BASE-T1 Autonegotiation Advertisement [15:0] Register.	0x0001	R/W
0x07	0x0203	AN_ADV_ABILITY_M	BASE-T1 Autonegotiation Advertisement [31:16] Register.	0x4000	R/W
0x07	0x0204	AN_ADV_ABILITY_H	BASE-T1 Autonegotiation Advertisement [47:32] Register.	0x0000	R/W
0x07	0x0205	AN_LP_ADV_ABILITY_L	BASE-T1 Autonegotiation Link Partner Base Page Ability [15:0] Register.	0x0000	R
0x07	0x0206	AN_LP_ADV_ABILITY_M	BASE-T1 Autonegotiation Link Partner Base Page Ability [31:16] Register.	0x0000	R
0x07	0x0207	AN_LP_ADV_ABILITY_H	BASE-T1 Autonegotiation Link Partner Base Page Ability [47:32] Register.	0x0000	R
0x07	0x0208	AN_NEXT_PAGE_L	BASE-T1 Autonegotiation Next Page Transmit [15:0] Register.	0x2001	R/W
0x07	0x0209	AN_NEXT_PAGE_M	BASE-T1 Autonegotiation Next Page Transmit [31:16] Register.	0x0000	R/W
0x07	0x020A	AN_NEXT_PAGE_H	BASE-T1 Autonegotiation Next Page Transmit [47:32] Register.	0x0000	R/W
0x07	0x020B	AN_LP_NEXT_PAGE_L	BASE-T1 Autonegotiation Link Partner Next Page Ability [15:0] Register.	0x0000	R
0x07	0x020C	AN_LP_NEXT_PAGE_M	BASE-T1 Autonegotiation Link Partner Next Page Ability [31:16] Register.	0x0000	R
0x07	0x020D	AN_LP_NEXT_PAGE_H	BASE-T1 Autonegotiation Link Partner Next Page Ability [47:32] Register.	0x0000	R
0x07	0x8001	AN_STATUS_EXTRA	Extra Autonegotiation Status Register.	0x0000	R
0x1E	0x0002	MMD1_DEV_ID1	Vendor Specific MMD 1 Device Identifier High Register.	0x0283	R
0x1E	0x0003	MMD1_DEV_ID2	Vendor Specific MMD 1 Device Identifier Low Register.	0xBC00	R
0x1E	0x0010	CRSM_IRQ_STATUS	System Interrupt Status Register.	0x0800	R
0x1E	0x0011	PHY_SUBSYS_IRQ_STATUS	PHY Subsystem Interrupt Status Register.	0x0000	R
0x1E	0x0020	CRSM_IRQ_MASK	System Interrupt Mask Register.	0x0FFF	R/W
0x1E	0x0021	PHY_SUBSYS_IRQ_MASK	PHY Subsystem Interrupt Mask Register.	0x2403	R/W
0x1E	0x8001	FC_EN	Frame Checker Enable Register.	0x0001	R/W
0x1E	0x8004	FC_IRQ_EN	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x1E	0x8005	FC_TX_SEL	Frame Checker Transmit Select Register.	0x0000	R/W
0x1E	0x8008	RX_ERR_CNT	Receive Error Count Register.	0x0000	R
0x1E	0x8009	FC_FRM_CNT_H	Frame Checker Count High Register.	0x0000	R
0x1E	0x800A	FC_FRM_CNT_L	Frame Checker Count Low Register.	0x0000	R
0x1E	0x800B	FC_LEN_ERR_CNT	Frame Checker Length Error Count Register.	0x0000	R

Device Address	Register Address	Name	Description	Reset	Access
0x1E	0x800C	FC_ALGN_ERR_CNT	Frame Checker Alignment Error Count Register.	0x0000	R
0x1E	0x800D	FC_SYMB_ERR_CNT	Frame Checker Symbol Error Count Register.	0x0000	R
0x1E	0x800E	FC_OSZ_CNT	Frame Checker Oversized Frame Count Register.	0x0000	R
0x1E	0x800F	FC_USZ_CNT	Frame Checker Undersized Frame Count Register.	0x0000	R
0x1E	0x8010	FC_ODD_CNT	Frame Checker Odd Nibble Frame Count Register.	0x0000	R
0x1E	0x8011	FC_ODD_PRE_CNT	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x1E	0x8013	FC_FALSE_CARRIER_CNT	Frame Checker False Carrier Count Register.	0x0000	R
0x1E	0x8015	FG_EN	Frame Generator Enable Register.	0x0000	R/W
0x1E	0x8016	FG_CNTRL_RSTRT	Frame Generator Control/Restart Register.	0x0001	R/W
0x1E	0x8017	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x1E	0x8018	FG_IRQ_EN	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x1E	0x801A	FG_FRM_LEN	Frame Generator Frame Length Register.	0x006B	R/W
0x1E	0x801C	FG_NFRM_H	Frame Generator Number of Frames High Register.	0x0000	R/W
0x1E	0x801D	FG_NFRM_L	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x1E	0x801E	FG_DONE	Frame Generator Done Register.	0x0000	R
0x1E	0x803D	MAC_IF_LOOPBACK	MAC Interface Loopbacks Configuration Register.	0x000A	R/W
0x1E	0x8810	CRSM_SFT_RST	Software Reset Register.	0x0000	R/W
0x1E	0x8812	CRSM_SFT_PD_CNTRL	Software Power-down Control Register.	0x0000	R/W
0x1E	0x8814	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset Register.	0x0000	R/W
0x1E	0x8815	CRSM_MAC_IF_RST	PHY MAC Interface Reset Register.	0x0000	R/W
0x1E	0x8818	CRSM_STAT	System Status Register.	0x0000	R
0x1E	0x882C	CRSM_DIAG_CLK_CTRL	CRSM Diagnostics Clock Control.	0x0002	R/W
0x1E	0x8C81	LED_CNTRL	LED Control Register.	0x0000	R/W

BASE-T1 PMA/PMD Extended Ability Register

Device Address: 0x01; Register Address: 0x0012, Reset: 0x0004, Name: PMA_PMD_BT1_ABILITY

This address corresponds to the BASE-T1 PMA/PMD extended ability register specified in Clause 45.2.1.16 of Standard 802.3. This register is read only and writes have no effect.

Table 103. Bit Descriptions for PMA_PMD_BT1_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	B10S_ABILITY	10BASE-T1S Ability. This bit always reads as 1'b0 because the PMA/PMD does not support 10BASE-T1S.	0x0	R
2	B10L_ABILITY	10BASE-T1L Ability. This bit always reads as 1'b1 because the PMA/PMD supports 10BASE-T1L.	0x1	R
1	B1000_ABILITY	1000BASE-T1 Ability. This bit always reads as 1'b0 because the PMA/PMD does not support 1000BASE-T1.	0x0	R
0	B100_ABILITY	100BASE-T1 Ability. This bit always reads as 1'b0 because the PMA/PMD does not support 100BASE-T1.	0x0	R

BASE-T1 PMA/PMD Control Register

Device Address: 0x01; Register Address: 0x0834, Reset: 0x8002, Name: PMA_PMD_BT1_CONTROL

This address corresponds to the BASE-T1 PMA/PMD control register specified in Clause 45.2.1.185 of Standard 802.3.

Table 104. Bit Descriptions for PMA_PMD_BT1_CONTROL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x1	R
14	CFG_MST	Master-slave Config. CFG_MST is used only when autonegotiation is disabled; otherwise this value is determined by the autonegotiation process itself. When this bit is set as one, the part is configured as master. Otherwise, the part is configured as slave.	Pin Dependent	R/W
[13:4]	RESERVED	Reserved.	0x0	R
[3:0]	TYPE_SEL	Type Selection. This configuration is only used when autonegotiation is disabled. See IEEE Std 802.3 Table 45-149. Values other than those shown below should be considered reserved. 0010: 10BASE-T1L.	0x2	R/W

10BASE-T1L PMA Control Register

Device Address: 0x01; Register Address: 0x08F6, Reset: 0x0000, Name: B10L_PMA_CNTRL

This address corresponds to the 10BASE-T1L PMA control register specified in Clause 45.2.1.186a of Standard 802.3cg

Table 105. Bit Descriptions for B10L_PMA_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_TX_DIS_MODE_EN	10BASE-T1L Transmit Disable Mode. When this bit is set to one it disables output on the transmit path. Otherwise, it enables output on the transmit path.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
12	B10L_TX_LVL_HI	10BASE-T1L Transmit Voltage Amplitude Control. This configuration is only used when autonegotiation is disabled. Otherwise, the configuration is decided by the autonegotiation process. When this bit is set as one, the part works in the 2.4 V pk-pk operating mode. Otherwise, the part works in the 1.0 V pk-pk operating mode.	Pin Dependent	R/W
11	RESERVED	Reserved.	Pin Dependent	R/W
[10:1]	RESERVED	Reserved.	0x0	R/W
0	B10L_LB_PMA_LOC_EN	10BASE-T1L PMA Loopback. When this bit is set to one, the PMA accepts data on the transmit path and returns it on the receive path. When this bit is set to zero, the PMA works in normal mode.	0x0	R/W

10BASE-T1L PMA Status Register

Device Address: 0x01; Register Address: 0x08F7, Reset: 0x2000, Name: B10L_PMA_STAT

This address corresponds to the 10BASE-T1L PMA status register specified in Clause 45.2.1.186b of Standard 802.3cg

Table 106. Bit Descriptions for B10L_PMA_STAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	B10L_LB_PMA_LOC_ABLE	10BASE-T1L PMA Loopback Ability. This bit always reads as 1'b1 as the PMA has loopback ability	0x1	R
12	B10L_TX_LVL_HI_ABLE	10BASE-T1L High Voltage Tx Ability. Indicates that the PHY supports 10BASE-T1L high voltage (2.4 V pk-pk) transmit level operating mode.	Pin Dependent	R

Bits	Bit Name	Description	Reset	Access
[11:3]	RESERVED	Reserved.	0x0	R
2	B10L_POL_INV	10BASE-T1L Polarity Inverse. When this bit is read as a zero, it means that the polarity of the receiver is not reversed. When it is read as a one, it indicates that the polarity of the receiver is reversed.	0x0	R
[1:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L Test Mode Control Register

Device Address: 0x01; Register Address: 0x08F8, Reset: 0x0000, Name: B10L_TEST_MODE_CNTRL

This address corresponds to the 10BASE-T1L PMA test mode control register specified in Clause 45.2.1.186c of Standard 802.3cg. The default value of this register selects normal operation without management intervention as the initial state of the device.

Table 107. Bit Descriptions for B10L_TEST_MODE_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:13]	B10L_TX_TEST_MODE	10BASE-T1L Transmitter Test Mode. 000: Normal operation. 001: Test mode 1 - Transmitter output voltage and timing jitter test mode. When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, -1). 010: Test mode 2 - Transmitter output droop test mode. When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "-1" symbols. 011: Test mode 3 - Normal operation in Idle mode. When test mode 3 is enabled, the PHY shall transmit as in non-test operation and in the MASTER data mode with data set to normal Inter-Frame idle signals.	0x0	R/W
[12:0]	RESERVED	Reserved.	0x0	R

10BASE-T1L PMA Link Status Register

Device Address: 0x01; Register Address: 0x8302, Reset: 0x0000, Name: B10L_PMA_LINK_STAT

This address may be read to determine the 10BASE-T1L PMA link status. Reading B10L_PMA_LINK_STAT clears the latching condition of these bits

Table 108. Bit Descriptions for B10L_PMA_LINK_STAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	B10L_REM_RCVR_STAT_OK_LL	10BASE-T1L Remote Receiver Status Ok Latch Low. Latched low version of B10L_REM_RCVR_STAT_OK.	0x0	R LL
12	B10L_REM_RCVR_STAT_OK	10BASE-T1L Remote Receiver Status Ok. When read as 1 this bit indicates that the remote receiver status is OK.	0x0	R
11	B10L_LOC_RCVR_STAT_OK_LL	10BASE-T1L Local Receiver Status Ok Latch Low. Latched low version of B10L_LOC_RCVR_STAT_OK.	0x0	R LL
10	B10L_LOC_RCVR_STAT_OK	10BASE-T1L Local Receiver Status Ok. When read as 1 this bit indicates that the local receiver status is OK.	0x0	R
9	B10L_DSCR_STAT_OK_LL	BASE-T1L Descrambler Status Ok Latch Low. When read as one this bit indicates that the descrambler status is OK.	0x0	R LL
8	B10L_DSCR_STAT_OK	10BASE-T1L Descrambler Status Ok. When read as 1 this bit indicates that the descrambler status is OK.	0x0	R
[7:2]	RESERVED	Reserved.	0x0	R
1	B10L_LINK_STAT_OK_LL	Link Status Ok Latch Low. When read as 1 this bit indicates that the link status is OK.	0x0	R LL
0	B10L_LINK_STAT_OK	Link Status OK. When read as 1 this bit indicates that the link status is OK.	0x0	R

10BASE-T1L PCS Control Register

Device Address: 0x03; Register Address: 0x08E6, Reset: 0x0000, Name: B10L_PCS_CNTRL

This address corresponds to the 10BASE-T1L PCS control register specified in Clause 45.2.3.68a of Standard 802.3cg.

Table 109. Bit Descriptions for B10L_PCS_CNTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	B10L_LB_PCS_EN	PCS Loopback Enable. When set to one, this bit enables the 10BASE-T1L PCS loopback.	0x0	R/W
[13:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Control Register

Device Address: 0x07; Register Address: 0x0200, Reset: 0x1000, Name: AN_CONTROL

This address corresponds to the BASE-T1 autonegotiation control register specified in Clause 45.2.7.19 of Standard 802.3.

Table 110. Bit Descriptions for AN_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	AN_EN	Autonegotiation Enable. When this bit is set to one the Auto-Negotiation is enabled. Auto-Negotiation is enabled by default and it is strongly recommended that it is always enabled.	0x1	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	AN_RESTART	Autonegotiation Restart. Setting this bit to one restarts the autonegotiation process. This bit is self-clearing and it returns a value of one until the autonegotiation process has been initiated.	0x0	R/W SC
[8:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x0201, Reset: 0x0008, Name: AN_STATUS

This address corresponds to the BASE-T1 autonegotiation status register specified in Clause 45.2.7.20 of Standard 802.3.

Table 111. Bit Descriptions for AN_STATUS

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	AN_PAGE_RX	Page Received. This bit is set to indicate that a new link codeword has been received and stored in the AN_LP_ADV_ABILITY register or the AN_LP_NEXT_PAGE. The contents of the AN_LP_ADV_ABILITY are valid when this bit is set the first time during autonegotiation. This bit resets to zero on a read of the AN_STATUS register.	0x0	R LH
5	AN_COMPLETE	Autonegotiation Complete. When this bit is read as one, it means that the autonegotiation process has been completed, the PHY link is up, and that the contents of the AN_ADV_ABILITY and AN_LP_ADV_ABILITY are valid. This bit returns zero if the autonegotiation is disabled clearing the AN_EN bit.	0x0	R
4	RESERVED	Reserved.	0x0	R
3	AN_ABLE	Autonegotiation Ability. When this bit is read as one, it indicates that the PHY is able to perform autonegotiation.	0x1	R
2	AN_LINK_STATUS	Link Status. When read as one, this bit indicates that a valid link has been established. If this bit reads zero, it means that the link has failed since the last time it was read.	0x0	R LL
[1:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement [15:0] Register

Device Address: 0x07; Register Address: 0x0202, Reset: 0x0001, Name: AN_ADV_ABILITY_L

This address corresponds to the BASE-T1 autonegotiation advertisement register [15:0] specified in Clause 45.2.7.21 of Standard 802.3.

Table 112. Bit Descriptions for AN_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_ADV_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R/W
14	AN_ADV_ACK	Acknowledge (ACK). This bit indicates that the device has successfully received its link partner's link codeword. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_ADV_REMOTE_FAULT	Remote Fault. See IEEE Std 802.3 subclause 98.2.1.2.7.	0x0	R/W
12	AN_ADV_FORCE_MS	Force Master/slave Configuration. This bit allows the PHY to force its master/slave configuration. When this bit is set as zero, the master/slave configuration is a preferred mode (The configuration in AN_ADV_MST is a preferred configuration). If this bit is set to one, then the master/slave configuration is a forced mode (The configuration in AN_ADV_MST is a forced configuration) See IEEE Std 802.3 subclause 98.2.1.2.5 for more details.	0x0	R/W
[11:10]	AN_ADV_PAUSE	Pause Ability. This field advertises support for asymmetric and symmetric pause functions on full-duplex links. See IEEE Std 802.3 subclause 98.2.1.2.6 for more details.	0x0	R/W
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_ADV_SELECTOR	Selector. The value of this field is fixed at 5'b00001, which is the IEEE 802.3 selector value. See IEEE Std 802.3 subclause 98.2.1.2.1.	0x1	R

BASE-T1 Autonegotiation Advertisement [31:16] Register

Device Address: 0x07; Register Address: 0x0203, Reset: 0x4000, Name: AN_ADV_ABILITY_M

This address corresponds to the BASE-T1 autonegotiation advertisement register [31:16] specified in Clause 45.2.7.21 of Standard 802.3.

Table 113. Bit Descriptions for AN_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_ADV_B10L	10BASE-T1L Ability. This bit indicates that the device is compatible with 10BASE-T1L.	0x1	R/W
[13:5]	RESERVED	Reserved.	0x0	R
4	AN_ADV_MST	Master/slave Configuration. This bit advertises the master/slave configuration, as follows: 0: Slave 1: Master. See also AN_ADV_FORCE_MS register, which determines whether this bit expresses a preference or a forced value. See IEEE Std 802.3 subclause 98.2.1.2.3; Master/slave configuration is bit 4 of the Transmitted Nonce Field.	Pin Dependent	R/W
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Advertisement [47:32] Register

Device Address: 0x07; Register Address: 0x0204, Reset: 0x0000, Name: AN_ADV_ABILITY_H

This address corresponds to the BASE-T1 autonegotiation advertisement register [47:32] specified in Clause 45.2.7.21 of Standard 802.3.

Table 114. Bit Descriptions for AN_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	AN_ADV_B10L_TX_LVL_HI_ABL	10BASE-T1L High Level Transmit Operating Mode Ability. This bit advertises that the PHY is capable of transmitting in the high-level (2.4 V pk-pk) transmit operating mode. This bit is used with AN_ADV_B10L_TX_LVL_HI_REQ to configure 10BASE-T1L transmission level (2.4 V pk-pk or 1.0 V pk-pk); see the AN_ADV_B10L_TX_LVL_HI_REQ for more details.	Pin Dependent	R/W
12	AN_ADV_B10L_TX_LVL_HI_REQ	10BASE-T1L High Level Transmit Operating Mode Request. This bit advertises that the PHY is requesting that high-level (2.4 V pk-pk) transmit operating mode is used. Note the transmit level is resolved as follows: If either PHY is not capable of high-level transmission (and has AN_ADV_B10L_TX_LVL_HI_ABL = 0), then both PHYs must use the low voltage (1.0 V pk-pk) transmit operating mode. Otherwise, if either PHY requests high-level transmission (and has AN_ADV_B10L_TX_LVL_HI_REQ = 1), then both PHYs must use the high voltage (2.4 V pk-pk) transmit operating mode. See IEEE P802.cg subclause 146.6.4 for more details.	Pin Dependent	R/W
[11:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability [15:0] Register

Device Address: 0x07; Register Address: 0x0205, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_L

This address corresponds to the link partner's BASE-T1 autonegotiation base page ability register [15:0] specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of registers AN_LP_ADV_ABILITY_M and AN_LP_ADV_ABILITY_H is latched when AN_LP_ADV_ABILITY_L is read.

Table 115. Bit Descriptions for AN_LP_ADV_ABILITY_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_ADV_NEXT_PAGE_REQ	Link Partner Next Page Request. This bit indicates that the link partner PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R
14	AN_LP_ADV_ACK	Link Partner Acknowledge (ACK). This bit indicates that the device has successfully received its link partner's link codeword. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_LP_ADV_REMOTE_FAULT	Link Partner Remote Fault. See IEEE Std 802.3 subclause 98.2.1.2.7.	0x0	R
12	AN_LP_ADV_FORCE_MS	Link Partner Force Master/slave Configuration. This bit reports the link partner's forced master/slave configuration, with values as follows: 0: Preferred mode (AN_LP_ADV_MSTR is a preferred configuration) 1: Forced mode (AN_LP_ADV_MSTR is a forced configuration) See IEEE Std 802.3 subclause 98.2.1.2.5 for more details.	0x0	R
[11:10]	AN_LP_ADV_PAUSE	Link Partner Pause Ability. This field reports the link partner's support for asymmetric and symmetric pause functions on full-duplex links. See IEEE Std 802.3 subclause 98.2.1.2.6 for more details.	0x0	R
[9:5]	RESERVED	Reserved.	0x0	R
[4:0]	AN_LP_ADV_SELECTOR	Link Partner Selector. The value of this field should be 5'b00001, which is the IEEE 802.3 selector value. See IEEE Std 802.3 subclause 98.2.1.2.1.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability [31:16] Register

Device Address: 0x07; Register Address: 0x0206, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_M

This address corresponds to the link partner's BASE-T1 autonegotiation base page ability register [31:16] specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 116. Bit Descriptions for AN_LP_ADV_ABILITY_M

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L	Link Partner 10BASE-T1L Ability. This bit indicates if the link partner has 10BASE-T1L ability.	0x0	R
[13:8]	RESERVED	Reserved.	0x0	R
7	AN_LP_ADV_B1000	Link Partner 1000BASE-T1 Ability. This bit indicates if the link partner has 1000BASE-T1 ability.	0x0	R
6	AN_LP_ADV_B10S_FD	Link Partner 10BASE-T1S Full Duplex Ability. This bit indicates if the link partner has 10BASE-T1S ability.	0x0	R
5	AN_LP_ADV_B100	Link Partner 100BASE-T1 Ability. This bit indicates if the link partner has 100BASE-T1 ability.	0x0	R
4	AN_LP_ADV_MST	Link Partner Master/Slave Configuration. This bit reports the link partner's master/slave configuration, as follows: 0: Slave. 1: Master. See also AN_LP_ADV_FORCE_MS register, which determines whether this bit expresses a preference or a forced value. See IEEE Std 802.3 subclause 98.2.1.2.3; Master/slave configuration is bit 4 of the Transmitted Nonce Field.	0x0	R
[3:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Link Partner Base Page Ability [47:32] Register

Device Address: 0x07; Register Address: 0x0207, Reset: 0x0000, Name: AN_LP_ADV_ABILITY_H

This address corresponds to the link partner's BASE-T1 autonegotiation base page ability register [47:32] specified in Clause 45.2.7.22 of Standard 802.3. Note that the value of this register is latched when AN_LP_ADV_ABILITY_L is read. Reading this register returns the latched value rather than the current value.

Table 117. Bit Descriptions for AN_LP_ADV_ABILITY_H

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	AN_LP_ADV_B10L_EEE	Link Partner 10BASE-T1L EEE Ability. This bit reports if the link partner is capable of using 10BASE-T1L energy efficient ethernet.	0x0	R
13	AN_LP_ADV_B10L_TX_LVL_HI_ABL	Link Partner 10BASE-T1L High Level Transmit Operating Mode Ability. This bit reports whether the link partner is capable of transmitting in the high level (2.4 V pk-pk) transmit operating mode. This bit is used with AN_LP_ADV_B10L_TX_LVL_HI_REQ to configure 10BASE-T1L transmission level (2.4 V pk-pk or 1.0 V pk-pk); see the AN_ADV_B10L_TX_LVL_HI_REQ for more details.	0x0	R
12	AN_LP_ADV_B10L_TX_LVL_HI_REQ	Link Partner 10BASE-T1L High Level Transmit Operating Mode Request. This bit reports whether the link partner is requesting that high level (2.4 V pk-pk) transmit operating mode is used. See the AN_ADV_B10L_TX_LVL_HI_REQ for more details.	0x0	R
11	AN_LP_ADV_B10S_HD	Link Partner 10BASE-T1S Half Duplex Ability. This bit reports if the link partner is capable of using 10BASE-T1S half-duplex.	0x0	R
[10:0]	RESERVED	Reserved.	0x0	R

BASE-T1 Autonegotiation Next Page Transmit [15:0] Register

Device Address: 0x07; Register Address: 0x0208, Reset: 0x2001, Name: AN_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation next page transmit register [15:0] specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represent a message page with the message code set to Null. AN_NEXT_PAGE_M and AN_NEXT_PAGE_H should be written before AN_NEXT_PAGE_L.

Table 118. Bit Descriptions for AN_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R/W
14	AN_NP_ACK	Next Page Acknowledge. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_NP_MESSAGE_PAGE	Next Page Encoding. Indicates encoding of next page, as follows: 0: Unformatted next page. 1: Message next page.	0x1	R/W
12	AN_NP_ACK2	Acknowledge 2. Indicates whether the PHY can comply with the message. See IEEE Std 802.3 subclause 28.2.3.4.6.	0x0	R/W
11	AN_NP_TOGGLE	Toggle Bit. The Toggle bit is used to synchronize pages between the PH_YS. This always read as 0 (the toggle bit is set automatically by the Arbitration state machine).	0x0	R
[10:0]	AN_NP_MESSAGE_CODE	Message/unformatted Code Field. For a message page (AN_NP_MESSAGE_PAGE = 1), the valid values are defined in IEEE Std 802.3 Table 45-329: 1: Null Message. 5: Organizationally Unique Identifier Tagged Message. 6: AN Device Identifier Tag Code.	0x1	R/W

BASE-T1 Autonegotiation Next Page Transmit [31:16] Register

Device Address: 0x07; Register Address: 0x0209, Reset: 0x0000, Name: AN_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation next page transmit register [31:16] specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represent a message page with the message code set to Null. AN_NEXT_PAGE_M and AN_NEXT_PAGE_H should be written before AN_NEXT_PAGE_L.

Table 119. Bit Descriptions for AN_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED1	Unformatted Code Field 1.	0x0	R/W

BASE-T1 Autonegotiation Next Page Transmit [47:32] Register

Device Address: 0x07; Register Address: 0x020A, Reset: 0x0000, Name: AN_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation next page transmit register [47:42] specified in Clause 45.2.7.23 of Standard 802.3. On power-up or autonegotiation reset, this register contains the default value, which represent a message page with the message code set to Null. AN_NEXT_PAGE_M and AN_NEXT_PAGE_H should be written before AN_NEXT_PAGE_L.

Table 120. Bit Descriptions for AN_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_NP_UNFORMATTED2	Unformatted Code Field 2.	0x0	R/W

BASE-T1 Autonegotiation Link Partner Next Page Ability [15:0] Register

Device Address: 0x07; Register Address: 0x020B, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_L

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register [15:0] specified in Clause 45.2.7.24 of Standard 802.3. The values of AN_LP_NEXT_PAGE_M and AN_LP_NEXT_PAGE_H are latched when this register is read.

Table 121. Bit Descriptions for AN_LP_NEXT_PAGE_L

Bits	Bit Name	Description	Reset	Access
15	AN_LP_NP_NEXT_PAGE_REQ	Next Page Request. This bit indicates to the link partner that the PHY wants to send a next page. See IEEE Std 802.3 subclause 98.2.1.2.9.	0x0	R
14	AN_LP_NP_ACK	Link Partner Next Page Acknowledge. See IEEE Std 802.3 subclause 98.2.1.2.8.	0x0	R
13	AN_LP_NP_MESSAGE_PAGE	Link Partner Next Page Encoding. Indicates encoding of link partner next page, as follows: 0: Unformatted next page. 1: Message next page.	0x0	R
12	AN_LP_NP_ACK2	Link Partner Acknowledge 2. See AN_NP_ACK2 for more details.	0x0	R
11	AN_LP_NP_TOGGLE	Link Partner Toggle Bit. Link partner Toggle bit.	0x0	R
[10:0]	AN_LP_NP_MESSAGE_CODE	Link Partner Message/unformatted Code Field. See AN_NP_MESSAGE_PAGE for more details. 1: Null Message. 5: Organizationally Unique Identifier Tagged Message. 6: AN Device Identifier Tag Code.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability [31:16] Register

Device Address: 0x07; Register Address: 0x020C, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_M

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register [31:16] specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 122. Bit Descriptions for AN_LP_NEXT_PAGE_M

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED1	Link Partner Unformatted Code Field 1.	0x0	R

BASE-T1 Autonegotiation Link Partner Next Page Ability [47:32] Register

Device Address: 0x07; Register Address: 0x020D, Reset: 0x0000, Name: AN_LP_NEXT_PAGE_H

This address corresponds to the BASE-T1 autonegotiation link partner's next page ability register [47:32] specified in Clause 45.2.7.24 of Standard 802.3. The values of this register are latched when AN_LP_NEXT_PAGE_L is read. Reading this register returns the latched value rather than the current value.

Table 123. Bit Descriptions for AN_LP_NEXT_PAGE_H

Bits	Bit Name	Description	Reset	Access
[15:0]	AN_LP_NP_UNFORMATTED2	Link Partner Unformatted Code Field 2.	0x0	R

Extra Autonegotiation Status Register

Device Address: 0x07; Register Address: 0x8001, Reset: 0x0000, Name: AN_STATUS_EXTRA

Provided in addition to AN_STATUS

Table 124. Bit Descriptions for AN_STATUS_EXTRA

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
8	AN_LP_NP_RX	Next Page Request Received from Link Partner.	0x0	R LH
7	AN_INC_LINK	Incompatible Link Indication. This corresponds to the state incompatible_link of IEEE Std 802.3 subclause 98.5.1. Its value is set by the Priority Resolution function run on entering the AN GOOD CHECK state.	0x0	R

Bits	Bit Name	Description	Reset	Access
[6:5]	AN_MS_CONFIG_RSLTN	Master/slave Resolution Result. Determined as per Table 98-4 - master-slave Configuration of IEEE Std 802.3. This is encoded as follows: 0: Not run. 1: Configuration fault. 2: Success, PHY is configured as SLAVE. 3: Success, PHY is configured as MASTER.	0x0	R
[4:1]	AN_HCD_TECH	Highest Common Denominator (HCD) PHY Technology. As selected by the Priority Resolution function of IEEE Std 802.3 subclause 98.2.4.2. Values other than those shown below should be considered reserved. 0: NULL (not run). 1: 10BASE-T1L.	0x0	R
0	AN_LINK_GOOD	Autonegotiation Complete Indication. This corresponds to the state an_link_good of IEEE Std 802.3 subclause 98.5.1. This signal indicates completion of the autonegotiation transmission, and that the enabled PHY technology is either bringing up its link, or that it has brought up its link. See also AN_COMPLETE, which is similar, but also indicates that PHY link is up.	0x0	R

Vendor Specific MMD 1 Device Identifier High Register

Device Address: 0x1E; Register Address: 0x0002, Reset: 0x0283, Name: MMD1_DEV_ID1

This address corresponds to the vendor specific MMD 1 device identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows 16 bits of the organizationally unique identifier (OUI) to be observed.

Table 125. Bit Descriptions for MMD1_DEV_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	MMD1_DEV_ID1	Organizationally Unique Identifier. Bits[3:18]	0x283	R

Vendor Specific MMD 1 Device Identifier Low Register

Device Address: 0x1E; Register Address: 0x0003, Reset: 0xBC00, Name: MMD1_DEV_ID2

This address corresponds to the vendor specific MMD 1 device identifier register specified in Clause 45.2.11.1 of Standard 802.3 and allows 6 bits of the OUI along with the model number and revision number to be observed.

Table 126. Bit Descriptions for MMD1_DEV_ID2

Bits	Bit Name	Description	Reset	Access
[15:10]	MMD1_DEV_ID2_OUI	Organizationally Unique Identifier. Bits[19:24]	0x2F	R
[9:4]	MMD1_MODEL_NUM	Model Number.	0x9	R
[3:0]	MMD1_REV_NUM	Revision Number.	0x0	R

System Interrupt Status Register

Device Address: 0x1E; Register Address: 0x0010, Reset: 0x0800, Name: CRSM_IRQ_STATUS

This address may be used to check which interrupt requests have been triggered since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of CRSM_IRQ_STATUS go high even when the associated interrupts are not enabled. A reserved interrupt being triggered indicates a fatal error in the system.

Table 127. Bit Descriptions for CRSM_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_LH	Software Requested Interrupt Event.	0x0	R LH
[14:12]	RESERVED	Reserved.	0x0	R
11	CRSM_HRD_RST_IRQ_LH	Hardware Reset Interrupt.	0x1	R LH
[10:0]	RESERVED	Reserved.	0x0	R LH

PHY Subsystem Interrupt Status Register

Device Address: 0x1E; Register Address: 0x0011, Reset: 0x0000, Name: PHY_SUBSYS_IRQ_STATUS

This address may be read to check which interrupt events have occurred since the last time it was read. Each bit goes high when the associated event occurs and then latches high until it is unlatched by reading. The bits of PHY_SUBSYS_IRQ_STATUS go high even when the associated bits in PHY_SUBSYS_IRQ_MASK are not set. A reserved interrupt being triggered indicates a fatal error in the system.

Table 128. Bit Descriptions for PHY_SUBSYS_IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R LH
14	MAC_IF_FC_FG_IRQ_LH	Mac Interface Frame Checker/Generator Interrupt.	0x0	R LH
13	MAC_IF_EBUF_ERR_IRQ_LH	Mac Interface Buffers Overflow/underflow Interrupt.	0x0	R LH
12	RESERVED	Reserved.	0x0	R LH
11	AN_STAT_CHNG_IRQ_LH	Autonegotiation Status Change Interrupt.	0x0	R LH
[10:2]	RESERVED	Reserved.	0x0	R LH
1	LINK_STAT_CHNG_LH	Link Status Change.	0x0	R LH
0	RESERVED	Reserved.	0x0	R LH

System Interrupt Mask Register

Device Address: 0x1E; Register Address: 0x0020, Reset: 0x0FFF, Name: CRSM_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 129. Bit Descriptions for CRSM_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	CRSM_SW_IRQ_REQ	Software Interrupt Request. Software can set this bit to generate an interrupt for system level testing. This bit always reads as zero as it is self-clearing.	0x0	R/W SC
[14:12]	RESERVED	Reserved.	0x0	R
11	CRSM_HRD_RST_IRQ_EN	Enable Hardware Reset Interrupt. Note that writing a 0 to this register does not mask the interrupt since this register is initialized when a hardware reset occurs.	0x1	R/W
[10:0]	RESERVED	Reserved.	0x7FF	R/W

PHY Subsystem Interrupt Mask Register

Device Address: 0x1E; Register Address: 0x0021, Reset: 0x2403, Name: PHY_SUBSYS_IRQ_MASK

Controls whether or not the interrupt signal is asserted in response to various events.

Table 130. Bit Descriptions for PHY_SUBSYS_IRQ_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R/W SC
14	MAC_IF_FC_FG_IRQ_EN	Enable Mac Interface Frame Checker/Generator Interrupt.	0x0	R/W
13	MAC_IF_EBUF_ERR_IRQ_EN	Enable Mac Interface Buffers Overflow/underflow Interrupt.	0x1	R/W
12	RESERVED	Reserved.	0x0	R/W
11	AN_STAT_CHNG_IRQ_EN	Enable Autonegotiation Status Change Interrupt.	0x0	R/W
[10:2]	RESERVED	Reserved.	0x100	R/W
1	LINK_STAT_CHNG_IRQ_EN	Enable Link Status Change Interrupt.	0x1	R/W
0	RESERVED	Reserved.	0x1	R/W

Frame Checker Enable Register

Device Address: 0x1E; Register Address: 0x8001, Reset: 0x0001, Name: FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the FC_TX_SEL register) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 131. Bit Descriptions for FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_EN	Frame Checker Enable. Set to 1'b1 to enable the frame checker	0x1	R/W

Frame Checker Interrupt Enable Register

Device Address: 0x1E; Register Address: 0x8004, Reset: 0x0001, Name: FC_IRQ_EN

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register.

Table 132. Bit Descriptions for FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_IRQ_EN	Frame Checker Interrupt Enable. When set, this bit enables the frame checker interrupt.	0x1	R/W

Frame Checker Transmit Select Register

Device Address: 0x1E; Register Address: 0x8005, Reset: 0x0000, Name: FC_TX_SEL

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received from the MAC interface to be transmitted are checked. The frame checker can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (see the MAC_IF_REM_LB_EN bit in the MAC_IF_LOOPBACK register) because it can be used to check the received data after it is looped back at the MAC interface.

Table 133. Bit Descriptions for FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_TX_SEL	Frame Checker Transmit Select. When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

Receive Error Count Register

Device Address: 0x1E; Register Address: 0x8008, Reset: 0x0000, Name: RX_ERR_CNT

The receive error counter register is used to access the receive error counter associated with the frame checker in the PHY

Table 134. Bit Descriptions for RX_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	RX_ERR_CNT	Receive Error Count. This is the receive error counter associated with the frame checker in the PHY. Note that this bit is self clearing upon reading.	0x0	R SC

Frame Checker Count High Register

Device Address: 0x1E; Register Address: 0x8009, Reset: 0x0000, Name: FC_FRM_CNT_H

This register is a latched copy of Bits [31:16] of the 32-bit of the receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and the receive frame count are synchronized.

Table 135. Bit Descriptions for FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_H	Bits [31:16] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Count Low Register

Device Address: 0x1E; Register Address: 0x800A, Reset: 0x0000, Name: FC_FRM_CNT_L

This register is a latched copy of Bits [15:0] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT) is read, the receive frame counter register is latched so that the error count and receive frame count are synchronized.

Table 136. Bit Descriptions for FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_L	Bits [15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Length Error Count Register

Device Address: 0x1E; Register Address: 0x800B, Reset: 0x0000, Name: FC_LEN_ERR_CNT

This register is a latched copy of the frame length error counter register. This register is a count of received frames with a length error status. When the receive error counter (RX_ERR_CNT) is read, the frame length error counter register is latched, which ensures that the frame length error count and receive frame count are synchronized

Table 137. Bit Descriptions for FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter.	0x0	R

Frame Checker Alignment Error Count Register

Device Address: 0x1E; Register Address: 0x800C, Reset: 0x0000, Name: FC_ALGN_ERR_CNT

This register is a latched copy of the frame alignment error counter register. This register is a count of received frames with an alignment error status. When the receive error counter (RX_ERR_CNT) is read, the alignment error counter is latched, which ensures that the frame alignment error count and the receive frame count are synchronized.

Table 138. Bit Descriptions for FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Count Register

Device Address: 0x1E; Register Address: 0x800D, Reset: 0x0000, Name: FC_SYMB_ERR_CNT

This register is a latched copy of the symbol error counter register. This register is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RX_ERR_CNT) is read, the symbol error count is latched, which ensures that the symbol error count and the frame receive count are synchronized.

Table 139. Bit Descriptions for FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_SYMB_ERR_CNT	Latched Copy of the Symbol Error Counter.	0x0	R

Frame Checker Oversized Frame Count Register

Device Address: 0x1E; Register Address: 0x800E, Reset: 0x0000, Name: FC_OSZ_CNT

This register is a latched copy of the oversized frame error counter register. This register is a count of receiver frames with a length greater than specified in frame checker maximum frame size (FC_MAX_FRM_SIZE). When the receive error counter (RX_ERR_CNT) is read, the oversized frame counter register is latched, which ensures that the oversized error count and the receive frame count are synchronized.

Table 140. Bit Descriptions for FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_OSZ_CNT	Latched copy of the Overisized Frame Error Counter.	0x0	R

Frame Checker Undersized Frame Count Register

Device Address: 0x1E; Register Address: 0x800F, Reset: 0x0000, Name: FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with less than 64 bytes. When the receive error counter (RX_ERR_CNT) is read, the undersized frame error counter is latched, which ensures that the undersized frame error count and the receive frame count are synchronized.

Table 141. Bit Descriptions for FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter.	0x0	R

Frame Checker Odd Nibble Frame Count Register

Device Address: 0x1E; Register Address: 0x8010, Reset: 0x0000, Name: FC_ODD_CNT

This register is a latched copy of the odd nibble frame register. This register is a count of received frames with an odd number of frames in the frame. When the receive error counter (RX_ERR_CNT) is read, the odd nibble frame counter register is latched, which ensures that the odd nibble frame count and the receive frame count are synchronized.

Table 142. Bit Descriptions for FC_ODD_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_CNT	Latched Copy of the Odd Nibble Counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Device Address: 0x1E; Register Address: 0x8011, Reset: 0x0000, Name: FC_ODD_PRE_CNT

This register is a latched copy of the odd preamble packet counter register. This register is a count of received packets with an odd number of nibbles in the preamble. When the receive error counter (RX_ERR_CNT) is read, the odd preamble packet counter register is latched, which ensures that the odd preamble packet count and the receive frame count are synchronized.

Table 143. Bit Descriptions for FC_ODD_PRE_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_PRE_CNT	Latched Copy of the Odd Preamble Packet Counter.	0x0	R

Frame Checker False Carrier Count Register

Device Address: 0x1E; Register Address: 0x8013, Reset: 0x0000, Name: FC_FALSE_CARRIER_CNT

This register is a latched copy of the false carrier events counter register. This is a count of the number of times the BAD SSD state is entered. When the receive error counter (RX_CNT_ERR) is read, the false carrier events counter register is latched, which ensures that the false carrier events count and the receive frame count are synchronized.

Table 144. Bit Descriptions for FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

Frame Generator Enable Register

Device Address: 0x1E; Register Address: 0x8015, Reset: 0x0000, Name: FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled (DIAG_CLK_EN)

Table 145. Bit Descriptions for FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_EN	Frame Generator Enable.	0x0	R/W

Frame Generator Control/Restart Register

Device Address: 0x1E; Register Address: 0x8016, Reset: 0x0001, Name: FG_CNTRL_RSTRT

This register controls the frame generator. The FG_CNTRL bitfield specifies data field type used by the frame generator, e.g. random, all zeros, etc. The FG_RSTRT bit restarts the frame generator.

Table 146. Bit Descriptions for FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FG_RSTRT	Frame Generator Restart. When set, this bit restarts the frame generator. This bit is self-clearing	0x0	R/W SC
[2:0]	FG_CNTRL	Frame Generator Control. 000: No frames after completion of current frame 001: Random number data frame 010: All zeros data frame 011: All ones data frame 100: Alternative 0x55 data field 101: Data field decrementing from 255 (decimal) to 0	0x1	R/W

Frame Generator Continuous Mode Enable Register

Device Address: 0x1E; Register Address: 0x8017, Reset: 0x0000, Name: FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FG_NFRM_H and FG_NFRM_L registers.

Table 147. Bit Descriptions for FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_CONT_MODE_EN	This bit is used to put the frame generator into continuous mode or burst mode. 1: Frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: Frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames is determined by the FG_NFRM_H and FG_NFRM_L registers.	0x0	R/W

Frame Generator Interrupt Enable Register

Device Address: 0x1E; Register Address: 0x8018, Reset: 0x0000, Name: FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the PHY_SUBSYS_IRQ_MASK register. Set the MAC_IF_FC_FG_IRQ_EN bit.

The interrupt status can be read via the MAC_IF_FC_FG_IRQ_LH bit in the PHY_SUBSYS_IRQ_STATUS register

Table 148. Bit Descriptions for FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_IRQ_EN	Frame Generator Interrupt Enable. When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

Frame Generator Frame Length Register

Device Address: 0x1E; Register Address: 0x801A, Reset: 0x006B, Name: FG_FRM_LEN

This register specifies the data field frame length in bytes. In addition to the data field, 6 bytes are added for the source address, 6 bytes for the destination address, 2 bytes for the length field, and 4 bytes for the frame check sequence (FCS). The total length is the data field length plus 18.

Table 149. Bit Descriptions for FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

Frame Generator Number of Frames High Register

Device Address: 0x1E; Register Address: 0x801C, Reset: 0x0000, Name: FG_NFRM_H

This register is Bits [31:16] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 150. Bit Descriptions for FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_H	Bits [31:16] of the Number of Frames to be Generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Device Address: 0x1E; Register Address: 0x801D, Reset: 0x0100, Name: FG_NFRM_L

This register is Bits [15:0] of a 32-bit register that specifies the number of frames to be generated each time the frame generator is enabled or restarted.

Table 151. Bit Descriptions for FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_L	Bits [15:0] of the Number of Frames to be Generated.	0x100	R/W

Frame Generator Done Register

Device Address: 0x1E; Register Address: 0x801E, Reset: 0x0000, Name: FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FG_NFRM_H and FG_NFRM_L registers.

Table 152. Bit Descriptions for FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_DONE	Frame Generator Done. This bit reads as 1'b1 to indicate that the generation of frames has completed. When set, this bit goes high and it latches high until its unlatched by reading.	0x0	R LH

MAC Interface Loopbacks Configuration Register

Device Address: 0x1E; Register Address: 0x803D, Reset: 0x000A, Name: MAC_IF_LOOPBACK

MAC interface loopbacks configuration

Table 153. Bit Descriptions for MAC_IF_LOOPBACK

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	MAC_IF_REM_LB_RX_SUP_EN	Suppress RX Enable. Suppress RX to the MAC when MAC_IF_REM_LB_EN is set	0x1	R/W
2	MAC_IF_REM_LB_EN	MAC Interface Remote Loopback Enable. RX data is looped back to TX	0x0	R/W
1	MAC_IF_LB_TX_SUP_EN	Suppress Transmission Enable. Suppress transmission to the PHY when MAC_IF_LB_EN is set	0x1	R/W
0	MAC_IF_LB_EN	MAC Interface Loopback Enable. TX data is looped back to RX	0x0	R/W

Software Reset Register

Device Address: 0x1E; Register Address: 0x8810, Reset: 0x0000, Name: CRSM_SFT_RST

Table 154. Bit Descriptions for CRSM_SFT_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_RST	Software Reset Register. The software reset bit allows the chip to be reset. When this bit is set, a full initialization of the chip, almost equivalent to a hardware reset, is done.	0x0	R/W SC

Software Power-down Control Register

Device Address: 0x1E; Register Address: 0x8812, Reset: 0x0000, Name: CRSM_SFT_PD_CNTRL

Table 155. Bit Descriptions for CRSM_SFT_PD_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_SFT_PD	Software Power-down. The software power-down register puts the chip in a lower power mode. In this mode most of the circuitry is switched off. However, MDIO access to all registers is still possible. The default value for this register is configurable via a pin. This allows the chip to be held in power-down mode until an appropriate software initialization has been performed.	Pin Dependent	R/W

PHY Subsystem Reset Register

Device Address: 0x1E; Register Address: 0x8814, Reset: 0x0000, Name: CRSM_PHY_SUBSYS_RST

Table 156. Bit Descriptions for CRSM_PHY_SUBSYS_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_PHY_SUBSYS_RST	PHY Subsystem Reset. The PHY subsystem reset register allows a managed subsystem reset to be initiated. When the PHY subsystem is reset, normal operation resumes, and the bit is self-cleared.	0x0	R/W SC

PHY MAC Interface Reset Register

Device Address: 0x1E; Register Address: 0x8815, Reset: 0x0000, Name: CRSM_MAC_IF_RST

Table 157. Bit Descriptions for CRSM_MAC_IF_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CRSM_MAC_IF_RST	PHY MAC Interface Reset. The PHY MAC interface reset register allows a managed PHY MAC interface reset to be initiated. When the PHY MAC interface is reset, normal operation resumes, and the bit is self-cleared.	0x0	R/W SC

System Status Register

Device Address: 0x1E; Register Address: 0x8818, Reset: 0x0000, Name: CRSM_STAT

Table 158. Bit Descriptions for CRSM_STAT

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	CRSM_SFT_PD_RDY	Software Power-down Status. This bit indicates that the system is in the software power-down state.	0x0	R
0	CRSM_SYS_RDY	System Ready. This bit indicates that the start-up sequence is complete and the system is ready for normal operation.	0x0	R

CRSM Diagnostics Clock Control Register

Device Address: 0x1E; Register Address: 0x882C, Reset: 0x0002, Name: CRSM_DIAG_CLK_CTRL

CRSM Diagnostics clock control.

Table 159. Bit Descriptions for CRSM_DIAG_CLK_CTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x1	R
0	CRSM_DIAG_CLK_EN	Enable the Diagnostics Clock.	0x0	R/W

LED Control Register

Device Address: 0x1E; Register Address: 0x8C81, Reset: 0x0000, Name: LED_CNTRL

LED control register

Table 160. Bit Descriptions for LED_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	LED_EN	LED Enable. When this bit is 1'b1 the LED is enabled. Otherwise, the LED is disabled.	0x0	R/W

PCB LAYOUT RECOMMENDATIONS

This is an overview of the key areas of interest during placement and layout of the PHY and corresponding support components.

PHY PACKAGE LAYOUT

The LFCSP has an exposed pad underneath the package that must be soldered to the PCB ground for mechanical, electrical and thermal reasons. For thermal impedance performance and to maximize heat removal, use of a 4 × 4 array of thermal vias beneath the exposed ground pad is recommended. The PCB land pattern must incorporate the exposed ground paddle with these vias in the footprint. The EVAL-ADIN1110EBZ uses an array of 4 × 4 filled vias on a 1.00 mm grid arrangement. The via pad diameter dimension is 0.02 in. (0.5015 mm).

COMPONENT PLACEMENT

Prioritization of the critical traces and components helps simplify the routing exercise. Place and orient the critical traces and components first to ensure an effective layout with minimal turns, vias, and crossing traces. For an 10BASE-T1L PHY layout, the important components are the crystal and load capacitors, the CEXT_1, CEXT_2, CEXT_3 and CEXT_4 capacitors as well as all bypass capacitors local to the ADIN1110 device. Prioritize these components and the routing to them. Keeping the MDI traces (RXP, RXN, TXP and TXN) closest to the ADIN110 as short as possible is also important.

Crystal Placement and Routing

To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1110 as possible.

OUTLINE DIMENSIONS

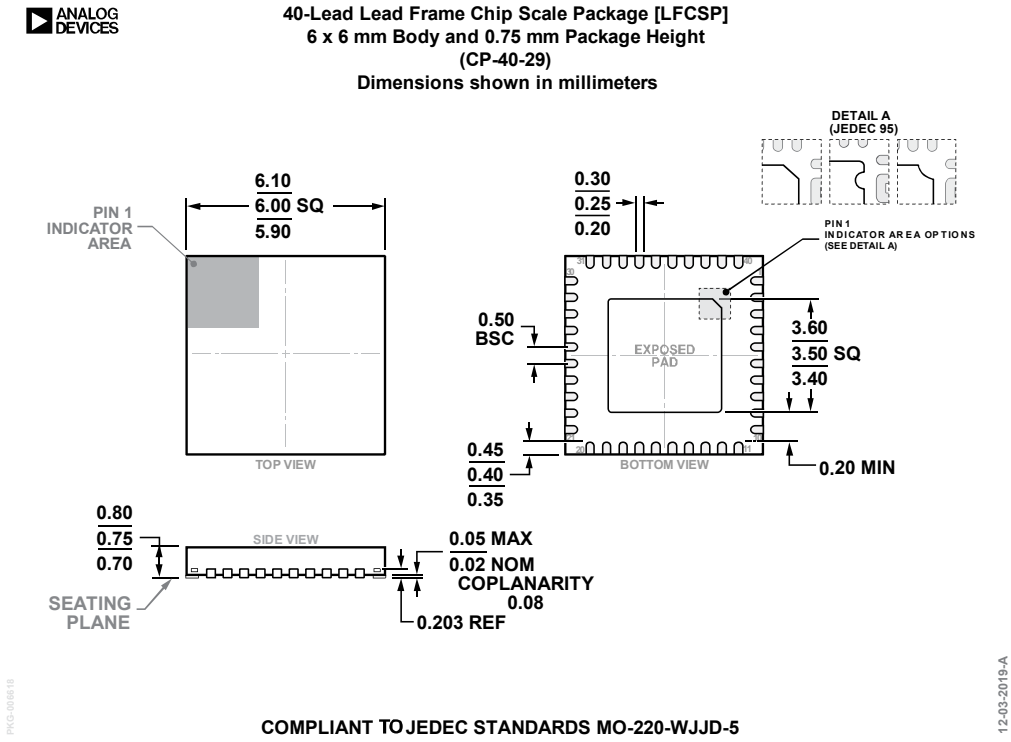


Figure 14. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm x 6 mm Body and 0.75 mm Package Height
(CP-40-29).
Dimensions shown in millimeters

PR26155-2/21(PrA)