

Evaluation Boards for ADF7023 ISM Band Transceiver EVAL-ADF7023DBxZ

Features

Frequency bands
862 MHz to 928 MHz
431 MHz to 464 MHz
Programmable datarates and modulation
1 kbps to 300 kbps
FSK/GFSK/OOK/MSK/GMSK modulation
Very low power consumption
12.8 mA in PHY_RX mode (maximum front-end gain)
24.1 mA in PHY_TX mode (10 dBm output, single-ended PA)
0.75 μA in PHY_SLEEP mode (32 kHz RC oscillator active)
1.28 μA in PHY_SLEEP mode (32 kHz XTAL oscillator active)
0.33 μA in PHY_SLEEP mode (Deep Sleep Mode 1)
High Sensitivity
Programmable output power
–20 dBm to +13.5 dBm (single-ended PA)
–20 dBm to +10 dBm (differential PA)
Excellent receiver selectivity and blocker resilience

General Description

The ADF7023 is a very low power, high performance, highly integrated 2FSK/GFSK/OOK/MSK/GMSK transceiver designed for operation in the 862 MHz to 928 MHz and 431 MHz to 464 MHz frequency bands, which cover the worldwide licensefree ISM bands at 433 MHz, 868 MHz, and 915 MHz. It is suitable for circuit applications that operate under the European ETSI EN300-220, the North American FCC (Part 15), the Chinese short-range wireless regulatory standards, or other similar regional standards.

The ADF7023 evaluation platform consists of a 4-layer PCB daughter card which plugs into the Eval-ADF7xxxMB3Z motherboard.

Board Number RF Frequency Description EVAL-ADF7XXXMBZ3 Mother board required for evaluation of the ADF7023 daughter boards Eval-ADF7023DB1Z 868/915 MHz Two separate matching networks: One for the single ended PA and one for the LNA Eval-ADF7023DB2Z 868/915 MHz One combined matching network incorporating the single ended PA and LNA Eval-ADF7023DB3Z 433 MHz Two separate matching networks: One for the single ended PA and one for the LNA Eval-ADF7023DB4Z 433 MHz One combined matching network incorporating the single ended PA and LNA

Table 1 Evaluation Boards

TABLE OF CONTENTS

Features
General Description
Revision History
Hardware Overview
Getting Started
Installing Software4
Mother Board Firmware Version
Basic RF testing in SPORT Mode
Entering PHY_TX for basic RF Carrier testing
Entering PHY_TX for basic RF Data testing21
Simple Rx / Tx Test in Packet Mode
Rx Setup in Packet Mode
Tx Setup in Packet Mode27
Reading Interrupt Source on Transmitter board
Reading Interrupt Source on Receiver board
Running a Packet Error Rate Test
Running a Script
ADF7023 Evaluation Board Schematics and BOMs
Eval-ADF7XXXMB3Z Mother Board Schematics and Silk Screen

Revision History

Date: April 18th 2013 Revision: Rev. 1.1

This document accompanies:

ADF7023 software release 1.5.4 Daughter boards using the layout files ADF702xDBExZ RevB and ADF702xDBFxZ RevB Mother board version EVAL-ADF7XXX_MB3Z RevB running firmware version 2.0.2.3 or higher

Hardware Overview

The Evaluation Platform consists of the Eval-ADF7XXXMB3Z mother board to which an appropriate daughter card may be connected. The available daughter cards are given in Table 1. Schematics for the daughter cards are given in the *ADF7023 Evaluation Board Schematics and BOMs* section of this document.

The mother board may be powered via the USB cable supplied. The 5V from the USB cable is regulated down to 3.3 V for the Cypress EZ USB IC, the ADuC7020 microcontroller and the ADF7023 transceiver. Alternatively a battery may be used to power the microcontroller and transceiver. A 3.6V battery is shipped with the boards.



Hardware Overview

Getting Started

Installing Software

The ADF7023 evaluation software and documentation can be installed from the Analog Devices ftp site.

(ftp.analog.com/pub/RFL/ADF7023)

The software installation should be carried out before plugging in the ADF7023 Evaluation Boards.

Installation Procedure

- Run ADF7023 Rev1.5.4 FULL.exe to install the evaluation software for the ADF7023. The install will place the relevant files in the folder C:\Program Files\Analog Devices BV\ADF7023. It will also create shortcuts on the start menu. Any previous versions of the software will be removed before the installation commences (Figure 1).
- 2.





3. Click on "Yes" to install the software (Figure 2).





4. Click "*Next*" (Figure 3):



Figure 3

5. Click "*Next*" (Figure 4):

# ADF7023 Evaluation Software Rev 1.5.4	
Destination Directory Select the primary installation directory.	
All software will be installed in the following location(s). To install software into a different location(s), click the Browse button and select another directory.	
Directory for ADF7023 Evaluation Software Rev 1.5.4 C:\Program Files\Analog Devices BV\ADF7023\ Browse	
C Back Next >>	Cancel

Figure 4

6. Click "I accept this license Agreement"

Then Click " <i>Next</i> " (Figure 5):		
🖏 ADF7023 Evaluation Software Rev 1.4.4		
License Agreement You must accept the license(s) displayed below to proceed.		
NATIONAL INSTRUMENTS SOFTWARE LI		
INSTALLATION NOTICE: THIS IS A CONTRACT. BEFORE YOU DOW AND/OR COMPLETE THE INSTALLATION PROCESS, CAREFULLY DOWNLOADING THE SOFTWARE AND/OR CLICKING THE APPLIC COMPLETE THE INSTALLATION PROCESS, YOU CONSENT TO TH AGREEMENT AND YOU AGREE TO BE BOUND BY THIS AGREEME BECOME A PARTY TO THIS AGREEMENT AND BE BOUND BY ALL CONDITIONS, CLICK THE APPROPRIATE BUTTON TO CANCEL TH DO NOT INSTALL OR USE THE SOFTWARE, AND RETURN THES (30) DAYS OF RECEIPT OF THE SOFTWARE (WITH ALL ACCOMPA ALONG WITH THEIR CONTAINERS) TO THE PLACE YOU OBTAINE SHALL BE SUBJECT TO NI'S THEN CURRENT RETURN POLICY.	WNLOAD THE SOFTWARE READ THIS AGREEMENT. BY CABLE BUTTON TO HE TERMS OF THIS ENT. IF YOU DO NOT WISH TO OF ITS TERMS AND HE INSTALLATION PROCESS, OFTWARE WITHIN THIRTY ANYING WRITTEN MATERIALS, ED THEM. ALL RETURNS	
 I accept the 	License Agreement.	
O I do not acc	ept the License Agreement.	
< Back	Next >> Cancel	

Figure 5

7. Click "*Next*" (Figure 6):

W ADF7023 Evaluation Software Rev 1.5.4	
Start Installation Review the following summary before continuing.	
Adding or Changing • ADF7023 Evaluation Software Rev 1.5.4 Files	
Click the Next button to begin installation. Click the back button to change the installation settings.	
Save File) << Back Next >>	Cancel

Figure 6

8. Click "*Next*" (Figure 7):

ADF7023 Evaluation Software Rev 1.5.4			
Installation Complete			
The installer has finished updating your system.			
	<< <u>B</u> ack	<u>N</u> ext >>	<u>F</u> inish

Figure 7

9. Click "*Next*" (Figure 8):

😽 ADF7xMB3 Drivers Insta	ıll 3.4. 2.0 Setup
ADT /XMD3 DITVETS INSIG	Welcome to the ADF7xMB3 Drivers Install 3.4.2.0 Setup Wizard This wizard will guide you through the installation of ADF7xMB3 Drivers Install 3.4.2.0. It is recommended that you close all other applications before starting Setup. This will make it possible to update relevant system files without having to reboot your computer. Click Next to continue.
	Next > Cancel

Figure 8

10. Click "*Next*" (Figure 9):

🗟 ADF7xMB3 Drivers Install 3.4.2.0 Setup	×
Choose Install Location Choose the folder in which to install ADF7xMB3 Drivers Install 3.4.2.0.	
Setup will install ADF7xMB3 Drivers Install 3.4.2.0 in the following folder. To install in a different folder, click Browse and select another folder. Click Install to start the installation.	
Destination Folder C:\Program Files\Analog Devices\ADF7x_MB3 32\Drivers Browse	
Space required: 2.5MB Space available: 42.3GB	
Nullsoft Install System v2.46	

Figure 9

11. Click "*Next*" (Figure 10):

😽 ADF7xMB3 Drivers Insta	all 3.4.2.0 Setup
	Completing the ADF7xMB3 Drivers Install 3.4.2.0 Setup Wizard ADF7xMB3 Drivers Install 3.4.2.0 has been installed on your computer. Click Finish to close this wizard.
< <u>B</u> ack <u>Finish</u> Cancel	
Figure 10	

12. At this point the ADF7xxxMB3Z Motherboard can be plugged into a free USB port.

13. The following screen will appear:

Ensure the "Install the software automatically" option is checked as in Figure 11. Then click "*Next*":

Found New Hardware Wizard	
	Welcome to the Found New Hardware Wizard
	This wizard helps you install software for:
	ADF7XXXMBZ3 Board #2
	If your hardware came with an installation CD or floppy disk, insert it now.
	What do you want the wizard to do?
	 Install the software automatically (Recommended) Install from a list or specific location (Advanced)
	Click Next to continue.
	< Back Next > Cancel

Figure 11

14. Click "Continue Anyway" (

ick " Contin	uue Anyway" (Figure 12):
lardware	e Installation
<u>.</u>	The software you are installing for this hardware: ADF7XXXMBZ3 Board #2 has not passed Windows Logo testing to verify its compatibility with Windows XP. (Tell me why this testing is important.) Continuing your installation of this software may impair or destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware vendor for software that has passed Windows Logo testing.
	Continue Anyway

Figure 12

15. Click "Finish" (Figure 13):

Found New Hardware Wizard	
	Completing the Found New Hardware Wizard The wizard has finished installing the software for: ADF7XXXMBZ3 Board #2
	Click Finish to close the wizard.
	< Back Finish Cancel

Figure 13

Connecting the Evaluation Boards

This software can allow **TWO** evaluation boards to be connected to a single PC. The EVAL board and the software must be setup accordingly.

Ensure that Switch 4 is in the correct position before connecting to the PC as shown in Figure 14.





- To set the first board as "BOARD 1" (Figure 15) on the Software set the switch shown in Figure 14 to "B1"
- To set the second board as "BOARD 2" (Figure 15) on the Software set the switch shown in Figure 14 to "B2"

Ensure the evaluation mother board with the desired daughter card is connected to the PC via USB cable before running the software.

Run the ADF7023 software from Start-> Programs->Analog Devices->ADF7xxx->ADF7023.

Once the software is running press Connect USB (Figure 16).



Figure 15

Using the Evaluation Software



Figure 16

Wait until the BUSY signal above the Connect USB button is turned off before pressing any further buttons on the software interface.

The Firmware for the motherboard is automatically checked each time the software is loaded to ensure the revisions are kept up to date.

If the firmware is out of date the following message will pop up (Figure 17):

D.	×
The Firmware Revision on this board is out of date Do you want to update this Firmware?	
Yes No	

Figure 17

To go through the update procedure, refer to the *Mother Board Firmware Update* section.

Next enter state PHY_ON by pressing the command CMD_PHY_ON.



This can be done by pressing Button A or Button B (Figure 18).

Figure 18

The current status of the ADF7023 will be reflected by the color of the buttons on the "Commands" tab.



Note: If at any time it is desired to unplug the USB cable, click "*Disconnect USB*" first (Figure 19).

Figure 19

Mother Board Firmware Version

The Motherboard firmware revision check is done automatically when "Connect USB" is clicked. If the firmware revision is not correct a popup screen will appear asking the user to update the Firmware (Figure 20).

The Firmware Revision on this board is out of date. Do you want to update this Firmware?
Yes No



To manually check the firmware after connecting the USB select <u>Help</u> -> <u>Check Firmware Revision</u> as shown in

Figure 21Error! Reference source not found..

If this value is less than 02.00.02.05 then the firmware version will need to be updated.

Firmware update procedure can be found in the *Mother Board Firmware Update* section.

Tools Help		-							
Check Firmw SW Rev 1.5	vare Revision .4		PI	aressa	USP	*	32-		MEMS
	Commands	RF Settings	Tx/Rx Packet	Interrupts	Register \	/iew	Memory Check	PER	
	P Firmwa	re Revision	Readback.vi						Z
Disconnect USB									
Board Board 1						C		1	
Launch USB		F	irmware	Revision	Code	02.	00.02.05		
Status				Major Re	vision	02			
Status B1				Minor Re	vision	00			
spi_ready					REV	02			
irq_status 🔘				In	ternal	05			
cmd_ready 🔵							÷		

Figure 21

Mother Board Firmware Update

- 1. Before beginning this procedure ensure ONLY the board you wish to update the firmware on is connected to the PC.
- 2. To update the firmware select "*Tools*" -> "*Motherboard Firmware Download*" (Figure 22).



3. Select the desired firmware version "*EVAL_ADF7XXXMB3Z_Rev_2.0.2.5.hex*" from the default directory (Figure 23).

12C_Downloader_Vi.vi	
File	
Source Directory g C:\Program Files\Analog Devices BV\ADF7xxxMB3z Firmware\ EVAL_ADF70xxMB23_Rev2.0.2.3hex	
Download Firmware	

Figure 23

4. Click "*Download Firmware*" and follow the onscreen instructions (Figure 24).

🛿 12C_Downloader_Vi.vi
File
Source Directory
C:\Program Files\Analog Devices BV\ADF7xxxMB3z Firmware\
Download Firmware

Figure 24

5. "*SER DLOAD* and "*RESET*" buttons will be referenced and can be found as shown in Figure 25.



Figure 25

- 6. Disconnect and then reconnect the USB cable from the evaluation platform.
- 7. The mother board firmware is now updated.

Basic RF testing in SPORT Mode

- 1. Select the "<u>RF Settings</u>" Tab and set the RF parameters as required. (Figure 26 point(<u>1</u>))
- 2. If not already in *PHY_ON* enter this state by pressing *CMD_PHY_ON*. (*Figure 26 point* (<u>5</u>))
- 3. Select the SPORT Mode (Figure 26 point (2))
- Press *Update Needed*. This writes the settings to BBRAM and then does a CMD_CONFIG_DEV. (*Figure 26 point* (<u>3</u>))
- 5. Press CMD_PHY_RX. The part now enters PHY_RX. (Figure 26 point (4))
- 6. To exit <u>PHY_RX</u> press <u>CMD_PHY_ON</u> (Figure 26 point (<u>5</u>))

angenfie	
Connect USB	Commands RF Settings Tx/Rx Packet Interrupts Register View Memory Check PER Mode (SPORT Mode (GP0 = RxData, GP1 = DataClk, GP2 = TxData, GP4 = SWD) 2 Specific Standard Image: Specific Standard Image: Specific Standard
ard 1 🛛 💽	Channel Frequency 915.0000 S IF Bandwidth 100kHz V
Monitor us tus B1 rd	Frequency Deviation (kHz) 20.0 Demod Scheme 2FSK/GFSK/MSK/GMSK Tx Test Mode None Deta Rate (kbps) 40.0 AFC Mode Disable Select GPIO None Expected Max RF Free Error (KHz) 50.0 Solo Test Mode Select GPIO
_status _status _t_ready _Get Status	Transmitter AFC Kp 3 Readback Modulation Scheme 2FSK AFC Ki 7 PA Level 15 AGC Mode Free Running
LASH LEDs	PA Ramp 4 codes/bit V PA Select Single ended V PA Select Single ended V External PA enable (ATB3) Readback Readback
	CMD_PHY_OFF 5 CMD_PHY_SLEEP CMD_LIST 3 Current State PHY_OF

Figure 26

- While in *PHY_RX* with SPORT mode enabled, the received data demodulated by the ADF7023 will appear at the **DR** SMA connector on the mother board as shown in *Figure 27*
- A clock synchronized with the demodulated data will appear at the CLK SMA connector as shown in *Figure 27*.



Figure 27

Entering PHY_TX for basic RF Carrier testing

- 1. Select the "<u>*RF Settings*</u>" Tab and set the RF parameters as required. (*Figure 28point* (<u>1</u>)
- 2. Select "*Packet Mode*" (Figure 28point (2))
- 3. Set Tx Test Mode to "*Transmit Carrier*" (*Figure 28point* (<u>3</u>))
- 4. Ensure part is in <u>PHY_ON</u> (Figure 28point (<u>4</u>))
- Press Update Needed. This writes the settings to BBRAM and then does a CMD_CONFIG_DEV (Figure 28point (5))
- 6. Press "<u>CMD PHY TX</u>" to enter transmit mode (continuous carrier transmission) (*Figure 28point* (<u>6</u>))
- 7. To exit <u>PHY TX</u> press <u>CMD PHY ON</u>(Figure 28point (<u>4</u>))

ADF7023 Evaluatio	n Software
File Tools Help	
Amenner	Planen Pl
	Commands RF Settings Tx/Rx Packet Interrupts Register View Memory Check PER
	Mode (Packet Mode (Comms processor handles Tx/R× packets) 2
Connect USB	Specific Standard Vormal Standard
Board Board 1	RF/Modualtion Receiver Test Modes/Debug
Launch USB Monitor	Channel Frequency 915.0000 C Tx Test Mode Transmit Carrier 3
Status B1 Word	Data Rate (kbps) 40.0
spi_ready 💛 irq_status 🌑	Transmitter AFC Kp 3 © Readback
cmd_ready 🔵	Modulation Scheme 2FSK AFC Ki 7 PHY_RX ADC
Get Status	PA Level 15 V AGC Mode Free Running V RSSI LNA
FLASH LEDs	PA Select Single ended TX_auto_turnaround
	RX_auto_turnaround
	External PA enable (ATB3)
	CMD_PHY_OFF 4 CMD_PHY_SLEEP 5
	6 CMD_PHY_ON CMD LIST Update Needed Last Command 0

Figure 28

Entering PHY_TX for basic RF Data testing

- 1. Select the "<u>RF Settings</u>" Tab and set the RF parameters as required. (Figure 29 point (<u>1</u>))
- 2. Select the SPORT Mode . (Figure 29 point (2))
- 3. Ensure part is in <u>PHY_ON</u> (Figure 29 point (<u>4</u>))
- Press *Update Needed*. This writes the settings to BBRAM and then does a CMD_CONFIG_DEV. (*Figure 29 point* (<u>3</u>))
- 5. Press "<u>CMD PHY TX</u>" to enter transmit mode (continuous carrier transmission) (Figure 29 point (<u>5</u>))
- 6. To exit <u>PHY_TX</u> press <u>CMD_PHY_ON</u>(Figure 29 point (<u>4</u>))

Constant of the	Connects DESettings T. JD. Dedict. Takenak. Desidentilis	Marrie Charle DED	www.analog.com/srd
	Commands N Settings TXXX Packet Interrupts Register vie		0
Coppect USB	Specific Standard Normal Standard	(120ata, GFT = 500)	2
ard	RF/ModualtionReceiver		Test Modes/Debug
oard 1 💌	Channel Frequency 915,0000	IF Bandwidth 100kHz 💌	
Monitor	Frequency Deviation (kHz) 20.0 📚 Demod Sch	eme 2FSK/GFSK/MSK/GMSK 💌	Tx Test Mode None
atus B1 ord	Data Rate (kbps) 40.0 📚 AFC M	ode Disable pected Max RF reg Error (KHz) 50.0	Select GPIO None 💌 Test Mode
q_status 🔘	Transmitter	AFC Kb 3 3	Readback
d_ready 🥥	Modulation Scheme 2F5K	AFC Ki 7	PHY RX ADC
Get Status	PA Level 15 AGC Mc	ide Free Running 💌	
	PA Ramp 4 codes/bit Other		RSSI INA
FLASH LEDs	PA Select Single ended	TX_auto_turnaround 🗌 RX_auto_turnaround 🔲	AFC Mixer
	E	External PA enable (ATB3)	Readback
			2

Figure 29

- While in <u>PHY_Tx</u> with SPORT mode enabled, the transmitted data must synchronized with the output clock seen on the **CLK** SMA connector on the mother board as shown in (*Figure 30*)
- The Tx data line, from the users Tx device, should be connected to the **DT** SMA connector as shown in (*Figure 30*).



Figure 30

Simple Rx / Tx Test in Packet Mode

This section gives a brief introduction on how to Transmit and Receive a packet using the ADF7023 Platform.

Rx Setup in Packet Mode

The settings which follow are for use with EVAL-ADF7023DB1z daughter boards. If you are using a different Daughter board, ensure that the frequency is set within the correct range of the board you are using. Please refer to *Table 1 Evaluation Boards* if you are unsure what the frequency range of you board is designed for.

Receiver Board RF Settings

- Ensure the First ADF7023 Daughter board is correctly plugged into the First Mother board and that the "Current_State" is "<u>PHY_ON</u>" on the First instance of the ADF7023 Software. Refer to Connecting the Evaluation Boards for setup procedures.
- 2. Select the "*RF Settings*" Tab (Figure 31 point (<u>1</u>))
- 3. Ensure "Packet mode" is selected. (Figure 31 point (2))
- 4. Set the "*RF/Modulation*" parameters as required. (Figure 31 point (<u>3</u>))
- Set the "*Receiver*" parameters as required. (Figure 31 point (<u>4</u>)) If using AFC ensure the AFC pull in range is set to the desired value. (A value of half the IF bandwidth is recommended.)

🕒 ADF7023 Evaluatio	n Software
File Tools Help	
Amediter	Compande RE Settings Ty/Ry Packet Toterrunk Pencicker View Memory Check RED www.analog.com/srd
	Mode (Packet mode (Comms processor nandles 1x/Rx packets)
Disconnect USB	Specific Standard
Board Board 1	RF/Modualtion Receiver 4 Test Modes/Debug
Monitor	Frequency Deviation (kHz) 20.0 C Demod Scheme 2FSK/GFSK/MSK/GMSK V Tx Test Mode None
Status B2 Word	Data Rate (kbps) 40.0 AFC Mode Disable Select GPIO None Expected Max RF From Ref. (Kbps)
spi_ready 💙	Freq Error (kHz)
cmd_ready	AFC Kp 3 C Readback
Get Status	PA Level 15 C AGC Mode Free Running RSSI LNA
FLASH LEDs	PA Rainp Constraint Other AFC IF Filter
	RX_auto_turnaround
	External PA enable (ATB3)
	CMD_PHY_OFF CMD_PHY_SLEEP CMD LIST Current State PHY_ON
	CMD_PHY_ON Normal Commands Write Settings Last Command B1

Figure 31

Receiver Board Rx Packet Settings

Using the Tx/Rx packet tab you can set up the packet format and configure the packet handler. (Figure 32point (<u>1</u>))

- 1. The transmitted preamble length sync word and CRC can be defined by the user. (Figure 32point (2)) (Note: Ensure CRC is enabled for this test. You have the choice to use the default CRC or enable a programmable CRC whose polynomial may be set in registers 0x11E and 0x11F.)
- Ensure you are using a fixed packet length and that, "*Packet Length Max*" is set equal the payload length. (Figure 32point (<u>3</u>))
- Set up the Rx base address. (Figure 32point (<u>4</u>)) (Note : This is the start address of the received packet in Packet Ram Memory.)
- 4. Write the settings to the device using the "<u>Update Needed</u>" button. (Figure 32point (<u>5</u>))

ADF7023 Evaluation	Software
ile Tools Help	
Amenners	PIOLESCOP CONVERTISE
-	Commands RF Settings Tx/Rx Packet Interrupts Register View Memory Check PER
Disconnect USB Board Board 1	Transmit Packet Format Preamble SWD Payload Data (Enter in Hex) CRC AAAAAAAAAAAAAAAA 123456 0102030405060708090A0B0C0D0E0F10111213141516171819 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
Launch USB Monitor Status	Tx Base Address ×10 Write Payload to RAM SWD/Preamble/CRC Data Coding (Packet Length)
Status B1 Word spi ready	Preamble Length (bytes) 8 CRC Enable Enabled V
irq_status 🔘	Sync Byte (Hex) × 123456 Example CRCs X(16) + X(12) +X(5) + 1 (derault) Sync Byte (Hex) × 123456 Programmable CRC
Get Status	Receive Packet Filtering
FLASH LEDs	Preamble/Sync/CRC Filtering Address Filtering Preamble Match 0 bit errors allowed Sync Error Tolerance 0 bit errors allowed
	CMD_PHY_OFF CMD_PHY_SLEEP CMD LIST 5 Current State PHY_ON CMD_PHY_ON Normal Commands Vpdate Needed Current State PHY_ON
	CMD_PHY_TX CMD_PHY_RX

Figure 32

Receiver Board Interrupts

Interrupts may be configured for various conditions in the "*Interrupts*" tab. (Figure 33 point (<u>1</u>))

- Set the "*crc_correct*" interrupt. (Figure 33 point (<u>2</u>)) This will give an interrupt signal upon reception of a packet with a valid CRC.
- 2. Write the settings to the device using the "*Update Needed*" button. (Figure 33 point (<u>3</u>))
- Put the part into Receive by pressing "<u>CMD_PHY_RX</u>" (Figure 33 point (<u>4</u>)) (Note: Ensure that the current state of the part is in "PHY_ON" before pressing "<u>CMD_PHY_RX</u>".)

"*Board* 1" is now in Receive and waits for a transmitted signal. It will remain in Rx until a valid packet with a valid CRC is received.

ADF7023 Evaluatio	n Software
File Tools Help	
Amenner	
	Commands RF Settings Tx/Rx Packet Interrupts Register View Memory Check PER
Disconnect USB Board Board 1 Launch USB Monitor Status Status Status Status B2 Word spi_ready irq_status cmd_ready	num_wakeups Image: Constraint of the second sec
FLASH LEDs	CMD_PHY_OFF CMD_PHY_SLEEP CMD_LIST Update Needed Current State PHY_ON CMD_PHY_IX CMD_PHY_RX Normal Commands V B1

Figure 33

Tx Setup in Packet Mode

The settings which follow are for use with EVAL-ADF7023DB1z daughter boards. If you are using a different Daughter board, ensure that the frequency is set within the correct range of the board you are using. Please refer to table x if you are unsure what the frequency range of you board is designed for.

Transmitter Board RF Settings

- Ensure the Second ADF7023 Daughter board is correctly plugged into the Second Mother board and that the "Current_State" is "<u>PHY_ON</u>" on the Second instance of the ADF7023 Software. Refer to Connecting the Evaluation Boards section for setup procedures.
- 2. Select the "*RF Settings*" Tab (Figure 34 point (<u>1</u>))
- 3. Ensure "*Packet mode*" is selected. (Figure 34 point (<u>2</u>))
- Set the "*RF/Modulation*" parameters as required. (Figure 34 point (3))
 (Note : Ensure the Transmitter *RF/Modulation* parameters are the same as the Receiver *RF/Modulation* parameters previously setup).

5. Set the Transmitter parameters as required. (Figure 54 point)	mi (<u>±</u>)
---	-----------------

🛄 ADF7023 Evaluatio	n Software
File Tools Help	
Anjentier	Rior BSON SP
Disconnect USB	Ki Settings TX/RX Packet Interrupts Register view View PER Mode (Comms processor handles TX/Rx packets) 2 Specific Standard V
Board 2	RECEIVER Test Modes/Debug Channel Frequency 915.0000 C Frequency Deviation (kHz) 20.0 C Demod Scheme 2PSK/GFSK/MSK/GMSK V
Status B2 Word spi_ready	Data Rate (kbps) 40.0 AFC Mode Disable Expected Max RF Freq Error (Hrb) 50.0
rrq_status	AFC Kp 3 C Modulation Scheme 2FSK AFC Kp 3 C PA Level 15 C AGC Mode Free Running K AGC Mode Free Running K AGS Mode Free Running K AGS Mode Free Running K RSSI LINA
FLASH LEDs	PA Ramp 4 cooles/out Cher PA Select Single ended Cher RX_auto_turnaround Cher Mixer Mixer RX_auto_turnaround Cher RX_auto_turnaround Cher RX_auto_turnaround Cher Readback Cher Cher Cher Cher Cher Cher Cher Cher
	CMD_PHY_OFF CMD_PHY_SLEEP CMD LIST Current State CMD_PHY_ON Normal Commands Write Settings Last Command CMD_PHY_TX CMD_PHY_RX

Figure 34

Transmitter Board Tx Packet Settings

Using the Tx/Rx packet tab you can set up the packet format and configure the packet handler. Ensure these settings are the same as the Receiver settings previously set. (Figure 35 point ($\underline{1}$))

- 1. The transmitted preamble length sync word and CRC can be defined by the user. (Figure 35 point (2)) (Note: Ensure CRC is enabled for this test. You have the choice to use the default CRC or enable a programmable CRC whose polynomial may be set in registers 0x11E and 0x11F.)
- Ensure you are using a fixed packet length and that, "*Packet Length Max*" is set equal the payload length. (Figure 35 point (<u>3</u>))
- Set up the Tx base address. (Figure 35 point (<u>4</u>))
 (Note : This is the start address of the Transmitted packet in Packet Ram Memory.)
- Insert Hex data in the <u>Payload Data</u> field (Figure 35 point (<u>5</u>)) then click "<u>Write Payload to RAM</u>" (Figure 35 point (<u>6</u>))
- 5. Write the settings to the device using the "<u>Update Needed</u>" button. (Figure 35 point (<u>Z</u>))

ADF7023 Evaluatio	n Software
Tools Help	
Americ	- Stand Strand Mensel & Cook
Parifier	1 www.analoa.com/srd
	Commands RF Settings TX/R× Packet Interrupts Register View Memory Check PER
	Transmit Packet Format
Disconnect USB	Preamble SWD Pavload Data (Enter in Hex) 6 CRC
Board	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA
board 2	
Monitor	4 Tx Base Address × 10 Write Payload to RAM 5
Status	SWD/Preamble/CRC Data Coding Packet Length
Status B2	Preamble Length (hytes) 8 2
Word	CRC Enable Enabled
spi_ready	Sync Word Length (bits) 24 Example CRCs X(16) + X(12) + X(5) + 1 (default)
irq_status	Sync Byte (Hex) × 123456 Programmable CRC
cmd_ready 🔵	
Get Status	Receive Packet Filtering
	Preamble/Sync/CRC Filtering Address Filtering Rx Packet RAM
FLASH LEDs	20 20 0F 0F 1F 05 1F 33 22 00 02 03 04 00 00 00 00 00 00 00 00
1	Preamble Match 0 bit errors allowed M
	Sync Error Tolerance 0 bit errors allowed
	CMD_PHY_OFF CMD_PHY_SLEEP CMD_LIST 7 Current State PHY_ON
	CMD PHY ON Normal Commands V Update Needed
	CMD_PHV_TX CMD_PHV_PX

Figure 35

Transmitter Board Interrupts

Interrupts may be configured for various conditions in the "*Interrupts*" tab. (Figure 36point (<u>1</u>))

- Set the "*tx_eof*" interrupt. (Figure 36point (<u>2</u>)) This will give an interrupt signal after a packet has been fully transmitted.
- 2. Write the settings to the device using the "<u>Update Needed</u>" button. (Figure 36point (<u>3</u>))
- Transmit a packet by clicking "<u>CMD PHY TX</u>" (Figure 36point (<u>4</u>)) (Note: Ensure that the current state of the part is in "PHY_ON" before pressing "<u>CMD PHY TX</u>".)

"Board 2" is now in Transmit and once a packet is transmitted the part returns to the PHY_ON state.

ADF7023 Evaluatio	n Software	
File Tools Help		
Parsoner	Commands BE Settings Tyley Packet Interrupts Register View	Memory Check PEP
Disconnect USB Board Board 2 V Launch USB Monitor Status Status Status Status B2 Word spi_ready irq_status cmd_ready	Commands RF Settings Tx/Rx Packet Interrupts Register View	w Memory Check PER num_wakeups
Get Status FLASH LEDs	CMD_PHY_OFF CMD_PHY_OFF CMD_PHY_ON CMD_PHY_TX CMD_PHY_RX	CMD LIST Current State PHY_ON Normal Commands V Normal Command BI

Figure 36

Reading Interrupt Source on Transmitter board

Once the Transmitter has transmitted a packet you should now see "Interrupt Detected!" on both instances of the software. (Figure 37 point (<u>1</u>))

On the Transmitter board the interrupt signifies that a packet has been successfully transmitted. To check the source of the interrupt, click "*Read Source*" (Figure 37 point (<u>2</u>))

To Clear the interrupt status click "<u>Clear All Interrupts</u>" (Figure 37 point (<u>3</u>))

menners	Course Transfe	Phi Phi	Reser	nsp	-29-3	-	IEMS SO	Convertes
Com	mands RF Settings	Tx/Rx Packet	Interrupts	Register View	Memory Check	PER		www.analog.com/
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12								
unch USB					num_wakeups			
onitor					lpm_rssi_det			
s F2					ALS_DONE			
eady O		batt	ery_alarm 🖤		address match			
atus			rc_ready					
eady 🧿		WG	spi ready		sync_detect		Read Source	
		cm	d finished		premable detect 🧲			
et Status			_				Clear All Incerrupts	
SH LEDs								
			C (MD, D					
	PID PITT OFF		CMD_P	HT_SLEEP	CMD LICT			Compare Shake DHV C

Figure 37

Reading Interrupt Source on Receiver board

Once the Transmitter has transmitted a packet you should now see "Interrupt Detected!" on the Receiver software instance. (Figure 38 point (<u>1</u>))

On the Receiver board the interrupt signifies that a packet has been successfully Received with a valid CRC.

To check the source of the interrupt, click "*<u>Read Source</u>*" (Figure 38 point (<u>2</u>))

To Clear the interrupt status click "*Clear All Interrupts*" (Figure 38 point (<u>3</u>))

menners 200	ar man	Pro	Reser	USP	-72-	-	EHAS SS	Converter
Commands	RF Settings	Tx/Rx Packet	Interrupts	Register View	Memory Check	PER		www.analog.com/
onnect USB								
unch USB					num_wakeups			
nitor					lpm_rssi_det			
F2					AES_Done			
		batt	ery_alarm 🔘		cx_eor			
atus			rc_ready		address_match			
adv		WUG	timeout		sync detect		Read Source	
		cm	finished		premable detect			
t Status					<u> </u>			
5H LEDs								
			<u></u>					
CMD_PH	Y_OFF		CMD_P	HY_SLEEP	CMD LIST			Current State PHY_C

Figure 38

Running a Packet Error Rate Test

To run a packet error rate test the previous section, Simple Rx / Tx Test in Packet Mode, must first be followed. Once interrupts are observed, on both the Rx and Tx software instances, the Packet Error Rate (PER) test may be used.

Configuring the Receiver board for the PER test

- Once all of the Receiver and packet parameters are setup correctly (as in <u>Rx Setup in Packet Mode</u> section) then select the "<u>PER</u>" Tab. (Figure 39 point (<u>1</u>))
- 2. Select the "<u>*Rx Board Setup*</u>" Tab (Figure 39 point (<u>2</u>))
- 3. Set the number of packets to be received, "<u>No. of Packets to Rx</u>" (Figure 39 point (<u>3</u>))
- 4. Write these settings to the uC by clicking "*Write Rx Settings*" (Figure 39 point (<u>4</u>))
- To begin the test and put the receiver into Rx click "*Begin PER Rx*" (Figure 39 point (<u>5</u>)) (Note: The receiver will remain in Rx waiting for a packet to be transmitted from a valid transmitter.)
- If at any time you wish to terminate the test manually press "<u>Stop Test</u>". (Figure 39 point (<u>6</u>)) (Note: The test will stop automatically once it receives the final transmitted packet.)

DF7023 Evaluatio	n Software								
Tools Help									
Amenner	Couver man	Z Pr	arese	OSP DET	-72-1		EMS	2 C	Convertion
	Commands RF Settin	igs Tx/Rx Packet	Interrupts	Register View	Memory Check	PER			www.analog.com/srd
	TyBoard Setup	Ry Board Setup	Dockat Satur	1		1000			
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Board		A3	-	(D.					
Board 1		1,000	No. c	of Packets to KX			0	(Laboration	
Launch USB		Missed Packets	LED				U	essituly kecer	/ed Packets
Photneor	1		- 4				0 Misse	ed Packets	
Status B2		write	e Rx Settings				0 Total	Packets	
Word	1	Be	- 5						
spi_ready)ED %	UITER RA						
irq_status	Ĩ	ER 70							0%
.md_ready 🌙									0.0
Get Status	Т	ast Progression							
									0%
FLASH LEDs									
	1		6	,		-			
			Stop	p Test		Ensu	ure Rx is st	arted B	lefore Tx
	-								
			C CMD (
				HY_SLEEP	CMD LIST		Write Set	cinas	urrent State PHY_ON
		CMD_PHY_ON			Normanus	5		La	ust Command B1
	CMD_PHY_TX		CMD.	_PHY_RX					

Figure 39

Configuring the Transmitter board for the PER test

- Once all of the Transmitter and packet parameters are setup correctly (as in <u>Tx Setup in Packet Mode</u> section) then select the "<u>PER</u>" Tab. (Figure 40 point (<u>1</u>))
- 2. Select the "*<u>Tx Board Setup</u>*" Tab (Figure 40 point (<u>2</u>))
- Set the number of packets to be received, "<u>No. of Packets to Tx</u>" (Figure 40 point (<u>3</u>)) (Note: Ensure the number of packets on the Receive and Transmit side are set the same.)
- Set the delay between each transmitted packet from the "<u>Delay Between Packets</u>" dropdown menu. (Figure 40 point (<u>4</u>))
- 5. Write these settings to the uC by clicking "*Write Tx Settings*" (Figure 40 point (<u>5</u>))
- To begin the test and put the receiver into Tx click "*Begin PER Tx*" (Figure 40 point (<u>5</u>)) (Note: The transmitter will continuously transmit packets until "*No. of Packets to Tx*" value is reached.)
- If at any time you wish to terminate the test manually press <u>"Stop Test</u>". (Figure 40 point <u>(6)</u>) (Note: The test will stop automatically once the transmitter has transmitted the final packet.)

🕒 ADF7023 Evaluatio	n Software	
File Tools Help		
Amenner	Prot BS CTUS	Converter
	Commands RF Settings Tx/Rx Packet Interrupts Register View Memory Check PER	www.aralog.com/ara
	TxBoard Setup Rx Board Setup Packet Setup	
Disconnect USB		
Board Board 2		
Launch USB	No. of Packets to Tx	
Monitor	Delay Between Parkets	
Status B2		
Word spi_ready 🥥		
irq_status 🔘	5 Write Tx Settings	
cmd_ready 🌖		
Get Status	Bagin DED. Ty	
	begin EK IA.	
FLASH LEDS	7	
	Stop Test	
	Ensure RX is started before 1x	
	CMD_PHY_OFF CMD_PHY_SLEEP CMD LIST CMD LIST	urrent State PHY_ON
	CMD_PHY_ON Normal Commands Vite Settings	ast Command B1
	CMD_PHY_TX CMD_PHY_RX	

Figure 40

Running a Script



1. Select "*<u>Run Script</u>*" from the "<u>*CMD LIST*</u>" drop down menu as shown in *Figure 41*Figure 41.

Figure 41

2. Select the path where the script file is stored. (Figure 42Figure 40 point (<u>1</u>))



3. Click "*Execute Script*" to run the selected script. (Figure 42Figure 40 point (2)

Figure 42

Using Scripts

Scripts can be written in Notepad and saved with a file extension of .txt

The following are examples can be used:

- To write to a PACKET_RAM register enter the line "18xxyy" where "xx" represents the last eight bits of the address to be written to and "yy" represents the value to be stores at this address.
 - For Example if you need to write 0xAB to PACKET_RAM location 0x010, then the script code would be : 1810AB
- To write to a BBRAM register enter the line "19xxyy" where "xx" represents the last eight bits of the address to be written to and "yy" represents the value to be stores at this address.
 - For Example if you need to write 0xCD to BBRAM location 0x123, then the script code would be : 1923CD
- To write to a MCR register enter the line "1Bxxyy" where "xx" represents the last eight bits of the address to be written to and "yy" represents the value to be stores at this address.
 - For Example if you need to write 0xEF to MCR location 0x345, then the script code would be : 1B45EF
- To introduce a delay before the next script command enter the line "Sxxxx". Where "xxxx" represents an integer multiple of 1ms.
 - For example to enter a delay of 120ms before the next command is to be issued then the script code would be: "S120"
- To issue a COMMAND enter the desired command.
 - For Example to enter "*PHY_OFF*", then the script code would be : B1
 - For Example to enter "*PHY ON*", then the script code would be : B2
 - For Example to enter "*PHY TX*", then the script code would be : B5
- To introduce comments in the file use "//" before the comment.

Scripting Example

The following script would be used for the previous examples:

//Start of script

//Set Packet_Ram address 0x010 to AB
//Set BBRam address 0x123 to CD
//Set MCR address 0x345 to EF
//Delay for 120ms
//Enter PHY_OFF
//Enter PHY_ON
//Enter PHY_Tx

//End of script

ADF7023 Evaluation Board Schematics and BOMs

Qty	Name	Value	Tolerance	PCB Decal	Manufacturing Part No.
1	C1	1.5nF	±5%	0402	GRM155R71H152KA01D
9	C14, C16, C24, C28, C30, C33, C37, C62, C65	220nF	±10%	0402	GRM155R61A224KE19D
2	C15, C27	100pF	±5%	0402	GRM1555C1H101JZ01D
3	C23, C34, C35	18pF	±5%	0402	GRM1555C1H180JZ01D
1	C25	150nF	±5%	0402	GRM155R61A154KE19D
2	C26, C42	10uF	±20%	0603	6R3R14X106MV4T
2	C39, C40	5.6pF	±5%	0402	GRM1555C1H5R6DZ01D
4	R3, R4, R8, R9	DNI			Not inserted
1	R12	36k	±1%	0402	MCR01MZPF3602
1	R15	100k	±1%	0402	MCR01MZPF1003
1	R16	1.1k	±1%	0402	MCR01MZPF1101
1	Y1	26MHz			NX3225SA-26.000000MHZ-G2
1	Y2	32.768kHz			ABS07-32.768KHZ-7-T
1	U1			LFCSP-32	ADF7023

Table 2 Components Common to All Daughter Boards

Table 3 Eval-ADF7023DB1Z Components (868/915MHz Separate Matches)

Qty	Name	Value	Tolerance	PCB Decal	Manufacturing Part No.
1	C2	1pF	±0.25pF	0402	GRM1555C1H1R0CA01D
2	C3, C5	2.2pF	±0.25pF	0402	GRM1555C1H2R2CZ01D
1	C18	56pF	±5%	0402	GRM1555C1H470JZ01D
1	C19	2.7pF	±0.25pF	0402	GRM1555C1H2R7CZ01D
1	C20	1.2pF	±0.25pF	0402	GRM1555C1H1R2CZ01D
1	C66	100pF	±5%	0402	GRM1555C1H101JZ01D

1	C67	47pF	±5%	0402	GRM1555C1H470JZ01D
1	L1	1.8nH	±5%	0402	Coilcraft 0402CS-1N8XJL
1	L2	24nH	±5%	0402	Coilcraft 0402CS-24NXJL
1	L3	12nH	±5%	0402	Coilcraft 0402CS-12NXJL
1	L4	6.2nH	±5%	0402	Coilcraft 0402CS-6N2XJL
1	L6	47nH	±5%	0402	Coilcraft 0402CS-47NXJL
2	L5, L10	12nH	±5%	0402	Coilcraft 0402CS-12NXJL

Table 4 Eval-ADF7023DB2Z Components (868/915MHz Combined Match)

Qty	Name	Value	Tolerance	PCB Decal	Manufacturing Part No.
1	C2	DNI			Not Inserted
2	C3,C22	2.2pF	±0.25pF	0402	GRM1555C1H2R2CZ01D
1	C18	56pF	±5%	0402	GRM1555C1H470JZ01D
2	C19	2.7pF	±0.25pF	0402	GRM1555C1H2R7CZ01D
1	C20	1.8pF	±0.25pF	0402	GRM1555C1H1R8CZ01D
1	C66	100pF	±5%	0402	GRM1555C1H101JZ01D
1	C67	47pF	±5%	0402	GRM1555C1H470JZ01D
1	L1	1.8nH	±5%	0402	Coilcraft 0402CS-1N8XJL
3	L2, L4, L9	12nH	±5%	0402	Coilcraft 0402CS-11NXJL
1	L3	11nH	±5%	0402	Coilcraft 0402CS-11NXJL
1	L6	47nH	±5%	0402	Coilcraft 0402CS-47NXJL
1	L7	24nH	±5%	0402	Coilcraft 0402CS-24NXJL

Table 5 Eval-ADF7023DB3Z Components (433MHz Separate Matches)

Qty	Name	Value	Tolerance	PCB Decal	Manufacturing Part No.
1	C2	1.2pF	±0.25pF	0402	GRM1555C1H1R2CZ01D
2	C3, C5	3.9pF	±0.25pF	0402	GRM1555C1H3R9CZ01D
3	C19, C20	5.6pF	±0.25pF	0402	GRM1555C1H5R6DZ01D

2	C18, C67	270pF	±5%	0402	GRM1555C1H271JA01D
1	C66	100pF	±5%	0402	GRM1555C1H101JZ01D
1	L1	15nH	±5%	0402	Coilcraft 0402CS-15NXJL
1	L2	82nH	±5%	0402	Coilcraft 0402CS-82NXJL
2	L3, L4	27nH	±5%	0402	Coilcraft 0402CS-27NXJL
2	L5, L10	33nH	±5%	0402	Coilcraft 0402CS-11NXJL
1	L6	100nH	±5%	0402	Coilcraft 0402CS-R10XJL

Table 6 Eval-ADF7023DB4Z Components (433MHz Combined Match)

Qty	Name	Value	Tolerance	PCB Decal	Manufacturing Part No.
1	C2	DNI			Not Inserted
1	C3, C22	3.9pF	±0.25pF	0402	GRM1555C1H3R9CZ01D
2	C18, C67	270pF	±5%	0402	GRM1555C1H271JA01D
1	C19	4.7pF	±0.1pF	0402	GRM1555C1H4R7BA01D
1	C20	2.7pF	±0.1pF	0402	GRM1555C1H2R7BA01D
1	C66	100pF	±5%	0402	GRM1555C1H101JZ01D
1	L1	13nH	±5%	0402	Coilcraft 0402CS-13NXJL
1	L2, L9	33nH	±5%	0402	Coilcraft 0402CS-33NXJL
1	L3	30nH	±5%	0402	Coilcraft 0402CS-30NXJL
1	L4	41nH	±5%	0402	Coilcraft 0402CS-41NXJL
1	L6	100nH	±5%	0402	Coilcraft 0402CS-R10XJL
1	L7	82nH	±5%	0402	Coilcraft 0402CS-82NXJL



Figure 43 Separate PA and LNA Matches Board Schematic (DB1Z, DB3Z)



Figure 44 Combined PA and LNA Match Board Schematic (DB2Z, DB4Z)



Figure 45 Separate PA and LNA Matches Board Silkscreen (DB1Z, DB3Z)



Figure 46 Combined PA and LNA Match Board Silkscreen (DB2Z, DB4Z)

Eval-ADF7XXXMB3Z Mother Board Schematics and Silk Screen



Figure 47 Mother Board Silkscreen

ADF7xxxMB3Z RevB.sch-3 - Thu Sep 30 14:09:50 2010



ADF7xxxMB3Z RevB.sch-2 - Thu Sep 30 14:07:49 2010







ADF7xxxMB3Z RevB.sch-1 - Tue Sep 28 15:47:41 2010

