PLL Frequency Synthesizer

Data Sheet

ADF4106

FEATURES

- 6.0 GHz bandwidth
- 2.7 V to 3.3 V power supply
- Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
- Programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- Programmable antibacklash pulse width
- 3-wire serial interface
- Analog and digital lock detect
- Hardware and software power-down mode

APPLICATIONS

- Broadband wireless access
- Satellite systems
- Instrumentation
- Wireless LANS
- Base stations for wireless radios

GENERAL DESCRIPTION

The ADF4106 frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler (P/P + 1). The A (6-bit) counter and B (13-bit) counter, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

FUNCTIONAL BLOCK DIAGRAM

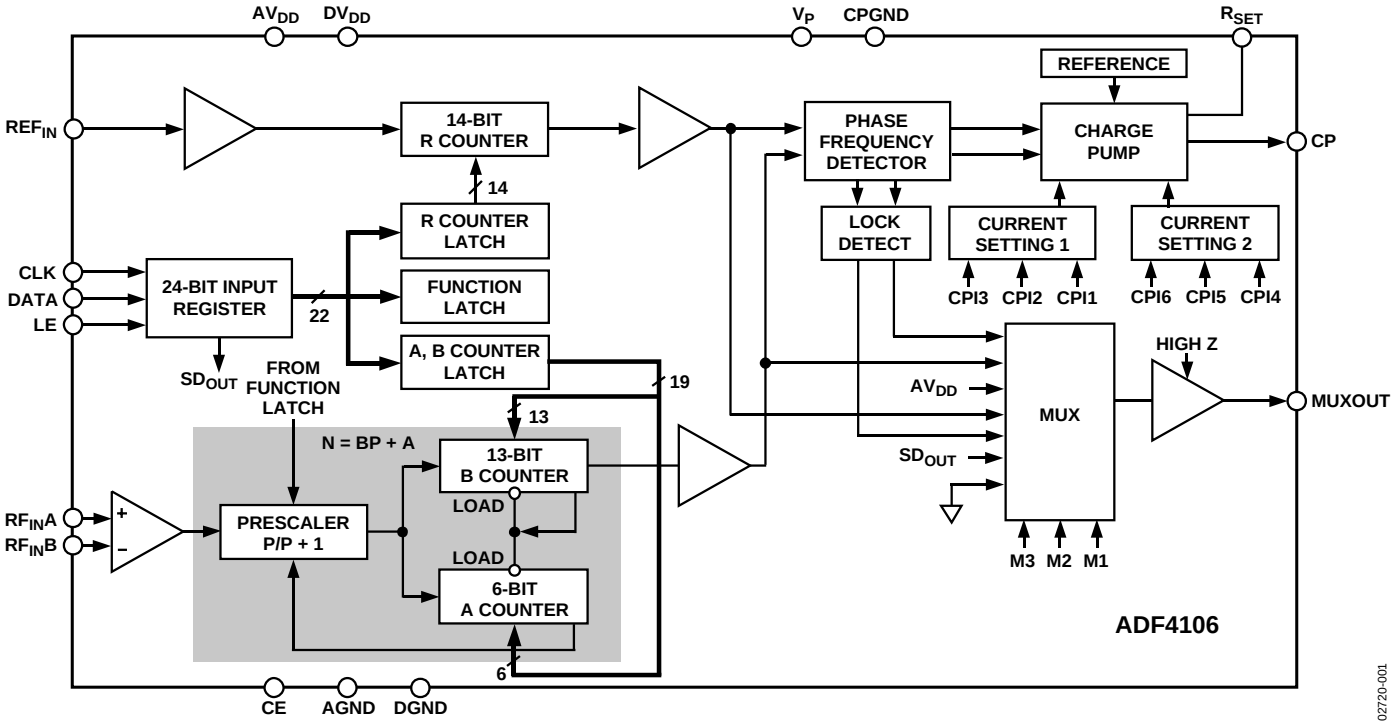


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADF4106* Product Page Quick Links

Last Content Update: 08/30/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- ADF4106 Evaluation Board

Documentation

Application Notes

- AN-30: Ask the Applications Engineer - PLL Synthesizers
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers

Data Sheet

- ADF4106-DSCC: Military Data Sheet
- ADF4106-EP: Enhanced Product Data Sheet
- ADF4106: PLL Frequency Synthesizer Data Sheet

User Guides

- UG-159: LMDS Evaluation Board for PLL Frequency Synthesizer
- UG-161: PLL Frequency Synthesizer Evaluation Board
- UG-476: PLL Software Installation Guide
- UG-582: Evaluating the EVAL-CN0290-SDPZ

Software and Systems Requirements

- Integer-N Software
- ADF4106 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- BeMicro FPGA Project for ADF4106 with Nios driver

Tools and Simulations

- ADIsimPLL™
- ADIsimRF
- dt_ADF411x_Register_Configuration
- ADF4106BCPZ IBIS Model
- ADF4106BRUZ IBIS Model

Reference Designs

- CN0290

Reference Materials

Analog Dialogue

- Ask the Applications Engineer—30: PLL SYNTHESIZERS
- Design a Direct 6-GHz Local Oscillator with a New, Wideband, Integer-N, PLL Synthesizer
- Direct Digital Synthesis (DDS) Controls Waveforms in Test, Measurement, and Communications
- Phase-locked loops for high-frequency receivers and transmitters

Product Selection Guide

- RF Source Booklet

Technical Articles

- Phase Locked Loops for High-Frequency Receivers and Transmitters – Part 1
- Phase Locked Loops for High-Frequency Receivers and Transmitters – Part 3
- Phase-Locked Loops for High-Frequency Receivers and Transmitters - Part 2

Design Resources

- ADF4106 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADF4106 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

TABLE OF CONTENTS

REVISION HISTORY

4/15—Rev. E to Rev. F

Change to $RF_{IN}A$ to $RF_{IN}B$ Parameter, Table 3 ... 6
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 22

11/12—Rev. D to Rev. E

Changed EVAL-ADF4106EBZ1 to EV-ADF4106SD1Z ... Universal
Added $RF_{IN}A$ to $RF_{IN}B$ Parameter, Table 3 ... 6
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 22

9/11—Rev. C to Rev. D

Changes to Normalized Phase Noise Floor (PN_{SYNTH}) Parameter, Table 1 ... 4
Added Normalized 1/f Noise (PN_{1_f}) Parameter and Endnote 12, Table 1 ... 4
Changes to Ordering Guide ... 22

2/10—Rev. B to Rev. C

Changes to Figure 4 and Table 4 ... 6
Changes to Figure 12 ... 8
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 21

6/05—Rev. A to Rev. B

Updated Format ... Universal
Changes to Figure 1 ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Table 3 ... 5
Changes to Figure 3 and Figure 4 ... 6
Changes to Figure 6 ... 7
Changes to Figure 10 ... 7
Deleted TPC 13 and TPC 14 ... 8
Changes to Figure 15 ... 8
Changes to Figure 20 Caption ... 10
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 21

5/03—Rev. 0 to Rev. A

Edits to Specifications ... 2
Edits to TPC 11 ... 7
Updated Outline Dimensions ... 19

10/01—Revision 0: Initial Revision

SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	B Chips[2] (typ)	Unit	Test Conditions/Comments
RF CHARACTERISTICS				See Figure 18 for input circuit
RF Input Frequency (RF_{IN})	0.5/6.0	0.5/6.0	GHz min/max	For lower frequencies, ensure slew rate (SR) > 320 V/µs
RF Input Sensitivity	−10/0	−10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	300	300	MHz max	P = 8
	325	325	MHz max	P = 16
REF_{IN} CHARACTERISTICS				
REF_{IN} Input Frequency	20/300	20/300	MHz min/max	For f < 20 MHz, ensure SR > 50 V/µs
REF_{IN} Input Sensitivity[4]	0.8/V_{DD}	0.8/V_{DD}	V p-p min/max	Biased at AV_{DD}/2 (see Note 5[5])
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[6]	104	104	MHz max	ABP = 0, 0 (2.9 ns antibacklash pulse width)
CHARGE PUMP				Programmable, see Table 9
I_{CP} Sink/Source				
High Value	5	5	mA typ	With R_{SET} = 5.1 kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With R_{SET} = 5.1 kΩ
R_{SET} Range	3.0/11	3.0/11	kΩ typ	See Table 9
I_{CP} Three-State Leakage	2	2	nA max	1 nA typical; T_A = 25°C
Sink and Source Current Matching	2	2	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}	1.5	1.5	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS				
V_{IH}, Input High Voltage	1.4	1.4	V min	
V_{IL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}, I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	1.4	1.4	V min	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	V_{DD} − 0.4	V_{DD} − 0.4	V min	CMOS output chosen
I_{OH}	100	100	µA max	
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	AV_{DD}/5.5	V min/V max	$AV_{DD} \le V_P \le 5.5$V
I_{DD}[7] (AI_{DD} + DI_{DD})	11	9.0	mA max	9.0 mA typ
I_{DD}[8] (AI_{DD} + DI_{DD})	11.5	9.5	mA max	9.5 mA typ
I_{DD}[9] (AI_{DD} + DI_{DD})	13	10.5	mA max	10.5 mA typ
I_P	0.4	0.4	mA max	T_A = 25°C
Power-Down Mode[10] (AI_{DD} + DI_{DD})	10	10	µA typ	

Parameter	B Version[1]	B Chips[2] (typ)	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS				
Normalized Phase Noise Floor (PN_{SYNTH})[11]	−223	−223	dBc/Hz typ	PLL loop B/W = 500 kHz, measured at 100 kHz offset
Normalized 1/f Noise (PN_{1_f})[12]	−122	−122	dBc/Hz typ	10 kHz offset; normalized to 1 GHz
Phase Noise Performance[13]				@ VCO output
900 MHz[14]	−92.5	−92.5	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
5800 MHz[15]	−76.5	−76.5	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
5800 MHz[16]	−83.5	−83.5	dBc/Hz typ	@ 1 kHz offset and 1 MHz PFD frequency
Spurious Signals				
900 MHz[14]	−90/−92	−90/−92	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
5800 MHz[15]	−65/−70	−65/−70	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
5800 MHz[16]	−70/−75	−70/−75	dBc typ	@ 1 MHz/2 MHz and 1 MHz PFD frequency

[1] Operating temperature range (B Version) is –40°C to +85°C.
[2] The B chip specifications are given as typical values.
[3] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[4] $AV_{DD} = DV_{DD} = 3$ V.
[5] AC coupling ensures $AV_{DD}/2$ bias.
[6] Guaranteed by design. Sample tested to ensure compliance.
[7] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 16; $RF_{IN} = 900$ MHz.
[8] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 16; $RF_{IN} = 2.0$ GHz.
[9] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 32; $RF_{IN} = 6.0$ GHz.
[10] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3.3$ V; R = 16383; A = 63; B = 891; P = 32; $RF_{IN} = 6.0$ GHz.
[11] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.
[12] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by $PN = PN_{1\_f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{RF}/1 \text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[13] The phase noise is measured with the EV-ADF4106SD1Z evaluation board and the Agilent E4440A Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).
[14] $f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; Offset Frequency = 1 kHz; $f_{RF} = 900$ MHz; N = 4500; Loop B/W = 20 kHz.
[15] $f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; Offset Frequency = 1 kHz; $f_{RF} = 5800$ MHz; N = 29000; Loop B/W = 20 kHz.
[16] $f_{REFIN} = 10$ MHz; $f_{PFD} = 1$ MHz; Offset Frequency = 1 kHz; $f_{RF} = 5800$ MHz; N = 5800; Loop B/W = 100 kHz.

TIMING CHARACTERISITICS

$AV_{DD} = DV_{DD} = 3$ V ± 10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.

Table 2.

Parameter	Limit[1] (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulse Width

[1] Operating temperature range (B Version) is –40°C to +85°C.

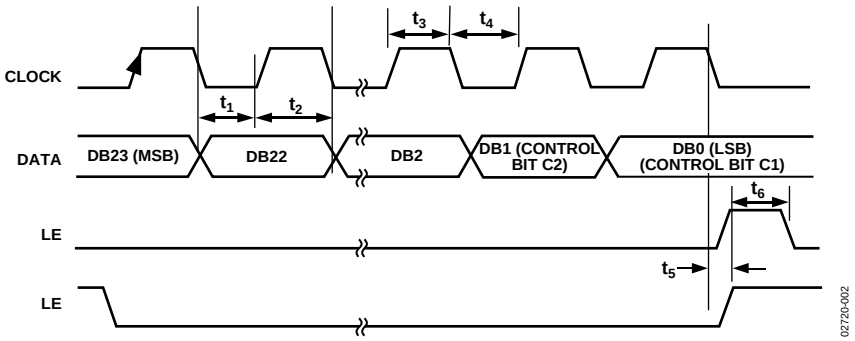


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	–0.3 V to + 3.6 V
AV_{DD} to DV_{DD}	–0.3 V to + 0.3 V
V_P to GND	–0.3 V to + 5.8 V
V_P to AV_{DD}	–0.3 V to + 5.8 V
Digital I/O Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	–0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	–0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±600 mV
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	112°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

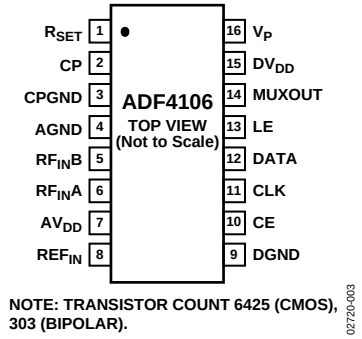


Figure 3. 16-Lead TSSOP Pin Configuration

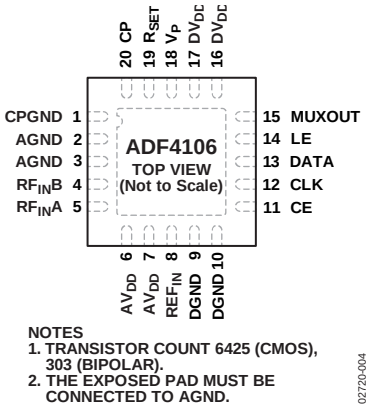


Figure 4. 20-Lead LFCSP_WQ Pin Configuration

Table 4. Pin Function Descriptions

Pin No. TSSOP	Pin No. LFCSP	Mnemonic	Function
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $I_{CP\,MAX} = \frac{25.5}{R_{SET}}$ So, with R_{SET} = 5.1 kΩ, $I_{CP\,MAX}$ = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 18.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and a dc equivalent input resistance of 100 kΩ. See Figure 18. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches with the latch being selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5 V.
		EP	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ UNIT GHz KEYWORD R
PARAM TYPE S IMPEDANCE 50Ω
DATA FORMAT MA

FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.500	0.89148	–17.2820	3.300	0.42777	–102.748
0.600	0.88133	– 20.6919	3.400	0.42859	–107.167
0.700	0.87152	– 24.5386	3.500	0.43365	–111.883
0.800	0.85855	–27.3228	3.600	0.43849	–117.548
0.900	0.84911	–31.0698	3.700	0.44475	–123.856
1.000	0.83512	– 34.8623	3.800	0.44800	–130.399
1.100	0.82374	–38.5574	3.900	0.45223	–136.744
1.200	0.80871	–41.9093	4.000	0.45555	–142.766
1.300	0.79176	– 45.6990	4.100	0.45313	–149.269
1.400	0.77205	–49.4185	4.200	0.45622	–154.884
1.500	0.75696	–52.8898	4.300	0.45555	–159.680
1.600	0.74234	–56.2923	4.400	0.46108	–164.916
1.700	0.72239	–60.2584	4.500	0.45325	–168.452
1.800	0.69419	–63.1446	4.600	0.45054	–173.462
1.900	0.67288	–65.6464	4.700	0.45200	–176.697
2.000	0.66227	–68.0742	4.800	0.45043	178.824
2.100	0.64758	–71.3530	4.900	0.45282	174.947
2.200	0.62454	–75.5658	5.000	0.44287	170.237
2.300	0.59466	–79.6404	5.100	0.44909	166.617
2.400	0.55932	–82.8246	5.200	0.44294	162.786
2.500	0.52256	–85.2795	5.300	0.44558	158.766
2.600	0.48754	–85.6298	5.400	0.45417	153.195
2.700	0.46411	–86.1854	5.500	0.46038	147.721
2.800	0.45776	–86.4997	5.600	0.47128	139.760
2.900	0.44859	–88.8080	5.700	0.47439	132.657
3.000	0.44588	–91.9737	5.800	0.48604	125.782
3.100	0.43810	–95.4087	5.900	0.50637	121.110
3.200	0.43269	–99.1282	6.000	0.52172	115.400

02720-005

Figure 5. S-Parameter Data for the RF Input

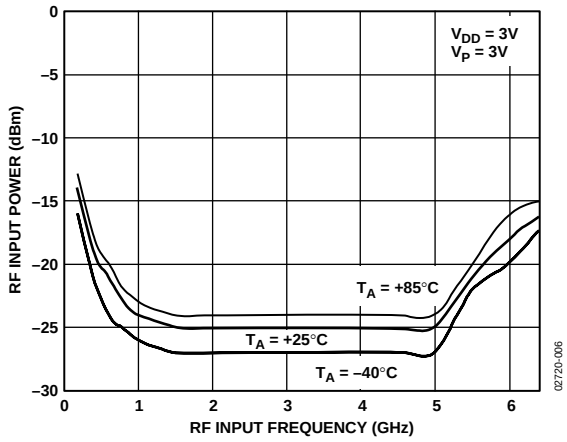


Figure 6. Input Sensitivity

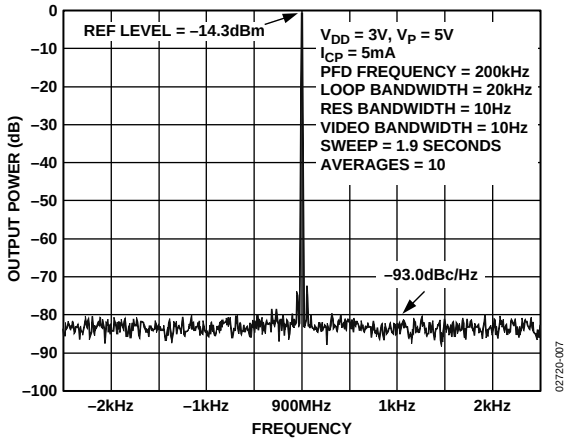


Figure 7. Phase Noise (900 MHz, 200 kHz, and 20 kHz)

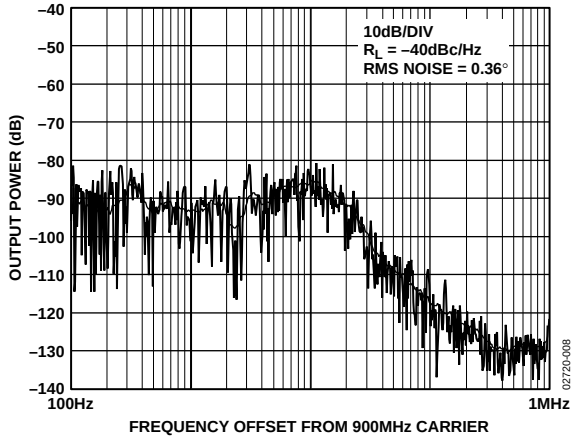


Figure 8. Integrated Phase Noise (900 MHz, 200 kHz, and 20 kHz)

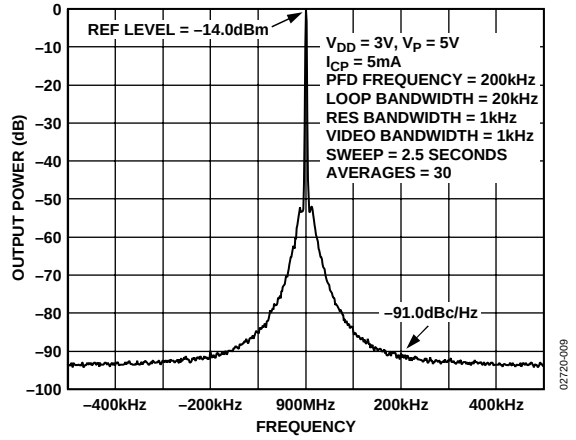


Figure 9. Reference Spurs (900 MHz, 200 kHz, and 20 kHz)

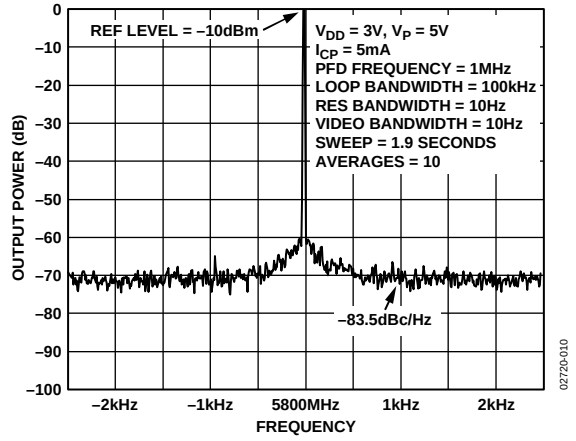


Figure 10. Phase Noise (5.8 GHz,1 MHz, and 100 kHz)

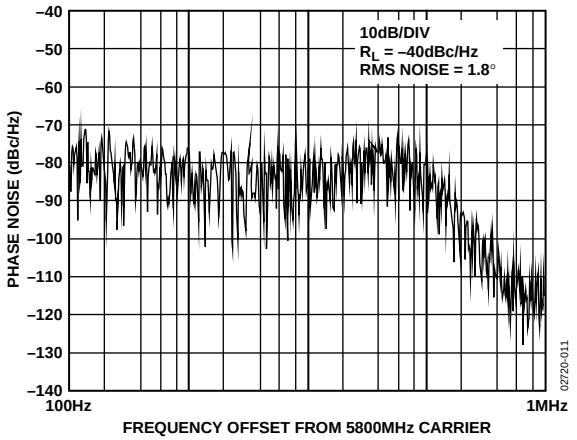


Figure 11. Integrated Phase Noise (5.8 GHz,1 MHz, and 100 kHz)

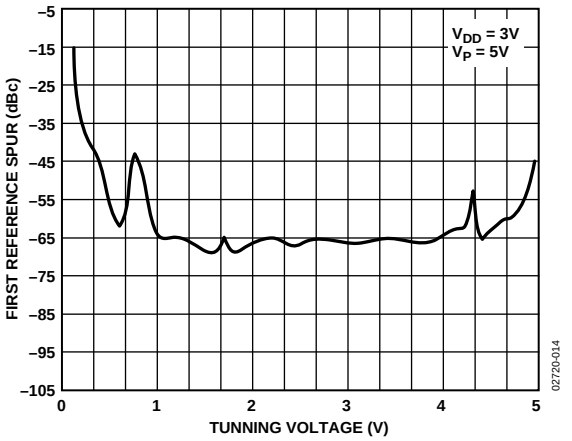


Figure 14. Reference Spurs vs. V_{TUNE} (5.8 GHz,1 MHz, and 100 kHz)

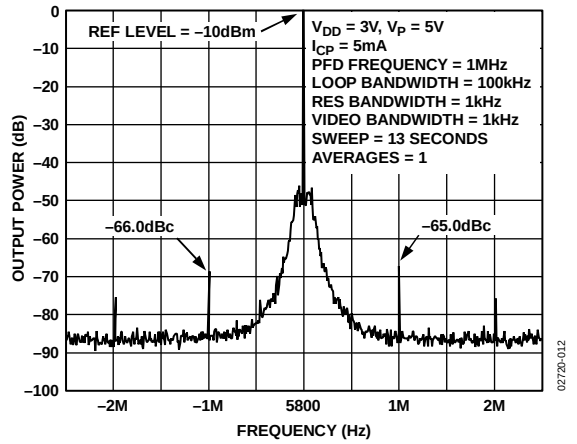


Figure 12. Reference Spurs (5.8 GHz,1 MHz, and 100 kHz)

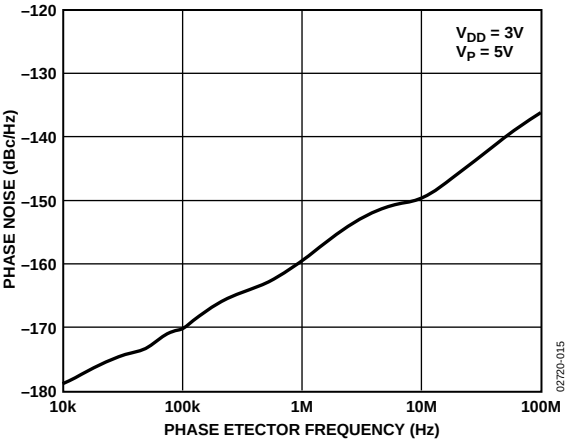


Figure 15. Phase Noise (Referred to CP Output) vs. PFD Frequency

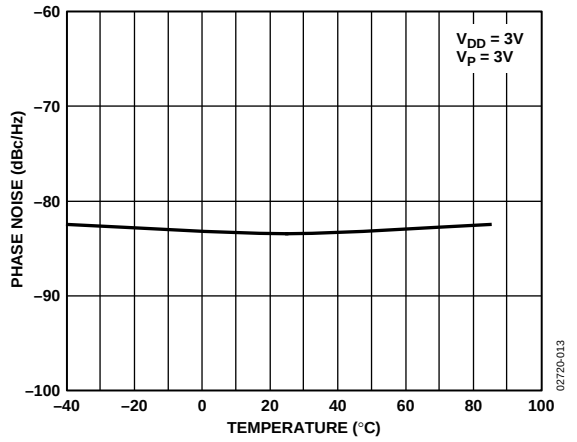


Figure 13. Phase Noise (5.8 GHz,1 MHz, and 100 kHz) vs. Temperature

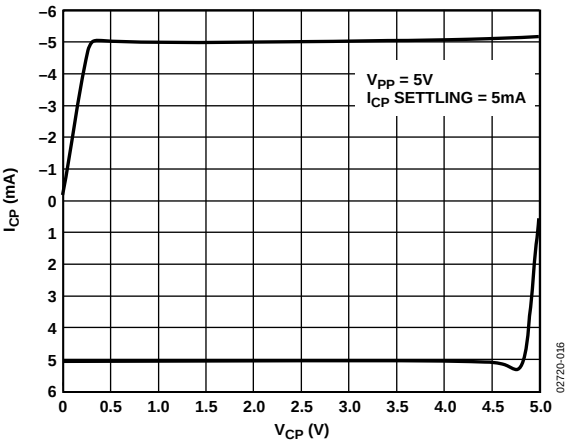


Figure 16. Charge Pump Output Characteristics

GENERAL DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 17. SW1 and SW2 are normally closed switches. SW3 is a normally open switch. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

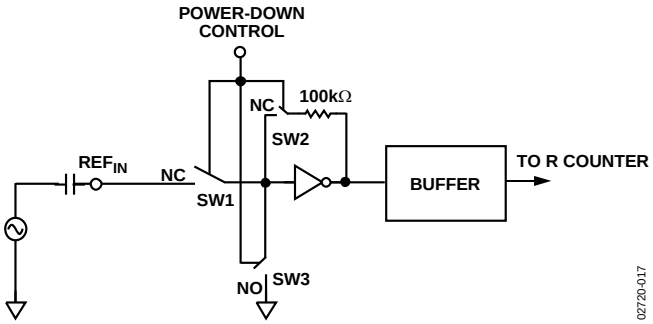


Figure 17. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 18. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

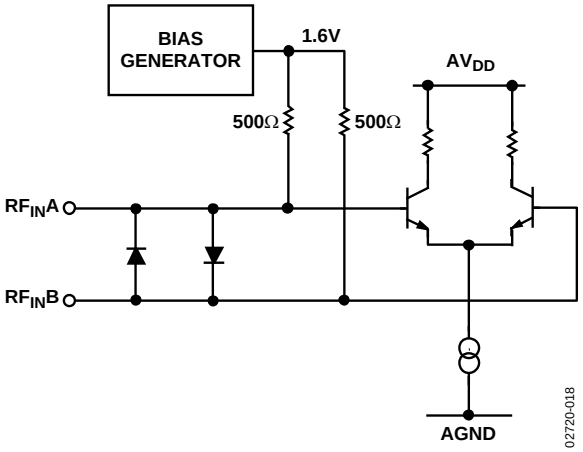


Figure 18. RF Input Stage

PRESCALER (P/P +1)

The dual-modulus prescaler (P/P + 1), along with the A counter and B counter, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by ($P^2 - P$).

A COUNTER AND B COUNTER

The A counter and B CMOS counter combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 325 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

Pulse Swallow Function

The A counter and B counter, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = \left[\left(P \times B\right) + A\right] \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 13-bit counter (3 to 8191).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

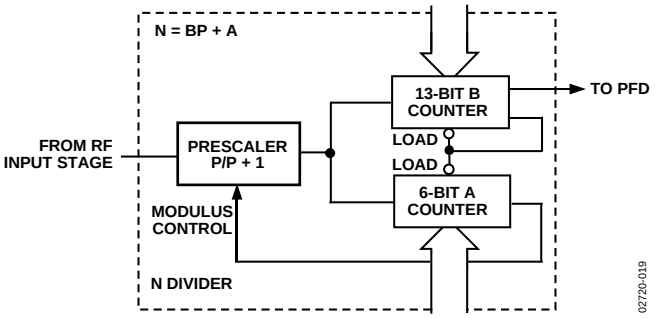


Figure 19. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 20 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. See Table 7.

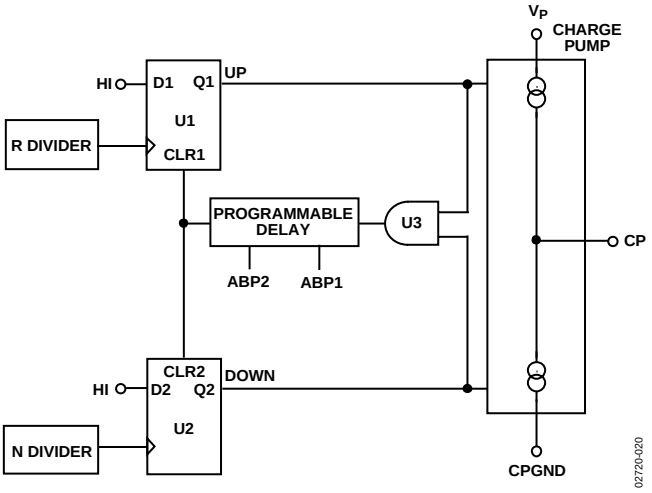


Figure 20. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4106 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table 9 shows the full truth table. Figure 21 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, this output is high with narrow, low-going pulses.

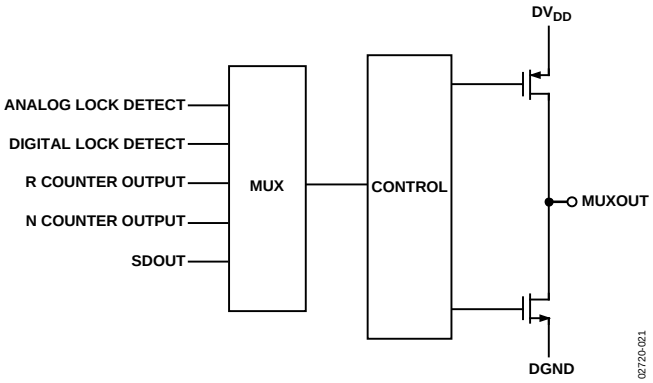


Figure 21. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4106 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5. Table 6 shows a summary of how the latches are programmed.

Table 5. C1, C2 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table 6. Latch Summary

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

02720-022

Table 7. Reference Counter Latch Map

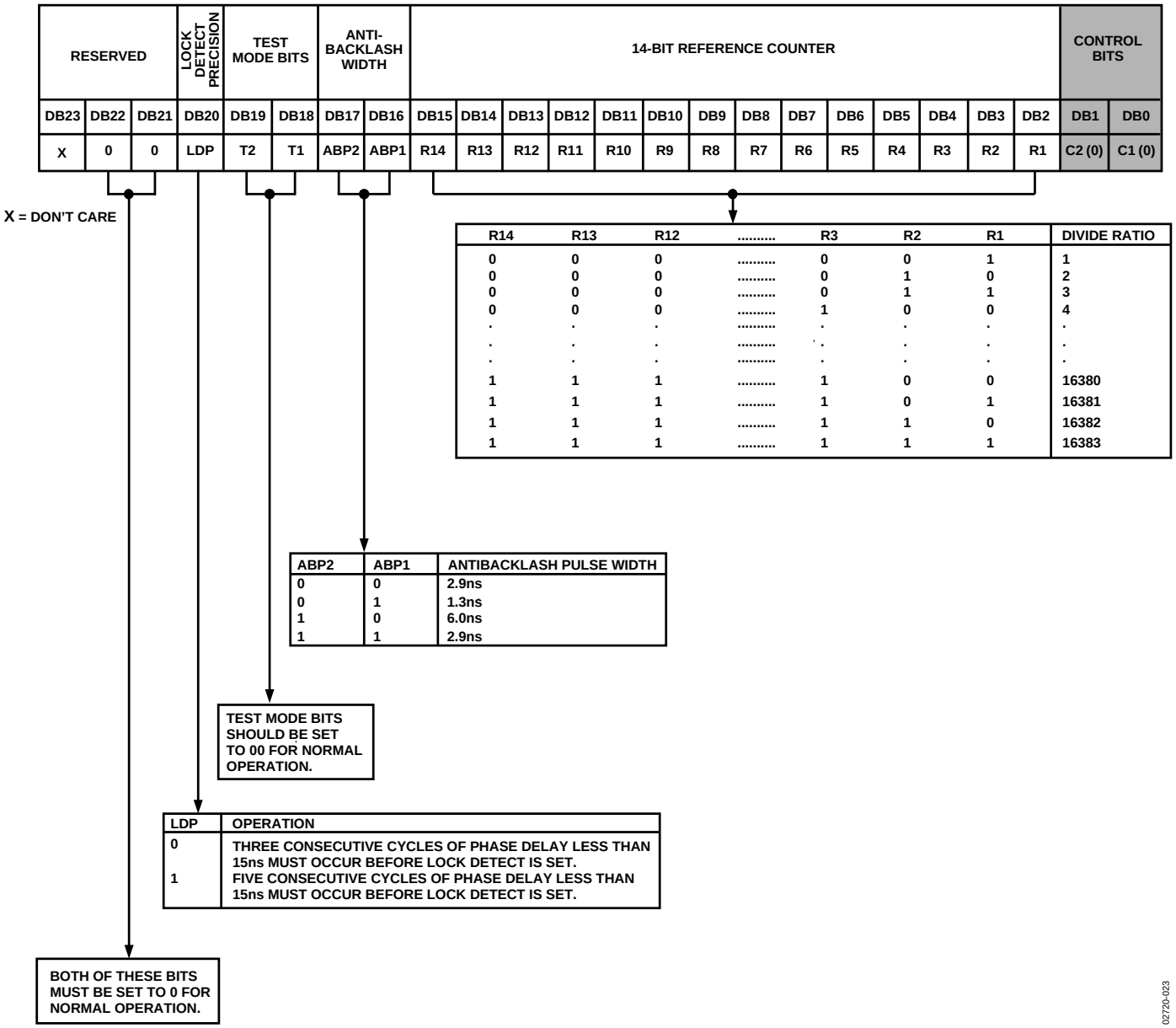


Table 8. N (A, B) Counter Latch Map

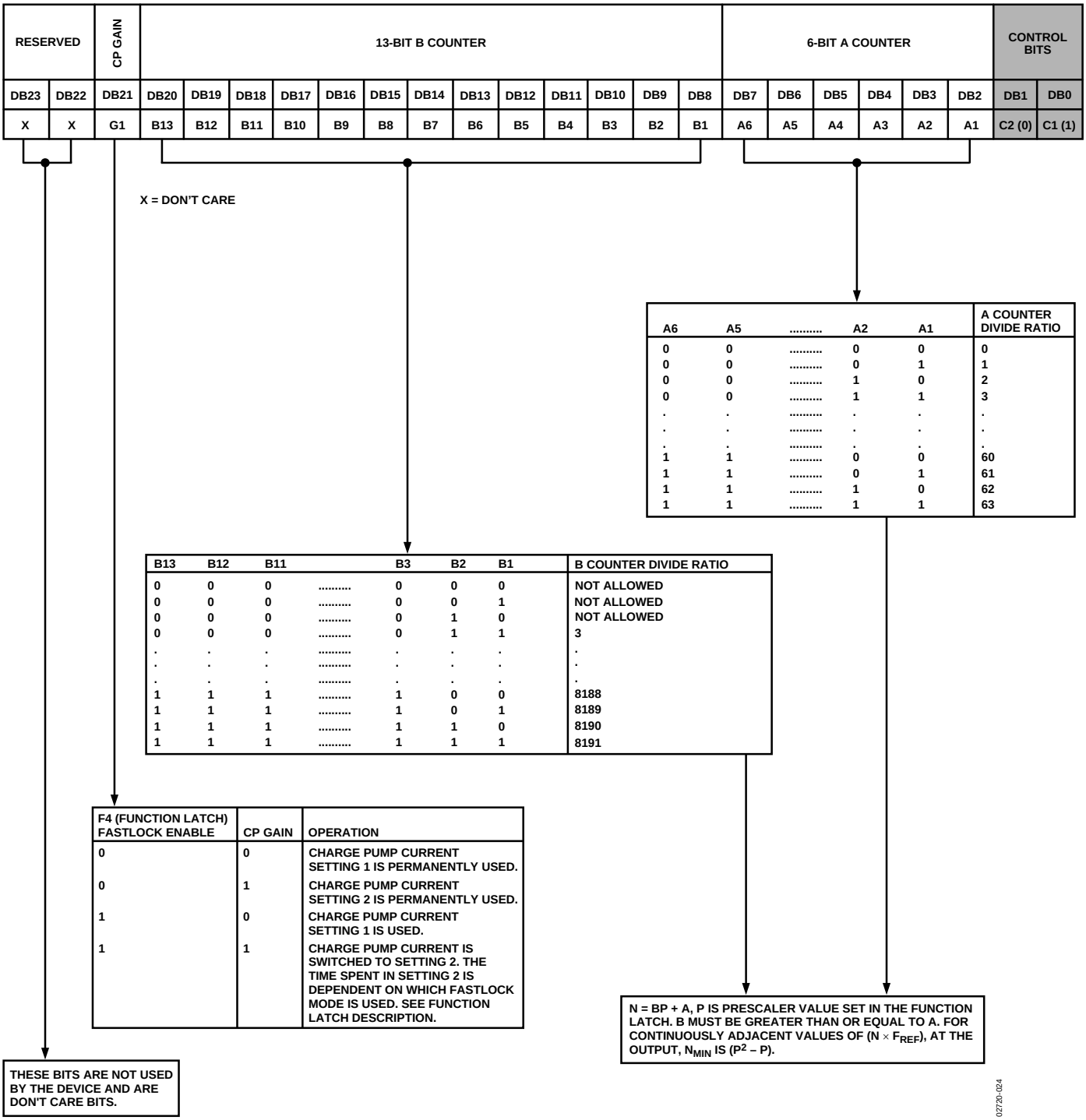


Table 9. Function Latch Map

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

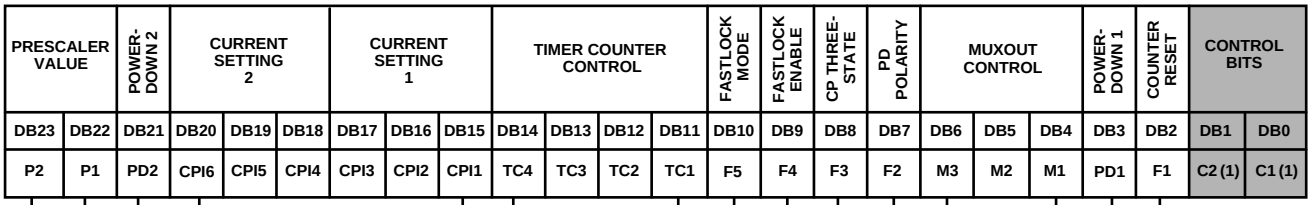
CPI6	CPI5	CPI4	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.580
0	1	0	3.18	1.875	0.870
0	1	1	4.24	2.5	1.160
1	0	0	5.30	3.125	1.450
1	0	1	6.36	3.75	1.730
1	1	0	7.42	4.375	2.020
1	1	1	8.50	5.0	2.320

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

02720-025

Table 10. Initialization Latch Map



PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CPI4	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.580
0	1	0	3.18	1.875	0.870
0	1	1	4.24	2.5	1.160
1	0	0	5.30	3.125	1.450
1	0	1	6.36	3.75	1.730
1	1	0	7.42	4.375	2.020
1	1	1	8.50	5.0	2.320

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

02720-026

THE FUNCTION LATCH

With C2 and C1 set to 1 and 0, respectively, the on-chip function latch is programmed. Table 9 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is 1, the R counter and the N (A, B) counter are reset. For normal operation, this bit should be 0. When powering up, disable the F1 bit (set to 0). The N counter will then resume counting in close alignment with the R counter. (The maximum error is one prescaler cycle).

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching 1 into the PD1 bit, with the condition that PD2 is loaded with 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing 1 into the PD1 bit (provided that 1 has also been loaded to PD2), then the device goes into power-down during the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4106 family. Table 9 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. When this bit is 1, fastlock is enabled.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fastlock when 0 is written to the CP gain bit in the N (A, B) counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fastlock under the control of the timer counter. After the timeout period, which is determined by the value in TC4 to TC1, the CP gain bit in the N (A, B) counter latch is automatically reset to 0, and the device reverts to normal mode instead of fastlock. See Table 9 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed). The normal sequence of events follows.

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as the Current Setting 2.

Simultaneously, the decision must be made as to how long the secondary current stays active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Table 9.

To program a new output frequency, simply program the N (A, B) counter latch with new values for A and B. Simultaneously, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N (A, B) counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table 9.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 325 MHz. Therefore, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

PD Polarity

This bit sets the phase detector polarity bit. See Table 9.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

THE INITIALIZATION LATCH

When C2 and C1 = 1 and 1, respectively, the initialization latch is programmed. This is essentially the same as the function latch (programmed when C2 and C1 = 1 and 0, respectively).

However, when the initialization latch is programmed, there is an additional internal reset pulse applied to the R and N (A, B) counters. This pulse ensures that the N (A, B) counter is at the load point when the N (A, B) counter data is latched and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high, PD1 bit is high, and PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse; therefore, close phase alignment is maintained when counting resumes.

When the first N (A, B) counter data is latched after initialization, the internal reset pulse is again activated. However, successive N (A, B) counter loads after this will not trigger the internal reset pulse.

Device Programming After Initial Power-Up

After initial power up of the device, there are three methods for programming the device: initialization latch, CE pin, and counter reset.

Initialization Latch Method

- Apply V_{DD}.
- Program the initialization latch (11 in two LSBs of input word). Make sure that the F1 bit is programmed to 0.
- Do a function latch load (10 in two LSBs of the control word), making sure that the F1 bit is programmed to a 0.
- Do an R load (00 in two LSBs).
- Do an N (A, B) load (01 in two LSBs).

When the initialization latch is loaded, the following occurs:

- The function latch contents are loaded.
- An internal pulse resets the R, N (A, B), and timeout counters to load-state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N (A, B) counter data after the initialization word activates the same internal reset pulse. Successive N (A, B) loads will not trigger the internal reset pulse, unless there is another initialization.

CE PIN METHOD

- Apply V_{DD}.
- Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.
- Program the function latch (10).
- Program the R counter latch (00).
- Program the N (A, B) counter latch (01).
- Bring CE high to take the device out of power-down. The R and N (A, B) counters now resume counting in close alignment.

Note that after CE goes high, a 1 µs duration may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it is programmed at least once after V_{DD} is initially applied.

COUNTER RESET METHOD

- Apply V_{DD}.
- Do a function latch load (10 in two LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
- Do an R counter load (00 in two LSBs).
- Do an N (A, B) counter load (01 in two LSBs).
- Do a function latch load (10 in two LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump but does not trigger synchronous power-down.

APPLICATIONS

LOCAL OSCILLATOR FOR LMDS BASE STATION TRANSMITTER

Figure 22 shows the ADF4106 being used with a VCO to produce the LO for an LMDS base station.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical base station system would have either a TCXO or an OCXO driving the reference input without any 50 Ω termination.

To achieve a channel spacing of 1 MHz at the output, the 10 MHz reference input must be divided by 10, using the on-chip reference divider of the ADF4106.

The charge pump output of the ADF4106 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45°.

Other PLL system specifications include:

K_D = 2.5 mA

K_V = 80 MHz/V

Loop Bandwidth = 50 kHz

F_{PFD} = 1 MHz

N = 5800

Extra Reference Spur Attenuation = 10 dB

These specifications are needed and used to derive the loop filter component values shown in Figure 22.

The circuit in Figure 22 shows a typical phase noise performance of −83.5 dBc/Hz at 1 kHz offset from the carrier. Spurs are better than −62 dBc.

The loop filter output drives the VCO, which in turn is fed back to the RF input of the PLL synthesizer and also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the system is in lock. In Figure 22, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal.

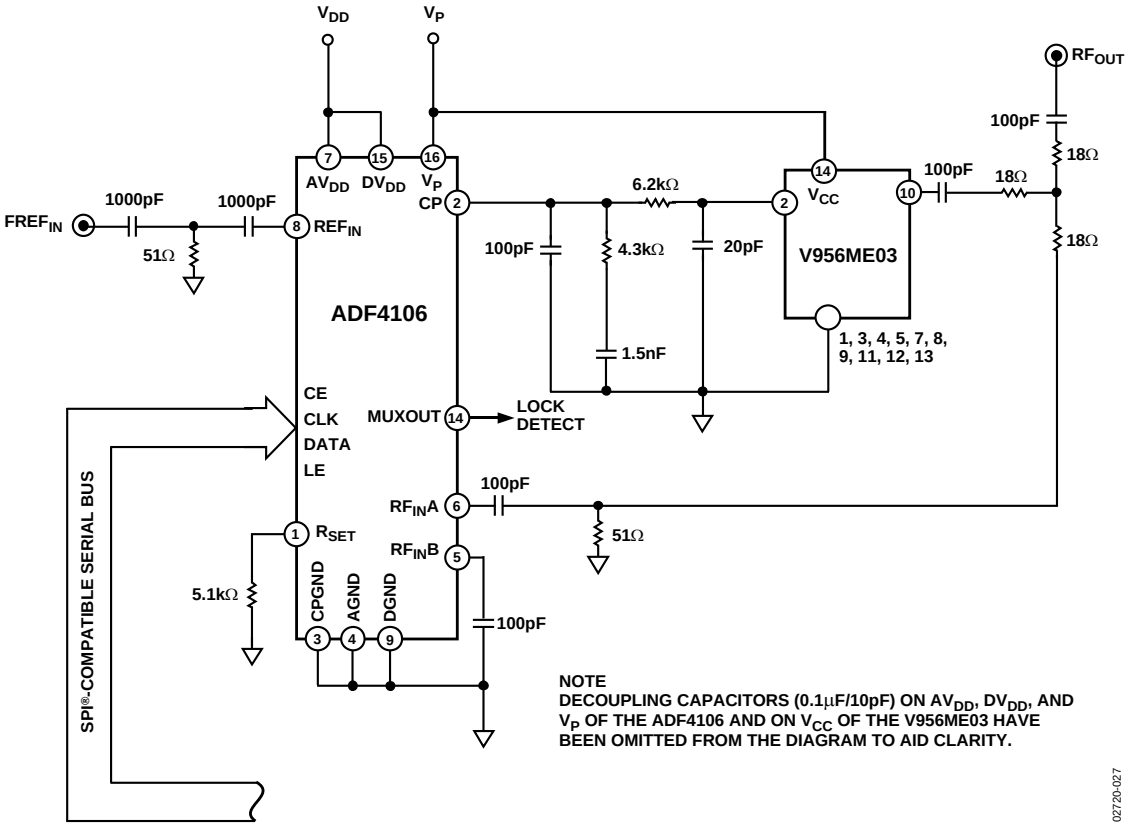


Figure 22. Local Oscillator for LMDS Base Station

INTERFACING

The ADF4106 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate for the device is 833 kHz, or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 23 shows the interface between the ADF4106 and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4106 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte is written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4106, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

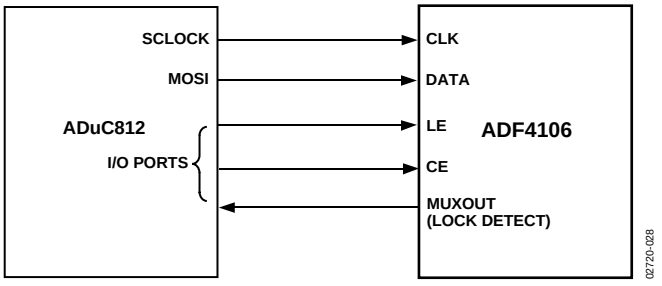


Figure 23. ADuC812-to-ADF4106 Interface

ADSP-2181 Interface

Figure 24 shows the interface between the ADF4106 and the ADSP-21xx digital signal processor (DSP). The ADF4106 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

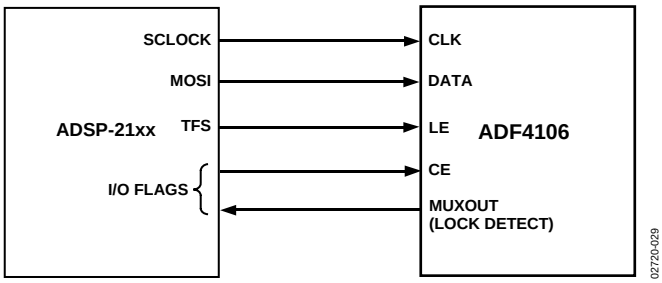


Figure 24. ADSP-21xx-to-ADF4106 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

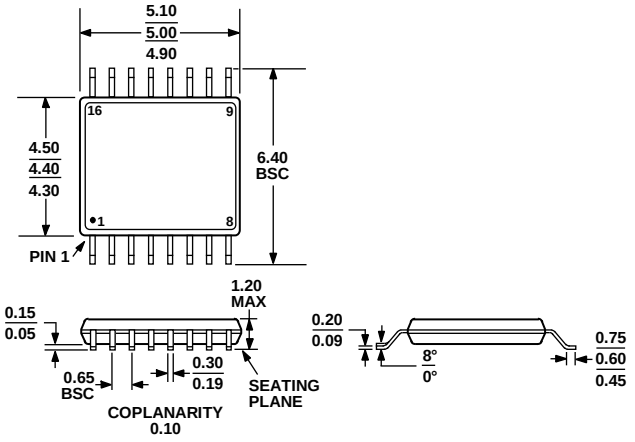
The lands on the LFCSP (CP-20-6) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central thermal pad.

The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

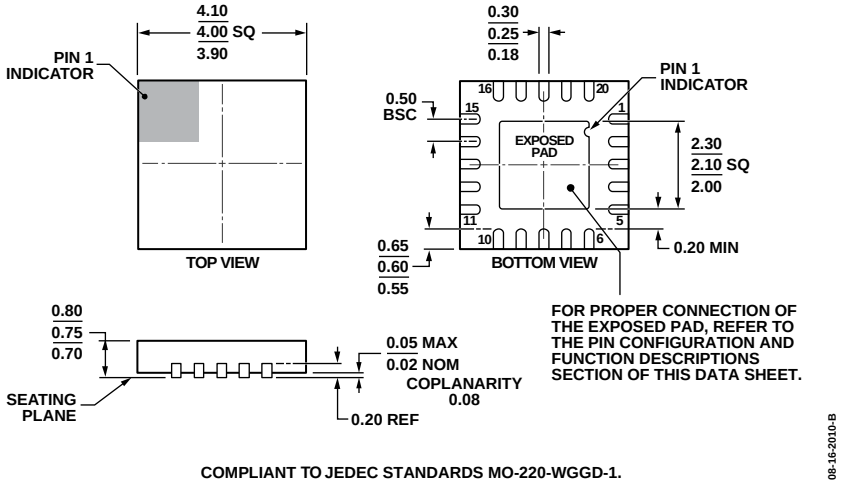
The user should connect the PCB thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 26. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4106BRU	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRU-REEL	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRU-REEL7	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRUZ	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRUZ-RL	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BRUZ-R7	–40°C to + 85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4106BCPZ	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
ADF4106BCPZ-RL	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
ADF4106BCPZ-R7	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
EV-ADF4106SD1Z		Evaluation Board	
EV-ADF411XSD1Z		Evaluation Board	

[1] Z = RoHS Compliant.

NOTES

NOTES

D02720-0-4/15(F)