ANALOG DEVICES

Programmable, Reinforced Isolation, Binary Input IC

Preliminary Technical Data

ADE1201/ADE1202

FEATURES

Binary Input Monitor Supports Wide Voltage Range:

- **10 V - 300 V**

Programmable Threshold & Filtering

Programmable Load Current

- **Pulse of up to 200mA**
- **Constant current up to 6 mA**
- **Programmable idle current**

Single 3.3V Supply

Integrated *iso*Power®, Isolated DC to DC converter

Interfaces

- **DOUTx pin reflects state of binary input**
- **Configurable using 4-wire SPI serial interface**
- **$\overline{\text{IRQ}}$ interrupt pin**

Operating temperature: −40°C to +105°C

20-lead, LGA package with 6.4mm creepage

Safety and regulatory approvals (Pending)

UL

- **3750V for 1min as per UL1577**

CSA

- **IEC 61010-1: 300 Vrms**

VDE

- **DIN VDE V 0884-11**
- **VIORM = TBD V peak**

APPLICATIONS

- Multifunction relay protection
- Substation battery monitoring
- Bay or substation interlocking
- Breaker status indication
- Remote I/O
- Merge unit
- Fault indication (alarm)

GENERAL DESCRIPTION

The ADE1201/ADE1202 is an isolated binary input monitor. It performs an isolated measurement of the binary input voltage and communicates the status of this input to low voltage processors or logic circuits. The ADE1201/ADE1202 application circuit can accept a wide range of binary input voltages from 10 V to 300 V scaled using a resistor divider before applying to the pins.

Figure 1 presents an ADE1201 applications example in a substation, where intelligent devices such as protective relays, merge units and circuit breakers include binary inputs to get information about the system around them.

The ADE1201/ADE1202 include *iso*Power®, an integrated, isolated dc-to-dc converter, eliminating the need for an external isolated power supply. The *i*Coupler® chip scale transformer technology is used to isolate the logic signals between the high voltage, isolated side and the low voltage, non-isolated side of the binary input monitor. The result is a small form factor, data and power isolation.

ADE1201 APPLICATIONS CIRCUIT EXAMPLE

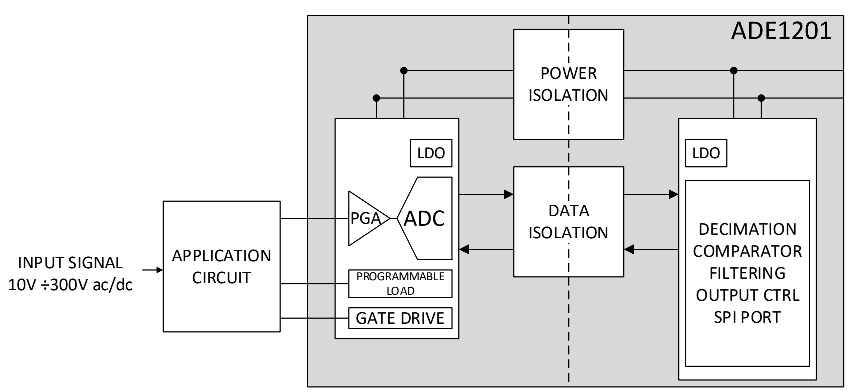

Figure 1. Typical Applications Circuit

Rev. PrK Document Feedback

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FEATURES COMPARISON: ADE1201/ADE1202

Part	No. of Channels	Programmable Load Current	Max Pulsed Current (mA)	Package
ADE1201	1	Yes	200 mA	20pin LGA
ADE1202	2	Yes	50 mA	20pin LGA

The ADE1201/ADE1202 uses an 8bit Successive Approximation Register (SAR) Analog to Digital Converter (ADC) to digitize the analog signal in INx. The input of the ADC has a Programmable Gain Amplifier (PGA). Using the PGA, the user can improve the signal resolution for small scale signals. Signal conditioning of the binary input signal is provided by configurable filters and thresholds within the ADE1201/ADE1202 registers.

The ADE1201/ADE1202 configuration and status registers are accessed via a SPI port for easy interfacing with microcontrollers. The SPI ports have CRC and write protection to improve communication robustness. Multiple ADE1201/ADE1202 devices can be operated on a single SPI bus using the broadcast mode configuration. This reduces the system configuration time. The hardware addressing mode reduces the number of chip select lines the microcontroller has to use to manage multiple ADE1201/ADE1202s.

The ADE1201/ADE1202 are available in a 20-lead, Pb-free, LGA package with 6.4 mm creepage.

The device variants are ADE1201(single channel) and ADE1202(dual channel) .

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REVISION HISTORY

FUNCTIONAL DIAGRAMS

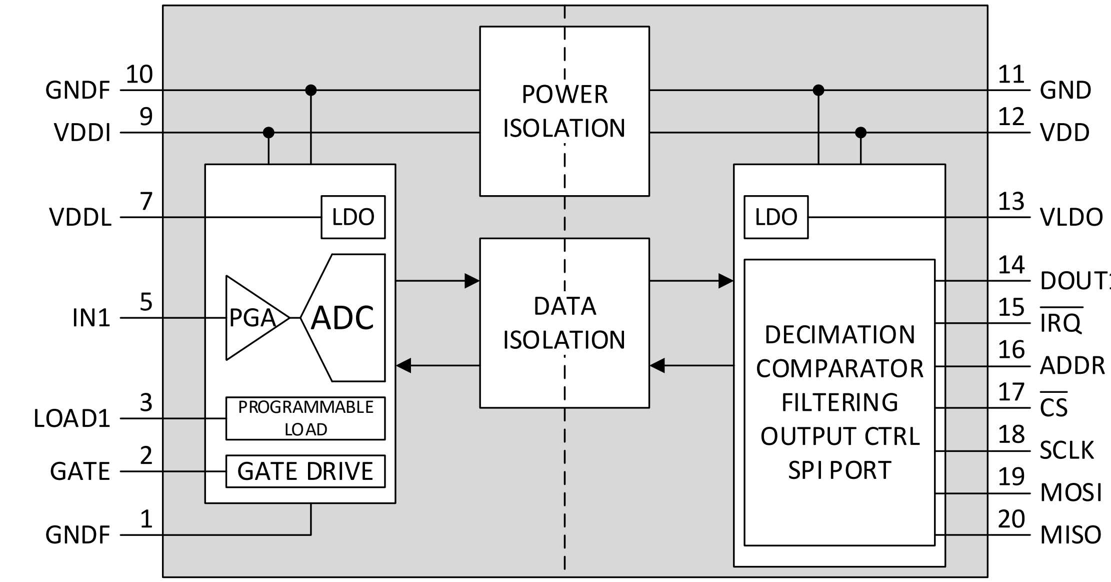

Figure 2. ADE1201 Functional Block Diagram

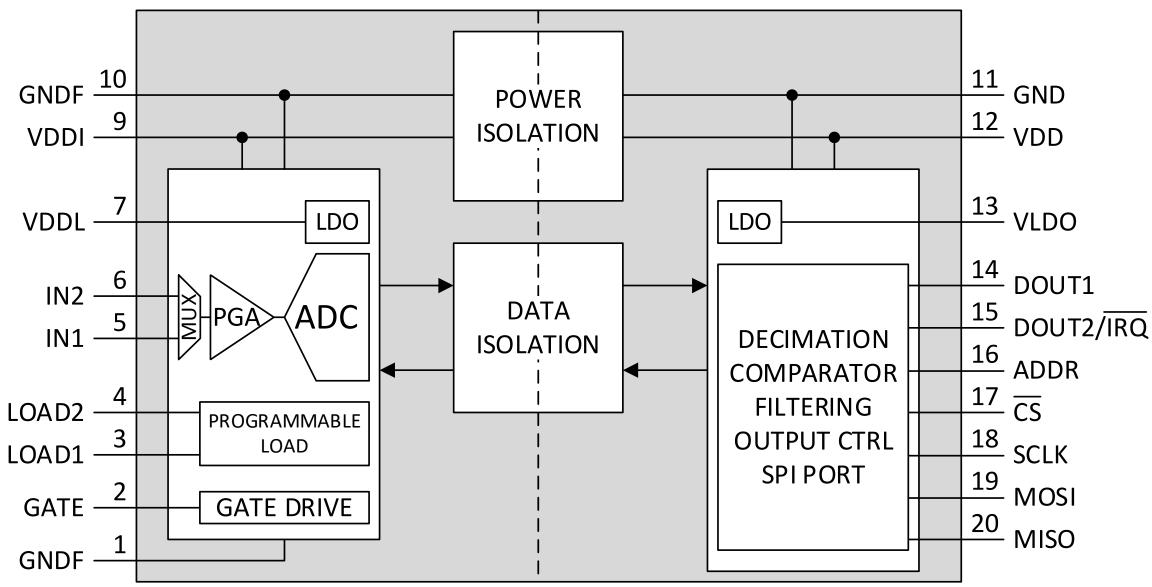

Figure 3. ADE1202 Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, T_{MIN} to T_{MAX} = −40°C to +105°C, T_A = 25°C (typical).

Table 1. Static Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS— INx					
Input Voltage Range (V_{IN})	0		1.25/ PGA	V	PGA= 1, 2, 5 and 10
Input Sampling Current (I_{INx})	-50		50	nA	PGA = 1, 2, 5 and 10
GATE DRIVE— GATE					
Output Voltage ($V_{GATENOM}$)		6.9		V	
Output Current (I_{GATE})			3.5	µA	
PROGRAMABLE LOAD— LOADx					
Leakage Resistance		56		KΩ	When LOADx is OFF
Constant Current Range	0.1		6.3	mA	
Constant Current Offset		0.1		mA	
Constant Current DAC resolution		6		bits	
Constant Current resolution		0.1		mA	
Pulsed Current Range (ADE1201)	0.2		200	mA	
Pulsed Current Range (ADE1202)	0.2		51	mA	
Pulsed Current DAC resolution		10		bits	
Pulsed Current resolution		0.2		mA	
Gain Error		0.49		%	
Offset Error		TBD		%	
Gain Drift over Temperature			5	ppm/°C	
Offset Drift over Temperature			TBD	ppm/°C	
LOGIC INPUTS— MOSI, SCLK, $\overline{CS}$					
Input High Voltage (V_{INH})	2.4			V	
Input Low Voltage (V_{INL})			0.8	V	
Input Current (I_{INH})		0.015		µA	
Input Current (I_{INL})		10		µA	
Input Capacitance (C_{IN})			10	pF	Guaranteed by design
LOGIC OUTPUTS— MISO,DOUT, $\overline{IRQ}$					
Output High Voltage (V_{OH})	2.4			V	I_{SOURCE} = 6 mA
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = 6 mA
POWER SUPPLY					
Operating Voltage Range (VDD)	2.97		3.63	V	
Supply Current (I_{DD})		TBD	TBD	mA	FET connected to ADE1201 When Pulsed current load is set to 200mA for 40.95 ms periods.
		TBD	TBD	mA	When constant current load is set to 3 mA

Table 2. SAR ADC and PGA Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPEED AND PERFORMANCE					
ADC Resolution		8		bits	No missing codes
Throughput		100		kSPS	Guaranteed By design
DC ACCURACY					
INL		0.5		LSB	Guaranteed by characterization
DNL		0.5		LSB	Guaranteed by characterization
Gain Error			2.4	%	Max overall gain settings at 25°C
Gain Error Temperature Coefficient		60		ppm/°C	
Offset Error			0.9	%	Max overall gain settings at 25°C
Offset Error Temperature Coefficient		60		ppm/°C	

TIMING CHARACTERISTICS

Table 3. Input Signal Timing Characteristics

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Signal Filter Time	0.02		82	ms	When disabled, minimum value is 0 ms
Input Signal Filter resolution		0.02		ms	
Time delay from Binary Input signal filter to Data output valid		20		µs	The binary input signal filter is bypassed
Power Up time		150		ms	R_g=10Ω, C_g= 0.1µF

Table 4. Programmable Load Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Turn ON Rise Time	t_r	TBD		TBD	µs	In High idle mode
Pulsed Current ON Time	t_{pk}			20	ms	
Turn OFF Fall time	t_f	TBD		TBD	µs	

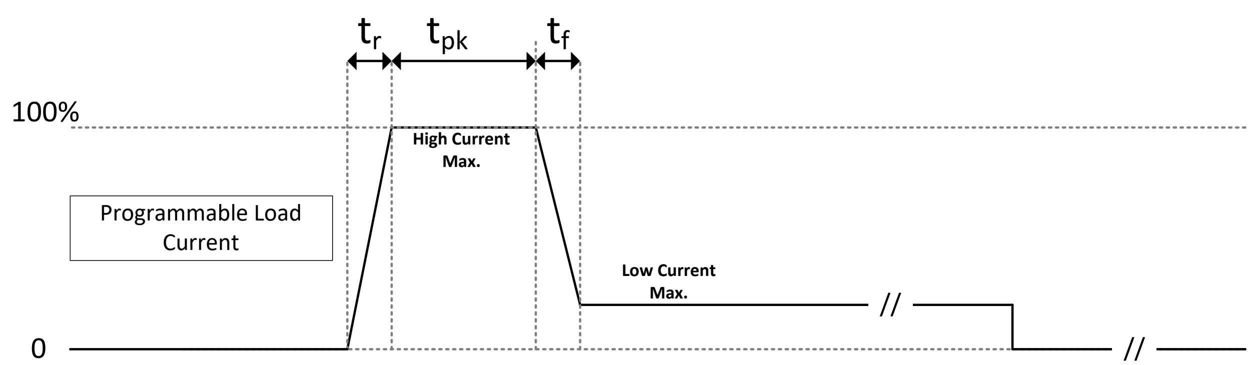

Figure 4. Programmable Load Timing Characteristics

Table 5. SPI Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}	10			ns
SCLK Frequency[1]		TBD		10	MHz
SCLK Low Pulse Width	t_{SL}	40			ns
SCLK High Pulse Width	t_{SH}	40			ns
Data Output Valid After SCLK Edge	t_{DAV}			20	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Rise Time	t_{SR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}			100	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}	0			ns

[1] Minimum and maximum specifications are guaranteed by design.

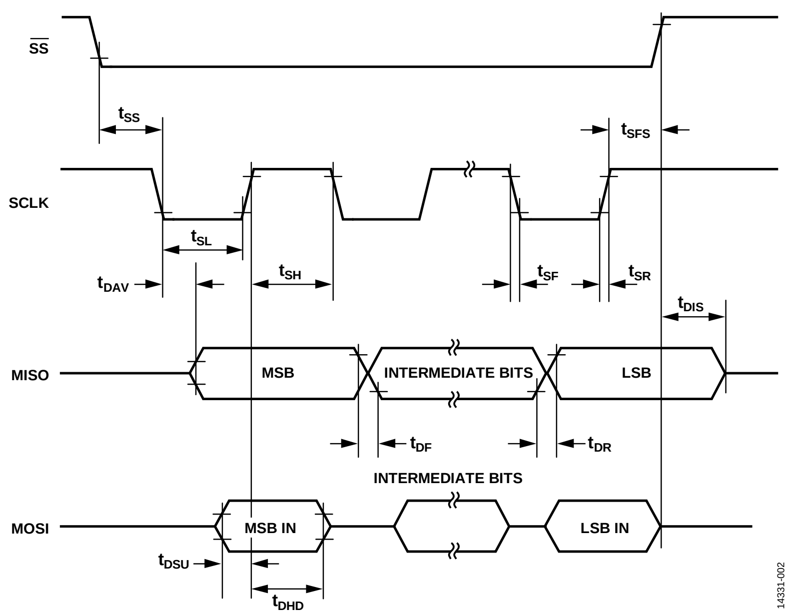

Figure 5. SPI Interface Timing

REGULATORY INFORMATION

The ADE1201/ADE1202 are pending approval by the organizations listed in Table 6.

Table 6. Regulatory Approvals

UL	CSA	VDE
Recognized Under UL 1577 Component Recognition Program Single Protection, 3750 V rms Isolation Voltage Approved under CSA Component Acceptance Notice 5A	Reinforced insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed. Based on 61010-1 C1 14.1 a) for use in 61010-1 end products because they meet the requirements of the 62368-1 evaluation (Pollution Degree 2, Material Group III, Overvoltage Category II, and III): 300 V rms (424 V peak) maximum working voltage.	Certified according to DIN VDE V 0884-10 (VDE V 0884-10):2006-12 Reinforced insulation, TBD V peak
FILE TBD	FILE TBD	FILE TBD

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 7. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	6.4	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PCB layout
Minimum External Tracking (Creepage)	L(I02)	6.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		TBD min	μm	Insulation distance through insulation
Common Mode Transient Immunity	CMTI	TBD	kV/ μs	
Insulation Resistance	R_S	TBD	kΩ	
Barrier Capacitance	C_S	1.5	pF	
Tracking Resistance (Comparative Tracking Index)	CTI	TBD	V	IEC 60112
Isolation Group		TBD		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTIC

The ADE1201/ADE1202 are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits.

Table 8. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			TBD	
Pollution Degree per DIN VDE 0110, Table 1			TBD	
Maximum Working Insulation Voltage		V_{IORM}	TBD	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	TBD	V peak
Input-to-Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		TBD	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		TBD	V peak
Highest Allowable Overvoltage		V_{IOTM}	TBD	V peak
Surge Isolation Voltage	V_{PEAK} = TBD kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	TBD	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)			
Maximum Junction Temperature		T_S	TBD	°C

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Total Power Dissipation at 25°C		P_S	TBD	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	TBD	Ω

TBD

Figure 6. Thermal Derating Curve, Dependence of Safety Limiting Values on case Temperature, per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
VDD to GND	−0.3 V to +3.7V
IN1, IN2 to GNDF	−0.2V to +2V
LOAD1, LOAD2 to GNDF	−TBDV to +TBDV
GATE to GNDF	−TBDV to +TBDV
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature	
Industrial range	-40 °C to +105 °C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	TBD °C
Lead Temperature (Soldering, 10 sec)[1]	300 °C
ESD	
Human Body Model[2]	±2kV
Machine Model[3]	
Field Induced Charged Device Model (FICDM)[4]	±1.25kV

[1]Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for latest revision of this standard.

[2] Applicable standard: ANSI/ESDA/JEDEC JS-001-2014.

[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).

[4] Applicable standard: JESD22-C101F (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

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THERMAL RESISTANCE

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 10. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
Land Grid Array (LGA)	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 11. Maximum Continuous Working Voltage Supporting a 20-Year Minimum Lifetime[1]

Parameter	Max	Unit
DC Voltage, Reinforced Insulation	300	V peak
AC Voltage, Bipolar Waveform	300	V rms

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation and Safety Related Specifications section for more details.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

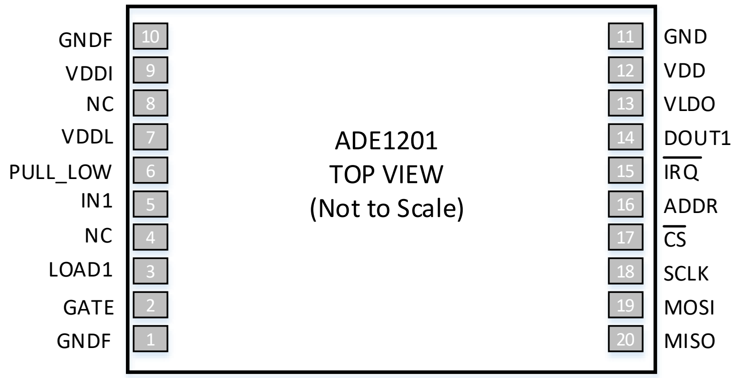

Figure 7. ADE1201 Pin Configuration

Table 12. ADE1201 Pin Function Descriptions

Pin No.	Mnemonic	Description
9	VDDI	Isolated Side Power Supply Output pin. This pin provides access to the 2.0 V on-chip isolated power supply. Do not connect external load circuitry to this pin. Decouple this pin with a 1µF ceramic capacitor using Pin 10, GNDF.
1,10	GNDF	Ground Reference of the Isolated Side. These pins provide the ground reference for the analog circuitry. Use these quiet ground references for all analog circuitry. These two pins are connected together internally.
2	GATE	Pin used to drive the gate pin of an Enhancement Mode FET.
3	LOAD1	Programmable load pin. Used to command a preset current required for loading the relay contacts.
4, 8	NC	Not connect pin. Do not connect this pin to any external circuit.
6	PULL_LOW	Connect this pin to GNDF
7	VDDL	1.8 V Output of the isolated side Low Dropout (LDO). Do not connect external load circuitry to this pin. Decouple this pin with a 1µF ceramic capacitor using Pin 10, GNDF.
5	IN1	Binary input pin. The scaled input signal is applied at this pin.
15	$\overline{\text{IRQ}}$	Interrupt pin. Provides a signal based on the settings of the internal MASK register.
16	ADDR	Address mode pin. It is used for multi-chip addressing.
14	DOUT1	Digital data output pin. It transitions to HIGH (V_{DD}) or LOW (GND) replicating the Binary Input signal at IN1 pin.
17	$\overline{\text{CS}}$	Chip Select for SPI Port.
19	MOSI	Data Input for SPI Port.
18	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock.
20	MISO	Data Output for SPI Port.
11	GND	GND pin. The system controller side ground pin.
12	VDD	Primary Supply Voltage. This pin provides the supply voltage for the ADE1201. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin with a 1µF capacitor ceramic capacitor using Pin 11, GND.
13	VLDO	1.8 V Output of the Low Dropout (LDO) Regulator. Decouple this pin with a 1µF capacitor ceramic capacitor using Pin 11, GND.

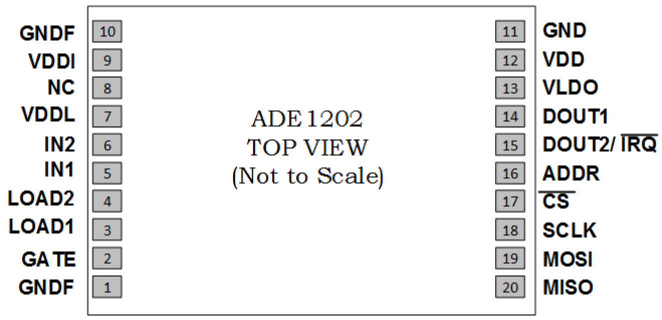

Figure 8. ADE1202 Pin Configuration

Table 13. ADE1202 Pin Function Descriptions

Pin No.	Mnemonic	Description
9	VDDI	Isolated Secondary Side Power Supply Output pins. These pins provide access to the 2.0 V on-chip isolated power supply. Do not connect external load circuitry to this pin. Decouple this pin with a 1µF ceramic capacitor using Pin 10, GNDF.
7	VDDL	1.8 V Output of the Analog Low Dropout (LDO) Regulator. Do not connect external load circuitry to this pin. Decouple this pin with a 1µF ceramic capacitor using Pin 10, GNDF.
10, 1	GNDF	Ground Reference of the Isolated Secondary Side. These pins provide the ground reference for the analog circuitry. Use these quiet ground references for all analog circuitry. These two pins are connected together internally.
5, 6	IN1, IN2	Binary input pins. The scaled input signals are applied at these pins.
3, 4	LOAD1, LOAD2	Programmable load pin. Used to command a preset current required for loading the relay contacts.
2	GATE	Pin used to drive the gate pin of an Enhancement Mode FET.
15	DOUT2/$\overline{\text{IRQ}}$	Digital data output pin. It transitions to HIGH (V_{DD}) or LOW (GND) replicating the Binary Input signal at IN2 pin. Interrupt pin. Provides a signal based on the settings of the internal MASK register.
16	ADDR	Address mode pin. It is used for multi-chip addressing.
14	DOUT1	Digital data output pin. It transitions to HIGH (V_{DD}) or LOW (GND) replicating the Binary Input signal at IN1 pin.
17	$\overline{\text{CS}}$	Chip Select for SPI Port.
19	MOSI	Data Input for SPI Port.
18	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock.
20	MISO	Data Output for SPI Port.
11	GND	GND pin. The system controller side ground pin.
12	VDD	Primary Supply Voltage. This pin provides the supply voltage for the ADE1201/1202. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple these pins with a 1µF capacitor ceramic capacitor using Pin 11, GND.
13	VLDO	1.8 V Output of the Low Dropout (LDO) Regulator. Decouple this pin with a 1µF capacitor ceramic capacitor using Pin 11, GND.

TEST CIRCUIT

TBD

Figure 9. ADE1201 Test Circuit

TERMINOLOGY

TBD

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

DETAILED DESCRIPTION

The ADE1201/ADE1202 is an isolated binary input monitor that contains a non-isolated side and an isolated side (see Figure 10 for ADE1201). The non-isolated side is supplied from the power supply of the microcontroller that manages the IC. The isolated side is supplied from an internal isolated dc to dc converter that takes the IC non-isolated side supply and creates an isolated power supply that floats on the binary input ground.

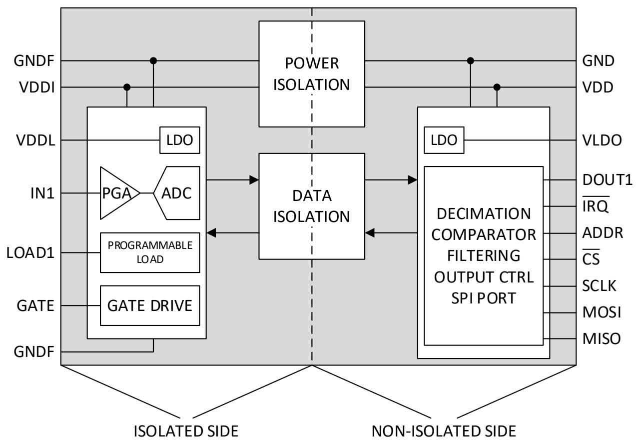

Figure 10. ADE1201 Non-Isolated and Isolated Sides

The isolated side contains a programmable gain amplifier (PGA) coupled to a successive approximation analog to digital converter (SAR ADC), a programmable load and a gate drive. The information from these blocks is transmitted to the non-isolated side through digital isolators.

The non-isolated side processes the data coming from the isolated side and creates the digital outputs DOUT1 and DOUT2 (only on the ADE1202) that reflect the status of the binary inputs from the isolated side, IN1 and IN2 (only on the ADE1202). There is a SPI port that a microcontroller can use to initialize the ADE1201/ADE1202 and to read various warnings and status bits.

POWER SUPPLY AND CONDITIONING

The ADE1201/ADE1202 is powered using a single 3.3V power supply provided at the VDD pin. Using an integrated dc-to-dc converter, the device powers the isolated high voltage side circuits. This eliminates the need for an external isolated power supply.

VDD, VLDO and GND

VDD is the power-supply pin for the ADE1201/ADE1202. Connect VDD to a 3.3V logic-level supply. Decouple the VDD pin to the GND pin with at least a 1μF capacitor and a 0.1μF ceramic capacitor placed as close as possible to the VDD pin.

The VLDO is the 1.8 V output of the internal power supply LDO. Decouple the VLDO pin to the GND pin with at least a 1μF capacitor placed as close as possible to the VLDO pin. See Figure 9.

GNDF

The GNDF pins are used to reference the high voltage side circuits after the isolation barrier. The GNDF pin located on pin 10 is used as a reference for internal isolated power supply filtering elements. The GNDF pin located on pin 1 next to the GATE pin is used for referencing and providing a current path for the internal programmable load. Both GNDF pins are required to be connected to high voltage ground plane on the printed circuit board. The detailed grounding method is described in the Layout Guidelines section.

VDDI and VDDL

The VDDI pin is the 2.0 V isolated side power supply output, while VDDL pin is the 1.8 V output of the analog LDO regulator. Decouple these pins to the GNDF pin using a 1 μF ceramic capacitor to reduce the emissions generated by the isolated dc-to-dc converter.

Note that no external component can be supplied from the isolated power supply outputs VDDI and GNDF.

Power-Up

At power-up, the following steps must be executed for a microcontroller managing a system formed by one or multiple ADE1201/ADE1202 devices:

1. Supply VDD to the ADE1201/ADE1202 devices. To ensure that the ADE1201/ADE1202 devices start functioning correctly, the supply must reach 3.3 V – 10% in less than TBD ms from approximately a 2.4 V to 2.6 V level.
2. The dc-to-dc converter powers up and supplies the isolated side of the ADE1201/ADE1202. The full devices become functional. This process takes approximately 200 ms to execute when the recommended capacitors on the VDDI and VDDL pins described in Table 12and Table 13 are used.
3. To determine when the ADE1201/ADE1202 devices are ready to accept commands, read INT_STATUS register of each device until bit 14 (RSTDONE) is set to 1.
4. Initialize the configuration registers of each ADE1201/ADE1202 using the SPI interface.
5. Lock each device by writing 0xADE1 to CONFIG_LOCK register.

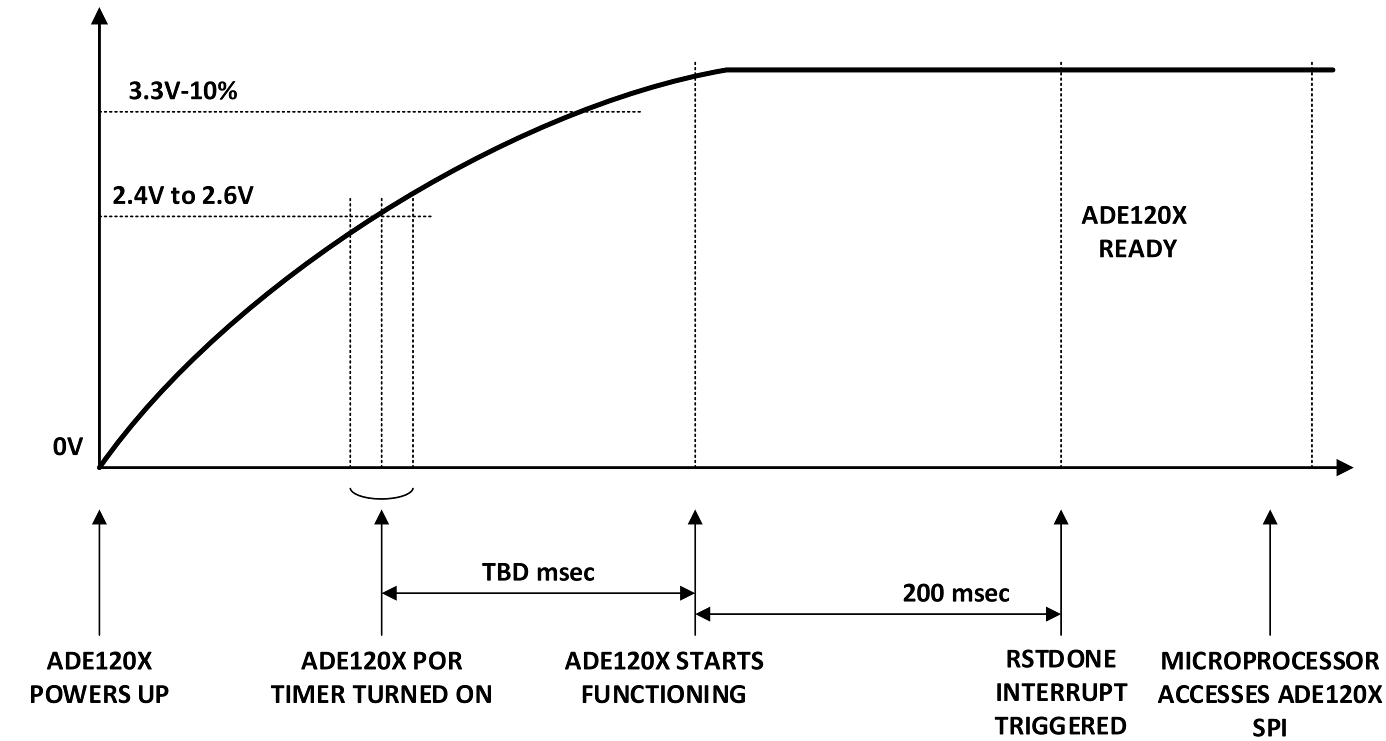

Figure 11. Power-Up procedure for Systems with ADE1201/ADE1202 Devices

BINARY INPUTS SIGNAL PATH

The device input to output signal path is shown in Figure 12. The input signal must be scaled externally using a voltage divider as shown in **Error! Reference source not found.**. The applicable voltage between the INx and GNDF pins is mentioned in Table 1. For sensing AC signals, a full bridge rectifier is required at the input before the voltage divider as shown in **Error! Reference source not found.**.

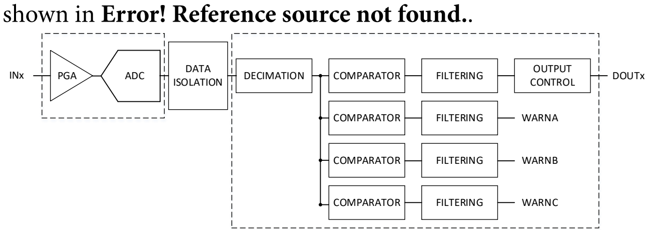

Figure 12. Binary Input Signal Path

Programmable Gain Amplifier (PGA)

The ADE1201/ADE1202 has a input programmable gain amplifier stage that allows the user to scale the input signal. The PGA has four PGA_{GAIN} gain modes presented in Table 14. The input voltage range is same as the INx Input Voltage Range (V_{IN} in Table 1 and Table 14). The gain mode is configurable over SPI by writing to the PGA_GAIN register (Address 0x201), bits 1:0 (PGA_GAIN). It is recommended to use the gain setting for a given binary input voltage that maximizes the range of the internal ADC, as shown in Table 14, without setting the system thresholds outside the range of PGA.

By default, the bits PGA_GAIN are cleared to 00, which means the PGA_{Gain} is set to 1.

Table 14. PGA Gain Settings

V_{IN}	PGA_{Gain}	Bits 1:0 in PGA_GAIN Register
1.25	1	00
0.625	2	01
0.25	5	10
0.125	10	11

Analog to Digital Converter (ADC)

As shown in Figure 12, after the programmable gain stage, the ADE1201/ADE1202 has an SAR ADC that produces 8 bit outputs. The ADC of the ADE1201 has one single channel and operates at 100 KSPS rate. The ADC of the ADE1202 has two multiplexed channels. In this case, although the ADC operates at 100 KSPS, the two INx channels are sampled at 50KSPS. The digitized data is then passed through the isolation barrier.
The Bit 15 (DREADY) in the INT_STATUS register is set to 1 every time a new ADC output is generated, which means every 100kHz for both the ADE1201 and the ADE1202. If the Bit 15

(DREADY) in the MASK register is set to 1 while all the other bits are cleared to 0, then the $\overline{\text{IRQ}}$ pin toggles to reflect the status of bit 15 (DREADY) in the INT_STATUS register. This functionality of the bit 15 (DREADY) in the INT_STATUS register is therefore different from the functionality of the other INT_STATUS register bits. See Interrupts section for details on the functionality of bits 14:0 of the INT_STATUS register. The Bit 15 (DREADY) in the STATUS register is set to 1 for 1 μs every time a new ADC output is generated. Then it is cleared to 0 automatically and remains low for 9 μs. This happens for both the ADE1201 and the ADE1202.

Decimation

The data from the ADC is passed through a decimator. The decimation filter has the same characteristics as a sampled average filter followed by decimation. The number of samples in the average is equal to the decimation rate. The decimator can be configured to decimate the data by 2, 4 or 8. The decimation can be enabled by setting Bit 0 (DECIMATE) to 1 in the BIN_CTRL register. The decimation rate is set in Bits 2:1 (DECRATE) in the BIN_CTRL register. By default, the decimator is disabled and the data from the ADC bypasses the decimator. To disable the decimator, clear the bits 2:1 (DECRATE) to 00.

Comparator and Filtering Paths

The ADE1201 has one output channel connected to the DOUT1 pin, while the ADE1202 has two output channels connected to the DOUT1 and DOUT2 pins.

Each channel data path contains a comparator and filtering path going to the DOUT1 and DOUT2 output control blocks (Figure 12). Three other comparator and filtering paths are available as warning channels: WARNA, WARNB and WARNC. The warning channels monitor the ADC data in parallel to DOUT1 and DOUT2 and can be configured to perform binary measurements. The warning channels can be configured to provide warnings to the user based on different criteria than the one used in the path of the DOUTx pin. Warning channels are read over SPI interface.

All four comparators use individual thresholds, a high threshold level and a low threshold level. The thresholds are programmable between 0x00 and 0xFF. An INx voltage of 1.25V/PGA translates to 0xFF. The threshold code can be derived by scaling the preferred threshold voltage to the above relationship:

$$THR = \frac{THRESHOLD(V)}{\frac{1.25}{PGA}} \times 255$$

Where: THRESHOLD (V) is the desired threshold level expressed in Volts and THR is the value that is written in the following control registers: BIN_THR, WARNA_THR, WARNB_THR and WARNC_THR.

The register BIN_THR contains the thresholds of the DOUT1 and DOUT2 data paths, while WARNA_THR, WARNB_THR and WARNC_THR registers contain the thresholds of the warning channels.

Every comparator has four configurable modes: Hysteretic, Midrange, Greater Than and Lesser Than. They are selected by Bits BIN_MODE, WARNA_MODE, WARNB_MODE, WARNC_MODE in BIN_CTRL register. After reset, the DOUT1 and DOUT2 channels are in Hysteretic mode, the WARNA channel is in Greater Than mode, WARNB is in Midrange mode, and WARNC is in Lesser Than mode.

Comparator in Hysteretic Output Mode

In the hysteretic output mode, when the ADC output is greater than the high threshold level of the comparator, the output is set high. The output is set low when the ADC output drops below the low threshold level. The behavior of the comparator in the hysteretic output mode is shown in Figure 13.

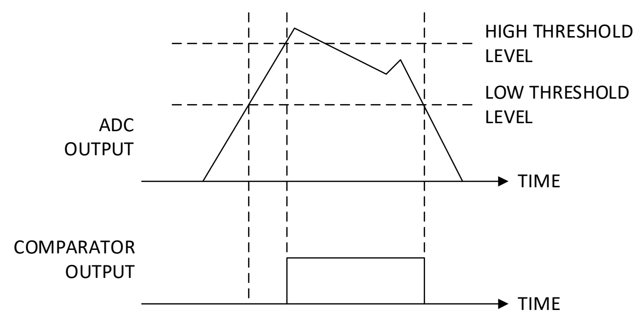

Figure 13. Comparator Behavior in Hysteretic Output Mode

Comparator in Midrange Output Mode

In the midrange output mode, when the ADC output is less than the high threshold level and greater than the low threshold level, the comparator output is set high. The output is set low when the ADC output drops below the low threshold level or goes above the high threshold level. The behavior of the comparator in the midrange output mode is shown in Figure 14.

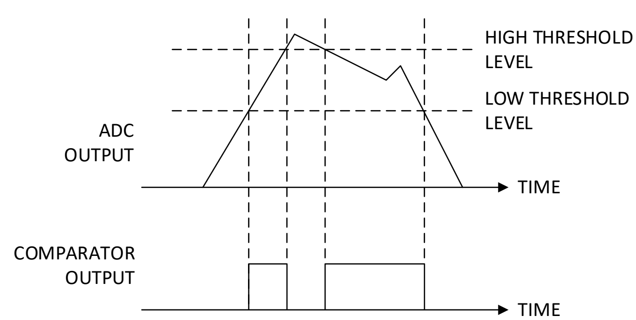

Figure 14. Comparator Behavior in Midrange Output Mode

Comparator in Greater Than (GT) Mode

In greater than (GT) output mode, when the ADC output is greater than the high threshold level, the comparator output is set high. The comparator output is set low when the ADC output drops below the high threshold level. The behavior of the comparator in the GT output mode is shown in Figure 15.

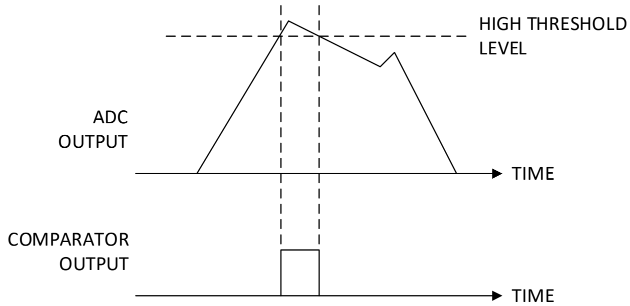

Figure 15. Comparator Behavior in Greater Than (GT) Output Mode

Comparator in Lower Than (LT) Mode

In lesser than (LT) output mode, when the ADC output is lower than or equal to the high threshold level, the comparator output is set high. The comparator output is set low when the ADC output is greater than the high threshold level. The behavior of the comparator in the LT output mode is shown in Figure 16.

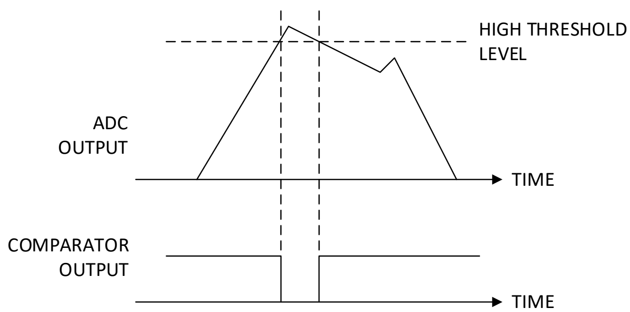

Figure 16. Comparator Behavior in Lower Than (LT) Output Mode

Glitch Filtering

After the comparators, the ADC outputs pass through a glitch filter. Each data path has its own glitch filter. The registers BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER manage the glitch filters.

The filters may be enabled by setting Bit 15 of the filter registers BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER.

The glitch filter consists of a counter that increments every 10 µs for the ADE1201 and every 20 µs for the ADE1202. The filter length is set by the user in the Bits 12:0 of the filter registers BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER. The maximum length of the filter is 163.82 ms for both the ADE1201 and ADE1202. Any input glitch lower than the filter length is rejected and the filter output is left unchanged. A filter length of 0 means the filter is bypassed.

$$FilterLength = \frac{GlitchWidth(\mu s)}{N \times GlitchUpdate}$$

Where:

- GlitchWidth is the desired length of the filter expressed in µs
- N is 2 in the case of ADE1201 and 1 in the case of the ADE1202
- GlitchUpdate is 10 µs for the ADE1201 and 20 µs for the ADE1202
- FilterLength is the number that is written in the filter registers: BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER.

There are two modes in which the glitch filter may function, managed by Bit 14 in of the filter registers BIN_FILTER, WARNA_FILTER, WARNB_FILTER, and WARNC_FILTER. If Bit 14 is 0, the default value, the mode is called Up/Clear. If Bit 14 is 1, the mode is called Up/Down.

In the Up/Clear mode, the filter counter increments when the comparator output, that is the filter input is high and it is cleared to 0 when the filter input is low. When the counter reaches the filter limit, it sets the filter output to high and stops incrementing. See Figure 17 for an example of the glitch filter working in the Up/Clear mode.

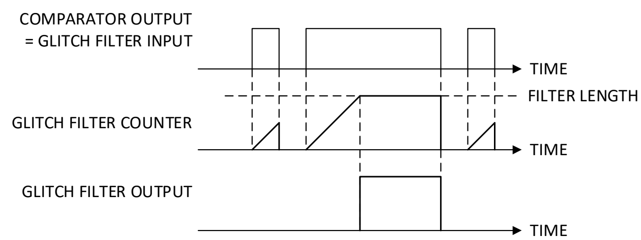

Figure 17. Glitch Filter in Up/Clear Mode

In the Up/Down mode, the filter increments when the comparator output, that is the filter input is high and is decremented when the filter input if low. When the counter reaches the filter limit, it sets the filter output to high and stops incrementing. When the filter input is low, the output stays high until the counter decrements to 0 and it stays low after the counter reached 0. See Figure 18 for an example of the glitch filter working in Up/Down mode.

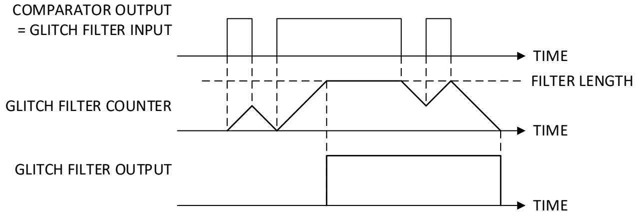

Figure 18. Glitch Filter in Up/Down Mode

INVALID MODE

When the MCU configures the ADE1201/ADE1202, it must disable the registers protection (see Protecting the Integrity of Configuration Registers section) and then initializes the configuration registers. During this time, the state of the DOUT1 and DOUT2 (available only on the ADE1202) pins cannot be trusted to correlate to the IN1 and IN2 input signals. The IC is in a state called invalid mode. This state lasts until the MCU enables the registers protection. The ADE1201/ADE1202 exits the invalid mode state and starts functioning normally.

During invalid mode, the ADE1201/ADE1202 provides an output based on the bits 5:4 (INVALID_MODE) and bit 3 (FORCEVAL) of the BIN_CTRL register.

If INVALID_MODE bits are equal to 00, DOUT1 and DOUT2 are set to the FORCEVAL value. If they are equal to 01, DOUT1 and DOUT2 are set to the binary input filter output. If they are equal to 10, DOUT1 and DOUT2 toggle the value they had upon entering this mode. If they are equal to 11, DOUT1 and DOUT2 hold the current value.

PROGRAMMABLE LOAD CURRENT

In substation application, when the binary input first switches on to a high voltage state, a high current on the order of 100 mA is normally drawn for a short period of time, on the order of 20 ms. This current is present to remove oxidation from the relay contacts and is called wetting current. It also has the role to act as a filter if during a fault, the input voltage goes high. In this case, the programmable load pulls the input voltage low to defeat the fault.
After the high current pulse, a constant current is drawn while the input is on (high). This constant current allows the driving circuit to verify the connection to the binary input and improves the EMC immunity of the circuit. This current draw is typically in the range of a few mA and can be an issue for higher input voltages due to heat dissipation required.
When the binary input voltage is high, the ADE1201/ADE1202 sets the load current and the FET limits the voltage to the LOAD1 or LOAD2 pins. When the binary input voltage is low, the ADE1201/ADE1202 tries to set a current to verify the relay status. This is called the idle current.

The ADE1201/ADE1202 programmable load current block diagram is shown in Figure 19. The input impedance of the programmable load is 28 kΩ for the ADE1201 and 56 kΩ for the ADE1202.

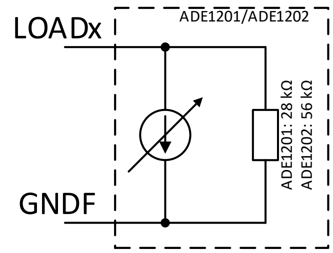

Figure 19. Programmable Load Block Diagram

When the binary input switches on to a high voltage, the ADE1201/ADE1202 injects a pulsed current load for a determined period of time and then switches to a constant current. The constant current minimizes the power dissipation in the FET and protects it.
When the binary input switches off to a low voltage, the programmable load can function in High idle mode or in Low idle mode by setting the Bit 0 (PL_MODE) in PL_CTRL register to 1 or respectively 0 (default value).
The High idle mode is used to create a fast response to a surge event.

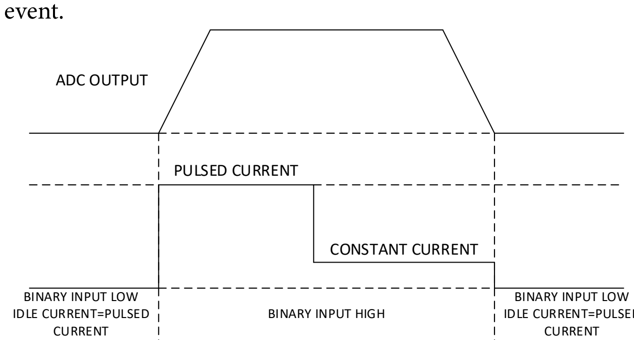

Figure 20. Programmable Load Current Waveform in High Idle Mode

Figure 20 presents the behavior of the ADE1201/ADE1202 when the programmable load functions in High idle mode. In the beginning the relay is open and the binary input is low. Then the relay closes and the binary input becomes high. The cycle ends when the relay closes and the binary input becomes back low. The programmable load allows for a pulsed current level set in Bits 9:0 (HIGH_CODE) of the PL_HIGH_CODE register:

$$HIGH\_CODE = \frac{Pulsed\ Current\ (mA)}{0.2}$$

where Pulsed Current is the desired current level expressed in mA. The resolution of the Pulsed Current is 0.2 mA. The maximum current is $(2^{10}-1)\times0.2 = 204.6$ mA in case of the

ADE1201. In case of the ADE1202, the maximum current is 51 mA.

The recommended range of the Pulsed current is between 20 mA and 200 mA, HIGH_CODE = 100 to 1000, although the minimum current that can be set is 0.2 mA, HIGH_CODE=1.

The pulsed current is applied for a time period set in Bits 11:1 (HIGH_TIME) in the PL_HIGH_TIME register:

$$HIGH\_TIME = \frac{Pulsed\ Current\ Period(\mu s)}{10}$$

where Pulsed Current Period is the desired time period expressed in µs. The resolution of the pulsed current period is 10 µs. The maximum period is $(2^{12}-1)\times 10$ (µs) = 40.95 ms.

After the pulsed current period, the programmable load switches to a constant current level set in Bits 5:0 (LOW_CODE) in the PL_LOW_CODE register:

$$LOW\_CODE = \frac{Constant\ Current\ (mA)}{0.1}$$

Where the Constant Current is the desired current level expressed in mA. The resolution of the Constant Current is 0.1 mA. The maximum current that can be set is $(2^{6}-1) \times 0.1 = 6.3$ mA.

When the binary input is low, the ADC output is low and the programmable load tries to set a current level called idle current. In High idle mode, this current is equal to the pulsed current level set in Bits 9:0 (HIGH_CODE) of the PL_HIGH_CODE register.

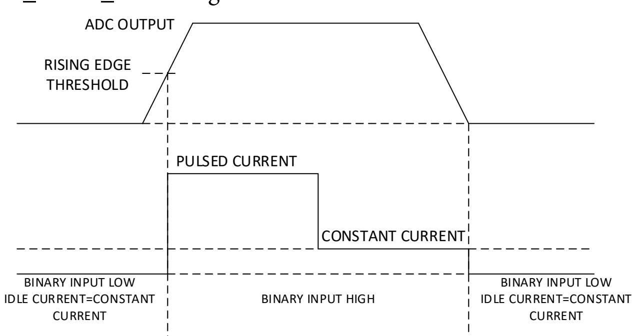

Figure 21. Programmable Load Current Waveform in Low Idle Mode

Figure 21 presents the behavior of the ADE1201/ADE1202 during a cycle of relay off/on when the programmable load functions in Low idle mode. These are the differences between the Low idle mode and the High idle mode:

When the binary input switches on to a high voltage and the ADC output changes from low to high, the pulsed current is generated after the ADC output reaches a rising edge threshold set in Bits 7:0 (RISE_THR) in the PL_RISE_THR. The Pulsed Current Period remains the same as in the High Idle Mode. Note that RISE_THR is not used in the High Idle Mode.

When the binary input is low, the idle current is equal to the constant current level set in the PL_LOW_CODE register.

FET Protection

The FET protection function monitors the approximate FET energy by tracking the programmed load current and measured binary input voltage over time. The ADC output, a measure of the binary input voltage, is accumulated at a 100 kHz rate when a pulse current state is asserted. Once the accumulation reaches a user programmed limit threshold that is function of the programmed current load, the pulsed current is turned off for a cool down period. The threshold is set in the EGY_MTR_THR register and is calculated according to the following expression:

$$EGY\_MTR\_THR = \\ = \frac{EnergyTHR(J) \times AccFreq(Hz) \times ADC\_FS}{PulsedCurrent(A) \times V\_FS(V) \times 2^7}$$

Where:

EnergyTHR(J) is the energy that can be safely dissipated by the FET. It is expressed in Joules.

AccFreq(Hz) is the accumulation frequency of 100kHz. It is expressed in Hz.

ADC_FS is the full scale ADC output, that is 255.

PulsedCurrent(A) is the pulsed current setting in the programmable load. It is expressed in Amps.

V_FS(V) is the ADC input voltage that corresponds to the full scale ADC output.

When the ADC output is equal to 0xFF in a pulsed current state, this may indicate the IN1 or IN2 input voltages are greater than the ADC input voltage range. The FET may reach the limit of the safe operating area much faster and the FET protection may have to be triggered much sooner. The bits 7:6 (OV_SCALE) in the EGY_MTR_CTRL register may be set to scale up the instantaneous accumulator adder for that energy sample to account for this eventual situation. When OV_SCALE is 00, the overvoltage scale factor is 1, 01 means a factor of 4, 10 means a factor of 8 and 11 means a factor of 16. The single pulse increase of the accumulator is calculated according to the following expression:

$$SinglePulseIncrease = \frac{ADC\_FS \times t_{PulseCurrent} \times OV\_SCALE \times AccFreq(Hz)}{2^7}$$

Where: $t_{PulseCurrent}$ is the pulsed current period expressed in seconds.

Once the monitored FET energy reaches the user programmed energy limit threshold, the pulsed current is turned off for a cool down period. The cool down period expressed in seconds is set in bits 3:0 (COOLDOWN_SEC) in the EGY_MTR_CTRL register (Address 0x015). If COOLDOWN_SEC bits are cleared to 0, the cooldown functionality is disabled, the load current is not turned off and the accumulator is forced to zero. The accumulator is decremented outside of the pulsed current period by a quantity set in the bits 15:8 (COOLDOWN_DECR) in the EGY_MTR_CTRL register. The decrement frequency is set in the bits 5:4 (COOLDOWN_TIMESTEP) in the EGY_MTR_CTRL register and it may be 10 µs (when bits 5:4=00), 20 µs (when bits 5:4=01), 40 µs (when bits 5:4=10) and 80 µs (when bits 5:4=11). If the ADE1201/ADE1202 is in the cooldown period, the accumulator is not decremented.

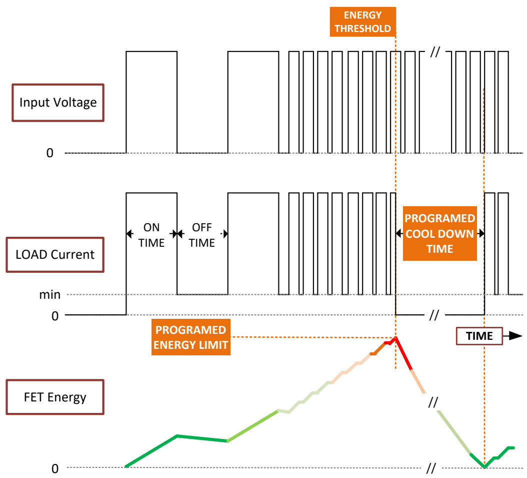

Figure 22. Energy limit function implemented by Programmable Load for a user programmed cool down time

GATE DRIVE

The GATE pin is used to drive an external high voltage Enhancement Mode MOSFET (Q1). After power up, the GATE pin is biased at a voltage $V_{GATENOM}$ to allow Q1 to conduct while protecting the load pin LOADx as shown in Figure 23. An external gate current limiting resistor (RG) 10Ω and gate capacitor (CG) 0.1µF are required. The limits of the GATE pin are stated in Table 1.

During a Pulsed Current, $V_{GATENOM}$ is regulated to reduce the voltage on the LOADx pin to a minimum voltage V_{PLREG} to allow for FET mismatches while minimizing the power consumed during pulsed current. For ADE1201, V_{PLREG} is 0.6V. For ADE1202, V_{PLREG} is 2.8V, if only a single MOSFET is conducting. If both MOSFETs are conducting, V_{PLREG} is 0.6V. After a pulsed current period, the GATE voltage is regulated back to $V_{GATENOM}$.

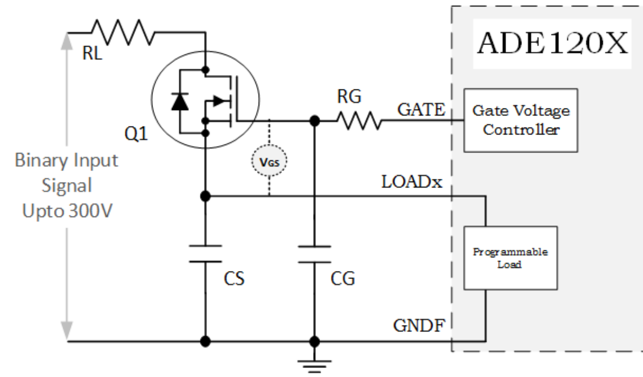

Figure 23. MOSFET Gate Control

INTERRUPTS

The ADE1201/ADE1202 has one interrupt pin, $\overline{IRQ}$. On the ADE1201, it is a stand alone pin. On the ADE1202, it is multiplexed with the DOUT2 pin. Use bit 2 (IRQ_PIN_MODE) in the CTRL register to select it. If bit is cleared to 0, the default, the pin functionality is DOUT2. If the bit is 1, the pin is assigned to $\overline{IRQ}$.

The $\overline{IRQ}$ pin is managed by a 16-bit interrupt mask register, MASK. To enable an interrupt, the appropriate bit in the MASK register must be set to 1. To disable an interrupt, the bit must be cleared to 0. One status register, INT_STATUS, is associated with the interrupt. There is a second status register, STATUS, that contains bits identical to the bits in the INT_STATUS (see STATUS register section for details). The INT_STATUS register flags are latched when they become 1 and must be written to 1 to clear, while the STATUS register flags reflect the real time status of the flags (see STATUS register section).

When the interrupt is triggered, the $\overline{IRQ}$ pin goes low. To determine the source of the interrupt, the microcontroller (MCU) reads the INT_STATUS register to identify which bit is set to 1. To clear the flag in the INT_STATUS register, the MCU writes back to the INT_STATUS register with the flag set to 1. The $\overline{IRQ}$ pin remains low until the status flag is cleared.

By default, all interrupts are disabled with the exception of the RSTDONE interrupt. This interrupt cannot be disabled (masked) and, therefore, Bit 14 (RSTDONE) in the MASK register has no function. During power up or until a software reset ends, the $\overline{IRQ}$ pin stays high. When the power up process ends or when the software reset ends, the bit 14 (RSTDONE) in INT_STATUS register is set to 1 and the $\overline{IRQ}$ pin goes low. To cancel the status flag and bring the $\overline{IRQ}$ pin high, the INT_STATUS register must be written with Bit 14 (RSTDONE) set to 1. On the ADE1202, the $\overline{IRQ}$ pin is not by default available, being multiplexed with DOUT2. In this case, at power up or after a software reset, the MCU reads INT_STATUS register until bit 14 (RSTDONE) is set to 1 to identify when the ADE1202 is ready to operate normally.

Note that bit 15 (DREADY) of the INT_STATUS and MASK registers functions differently than the bits 14:0. See Analog to Digital Converter (ADC) section for details on the functionality of the DREADY bits.

STATUS register

The INT_STATUS register contains status flags that remain set until the MCU clears them, while the STATUS register contains status flags that are updated in real time. When the condition related to a flag is triggered, the flag is set to 1. When the condition disappears, the flag is cleared to 0 automatically.

The bits in the STATUS register are identical with the bits in the INT_STATUS register, with one exception: Bit 14, which is RSTBUSY in the STATUS register, while being RSTDONE in INT_STATUS. The Bit RSTDONE has been explained in the Interrupts section. The Bit RSTBUSY is 1 after the ADE1201/ADE1202 is reset and becomes 0 when the chip is ready to accept commands.

SPI PROTOCOL OVERVIEW

The ADE1201/ADE1202 has an SPI-compatible interface, consisting of four pins: SCLK, MOSI, MISO, and $\overline{CS}$. The ADE1201/ADE1202 is always an SPI slave. The SPI interface is compatible with 16-bit read/write operations. The maximum serial clock frequency supported by this interface is 10MHz.

The $\overline{CS}$ input pin is the chip select input. Drive the $\overline{CS}$ pin low for the entire data transfer operation. Bringing the $\overline{CS}$ pin high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can be initiated by returning the $\overline{CS}$ pin low. Every time a register is written, its value should be verified by reading it back.

Data shifts into the ADE1201/ADE1202 at the MOSI pin on the falling edge of SCLK, and the ADE1201/ADE1202 samples it on the rising edge of SCLK. Data shifts out of the ADE1201/ADE1202 at the MISO pin on the falling edge of SCLK and is sampled by the MCU on the rising edge of SCLK. The most significant bit of the word is shifted in and out first. MISO stays in high impedance when no data is transmitted from the ADE1201/ADE1202.

Figure 24 shows the connection between the ADE1201/ADE1202 SPI interface and a master device that contains an SPI interface.

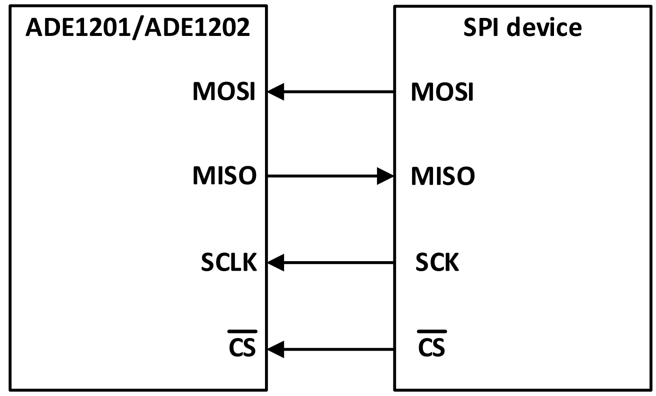

Figure 24. Connecting the ADE1201/ADE1202 SPI Interface to an SPI Device

SPI ADE1201/ADE1202 Addressing

Up to 8 ADE1201/ADE1202s may be accessed on the same SPI bus. A voltage ladder of up to seven equal resistors ranging from 1 kΩ to 10 kΩ values, 5% tolerance, may be used (Figure 26). The ADE1201/ADE1202 whose ADDR pin is connected to 3.3 V has the chip address of 7, while the ADE1201/ADE1202 whose ADDR pin is connected to ground has the chip address of 0. The remaining six ADE1201/ADE1202s have the chip address in sequence based on the applied voltage of the potential divider.

The chip address is indicated in the bits 2:0 of the 16-bit command header:

15	14 … 4	3	2 … 0
BROADCAST	REGISTER ADDRESS	R/$\overline{W}$	CHIP_ADDR

Figure 25. SPI Header Word

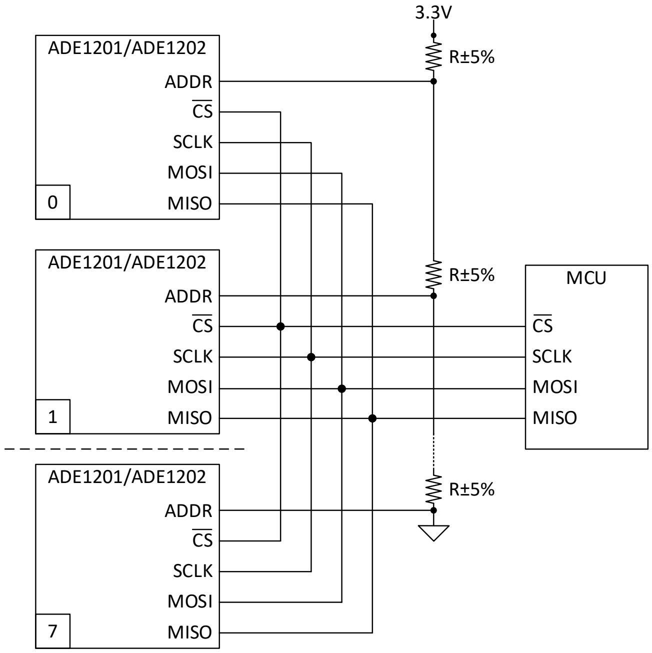

Figure 26. ADE1201/ADE1202 SPI Addressing Mode

SPI Write Operation

A write operation using the SPI interface of the ADE1201/ADE1202 is initiated when the MCU sets the $\overline{CS}$ pin low and begins sending a 16-bit command word, representing the slave address of the ADE1201/ADE1202 on the MOSI line (Figure 27).

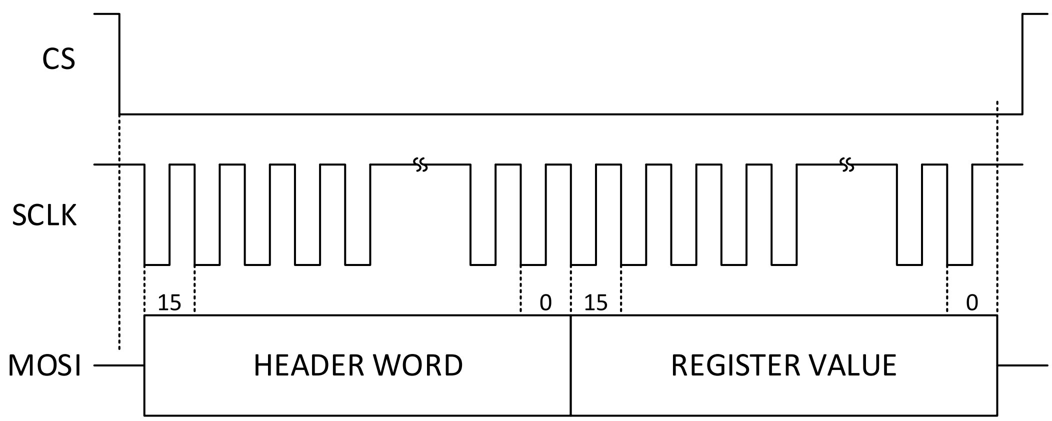

Figure 27. SPI Write Operation

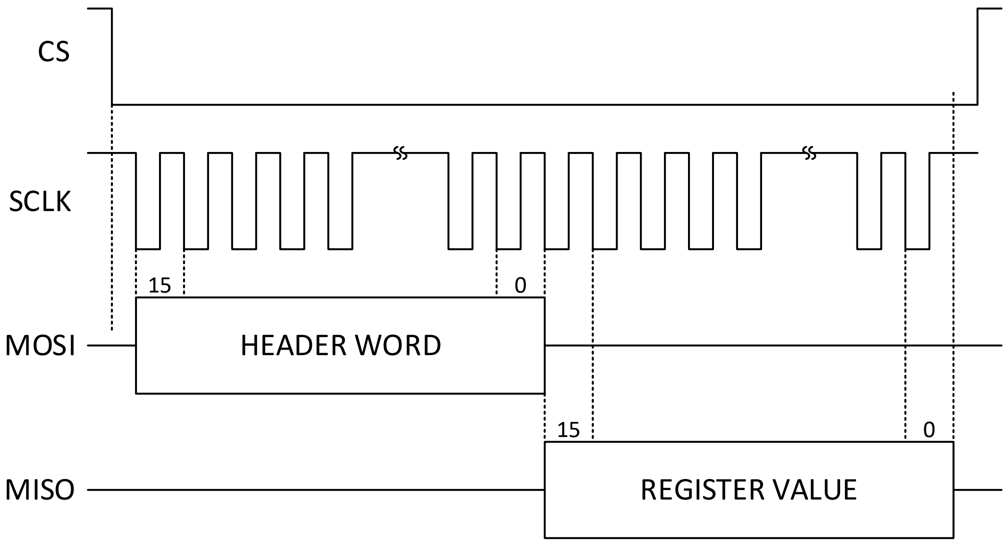

Figure 28. SPI Read Operation

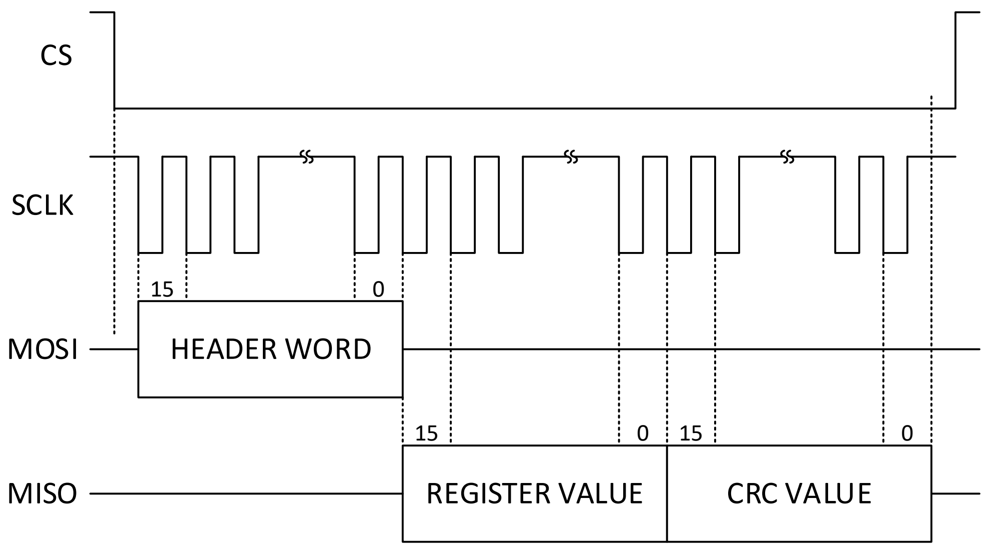

Figure 29. SPI Read Operation with Appended CRC

To execute a write operation, bit 3 of the command header must be cleared to 0 (Figure 25).

The address of the ADE1201/ADE1202 register to be written is indicated in the bits 14:4 of the command header.

Every time a register is written, its value should be verified by reading it back.

If multiple ADE1201/ADE1202s are placed on the same SPI bus (as shown in Figure 24) and the same register in multiple chips must be initialized with an identical value, the broadcast write functionality is available. Set bit 15 in the SPI header word to 1 to enable a broadcast write. The Bits 2:0 (CHIP_ADDR) of the header word that indicate the chip address on the SPI bus are ignored during a broadcast write.

SPI Read Operation

The registers of the ADE1201/ADE1202 may be read one at a time following the protocol shown in Figure 28.

A read operation using the SPI interface of the ADE1201/ADE1202 is initiated when the MCU sets the $\overline{\text{CS}}$ pin low and begins sending a 16-bit command word, representing the slave address of the ADE1201/ADE1202 on the MOSI line. After the ADE1201/ADE1202 receives the last bit of the header word, it begins to transmit the register contents on the MISO line when the next SCLK high to low transition occurs. The MCU samples the data on the low to high SCLK transition.

For a SPI read operation, the bit 3 of the command header must be set to 1 (Figure 25).

To ensure the integrity of the SPI read operation, the ADE1201/ADE1202 SPI port may calculate the 16-bit cyclic redundancy check (CRC-16) of the register value sent out on its MOSI pin. If enabled, the ADE1201/ADE1202 appends the 16-bit CRC value during the SPI read operation after the register value (Figure 29).

If bit 0 (SPI_CRC_APPEND_EN) in the CTRL register is cleared to 0, its default value, no CRC value is appended during a SPI read operation. If the bit is set to 1, the 16-bit CRC value is appended to the register value read during the SPI read operation.

The CRC algorithm is based on the CRC-16-CCITT algorithm. The registers are introduced into a linear feedback shift register (LFSR) based generator one byte at a time, most significant byte first, as shown in Figure 30. Each byte is then used with the most significant bit first.

Figure 31 shows how the LFSR works. The ADE1201/ADE1202 register forms the [a_{15}, a_{14}, …, a_0] bits used by the LFSR. Bit a_0 is Bit 15 of the register. Bit a_{15} is the Bit 0 of the register. The formulas that govern the LFSR are as follows:

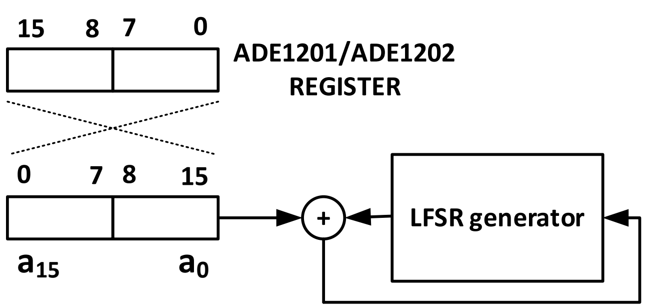

Figure 30. CRC Calculation of the ADE1201/ADE1202 registers

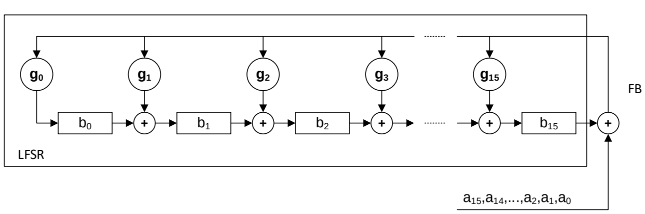

Figure 31. LFSR Generator Used for CRC Calculation

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (1)$$

$$g_0 = g_5 = g_{12} = 1 \quad (2)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (3)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (4)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (5)$$

Equation 3, Equation 4, and Equation 5 must be repeated for j = 1, 2, …, 16. The value written into the SPI communication CRC contains Bit $b_i(16)$, i = 0, 1, …, 15.

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

The configuration registers of the ADE1201/ADE1202 are either user accessible registers (the R/W registers listed in Table 15) or internal registers. The internal registers are not user accessible, and they must remain at their default values. To protect the integrity of all configuration registers, a write protection mechanism is available.

By default, the protection is disabled and the user accessible configuration registers can be written without restriction. When the protection is enabled, no writes to any configuration register are allowed. The registers can always be read, without restriction, independent of the write protection state.

To enable the protection, write 0xADE1 to the CONFIG_LOCK register. To disable the protection, write 0xADE0 to the same register. When the CONFIG_LOCK register is read, its bit 0 (LOCK) shows the protection status: if it is 0, the protection is disabled. If it is 1, the protection is enabled.

After enabling the protection, read back the CONFIG_LOCK register to verify the Bit 0 (LOCK) was set to 1.

It is recommended that the write protection be enabled after configuration registers are initialized. If any of the configuration registers must be changed, disable the protection, change the value of the register, and then reenable the protection.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADE1201/ADE1202 devices. Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 11 summarize the maximum working voltage for 20 years of service life for a dc and ac operating condition. In many cases, the approved working voltage is higher than the 20-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADE1201/ADE1202 devices depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac or dc. Figure 32 and Figure 33 illustrate these different isolation voltage waveforms. Bipolar ac voltage is the most stringent environment. The goal of a 20-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices. In the case of dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 20-year service life.

The working voltages listed in Table 11 can be applied while maintaining the 20-year minimum lifetime, provided that the voltage conforms to the dc voltage case. Treat any cross-insulation voltage waveform that does not conform to Figure 33 as a bipolar ac waveform, and limit the peak voltage to the 20-year lifetime voltage value listed in Table 11.

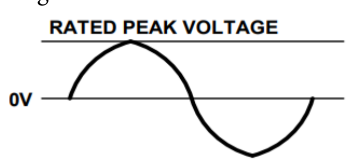

Figure 32. Bipolar AC waveform

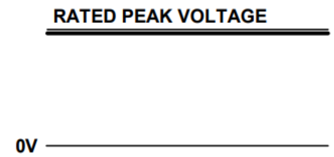

Figure 33. DC waveform

LAYOUT GUIDELINES

For detailed information on the layout guidelines to follow when using the ADE1201/ADE1202, use the TBD Application Note, *Architecting a Binary Input System using the ADE1201/ADE1202*.

ADE1201 EVALUATION BOARD

An evaluation board built upon the ADE1201 allows users to quickly evaluate this IC. It is used in conjunction with the system demonstration platform (EVAL-SDP-CB1Z).

Order both the ADE1201 evaluation board and the system demonstration platform from the ADE1201 product page to evaluate the ADE1201.

ADE1201/ADE1202 VERSION

Bits [8:5] (REVID) in the CTRL register identify the version of the ADE1201/ADE1202.

REGISTER MAP

Table 15. ADE1201/ADE1202 ADDRESS MAP Register Summary

Address	Name	Description	Reset	Access
0x000	LOCK	Lock register.	0x0001	R/W
0x001	CTRL	Control register.	0x0040	R/W
0x002	BIN_CTRL	Binary channel control register.	0x3610	R/W
0x003	BIN_THR	Binary channel threshold level.	0x5AAA	R/W
0x004	WARNA_THR	WarnA threshold.	0xCCCC	R/W
0x005	WARNB_THR	WarnB threshold.	0x5A88	R/W
0x006	WARNC_THR	WarnC threshold.	0x2D2D	R/W
0x007	BIN_FILTER	Binary channel filter length.	0x0096	R/W
0x008	WARNA_FILTER	WarnA filter length.	0x80FA	R/W
0x009	WARNB_FILTER	WarnB filter length.	0x80FA	R/W
0x00A	WARNC_FILTER	WarnC filter length.	0x80FA	R/W
0x00B	MASK	Interrupt Mask register.	0x4000	R/W
0x00C	INT_STATUS	Interrupt Status register.	0x0000	R
0x00D	STATUS	Status register.	0x4000	R
0x00E	ADC	ADC register.	0x0000	R
0x00F	ADCDEC	ADC decimated register.	0x0000	R
0x010	PL_CTRL	Programmable load control register.	0x0000	R/W
0x011	PL_RISE_THR	PL rise threshold.	0x001E	R/W
0x012	PL_LOW_CODE	PL low code.	0x001E	R/W
0x013	PL_HIGH_CODE	PL high code.	0x00C8	R/W
0x014	PL_HIGH_TIME	PL high current period.	0x012C	R/W
0x015	EGY_MTR_CTRL	Energy Meter control register.	0x0505	R/W
0x016	EGY_MTR_THR	Energy Meter max threshold.	0x9BA3	R/W
0x017	EGY_MTR1	Energy Meter channel 1 accumulator.	0x0000	R
0x018	EGY_MTR2	Energy Meter channel 2 accumulator.	0x0000	R
0x200	PL_EN	Programmable Load Enable Register.	0x0002	R/W
0x201	PGA_GAIN	PGA gain register.	0x0000	R/W

REGISTER DETAILS

CONFIG_LOCK REGISTER

Address: 0x000, Reset: 0x0001, Name: CONFIG_LOCK

The user must write to unlock the device before they can successfully write to any other configuration register. The user can always read registers even when the device is locked.

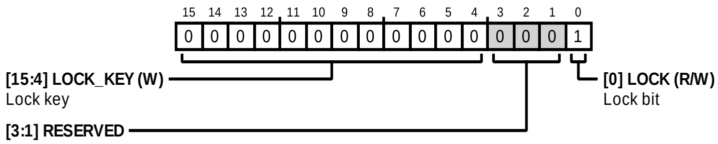

Table 16. Bit Descriptions for CONFIG_LOCK

Bits	Bit Name	Description	Reset	Access
[15:4]	LOCK_KEY	Lock key. To reset or set the LOCK bit the LOCK_KEY must be written as 12'ADE. To unlock the device the user should write 0xADE0 to the LOCK register. To lock the device the user should write 0xADE1.	0x0	W
[3:1]	RESERVED	Reserved.	0x0	R
0	LOCK	Lock bit. After reset the device is locked and the LOCK bit is set to 1. The user must write this bit to 0 in order to write to any other configuration register. After writing the user should write 1 to the LOCK bit and normal operation will be resumed in about 100us.	0x1	R/W

CONTROL REGISTER

Address: 0x001, Reset: 0x0040, Name: CTRL

The Control register allows the user to change several operating modes and also read model and revision information.

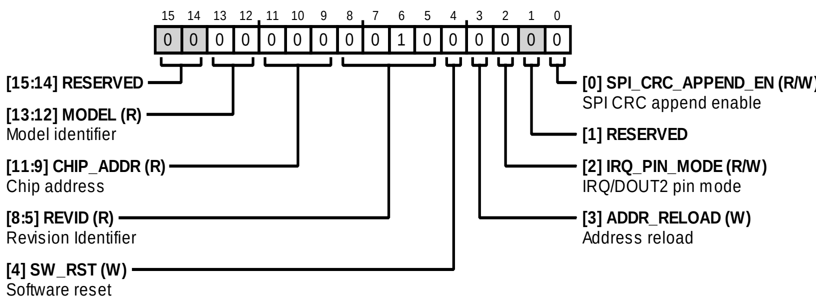

Table 17. Bit Descriptions for CTRL

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	W
[13:12]	MODEL	Model identifier 0: The device is an ADE1201. 1: The device is an ADE1202.	0x0	R
[11:9]	CHIP_ADDR	Chip address. The CHIP_ADDR is the chip address used by the SPI interface. It is decoded and latched from the voltage on the ADDR pin at power-up.	0x0	R
[8:5]	REVID	Revision Identifier. The current revision is 0x2.	0x2	R
4	SW_RST	Software reset. Writing a 1 to SW_RST will reset the device.	0x0	W
3	ADDR_RELOAD	Address reload. By writing a 1 to this bit the user forces the chip address to be decoded and latched from the voltage on the ADDR pin.	0x0	W

Bits	Bit Name	Description	Reset	Access
2	IRQ_PIN_MODE	IRQ/DOUT2 pin mode. For ADE1201 the pin is always IRQ and in pull-down mode. For ADE1202 the pin is controlled by this configuration bit and by default is DOUT2 in push-pull mode. 0: By default the pin is assigned to DOUT2 and is in push-pull mode. 1: The pin is assigned to IRQ and is in pull-down mode.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	SPI_CRC_APPEND_EN	SPI CRC append enable. If this bit is set when user performs an SPI read and keeps clocking for 16 cycles then a 16-bit CRC will be appended to the read operation.	0x0	R/W

BINARY CHANNEL CONTROL REGISTER

Address: 0x002, Reset: 0x3610, Name: BIN_CTRL

Binary channel and warning controls for decimation and filter modes.

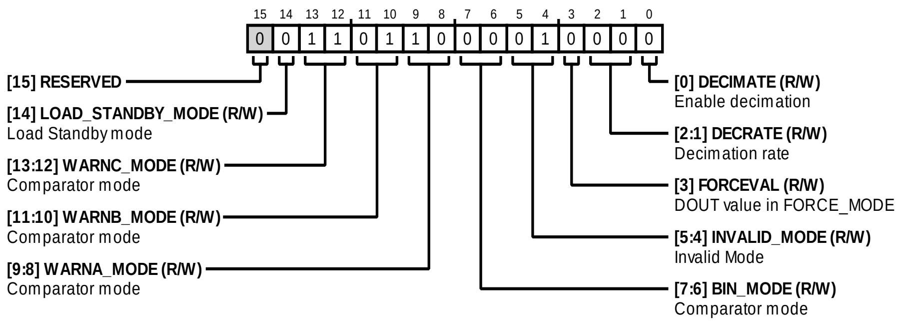

Table 18. Bit Descriptions for BIN_CTRL

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	LOAD_STANDBY_MODE	Load Standby mode. In Load Standby mode the binary channel monitors the load standby current instead of the ADC voltage values.	0x0	R/W
[13:12]	WARNC_MODE	Comparator mode 0: comparator output is hysteretic. 1: comparator output is set if input is between high and low thresholds. 10: comparator output is set if input is greater than the high threshold. 11: comparator output is set if input is less than or equal to high threshold.	0x3	R/W
[11:10]	WARNB_MODE	Comparator mode 0: comparator output is hysteretic. 1: comparator output is set if input is between high and low thresholds. 10: comparator output is set if input is greater than the high threshold. 11: comparator output is set if input is less than or equal to high threshold.	0x1	R/W
[9:8]	WARNA_MODE	Comparator mode 0: comparator output is hysteretic. 1: comparator output is set if input is between high and low thresholds. 10: comparator output is set if input is greater than the high threshold. 11: comparator output is set if input is less than or equal to high threshold.	0x2	R/W

Bits	Bit Name	Description	Reset	Access
[7:6]	BIN_MODE	Comparator mode 0: The comparator output is hysteretic. 1: The comparator output is set if the input is between high and low thresholds. 10: The comparator output is set if input is greater than the high threshold. 11: The comparator output is set if input is less than or equal to high threshold.	0x0	R/W
[5:4]	INVALID_MODE	Invalid Mode. Selects value driven onto DOUT in invalid mode. 00: DOUT equals the FORCEVAL value. 01: DOUT equals the binary filter output. 10: DOUT toggles value on entering invalid mode. 11: DOUT holds current value.	0x1	R/W
3	FORCEVAL	DOUT value in FORCE_MODE. Value to be forced onto DOUT in Invalid Mode.	0x0	R/W
[2:1]	DECRATE	Decimation rate. The decimation rate used when decimation is enabled. 0: Decimation rate equals 1. 1: Decimation rate equals 2. 10: Decimation rate equals 4. 11: Decimation rate equals 8.	0x0	R/W
0	DECIMATE	Enable decimation. If set then the ADC data will be decimated according to the DECRATE setting. The decimated samples can be read back from the ADCDEC register.	0x0	R/W

BINARY CHANNEL THRESHOLD LEVEL REGISTER

Address: 0x003, Reset: 0x5AAA, Name: BIN_THR

Binary channel high and low threshold values.

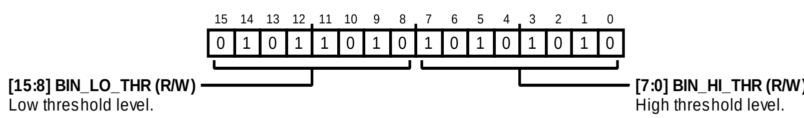

Table 19. Bit Descriptions for BIN_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	BIN_LO_THR	Low threshold level. If the ADC =< low threshold then comparator output will be reset.	0x5A	R/W
[7:0]	BIN_HI_THR	High threshold level. If the ADC > high threshold then the comparator output will be set.	0xAA	R/W

WARNA THRESHOLD REGISTER

Address: 0x004, Reset: 0xCCCC, Name: WARNA_THR

Warning A high and low threshold values.

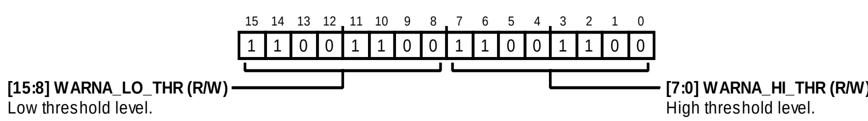

Table 20. Bit Descriptions for WARNA_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	WARNA_LO_THR	Low threshold level. If the ADC =< low threshold then comparator output will be reset.	0xCC	R/W
[7:0]	WARNA_HI_THR	High threshold level. If the ADC > high threshold then the comparator output will be set.	0xCC	R/W

WARNB THRESHOLD REGISTER

Address: 0x005, Reset: 0x5A88, Name: WARNB_THR

Warning B high and low threshold values.

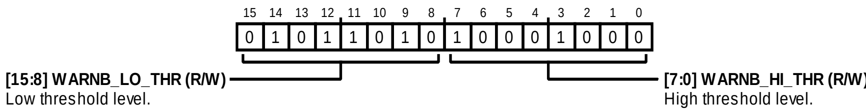

Table 21. Bit Descriptions for WARNB_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	WARNB_LO_THR	Low threshold level. If the ADC =< low threshold then comparator output will be reset.	0x5A	R/W
[7:0]	WARNB_HI_THR	High threshold level. If the ADC > high threshold then the comparator output will be set.	0x88	R/W

WARNC THRESHOLD REGISTER

Address: 0x006, Reset: 0x2D2D, Name: WARNC_THR

Warning C high and low threshold values.

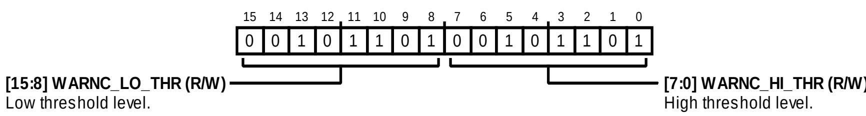

Table 22. Bit Descriptions for WARNC_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	WARNC_LO_THR	Low threshold level. If the ADC =< low threshold then comparator output will be reset.	0x2D	R/W
[7:0]	WARNC_HI_THR	High threshold level. If the ADC > high threshold then the comparator output will be set.	0x2D	R/W

BINARY CHANNEL FILTER LENGTH REGISTER

Address: 0x007, Reset: 0x0096, Name: BIN_FILTER

Binary channel glitch filter period.

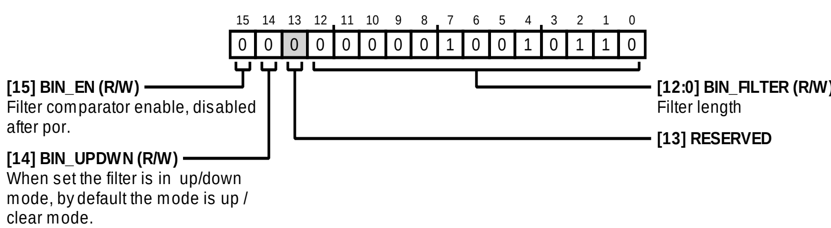

Table 23. Bit Descriptions for BIN_FILTER

Bits	Bit Name	Description	Reset	Access
15	BIN_EN	Filter comparator enable, disabled after por. If disabled comparator output is forced low.	0x0	R/W
14	BIN_UPDWN	When set the filter is in up/down mode, by default the mode is up / clear mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	BIN_FILTER	Filter length. The filter length is in 20us increments. Any input glitch less than the filter length will be rejected such that the output does not change. If the filter length is zero then the filter is bypassed so that the output equals the input with no latency.	0x96	R/W

WARNA FILTER LENGTH REGISTER

Address: 0x008, Reset: 0x80FA, Name: WARNA_FILTER

Warning A glitch filter period.

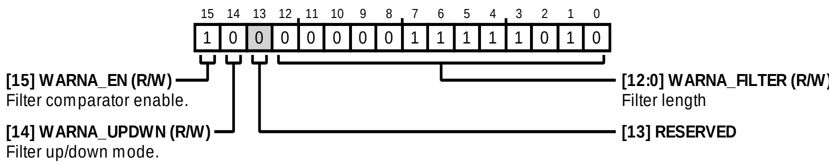

Table 24. Bit Descriptions for WARNA_FILTER

Bits	Bit Name	Description	Reset	Access
15	WARNA_EN	Filter comparator enable.	0x1	R/W
14	WARNA_UPDWN	Filter up/down mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	WARNA_FILTER	Filter length. Filter length in 20us increments. Any input glitch less than the filter length will be rejected such that the output does not change. If the filter length is zero then the filter is bypassed so that the output equals the input with no latency.	0xFA	R/W

WARNB FILTER LENGTH REGISTER

Address: 0x009, Reset: 0x80FA, Name: WARNB_FILTER

Warning A glitch filter period.

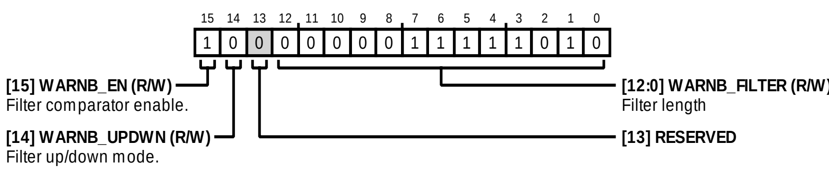

Table 25. Bit Descriptions for WARNB_FILTER

Bits	Bit Name	Description	Reset	Access
15	WARNB_EN	Filter comparator enable. Filter comparator enable.	0x1	R/W
14	WARNB_UPDWN	Filter up/down mode. Filter up/down mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	WARNB_FILTER	Filter length. The filter length is in 20us increments. Any input glitch less than the filter length will be rejected such that the output does not change. If the filter length is zero then the filter is bypassed so that the output equals the input with no latency.	0xFA	R/W

WARNC FILTER LENGTH REGISTER

Address: 0x00A, Reset: 0x80FA, Name: WARNC_FILTER

Warning A glitch filter period.

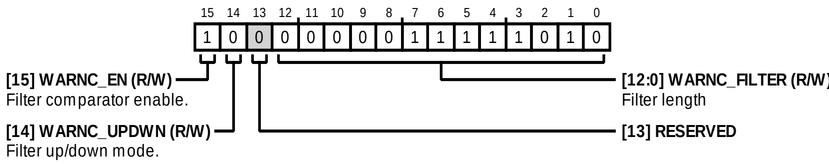

Table 26. Bit Descriptions for WARNC_FILTER

Bits	Bit Name	Description	Reset	Access
15	WARNC_EN	Filter comparator enable. Filter comparator enable.	0x1	R/W
14	WARNC_UPDWN	Filter up/down mode. Filter up/down mode.	0x0	R/W
13	RESERVED	Reserved.	0x0	R
[12:0]	WARNC_FILTER	Filter length. The filter length is in 20us increments. Any input glitch less than the filter length will be rejected such that the output does not change. If the filter length is zero then the filter is bypassed so that the output equals the input with no latency.	0xFA	R/W

INTERRUPT MASK REGISTER

Address: 0x00B, Reset: 0x4000, Name: MASK

If a MASK bit is set, the associated status flag generates an interrupt.

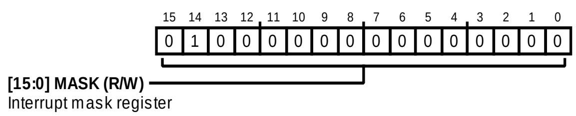

Table 27. Bit Descriptions for MASK

Bits	Bit Name	Description	Reset	Access
[15:0]	MASK	Interrupt mask register. If MASK is 1 then the associated status bit will generate an interrupt. If MASK is 0 then the associated status bit will not generate an interrupt. MASK[15] enables a 100Khz pulse to drive the IRQ pin. This pulse is timed with new ADC data being ready. To observe all pulses, the other IRQ/MASK bits should be disabled.	0x4000	R/W

INTERRUPT STATUS REGISTER

Address: 0x00C, Reset: 0x0000, Name: INT_STATUS

Interrupt Status register indicates that the interrupt has triggered since last being cleared. Write 1 to clear bit.

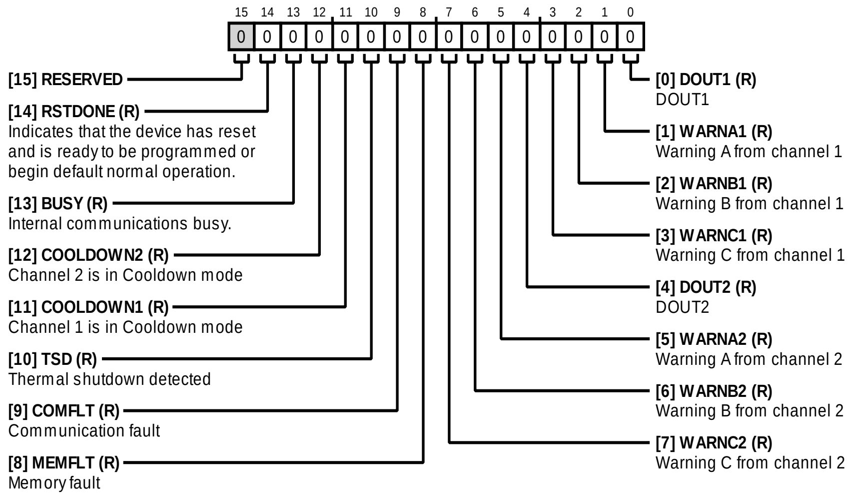

Table 28. Bit Descriptions for INT_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	RSTDONE	Indicates that the device has reset and is ready to be programmed or begin default normal operation.	0x0	R
13	BUSY[0:0]	Internal communications busy. SS Data layer busy.	0x0	R
12	COOLDOWN2[0:0]	Channel 2 is in Cooldown mode	0x0	R
11	COOLDOWN1[0:0]	Channel 1 is in Cooldown mode	0x0	R
10	TSD[0:0]	Thermal shutdown detected	0x0	R
9	COMFLT[0:0]	Communication fault	0x0	R
8	MEMFLT[0:0]	Memory fault. After a memory fault is detected the user could reconfigure the device.	0x0	R
7	WARNC2[0:0]	Warning C from channel 2	0x0	R
6	WARNB2[0:0]	Warning B from channel 2	0x0	R
5	WARNA2[0:0]	Warning A from channel 2	0x0	R
4	DOUT2[0:0]	DOUT2	0x0	R
3	WARNC1[0:0]	Warning C from channel 1	0x0	R
2	WARNB1[0:0]	Warning B from channel 1	0x0	R
1	WARNA1[0:0]	Warning A from channel 1	0x0	R
0	DOUT1[0:0]	DOUT1	0x0	R

STATUS REGISTER

Address: 0x00D, Reset: 0x4000, Name: STATUS

Level sensitive status register. When read the values represent the level of the associated status bit.

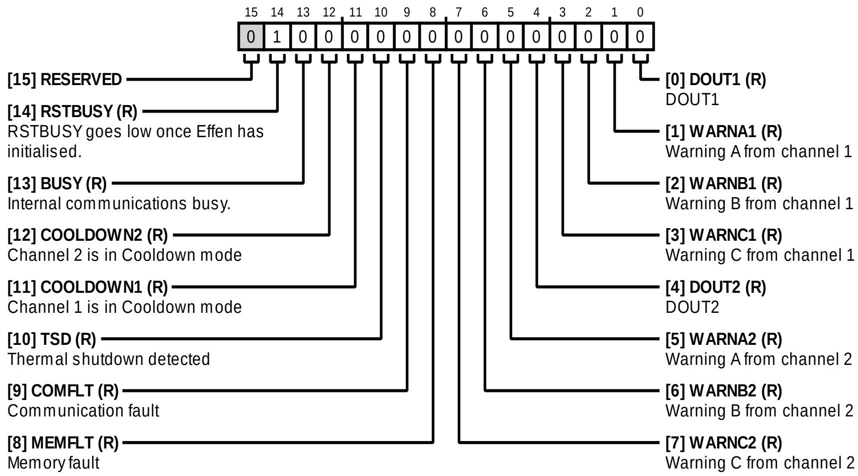

Table 29. Bit Descriptions for STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	RSTBUSY	RSTBUSY goes low once Effen has initialised. Notice this bit is active low since the default value of an SPI read is xFFFF and so the user can distinguish between a bad read and an initialised device.	0x1	R
13	BUSY[0:0]	Internal communications busy. SS Data layer busy.	0x0	R
12	COOLDOWN2[0:0]	Channel 2 is in Cooldown mode	0x0	R
11	COOLDOWN1[0:0]	Channel 1 is in Cooldown mode	0x0	R
10	TSD[0:0]	Thermal shutdown detected	0x0	R
9	COMFLT[0:0]	Communication fault	0x0	R
8	MEMFLT[0:0]	Memory fault. After a memory fault is detected the user could reconfigure the device.	0x0	R
7	WARNC2[0:0]	Warning C from channel 2	0x0	R
6	WARNB2[0:0]	Warning B from channel 2	0x0	R
5	WARNA2[0:0]	Warning A from channel 2	0x0	R
4	DOUT2[0:0]	DOUT2	0x0	R
3	WARNC1[0:0]	Warning C from channel 1	0x0	R
2	WARNB1[0:0]	Warning B from channel 1	0x0	R
1	WARNA1[0:0]	Warning A from channel 1	0x0	R
0	DOUT1[0:0]	DOUT1	0x0	R

ADC REGISTER

Address: 0x00E, Reset: 0x0000, Name: ADC

ADC sample updated every 100KHz for ADE1201 and every 50KHz for the ADE1202.

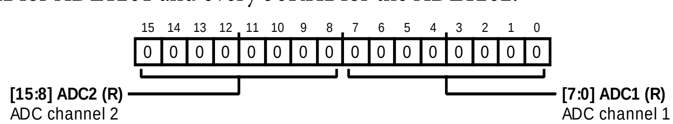

Table 30. Bit Descriptions for ADC

Bits	Bit Name	Description	Reset	Access
[15:8]	ADC2	ADC channel 2. The sample is updated every 50KHz for the ADE1202 only.	0x0	R
[7:0]	ADC1	ADC channel 1. The sample is updated every 100KHz or 50KHz for the ADE1202.	0x0	R

ADC DECIMATED REGISTER

Address: 0x00F, Reset: 0x0000, Name: ADCDEC

Decimated ADC sample(s).

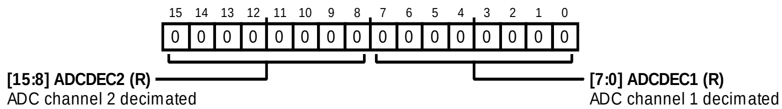

Table 31. Bit Descriptions for ADCDEC

Bits	Bit Name	Description	Reset	Access
[15:8]	ADCDEC2	ADC channel 2 decimated. The sample is decimated at rate determined by DECRATE.	0x0	R
[7:0]	ADCDEC1	ADC channel 1 decimated. The sample is decimated at the rate determined by DECRATE.	0x0	R

PROGRAMMABLE LOAD CONTROL REGISTER

Address: 0x010, Reset: 0x0000, Name: PL_CTRL

Safe side control reg1.

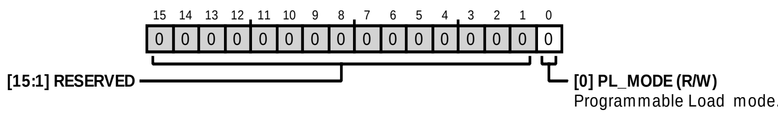

Table 32. Bit Descriptions for PL_CTRL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	PL_MODE	Programmable Load mode. 0: Low Idle State. In low idle state the Programmable load is set to the low current PL_LOW_CODE when the relay is open. When the relay is closed and the BI rises above the PL_RISE_THR the load is set to PL_HIGH_CODE. 1: High Idle State. In high idle state the Programmable load is set to PL_HIGH_CODE when the relay is open. When the relay is closed the current begins to flow as soon there is enough voltage headroom on the PL1 pin (or the PL2 pin for the ADE1202).	0x0	R/W

PL RISE THRESHOLD REGISTER

Address: 0x011, Reset: 0x001E, Name: PL_RISE_THR

Sets programmable load rising edge ADC sample threshold.

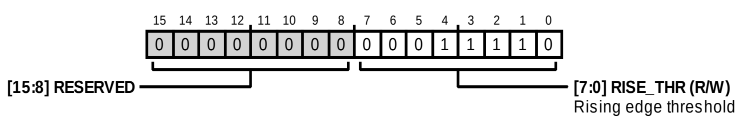

Table 33. Bit Descriptions for PL_RISE_THR

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	RISE_THR	Rising edge threshold. When the ADC is greater than the RISE_THR the PL1 pin pulls down a high current (PL_HIGH_CODE) when in PL_LOW_MODE. The minimum value that can be written is 8'h01 and the maximum value is 8'hFE. These values are enforced by the hardware such that a write of 8'h00 becomes 8'h01 and similarly 8h'FF becomes 8'hFE.	0x1E	R/W

PL LOW CODE REGISTER

Address: 0x012, Reset: 0x001E, Name: PL_LOW_CODE

PL low code.

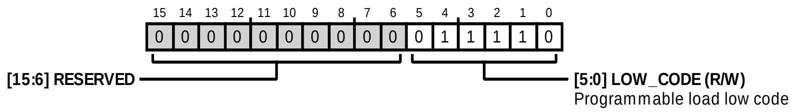

Table 34. Bit Descriptions for PL_LOW_CODE

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	LOW_CODE	Programmable load low code. Minimum low current value in units of 100uA. The minimum value is 0x1 so if 0x0 is written it is still set to 0x1.	0x1E	R/W

PL HIGH CODE REGISTER

Address: 0x013, Reset: 0x00C8, Name: PL_HIGH_CODE

PL high code.

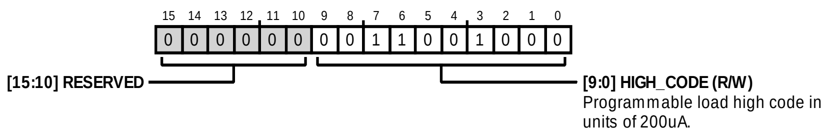

Table 35. Bit Descriptions for PL_HIGH_CODE

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
[9:0]	HIGH_CODE	Programmable load high code in units of 200uA. All 10-bits are used for ADE1201, but for the ADE1202 only the bottom 8-bits are used so the maximum value is 0xFF which equates to about 50mA. The minimum value that can be written is 0x1.	0xC8	R/W

PL HIGH CURRENT PERIOD REGISTER

Address: 0x014, Reset: 0x012C, Name: PL_HIGH_TIME

High current timer duration.

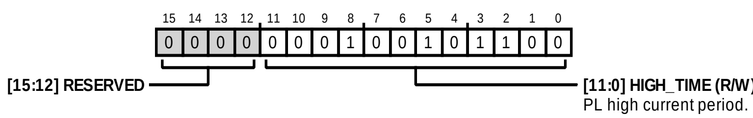

Table 36. Bit Descriptions for PL_HIGH_TIME

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:0]	HIGH_TIME	PL high current period. When the Programmable load goes into the high state it pulls down the high current for the HIGH_TIME period which is in units of 10us. The minimum HIGH_TIME is 10us so if 0 is written, the value is set to 1.	0x12C	R/W

ENERGY METER CONTROL REGISTER

Address: 0x015, Reset: 0x0505, Name: EGY_MTR_CTRL

Energy Meter control register.

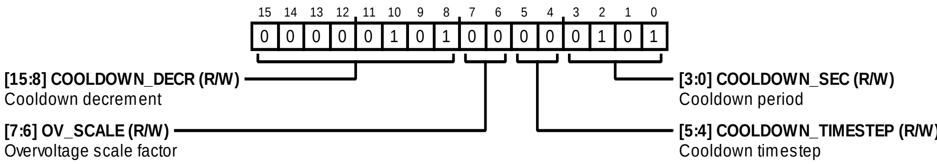

Table 37. Bit Descriptions for EGY_MTR_CTRL

Bits	Bit Name	Description	Reset	Access
[15:8]	COOLDOWN_DECR	Cooldown decrement. Once the device enters Cooldown mode the Cooldown timer is decremented by the COOLDOWN_DECR value every COOLDOWN_STEP.	0x5	R/W
[7:6]	OV_SCALE	Overvoltage scale factor. Overvoltage scaling factor applied when the ADC value is 0xFF. 0: Multiply by 1. 1: Multiply by 4. 10: Multiply by 8. 11: Multiply by 16.	0x0	R/W
[5:4]	COOLDOWN_TIMESTEP	Cooldown timestep. Once the device enters Coodown mode the Cooldown timer is decremented every Cooldown timestep. 0: 10us. 1: 20us. 10: 40us. 11: 80us.	0x0	R/W
[3:0]	COOLDOWN_SEC	Cooldown period. Cooldown period in seconds. A value of 0 disables the cooldown function.	0x5	R/W

ENERGY METER MAX THRESHOLD REGISTER

Address: 0x016, Reset: 0x9BA3, Name: EGY_MTR_THR

Energy Meter maximum energy threshold.

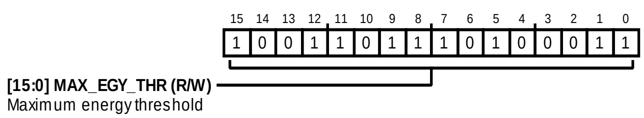

Table 38. Bit Descriptions for EGY_MTR_THR

Bits	Bit Name	Description	Reset	Access
[15:0]	MAX_EGY_THR	Maximum energy threshold. When the MAX_EGY_THR is exceeded the device enters Cooldown mode. The threshold is scaled by 128. The Energy Meter accumulates the over-scaled ADC values every 10us when the device is not in Cooldown mode.	0x9BA3	R/W

ENERGY METER CHANNEL 1 ACCUMULATOR REGISTER

Address: 0x017, Reset: 0x0000, Name: EGY_MTR1

Energy Meter channel 1.

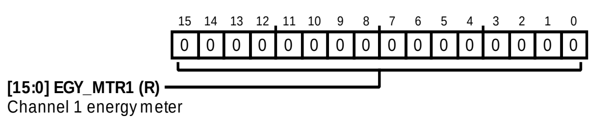

Table 39. Bit Descriptions for EGY_MTR1

Bits	Bit Name	Description	Reset	Access
[15:0]	EGY_MTR1	Channel 1 energy meter. Channel 1 Energy Meter, the current accumulated value.	0x0	R

ENERGY METER CHANNEL 2 ACCUMULATOR REGISTER

Address: 0x018, Reset: 0x0000, Name: EGY_MTR2

Energy Meter channel 1.

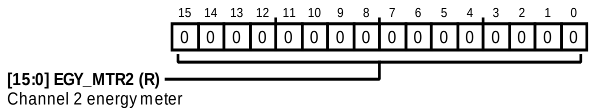

Table 40. Bit Descriptions for EGY_MTR2

Bits	Bit Name	Description	Reset	Access
[15:0]	EGY_MTR2	Channel 2 energy meter. Channel 1 Energy Meter, the current accumulated value.	0x0	R

PROGRAMMABLE LOAD ENABLE REGISTER

Address: 0x200, Reset: 0x0002, Name: PL_EN

The programmable load enable.

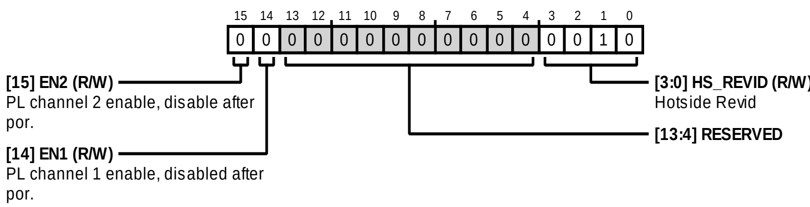

Table 41. Bit Descriptions for PL_EN

Bits	Bit Name	Description	Reset	Access
15	EN2	PL channel 2 enable, disable after por.	0x0	R/W
14	EN1	PL channel 1 enable, disabled after por.	0x0	R/W
[13:4]	RESERVED	Reserved.	0x0	R
[3:0]	HS_REVID	Hotside Revid	0x2	R/W

PGA GAIN REGISTER

Address: 0x201, Reset: 0x0000, Name: PGA_GAIN

Gain value as shown below.

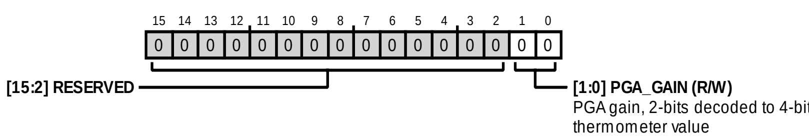

Table 42. Bit Descriptions for PGA_GAIN

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
[1:0]	PGA_GAIN	PGA gain, 2-bits decoded to 4-bit thermometer value. Supports 4 gain values as shown below. 0: Gain equals 1. 1: Gain equals 2. 10: Gain equals 5. 11: Gain equals 10.	0x0	R/W

OUTLINE DIMENSIONS

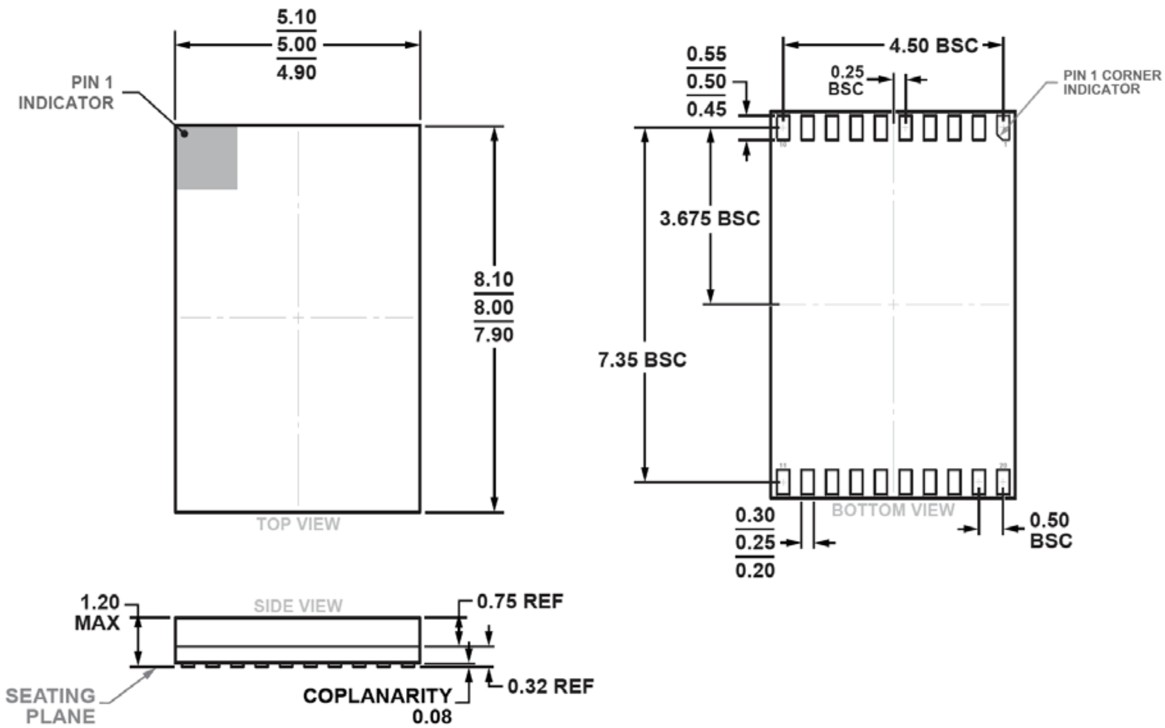

Figure 34. 20-Lead Land Grid Array (CC-20-5). Dimensions shown in mm

ORDERING GUIDE

Model[1,2]	Temperature Range	Package Description	Package Option
ADE1201ACCZ	−40°C to +105°C	20-Lead LGA	CC-20-5
ADE1201ACCZ-RL	−40°C to +105°C	20-Lead LGA	CC-20-5
ADE1202ACCZ	−40°C to +105°C	20-Lead LGA	CC-20-5
ADE1202ACCZ-RL	−40°C to +105°C	20-Lead LGA	CC-20-5
EVAL-ADE1201EBZ		Evaluation Board	
EVAL-SDP-CB1Z		Evaluation System Controller Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL_SDP-CB1Z is the controller board that manages the EVAL-ADE1201EBZ evaluation board. Both boards must be ordered together