One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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0.228ps rms jitter from 0.637 MHz to 10 MHz at 106.25 MHz
0.19 ps rms jitter from 1.875 MHz to 20 MHz at 156.25 MHz
0.428ps rms jitter from 12 kHz to 20 MHz at 125 MHz

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SPECIFICATIONS

PLL CHARACTERISTICS

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE NOISE CHARACTERISTICS					
PLL Noise (106.25 MHz LVDS Output)					
At 1 kHz		−123		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−127		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−129		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−150		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−152		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−153		dBc/Hz	33.33 MHz output disabled
PLL Noise (156.25 MHz LVDS Output)					
At 1 kHz		−118		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−125		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−126		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−145		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−151		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−151		dBc/Hz	33.33 MHz output disabled
PLL Noise (125 MHz LVDS Output)					
At 1 kHz		−119		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−127		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−147		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−151		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−152		dBc/Hz	33.33 MHz output disabled
PLL Noise (100 MHz LVDS Output)					
At 1 kHz		−121		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−130		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−147		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−150		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−150		dBc/Hz	33.33 MHz output disabled
PLL Noise (106.25 MHz LVPECL Output)					
At 1 kHz		−121		dBc/Hz	33.33 MHz output disabled
At 10 kHz				dBc/Hz	33.33 MHz output disabled
At 100 kHz		−129		dBc/Hz	33.33 MHz output disabled
At 1 MHz					

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL Noise (125 MHz LVPECL Output)					
At 1 kHz		−122		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−127		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−148		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−152		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−153		dBc/Hz	33.33 MHz output disabled
PLL Noise (100 MHz LVPECL Output)					
At 1 kHz		−122		dBc/Hz	33.33 MHz output disabled
At 10 kHz		−128		dBc/Hz	33.33 MHz output disabled
At 100 kHz		−130		dBc/Hz	33.33 MHz output disabled
At 1 MHz		−148		dBc/Hz	33.33 MHz output disabled
At 10 MHz		−150		dBc/Hz	33.33 MHz output disabled
At 30 MHz		−151		dBc/Hz	33.33 MHz output disabled
PLL Noise (33.33 MHz CMOS Output)					
At 1 kHz		−130		dBc/Hz	
At 10 kHz		−138		dBc/Hz	
At 100 kHz		−139		dBc/Hz	
At 1 MHz		−152		dBc/Hz	
At 5 MHz		−152		dBc/Hz	
Phase Noise (25 MHz CMOS Output)					
At 1 kHz		−133		dBc/Hz	
At 10 kHz		−142		dBc/Hz	
At 100 kHz		−148		dBc/Hz	
At 1 MHz		−148		dBc/Hz	
At 5 MHz		−148		dBc/Hz	
Spurious Content[1]		−70		dBc	Dominant amplitude, all outputs active
PLL Figure of Merit		−217.5		dBc/Hz	

[1] When the 33.33 MHz, 100 MHz, and 125 MHz clocks are enabled simultaneously, a worst-case −50 dBc spurious content might be presented on Pin 21 and Pin 22 only.

LVDS CLOCK OUTPUT JITTER

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 2.

Jitter Integration Bandwidth (Typ)	100 MHz	106.25 MHz	125 MHz 33M = Off/On[1]	156.25 MHz	Unit	Test Conditions/Comments
12 kHz to 20 MHz	0.51	0.44	0.42/0.88	0.42	ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
1.875 MHz to 20 MHz				0.19	ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
637 kHz to 10 MHz		0.22			ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
200 kHz to 10 MHz	0.32		0.25/0.78		ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
12 kHz to 35 MHz			0.50 (off only)		ps rms	LVDS output frequency combinations are 1 × 156.25 MHz, 2 × 125 MHz, 2 × 106.25 MHz

[1] The typical 125 MHz rms jitter data is collected from the differential pair, Pin 21 and Pin 22, unless otherwise noted.

LVPECL CLOCK OUTPUT JITTER

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 3.

Jitter Integration Bandwidth (Typ)	100 MHz	106.25 MHz	125 MHz 33M = Off/On	156.25 MHz	Unit	Test Conditions/Comments
12 kHz to 20 MHz (Typ)	0.61	0.45	0.44/2.2	0.46	ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
12 kHz to 20 MHz (Max)	0.87	0.81	0.56 (off only)	0.56	ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
1.875 MHz to 20 MHz (Typ)				0.28	ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
637 kHz to 10 MHz (Typ)		0.23			ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
200 kHz to 10 MHz (Typ)	0.38		0.24/2.2		ps rms	LVPECL output frequency combinations are 1 × 156.25 MHz, 1 × 100 MHz, 1 × 125 MHz, 2 × 106.25 MHz
12 kHz to 35 MHz (Typ)			0.52 (off only)		ps rms	LVPECL output frequency combinations are 156.25 MHz unterminated, 2 × 125 MHz, 2 × 106.25 MHz
12 kHz to 35 MHz (Max)			0.66 (off only)		ps rms	LVPECL output frequency combinations are 156.25 MHz unterminated, 2 × 125 MHz, 2 × 106.25 MHz

CMOS CLOCK OUTPUT JITTER

Typical (typ) is given for V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 4.

Jitter Integration Bandwidth	25 MHz	33.3 MHz	Unit	Test Conditions/Comments
12 kHz to 5 MHz (Typ)	0.78	0.41	ps rms	
12 kHz to 5 MHz (Max)	1.1	N/A	ps rms	
200 kHz to 5 MHz (Typ)	0.76	0.52	ps rms	
200 kHz to 5 MHz (Max)	1.0	N/A	ps rms	

REFERENCE INPUT

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT (REFCLK)					
Input Frequency		25		MHz	
Input High Voltage	2.0			V	
Input Low Voltage			0.8	V	
Input Current	−1.0		+1.0	µA	
Input Capacitance		2		pF	

CLOCK OUTPUTS

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					
Output Frequency			156.25	MHz	
Output High Voltage (V_{OH})	V_S − 1.24	V_S − 1.05	V_S − 0.83	V	
Output Low Voltage (V_{OL})	V_S − 2.07	V_S − 1.87	V_S − 1.62	V	
Output Differential Voltage (V_{OD})	700	825	950	mV	
Duty Cycle	45		55	%	
LVDS CLOCK OUTPUTS					
Output Frequency			156.25	MHz	
Differential Output Voltage (V_{OD})	250	350	475	mV	
Delta V_{OD}			25	mV	
Output Offset Voltage (V_{OS})	1.125	1.25	1.375	V	
Delta V_{OS}			25	mV	
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND
Duty Cycle	45		55	%	
CMOS CLOCK OUTPUTS					
Output Frequency			33.33	MHz	
Output High Voltage (V_{OH})	V_S − 0.1			V	Sourcing 1.0 mA current
Output Low Voltage (V_{OL})			0.1	V	Sinking 1.0 mA current
Duty Cycle	42		58	%	

TIMING CHARACTERISTICS

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 200 Ω to 0 V; C_{LOAD} = 0 pF; C_{AC} = 100 nF; oscilloscope set to 50 Ω termination
Output Rise Time, t_{RP}	480	625	810	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}	480	625	810	ps	80% to 20%, measured differentially
LVDS					Termination = 100 Ω differential; C_{LOAD} = 0 pF; C_{AC} = 100 nF; oscilloscope set to 50 Ω termination
Output Rise Time, t_{RL}	160	350	540	ps	20% to 80%, measured differentially
Output Fall Time, t_{FL}	160	350	540	ps	80% to 20%, measured differentially
CMOS					
Output Rise Time, t_{RC}	0.25	0.50	2.5	ns	20% to 80%; termination = 50 Ω to 0 V; C_{LOAD} = 5 pF; C_{AC} = 100 nF
Output Fall Time, t_{FC}	0.25	0.70	2.5	ns	80% to 20%; termination = 50 Ω to 0 V; C_{LOAD} = 5 pF; C_{AC} = 100 nF
Output Rise Time, t_{RC2}	1.3	2.1	2.6	ns	20% to 80%; active probe measurement, C_{probe} = 1 pF, R_{probe}=20 kΩ, C_{LOAD} = 3.9 pF
Output Fall Time, t_{FC2}	1.4	2.3	3.0	ns	80% to 20%; active probe measurement, C_{probe} = 1 pF, R_{probe}=20 kΩ, C_{LOAD} = 3.9 pF

CONTROL PINS

Typical (typ) is given for V_S = 3.3 V ± 10%, T_A = 25°C, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
					REFSEL has a 30 kΩ pull-up resistor.

TIMING DIAGRAMS

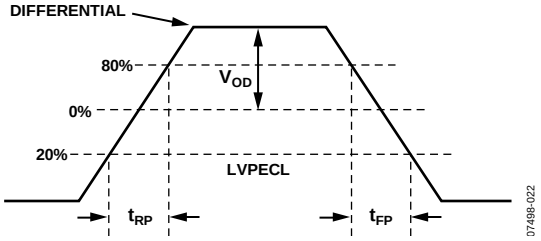


Figure 3. LVPECL Timing, Differential

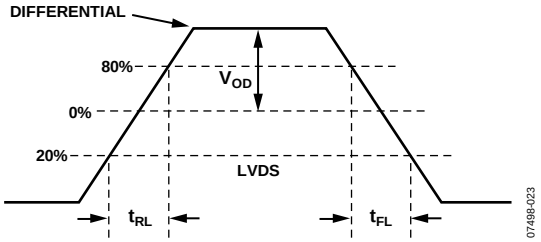


Figure 4. LVDS Timing, Differential

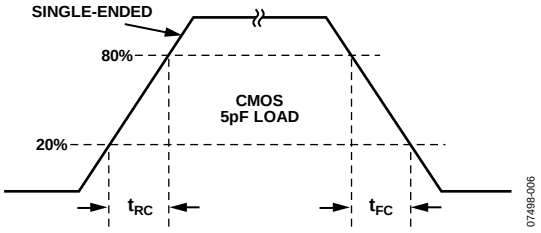


Figure 5. CMOS Timing, Single-Ended, 5 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 11.

Parameter	Rating
VS to GND	−0.3 V to +3.6 V
REFCLK to GND	−0.3 V to VS + 0.3 V
BYPASSx to GND	−0.3 V to VS + 0.3 V
XO to GND	−0.3 V to VS + 0.3 V
FREQSEL, FORCE_LOW, and REFSEL to GND	−0.3 V to VS + 0.3 V
25M, 33M, 100M/125M, 106M, and 156M to GND	−0.3 V to VS + 0.3 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C

[1] See Table 12 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

$_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.

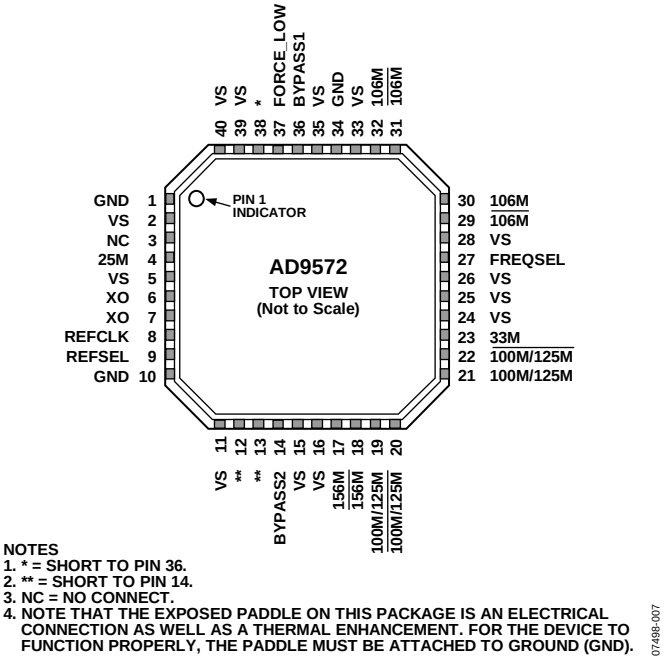
Table 12. Thermal ResistaNce

Package Type	θ_{JA}	Unit
40-Lead LFCSP	27.5	°C/W

ESD CAUTIO

ctrostatic discharge) sensitive device.
evices and circuit boards can discharge tion. Although this product features

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. * = SHORT TO PIN 36.
2. ** = SHORT TO PIN 14.
3. NC = NO CONNECT.
4. NOTE THAT THE EXPOSED PADDLE ON THIS PACKAGE IS AN ELECTRICAL CONNECTION AS WELL AS A THERMAL ENHANCEMENT. FOR THE DEVICE TO FUNCTION PROPERLY, THE PADDLE MUST BE ATTACHED TO GROUND (GND).

07498-007

Figure 6. Pin Configuration

Table 13. PiN FuNctioN DescriptioNs[1]

Pin No.	Mnemonic	Description
1, 10, 34	GND	Ground. Includes external paddle (EPAD).
2	VS	Power Supply Connection for the 25M CMOS Buffer.
3	NC	No Connect. This pin should be left floating.
4	25M	CMOS 25 MHz Output.
5	VS	Power Supply Connection for the Crystal Oscillator.
6, 7	XO	External 25 MHz Crystal.
8	REFCLK	25 MHz Reference Clock Input. Tie low when not in use.
9	REFSEL	Logic Input. Used to select the reference source.
11	VS	Power Supply Connection for the GbE PLL.
12, 13	N/A	Short to Pin 14.
14, 36	BYPASS2, BYPASS1	These pins are for bypassing each LDO to ground with a 220 nF capacitor.
15	VS	Power Supply Connection for the GbE VCO.
16	VS	Power Supply Connection for the 156M LVDS Output Buffer and Output Dividers.
17	156M	LVPECL/LVDS Output at 156.25 MHz.
18	$\overline{156M}$	Complementary LVPECL/LVDS Output at 156.25 MHz.
19, 21	100M/125M	LVPECL/LVDS Output at 100 MHz or 125 MHz. Selected by FREQSEL pin strapping.
20, 22	$\overline{100M}$	

Pin No.	Mnemonic	Description
33	VS	Power Supply Connection for the 106.25 MHz LVDS Output Buffer and Output Dividers.
35	VS	Power Supply Connection for the FC VCO.
37	FORCE_LOW	Forces the 33.33 MHz output into a low state.
38	N/A	Short to Pin 36.
39	VS	Power Supply Connection for the FC PLL.
40	VS	Power Supply Connection for Miscellaneous Logic.

[1] The exposed paddle on this package is an electrical connection as well as a thermal enhancement. For the device to function properly, the paddle must be attached to ground (GND).

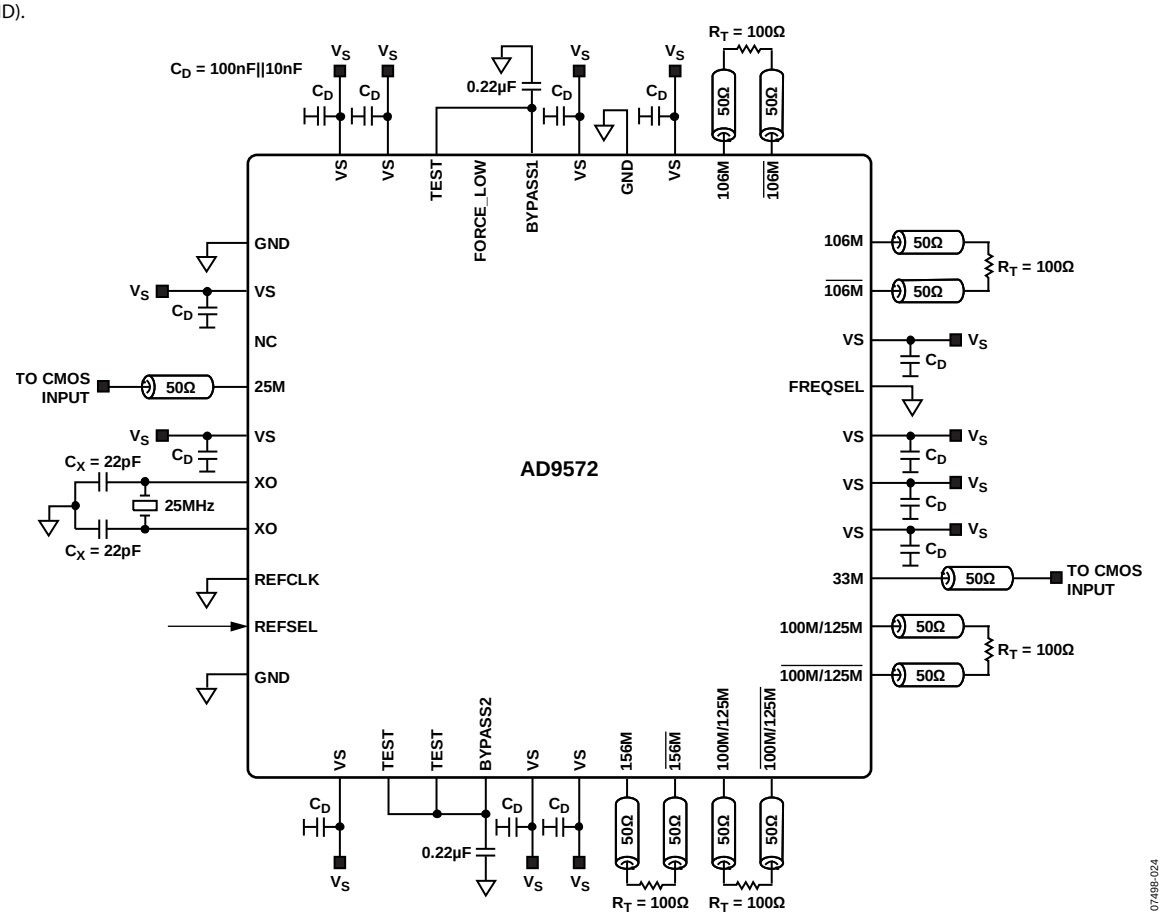


Figure 7. Typical Application Schematic, LVDS Format Outputs, 1 × 25 MHz, 1 × 156.25 MHz, 2 × 125 MHz, and 2 × 106.25 MHz

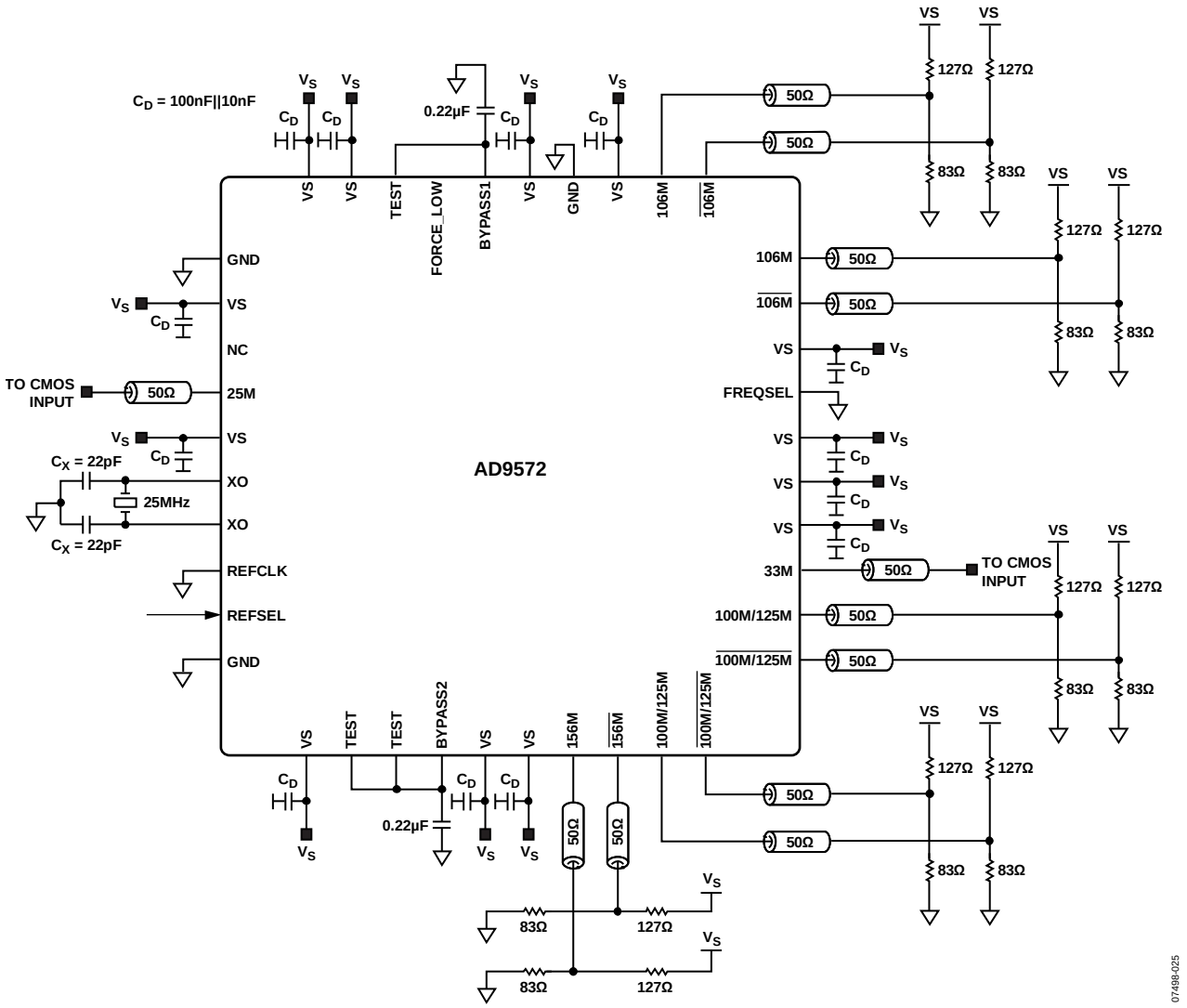
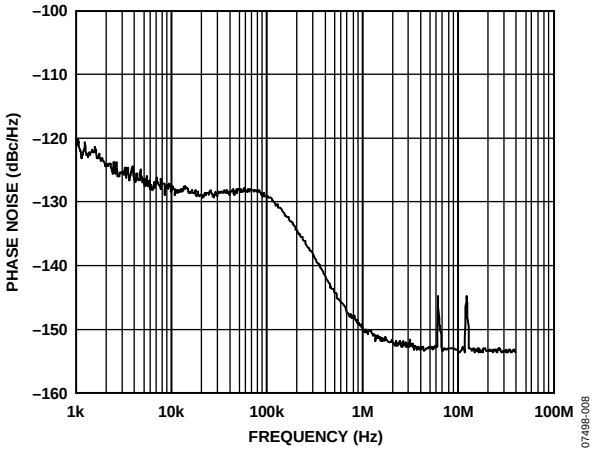


Figure 8. Typical Application Schematic, LPECL Format Outputs, 1 × 25 MHz, 1 × 156.25 MHz, 2 × 125 MHz, and 2 × 106.25 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

Phase noise plots taken with 100 MHz and 125 MHz outputs enabled; 33.3 MHz output disabled.



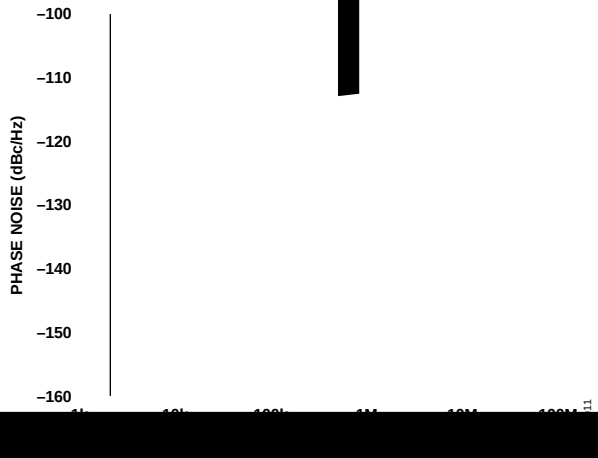
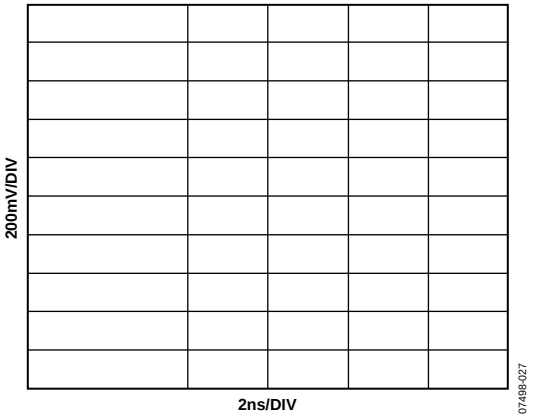


Figure 11. 25 MHz Phase Noise


200mV/DIV
2ns/DIV
07498-027

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from the ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous

THEORY OF OPERATION

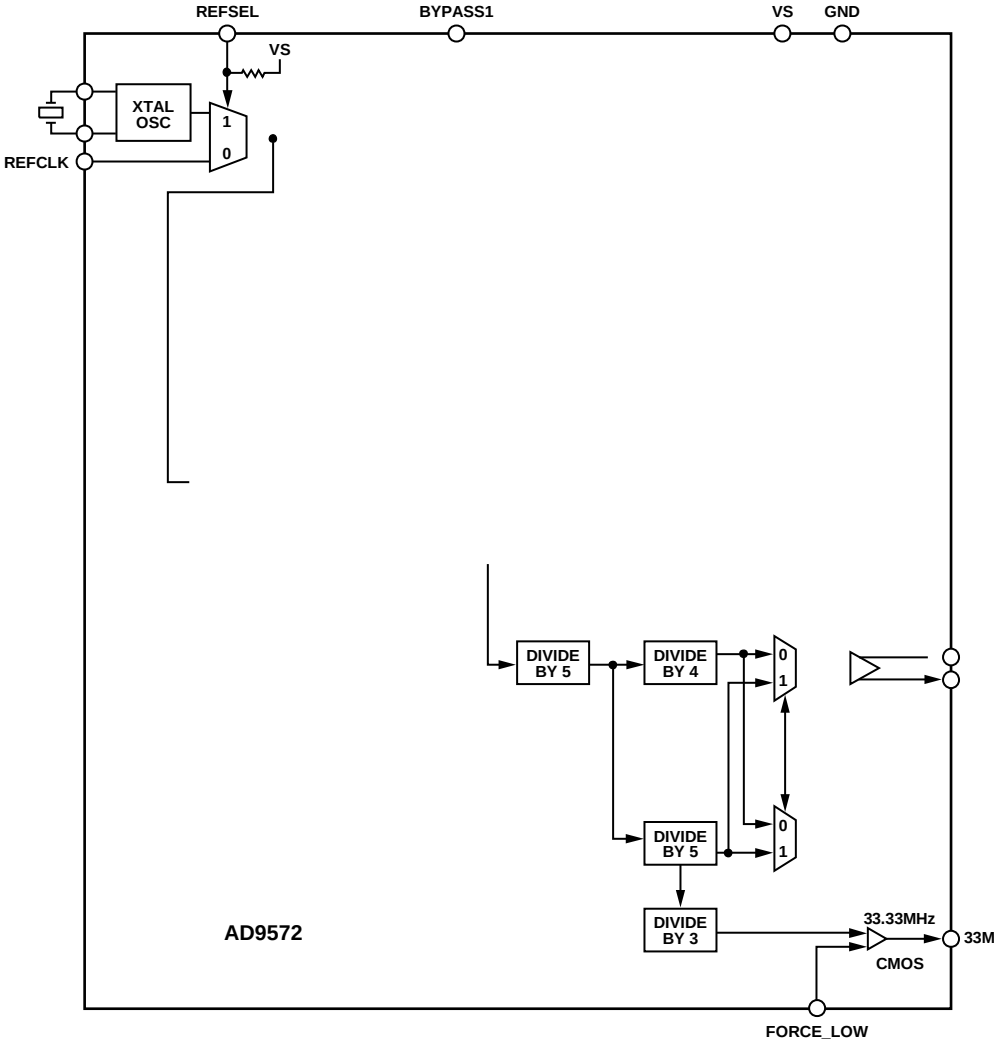


Table 15. FREQSEL (PIN 27) DEFINITION

FREQSEL	Frequency Available from Pin 19 and Pin 20 (MHZ)	Frequency Available from Pin 21 and Pin 22 (MHZ)
0	125	125
1	100	100
NC	125	100

The simplified equivalent circuits of the LVDS and LVPECL outputs are shown in Figure 18 and Figure 19.

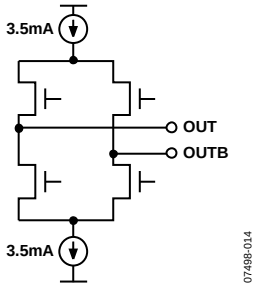


Figure 18. LVDS Output Simplified Equivalent Circuit

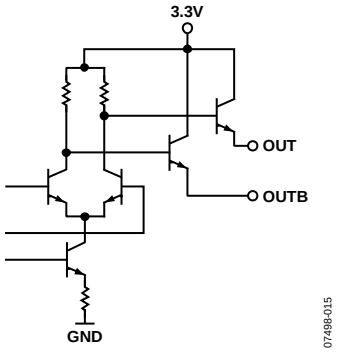


Figure 19. LVPECL Output Simplified Equivalent Circuit

The differential outputs are factory programmed to either LVPECL or LVDS format, and either option can be sampled on request.

CMOS drivers tend to generate more noise than differential outputs and, as a result, the proximity of the 33.33 MHz output to Pin 21 and Pin 22 does affect the jitter performance when FREQSEL = 0 (that is, when the differential output is generating 125 MHz). For this reason, the 33 MHz pin can be forced to a low state by asserting the FORCE_LOW signal on Pin 37 (see Table 16). An internal pull-down enables the 33.33 MHz output if the pin is not connected.

Table 16. FORCE_LOW (PIN 37) DEFINITION

FORCE_LOW	33.33 MHz Output (Pin 23)
0 or NC	33.33 MHz
1	0

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the reference clock and feedback divider to produce an output proportional to the phase and frequency difference between them. Figure 20 shows a simplified schematic.

termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

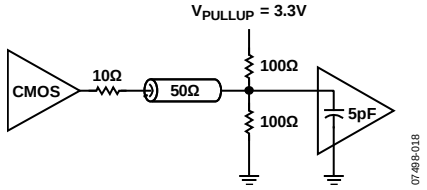


Figure 21. CMOS Output with Far-End Termination

LVPECL CLOCK DISTRIBUTION

The LVPECL outputs, which are open emitter, require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 19 shows the LVPECL output stage.

In most applications, a standard LVPECL far-end termination is recommended, as shown in Figure 22. The resistor network is designed to match the transmission line impedance (50 Ω) and establish a dc bias of (V… 2 V). An alternative dc-coupled LVPECL termination network with a reduced number of components is also possible as shown in Figure 23.

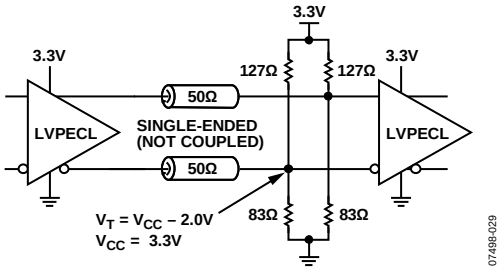
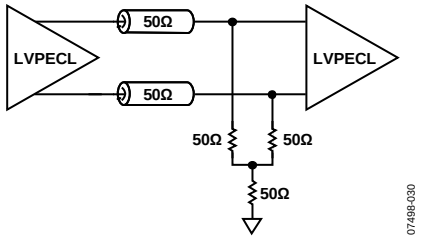


Figure 22. LVPECL Far-End Termination



sine wave or square wave, provided that an external divider is used to bias the input at $V_S/2$.

Table 17. REFSEL (PIN 9) DEFINITION

REFSEL	Reference Source
0	REFCLK input
1	Internal crystal oscillator

POWER AND GROUNDING CONSIDERATIONS AND POWER SUPPLY REJECTION

Many applications seek high speed and performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the PCB is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as for power supply bypassing and grounding to ensure optimum performance. Each power supply pin should have independent decoupling and connections to the power supply plane. It is recommended that the device exposed paddle be directly connected to the ground plane by a grid of at least nine vias. Care should be taken to ensure that the output traces cannot couple onto the reference or crystal input circuitry. Traces should not be routed under the crystal. Output signal traces should be kept on the top PCB layer; these traces have very high edge rates, and the use of PCB vias will result in signal integrity problems.

OUTLINE DIMENSIONS

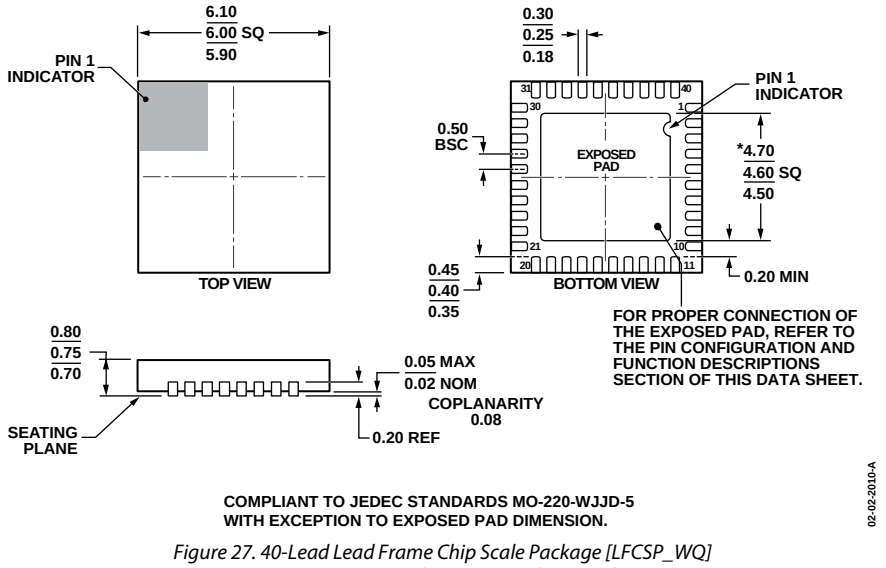


Figure 27. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
AD9572ACPZLVD	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-7
AD9572ACPZLVD-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 13″Tape and Reel, 2,500 Pieces	CP-40-7
AD9572ACPZLVD-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7″Tape and Reel, 750 Pieces	CP-40-7
AD9572ACPZPEC	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-7
AD9572ACPZPEC-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 13″Tape and Reel, 2,500 Pieces	CP-40-7
AD9572ACPZPEC-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7″Tape and Reel, 750 Pieces	CP-40-7
AD9572-EVALZ-LVD		Evaluation Board	
AD9572-EVALZ-PEC		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] LVD indicates LVDS-compliant, differential clock outputs.
[3] PEC indicates LVPECL-compliant, differential clock outputs.

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