74VHC08

Quad 2-Input AND Gate

General Description

The VHC08 is an advanced high speed CMOS 2 Input AND Gate fabricated with silicon gate CMOS technology. It achieves the high−speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit insures that 0 V to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 4.3 ns (Typ.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Low Power Dissipation: I_{CC} = 2 μA (Max.) @ T_A = 25°C
- Low Noise: V_{OLP} = 0.8 V (Max.)
- Pin and Function Compatible with 74HC08

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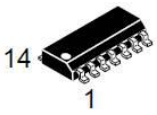
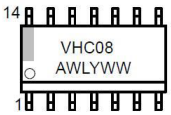
MARKING DIAGRAMS

Order Number: 74VHC08M

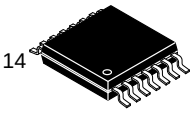


SOIC14
CASE 751EF

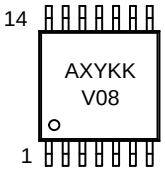


A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week

Order Number: 74VHC08MTCX



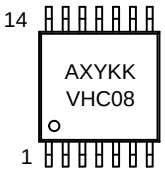
TSSOP−14 WB
CASE 948G



A	= Assembly Location
XY	= 2−digit 2 Weekly Date Code
KK	= 2−digit Lot Run Code

Order Number: 74VHC08SJX

SOP14
CASE 565BE



A	= Assembly Location
XY	= 2−digit 2 Weekly Date Code
KK	= 2−digit Lot Run Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

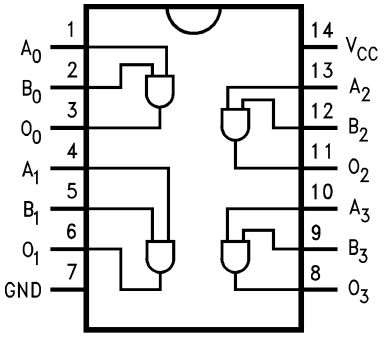


Figure 1. Connection Diagram

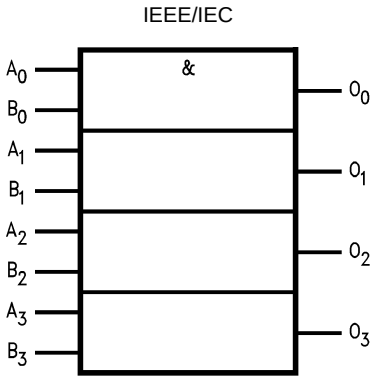


Figure 2. Logic Symbol

PIN DESCRIPTION

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

TRUTH TABLE

A	B	O
L	L	L
L	H	L
H	L	L
H	H	H

ORDERING INFORMATION

Part Number	Package Number	Package	Packing Method†
74VHC08M	M14A	SOIC14 (Pb−Free)	55 / Tube
74VHC08SJ	M14D	SOP14 (Pb−Free)	2000 / Tape & Reel
74VHC08MTC	MTC14	TSSOP−14 WB (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 V to +7.0 V
V_{IN}	DC Input Voltage	–0.5 V to +7.0 V
V_{OUT}	DC Output Voltage	–0.5 V to V_{CC} + 0.5 V
I_{IK}	Input Diode Current	–20 mA
I_{OK}	Output Diode Current	±20 mA
I_{OUT}	DC Output Current	±25 mA
I_{CC}	DC V_{CC} / GND Current	±50 mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS (Note 1)

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0 V to +5.5 V
V_{IN}	Input Voltage	0 V to +5.5 V
V_{OUT}	Output Voltage	0 V to V_{CC}
T_{OPR}	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time, V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	 0 ns/V ~ 100 ns/V 0 ns/V ~ 20 ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = –40°C to +85°C		Units
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	2.0			1.50			1.50		V
		3.0–5.5			0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0–5.5					0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50 μA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I_{OH} = –4 mA	2.58			2.48		
		4.5		I_{OH} = –8 mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I_{OL} = 4 mA			0.36		0.44	
		4.5		I_{OL} = 8 mA			0.36		0.44	
I_{IN}	Input Leakage Current	0–5.5	V_{IN} = 5.5 V or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				2.0		20.0	μA

NOISE CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C		Units
				Typ	Limits	
V_{OLP}[2]	Quiet Output Maximum Dynamic V_{OL}	5.0	C_L = 50 pF	0.3	0.8	V
V_{OLV}[2]	Quiet Output Minimum Dynamic V_{OL}	5.0	C_L = 50 pF	–0.3	–0.8	V
V_{IHD}[2]	Minimum HIGH Level Dynamic Input Voltage	5.0	C_L = 50 pF		3.5	V
V_{ILD}[2]	Maximum LOW Level Dynamic Input Voltage	5.0	C_L = 50 pF		1.5	V

2. Parameter guaranteed by design.

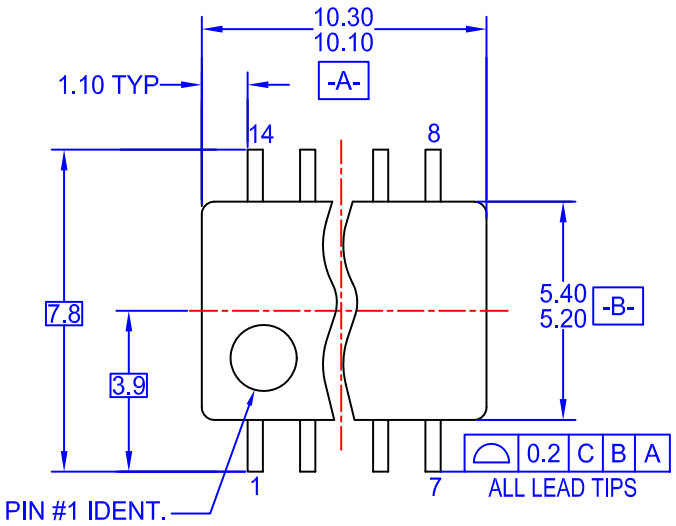
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C			T_A = –40°C to +85°C		Units
				Min	Typ	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay	3.3 ± 0.3	C_L = 15 pF		6.2	8.8	1.0	10.5	ns
			C_L = 50 pF		8.7	12.3	1.0	14.0	
		5.0 ± 0.5	C_L = 15 pF		4.3	5.9	1.0	7.0	ns
			C_L = 50 pF		5.8	7.9	1.0	9.0	
C_{IN}	Input Capacitance		V_{CC} = Open		4	10		10	pF
C_{PD}	Power Dissipation Capacitance		(Note 3)		18				pF

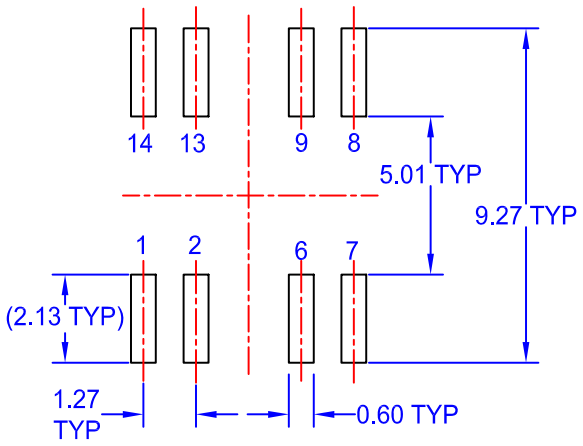
3. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC} / 4 (per gate).

SOP14
CASE 565BE
ISSUE O

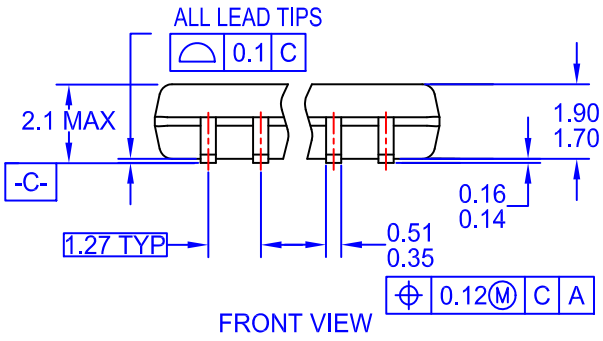
DATE 31 DEC 2016



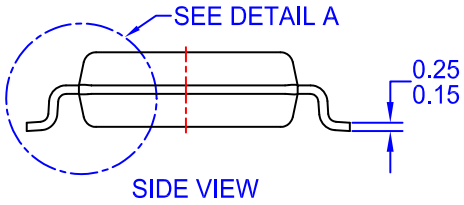
TOP VIEW



LAND PATTERN RECOMMENDATION

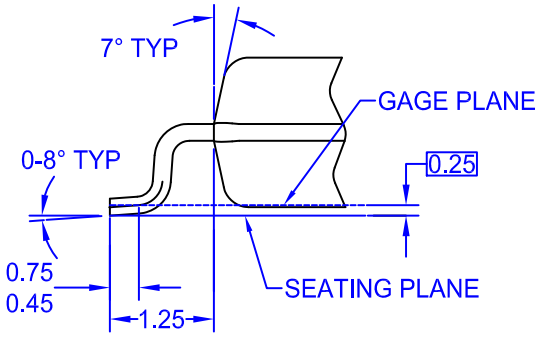


FRONT VIEW



SIDE VIEW

NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

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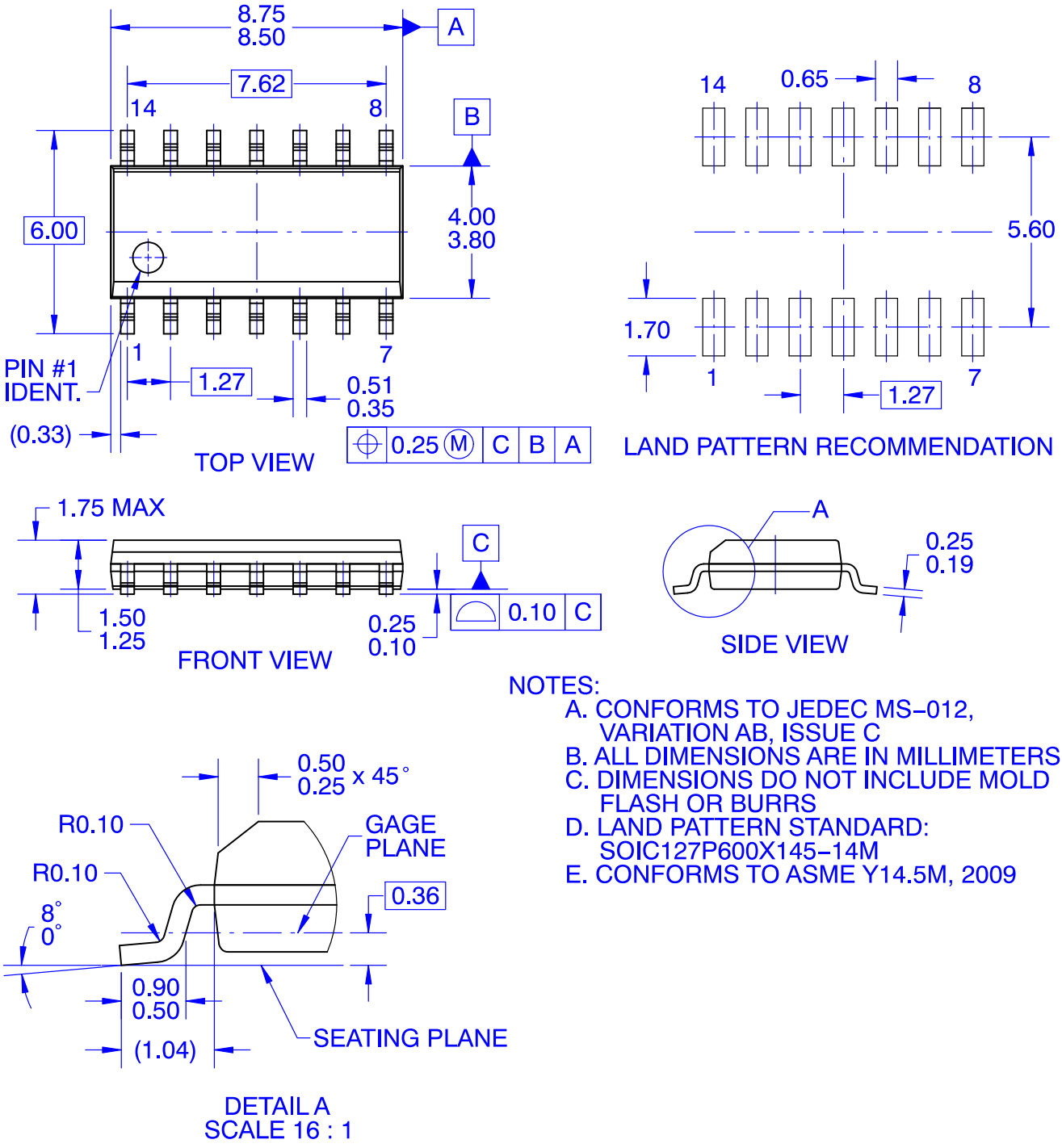
DESCRIPTION:	**SOP14**	**PAGE 1 OF 1**

SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:
A. CONFORMS TO JEDEC MS–012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145–14M
E. CONFORMS TO ASME Y14.5M, 2009

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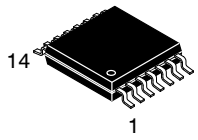
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

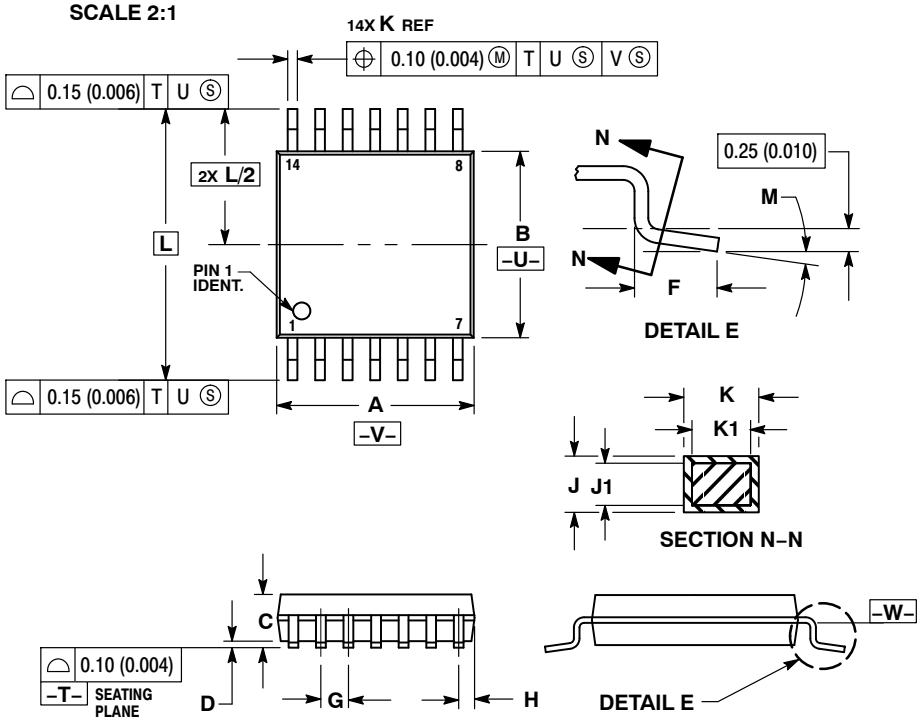
ON Semiconductor®

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



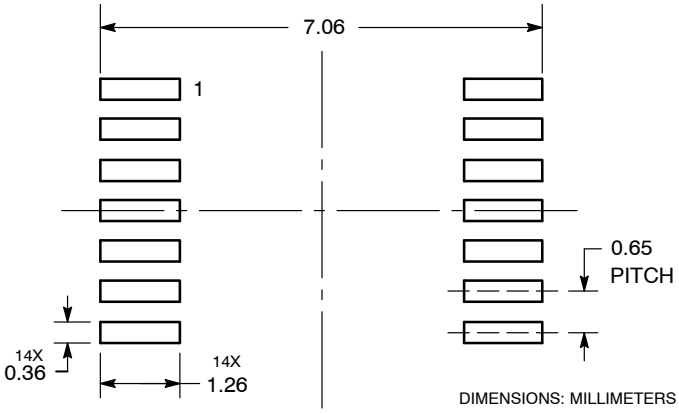
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

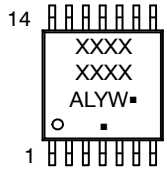
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98ASH70246A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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