EFR32FG1 Flex Gecko Proprietary Protocol SoC Family Data Sheet

The Flex Gecko proprietary protocol family of SoCs is part of the Wireless Gecko portfolio. Flex Gecko SoCs are ideal for enabling energy-friendly proprietary protocol networking for IoT devices.

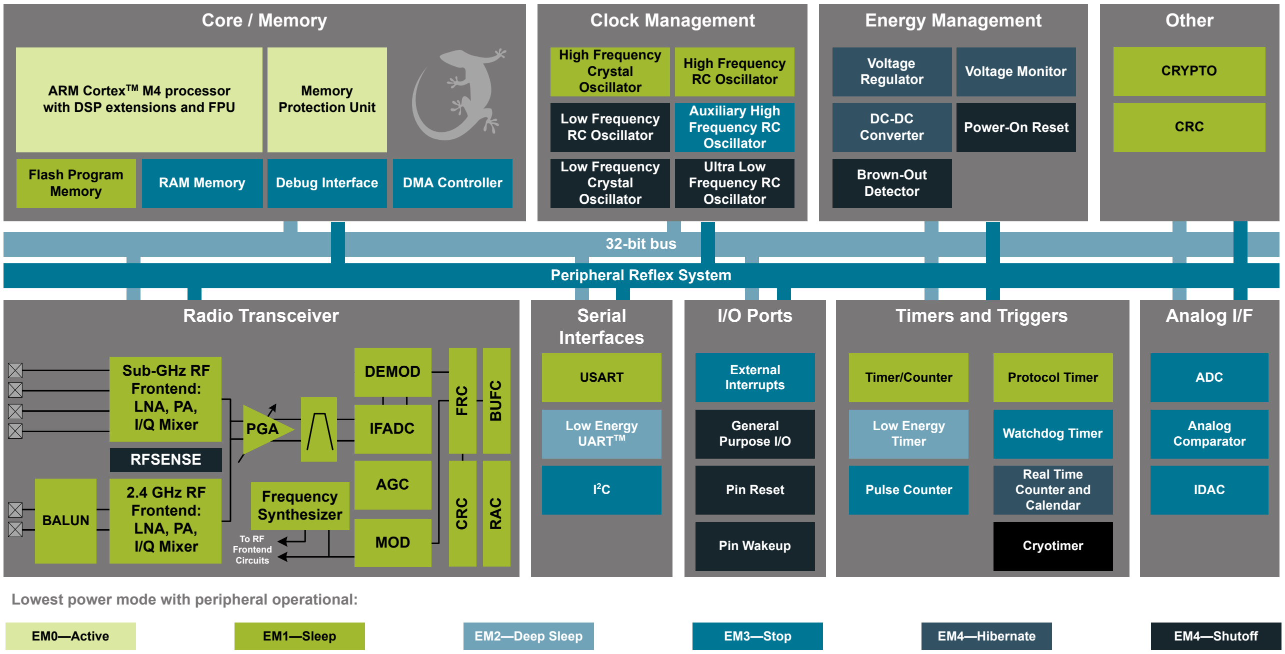
The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, an integrated balun and no-compromise MCU features.

Flex Gecko applications include:

- Home and Building Automation and Security
- Metering
- Electronic Shelf Labels
- Industrial Automation
- Commercial and Retail Lighting and Sensing

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- Up to 256 kB of flash and 32 kB of RAM
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated PA with up to 19 dBm (2.4 GHz) or 20 dBm (Sub-GHz) TX power
- Integrated balun for 2.4 GHz
- Robust peripheral set and up to 32 GPIO



1. Feature List

The EFR32FG1 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 256 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz and Sub-GHz radio operation
  - Transmit power:
    - 2.4 GHz radio: Up to 19.5 dBm
    - Sub-GHz radio: Up to 20 dBm
- **Low Energy Consumption**
  - 7.6 mA RX current at 38.4 kbps, GFSK, 169 MHz
  - 8.7 mA RX current at 1 Mbps, GFSK, 2.4 GHz
  - 9.8 mA RX current at 250 kbps, DSSS-OQPSK, 2.4 GHz
  - 8.2 mA TX current at 0 dBm output power at 2.4 GHz
  - 34.5 mA TX current at 14 dBm output power at 868 MHz
  - 63 μA/MHz in Active Mode (EM0)
  - 2.2 μA EM2 DeepSleep current (4 kB RAM retention and RTCC running from LFRCO)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -92.5 dBm sensitivity at 1 Mbit/s GFSK, 2.4 GHz
  - -99 dBm sensitivity at 250 kbps DSSS-OQPSK, 2.4 GHz
  - -126.4 dBm sensitivity at 600 bps, GFSK, 915 MHz
  - -121.4 dBm sensitivity at 2.4 kbps, GFSK, 868 MHz
  - -107 dBm sensitivity at 4.8 kbps, OOK, 433 MHz
  - -111.9 dBm sensitivity at 38.4 kbps, GFSK, 169 MHz
- **Supported Modulation Formats**
  - 2/4 (G)FSK with fully configurable shaping
  - BPSK / DBPSK TX
  - OOK / ASK
  - Shaped OQPSK / (G)MSK
  - Configurable DSSS and FEC
- **Supported Protocols**
  - Proprietary Protocols
  - Wireless M-Bus
  - Selected IEEE 802.15.4g SUN-FSK PHYs
  - Low Power Wide Area Networks
- **Suitable for Systems Targeting Compliance With:**
  - FCC Part 90.210 Mask D, FCC part 15.247, 15.231, 15.249
  - ETSI Category I Operation, EN 300 220, EN 300 328
  - ARIB T-108, T-96
  - China regulatory
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - Digital to Analog Current Converter (IDAC)
  - Up to 32 pins connected to analog channels (APORT) shared between analog peripherals
  - Up to 32 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 × 16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^{2}S)
  - Low Energy UART (LEUART™)
  - I^{2}C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.85 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C) and Extended (-40 °C to 125 °C) temperature grades available
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **QFN32 5x5 mm Package**
- **QFN48 7x7 mm Package**

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package	Temp Range
EFR32FG1P133F256GM48-C0	Proprietary	• 2.4 GHz @ 19 dBm • Sub-GHz @ 20 dBm	256	32	28	QFN48	-40 to +85°C
EFR32FG1P133F128GM48-C0	Proprietary	• 2.4 GHz @ 19 dBm • Sub-GHz @ 20 dBm	128	32	28	QFN48	-40 to +85°C
EFR32FG1P133F64GM48-C0	Proprietary	• 2.4 GHz @ 19 dBm • Sub-GHz @ 20 dBm	64	16	28	QFN48	-40 to +85°C
EFR32FG1P132F256GM48-C0	Proprietary	2.4 GHz @ 19 dBm	256	32	31	QFN48	-40 to +85°C
EFR32FG1P132F128GM48-C0	Proprietary	2.4 GHz @ 19 dBm	128	32	31	QFN48	-40 to +85°C
EFR32FG1P132F64GM48-C0	Proprietary	2.4 GHz @ 19 dBm	64	16	31	QFN48	-40 to +85°C
EFR32FG1P132F256GM32-C0	Proprietary	2.4 GHz @ 19 dBm	256	32	16	QFN32	-40 to +85°C
EFR32FG1P132F128GM32-C0	Proprietary	2.4 GHz @ 19 dBm	128	32	16	QFN32	-40 to +85°C
EFR32FG1P132F64GM32-C0	Proprietary	2.4 GHz @ 19 dBm	64	16	16	QFN32	-40 to +85°C
EFR32FG1P131F256GM48-C0	Proprietary	Sub-GHz @ 20 dBm	256	32	32	QFN48	-40 to +85°C
EFR32FG1P131F256IM48-C0	Proprietary	Sub-GHz @ 20 dBm	256	32	32	QFN48	-40 to +125°C
EFR32FG1P131F128GM48-C0	Proprietary	Sub-GHz @ 20 dBm	128	32	32	QFN48	-40 to +85°C
EFR32FG1P131F64GM48-C0	Proprietary	Sub-GHz @ 20 dBm	64	16	32	QFN48	-40 to +85°C
EFR32FG1P131F256GM32-C0	Proprietary	Sub-GHz @ 20 dBm	256	32	16	QFN32	-40 to +85°C
EFR32FG1P131F256IM32-C0	Proprietary	Sub-GHz @ 20 dBm	256	32	16	QFN32	-40 to +125°C
EFR32FG1P131F128GM32-C0	Proprietary	Sub-GHz @ 20 dBm	128	32	16	QFN32	-40 to +85°C
EFR32FG1P131F64GM32-C0	Proprietary	Sub-GHz @ 20 dBm	64	16	16	QFN32	-40 to +85°C
EFR32FG1V132F256GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	256	32	31	QFN48	-40 to +85°C
EFR32FG1V132F128GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	128	16	31	QFN48	-40 to +85°C
EFR32FG1V132F64GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	64	16	31	QFN48	-40 to +85°C
EFR32FG1V132F32GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	32	8	31	QFN48	-40 to +85°C
EFR32FG1V132F256GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	256	32	16	QFN32	-40 to +85°C
EFR32FG1V132F128GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	128	16	16	QFN32	-40 to +85°C
EFR32FG1V132F64GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	64	16	16	QFN32	-40 to +85°C
EFR32FG1V132F32GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	32	8	16	QFN32	-40 to +85°C
EFR32FG1V131F256GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	256	32	32	QFN48	-40 to +85°C
EFR32FG1V131F128GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	128	16	32	QFN48	-40 to +85°C
EFR32FG1V131F64GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	64	16	32	QFN48	-40 to +85°C
EFR32FG1V131F32GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	32	8	32	QFN48	-40 to +85°C
EFR32FG1V131F256GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	256	32	16	QFN32	-40 to +85°C

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EFR32FG1V131F64GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	64	16	16	QFN32	-40 to +85°C
EFR32FG1V131F32GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	32	8	16	QFN32	-40 to +85°C
EFR32FG1V032F256GM32-C0	Proprietary	2.4 GHz @ 8 dBm	256	32	16	QFN32	-40 to +85°C
EFR32FG1V032F128GM32-C0	Proprietary	2.4 GHz @ 8 dBm	128	16	16	QFN32	-40 to +85°C

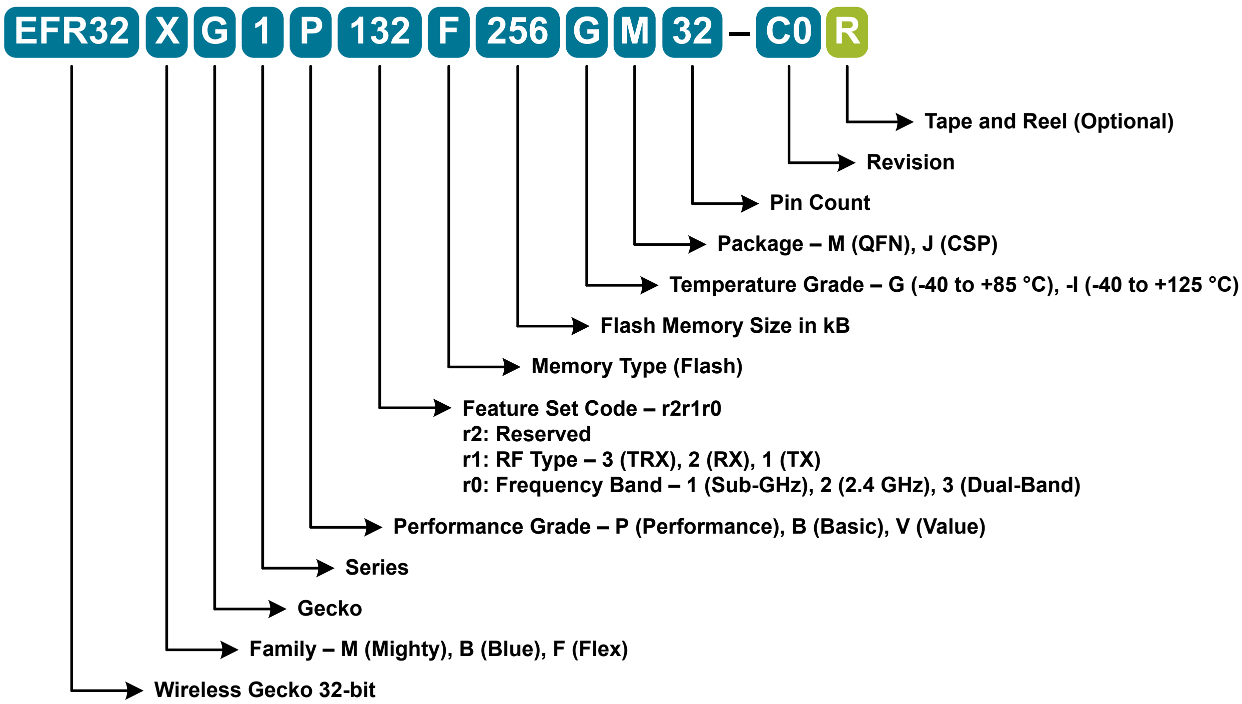

Figure 2.1. Ordering Code Key

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG1 Reference Manual.

A block diagram of the EFR32FG1 family is shown in Figure 3.1 Detailed EFR32FG1 Block Diagram on page 8. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

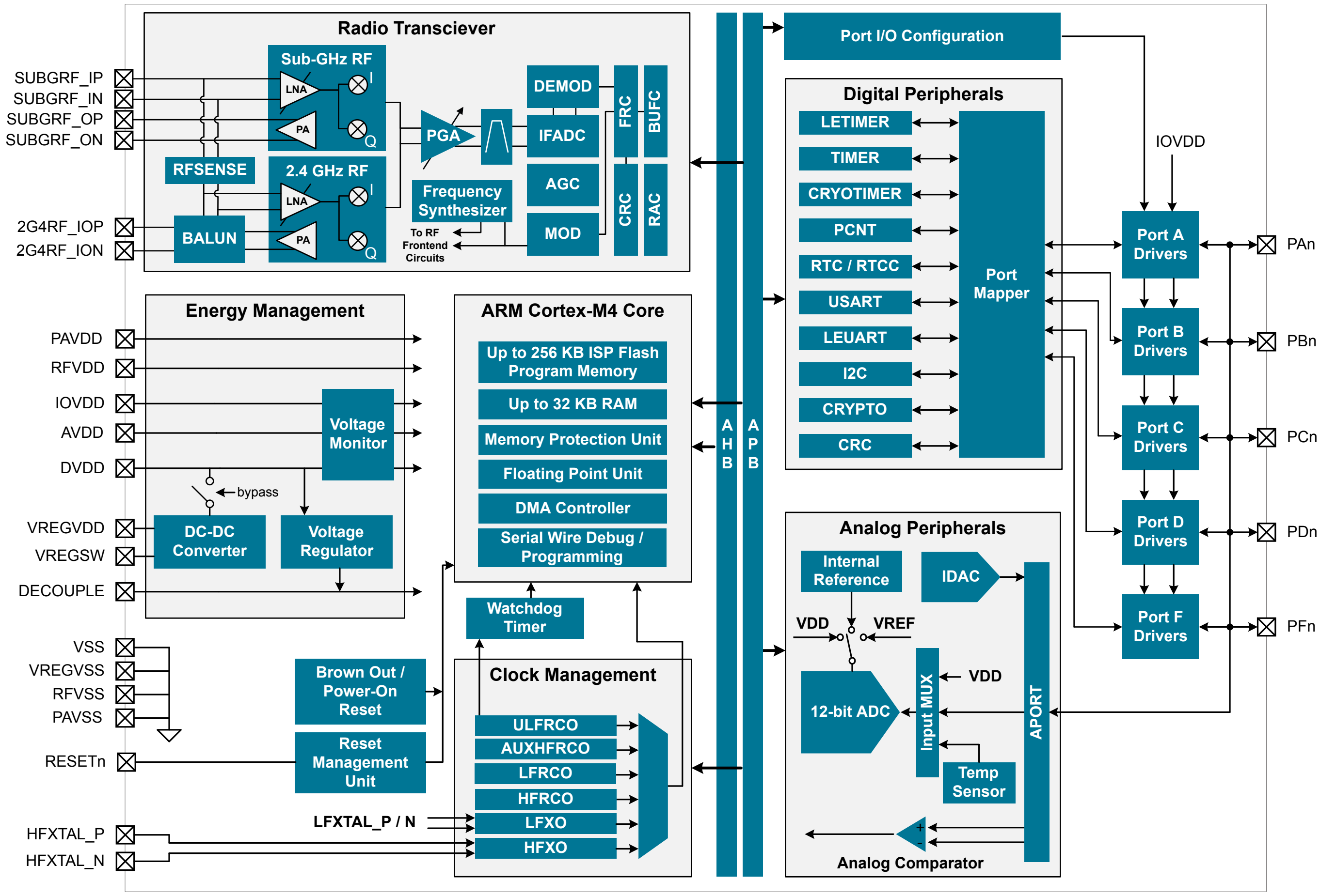


Figure 3.1. Detailed EFR32FG1 Block Diagram

3.2 Radio

The Flex Gecko family features a radio transceiver supporting proprietary wireless protocols.

3.2.1 Antenna Interface

The EFR32FG1 family includes devices which support both single-band and dual-band RF communication over separate physical RF interfaces.

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The sub-GHz antenna interface consists of a differential transmit interface (pins SUBGRF_OP and SUBGRF_ON) and a differential receive interface (pinsSUBGRF_IP and SUBGRF_IN).

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32FG1 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.2.3 Receiver Architecture

The EFR32FG1 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS) for 2.4 GHz and sub-GHz bands.

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32FG1 features integrated support for antenna diversity to mitigate the problem of frequency-selective fading due to multipath propagation and improve link budget. Support for antenna diversity is available for specific PHY configurations in 2.4 GHz and sub-GHz bands. Internal configurable hardware controls an external switch for automatic switching between antennae during RF receive detection operations.

Note: Due to the shorter preamble of 802.15.4 and BLE packets, RX diversity is not supported.

3.2.4 Transmitter Architecture

The EFR32FG1 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32FG1. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32FG1 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.6 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.7 Flexible Frame Handling

EFR32FG1 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.2.8 Packet and State Trace

The EFR32FG1 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.9 Data Buffering

The EFR32FG1 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32FG1. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The EFR32FG1 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

AVDD and VREGVDD need to be 1.85 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

EFR32FG1 has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32FG1. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32FG1 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM} provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32FG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32FG1 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

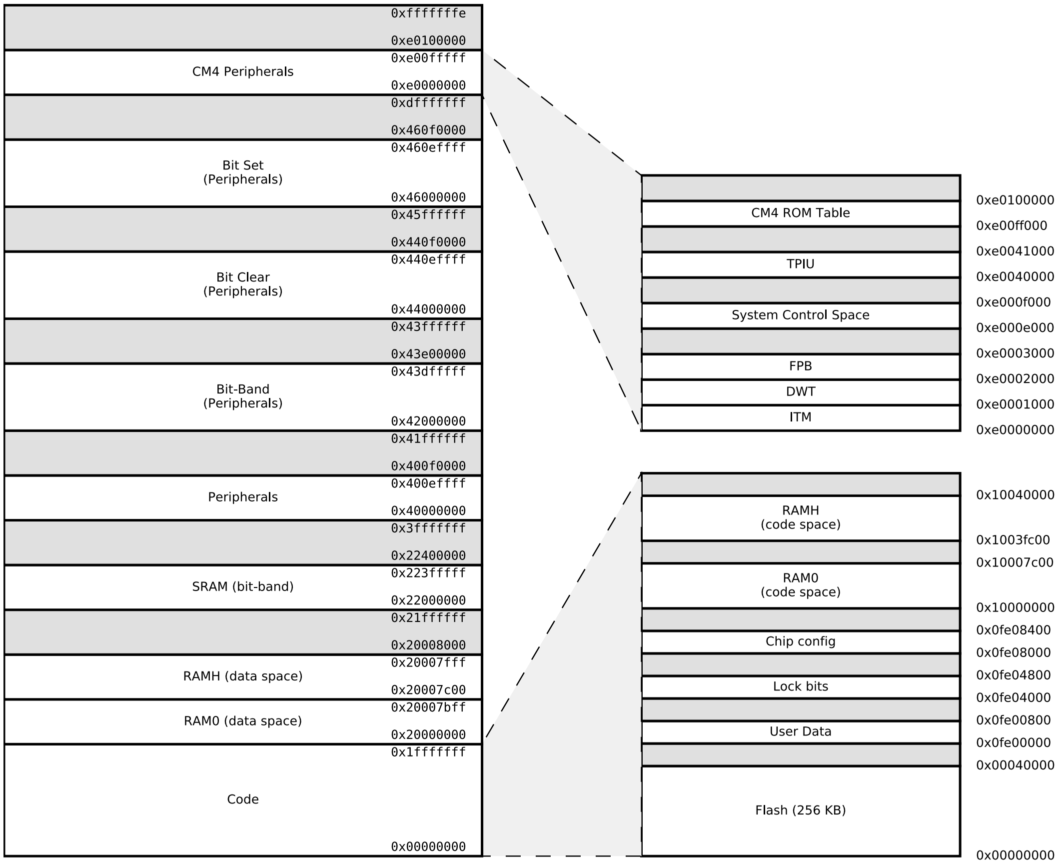


Figure 3.2. EFR32FG1 Memory Map — Core Peripherals and Code Space

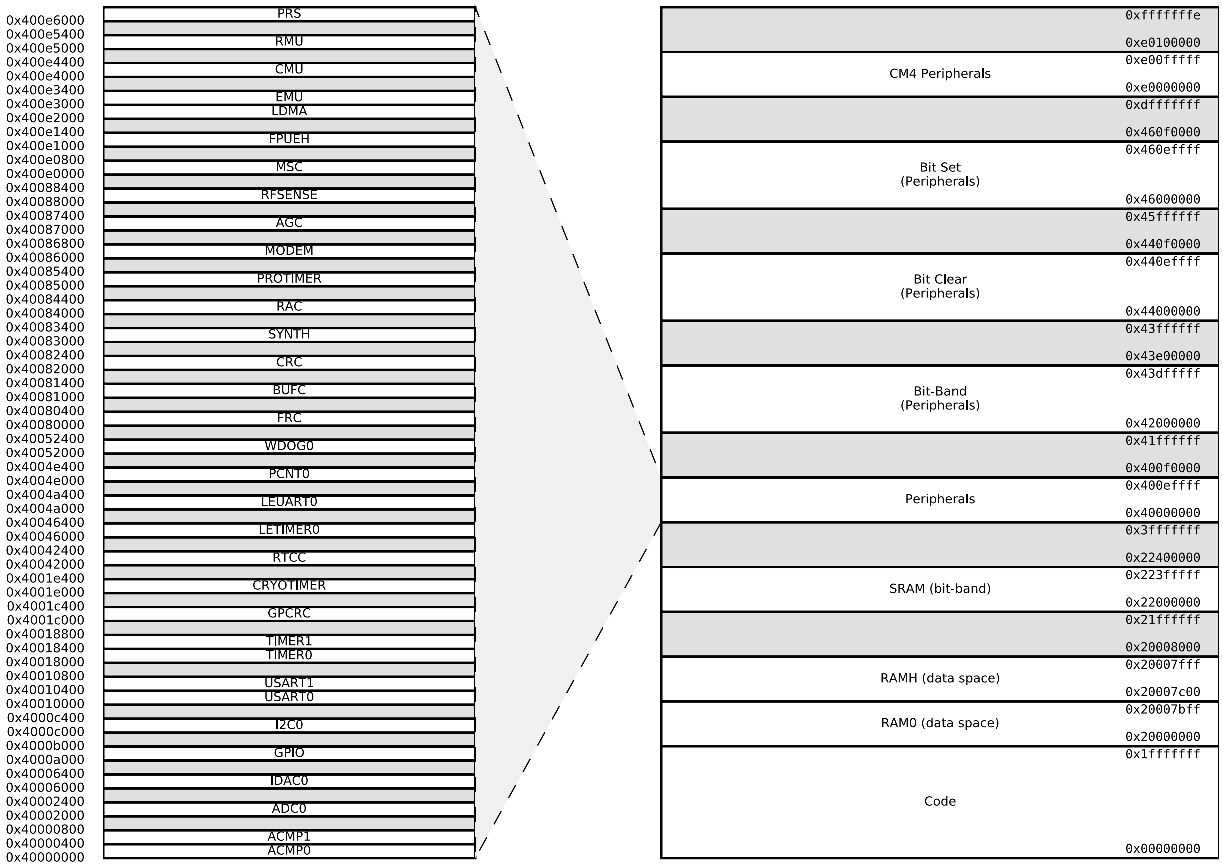


Figure 3.3. EFR32FG1 Memory Map — Peripherals

3.13 Configuration Summary

The features of the EFR32FG1 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}	5V tolerant GPIO pins[1 2 3]	-0.3	—	Min of 5.25 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Input RF level on pins 2G4RF_IOP and 2G4RF_ION	$P_{RFMAX2G4}$		—	—	10	dBm
Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION)	$V_{MAXDIFF2G4}$		-50	—	50	mV
Absolute voltage on RF pins 2G4RF_IOP and 2G4RF_ION	V_{MAX2G4}		-0.3	—	3.3	V
Absolute voltage on Sub-GHz RF pins	$V_{MAXSUBG}$	Pins SUBGRF_OP and SUBGRF_ON	-0.3	—	3.3	V
		Pins SUBGRF_IP and SUBGRF_IN,	-0.3	—	0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J	-G grade devices	-40	—	105	°C
		-I grade devices	-40	—	125	°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD, RFVDD, PAVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD
- PAVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[5]	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage[2]	V_{AVDD}		1.85	3.3	3.8	V
VREGVDD operating supply voltage[2] [1]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.85	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
RFVDD operating supply voltage	V_{RFVDD}		1.62	—	$V_{VREGVDD}$	V
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
PAVDD operating supply voltage	V_{PAVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[3] [4]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)[2]	dV_{DD}		—	—	0.1	V
HFCORECLK frequency	f_{CORE}	MODE = WS0	—	—	26	MHz
		MODE = WS1	—	—	40	MHz
HFCLK frequency	f_{HFCLK}	MODE = WS0	—	—	26	MHz
		MODE = WS1	—	—	40	MHz

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN48 Package	$THETA_{JA\_QFN48}$	2-Layer PCB, Air velocity = 0 m/s	—	64.5	—	°C/W
		2-Layer PCB, Air velocity = 1 m/s	—	51.6	—	°C/W
		2-Layer PCB, Air velocity = 2 m/s	—	47.7	—	°C/W
		4-Layer PCB, Air velocity = 0 m/s	—	26.2	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	23.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	22.1	—	°C/W
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	2-Layer PCB, Air velocity = 0 m/s	—	79	—	°C/W
		2-Layer PCB, Air velocity = 1 m/s	—	62.2	—	°C/W
		2-Layer PCB, Air velocity = 2 m/s	—	54.1	—	°C/W
		4-Layer PCB, Air velocity = 0 m/s	—	32	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	28.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	26.9	—	°C/W

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=1.0 µF (Murata GRM188R71A105KA61D), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.85	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	1.7	—	1.9	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIAS[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	1.63	—	2.2	V
		Low Power (LP) mode, LPCMPBIAS[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	1.63	—	2.1	V
Steady-state output ripple	V_R	Radio disabled	—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	—	150	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	—	150	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	50	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	125	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2], T ≤ 85 °C	—	—	200	mA
		Low noise (LN) mode, Heavy Drive[2], T > 85 °C	—	—	100	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIAS[3] = 0	—	—	75	μA
		Low power (LP) mode, LPCMPBIAS[3] = 3	—	—	10	mA
DCDC nominal output capacitor	C_{DCDC}	25% tolerance	1	1	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	2.5	Ω

Note:
1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. In the EMU_DCDCMISCCTRL register.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 3.3 V. T = 25 °C. EMU_PWRCFG_PWRCFG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	130	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	105	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	106	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	222	350	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	65	—	µA/MHz
		38 MHz HFRCO	—	35	38	µA/MHz
		26 MHz HFRCO	—	37	41	µA/MHz
		1 MHz HFRCO	—	157	275	µA/MHz
Current consumption in EM2 mode	I_{EM2}	Full 32 kB RAM retention and RTCC running from LFXO	—	3.3	—	µA
		1 bank (4 kB) RAM retention and RTCC running from LFRCO	—	3	6.3	µA
Current consumption in EM3 mode	I_{EM3}	Full 32 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.8	6	µA
Current consumption in EM4H mode	I_{EM4H}	128 byte RAM retention, RTCC running from LFXO	—	1.1	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.65	—	µA
		128 byte RAM retention, no RTCC	—	0.65	1.3	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.04	0.11	µA

Note:

1. CMU_HFXOCTRL_LOWPOWER=0.

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{ACTIVE_DCM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	71	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	76	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1]	I_{ACTIVE_CCM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	75	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	88	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	38.4 MHz crystal[4]	—	49	—	µA/MHz
		38 MHz HFRCO	—	32	—	µA/MHz
		26 MHz HFRCO	—	38	—	µA/MHz
Current consumption in EM2 mode, DCDC in LP mode[3]	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	2.5	—	µA
		1 bank (4 kB) RAM retention and RTCC running from LFRCO	—	2.2	—	µA
Current consumption in EM3 mode	I_{EM3}	Full 32 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.1	—	µA
Current consumption in EM4H mode	I_{EM4H}	128 byte RAM retention, RTCC running from LFXO	—	0.86	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.58	—	µA
		128 byte RAM retention, no RTCC	—	0.58	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.04	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIAS=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. CMU_HFXOCTRL_LOWPOWER=0.

4.1.5.3 Current Consumption 1.85 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 1.85 V. T = 25 °C. EMU_PWRCFG_PWRCFG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 1.85 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	131	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	220	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	65	—	μA/MHz
		38 MHz HFRCO	—	35	—	μA/MHz
		26 MHz HFRCO	—	37	—	μA/MHz
		1 MHz HFRCO	—	154	—	μA/MHz
Current consumption in EM2 mode	I_{EM2}	Full 32 kB RAM retention and RTCC running from LFXO	—	3.2	—	μA
		1 bank (4 kB) RAM retention and RTCC running from LFRCO	—	2.8	—	μA
Current consumption in EM3 mode	I_{EM3}	Full 32 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.7	—	μA
Current consumption in EM4H mode	I_{EM4H}	128 byte RAM retention, RTCC running from LFXO	—	1	—	μA
		128 byte RAM retention, RTCC running from LFXO, serial flash in deep power down	—	0.62	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.62	—	μA
Current consumption in EM4S mode	I_{EM4S}	no RAM retention, no RTCC	—	0.02	—	μA

Note:

1. CMU_HFXOCTRL_LOWPOWER=0.

4.1.5.4 Current Consumption Using Radio 3.3 V with DC-DC

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.8. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I_{RX_ACTIVE}	500 kbit/s, 2GFSK, F = 915 MHz, Radio clock prescaled by 4	—	8.4	10	mA
		38.4 kbit/s, 2GFSK, F = 868 MHz, Radio clock prescaled by 4	—	8.1	10	mA
		38.4 kbit/s, 2GFSK, F = 490 MHz, Radio clock prescaled by 4	—	7.9	10	mA
		50 kbit/s, 2GFSK, F = 433 MHz, Radio clock prescaled by 4	—	7.7	10	mA
		38.4 kbit/s, 2GFSK, F = 315 MHz, Radio clock prescaled by 4	—	7.9	10	mA
		38.4 kbit/s, 2GFSK, F = 169 MHz, Radio clock prescaled by 4	—	7.6	10	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	8.7	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	9.8	—	mA
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C	$I_{RX\_ACTIVE\_HT}$	500 kbit/s, 2GFSK, F = 915 MHz, Radio clock prescaled by 4	—	—	10.8	mA
		38.4 kbit/s, 2GFSK, F = 868 MHz, Radio clock prescaled by 4	—	—	10.5	mA
		38.4 kbit/s, 2GFSK, F = 490 MHz, Radio clock prescaled by 4	—	—	10.8	mA
		50 kbit/s, 2GFSK, F = 433 MHz, Radio clock prescaled by 4	—	—	10.5	mA
		38.4 kbit/s, 2GFSK, F = 315 MHz, Radio clock prescaled by 4	—	—	10.9	mA
		38.4 kbit/s, 2GFSK, F = 169 MHz, Radio clock prescaled by 4	—	—	10.2	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I_{TX}	F = 915 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	80.2	104	mA
		F = 915 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	35.5	40.9	mA
		F = 868 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	84.9	114	mA
		F = 868 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	34.5	42	mA
		F = 490 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	82.8	112	mA
		F = 433 MHz, CW, 10 dBm match, PAVDD connected to DCDC output	—	19.5	22.1	mA
		F = 433 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	32.3	37.8	mA
		F = 315 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	32.5	39.4	mA
		F = 169 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	80.2	106.9	mA
		F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3	—	8.2	—	mA
		F = 2.4 GHz, CW, 3 dBm output power	—	16.5	—	mA
		F = 2.4 GHz, CW, 8 dBm output power	—	23.3	—	mA
		F = 2.4 GHz, CW, 10.5 dBm output power	—	32.7	—	mA
		F = 2.4 GHz, CW, 16.5 dBm output power, PAVDD connected directly to external 3.3V supply	—	83.9	—	mA
		F = 2.4 GHz, CW, 19.5 dBm output power, PAVDD connected directly to external 3.3V supply	—	126.7	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C	I_{TX_HT}	F = 915 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	—	108.5	mA
		F = 915 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	—	42.9	mA
		F = 868 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	—	118.2	mA
		F = 868 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	—	42	mA
		F = 490 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	—	117	mA
		F = 433 MHz, CW, 10 dBm match, PAVDD connected to DCDC output	—	—	23	mA
		F = 433 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	—	37.8	mA
		F = 315 MHz, CW, 14 dBm match, PAVDD connected to DCDC output	—	—	39.4	mA
		F = 169 MHz, CW, 20 dBm match, PAVDD connected directly to external 3.3V supply	—	—	110.7	mA
RFSENSE current consumption	$I_{RFSENSE}$		—	51	—	nA

4.1.6 Wake Up Times

Table 4.9. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.7	—	μs
		Code execution from RAM	—	3	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.7	—	μs
		Code execution from RAM	—	3	—	μs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	60	—	μs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	290	—	μs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.

4.1.7 Brown Out Detector (BOD)

Table 4.10. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling	1.35	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	24	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.85	V
		AVDD falling	1.62	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	21	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	46	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.8 Frequency Synthesizer

Table 4.11. Frequency Synthesizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF synthesizer frequency range	f_{RANGE}	2400 - 2483.5 MHz	2400	—	2483.5	MHz
		779 - 956 MHz	779	—	956	MHz
		390 - 574 MHz	390	—	574	MHz
		195 - 358 MHz	195	—	358	MHz
		110 - 191 MHz	110	—	191	MHz
LO tuning frequency resolution with 38.4 MHz crystal	f_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
		779 - 956 MHz	—	—	24	Hz
		390 - 574 MHz	—	—	12.2	Hz
		195 - 358 MHz	—	—	7.3	Hz
		110 - 191 MHz	—	—	4.6	Hz
Frequency deviation resolution with 38.4 MHz crystal	df_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
		779 - 956 MHz	—	—	24	Hz
		390 - 574 MHz	—	—	12.2	Hz
		195 - 358 MHz	—	—	7.3	Hz
		110 - 191 MHz	—	—	4.6	Hz
Maximum frequency deviation with 38.4 MHz crystal	df_{MAX}	2400 - 2483.5 MHz	—	—	1677	kHz
		779 - 956 MHz	—	—	559	kHz
		390 - 574 MHz	—	—	280	kHz
		195 - 358 MHz	—	—	167	kHz
		110 - 191 MHz	—	—	105	kHz

4.1.9 2.4 GHz RF Transceiver Characteristics

4.1.9.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.12. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power[1]	$POUT_{MAX}$	19 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply[2]	—	19.5	—	dBm
		16 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply	—	16.5	—	dBm
		8 dBm-rated part numbers	—	8	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-30	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm< Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.85 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, for output power > 10.5 dBm.	—	4.5	—	dB
		1.85 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter	—	2.2	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR\_T}$	From -40 to +85 °C, PAVDD connected to DC-DC output	—	1.5	—	dB
		From -40 to +125 °C, PAVDD connected to DC-DC output	—	2.2	—	dB
		From -40 to +85 °C, PAVDD connected to external supply	—	1.5	—	dB
		From -40 to +125 °C, PAVDD connected to external supply	—	3.4	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR\_F}$	Over RF tuning frequency range	—	0.4	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

Note:
1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. For Bluetooth, the Maximum TX power on Channel 2456 is limited to +15 dBm to comply with In-band Spurious emissions.

4.1.9.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.13. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm
Level above which RFSENSE will trigger[2]	$RFSENSE_{TRIG}$	CW at 2.45 GHz	—	-24	—	dBm
Level below which RFSENSE will not trigger[2]	$RFSENSE_{THRES}$	CW at 2.45 GHz	—	-50	—	dBm
1% PER sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal[1]	—	-89.2	—	dBm
		250 kbps 2GFSK signal	—	-99.1	—	dBm

Note:

1. Channel at 2420 MHz will have degraded sensitivity. Sensitivity could be as high as -83 dBm on this channel.
2. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.9.3 RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 85%.

Table 4.14. RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6dB bandwidth	TXBW	10 dBm	—	740	—	kHz
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247 at 10 dBm	—	-6.5	—	dBm/ 3kHz
		Per FCC part 15.247 at 20 dBm	—	-2.6	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	10	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band, 10 dBm	—	1.1	—	MHz
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM\_FCC}$	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	—	-47	—	dBm
Spurious emissions out-of-band, excluding harmonics captured in $SPUR_{HARM,FCC}$. Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply	$SPUR_{OOB\_FCC}$	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands[1]	—	-47	—	dBm
		Per FCC part 15.247, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Non-Restricted Bands	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328	$SPUR_{ETSI328}$	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz	—	-42	—	dBm
		1-12 GHz	—	-36	—	dBm

Note:

1. For 2480 MHz, a maximum duty cycle of 20% is used to achieve this value.

4.1.9.4 RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz.

Table 4.15. RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[3]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER[1]	SENS	Signal is reference signal[3]. Using DC-DC converter.	—	-92.5	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity.	—	8.3	—	dB
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-3	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-0.5	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-43	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_3	Interferer is reference signal at ± 3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-46.7	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-38.7	—	dB
Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision	—	-48.2	—	dB
Blocking, less than 0.1% BER. Desired is -67dBm BLE reference signal at 2426MHz. Interferer is CW in OOB range[2]	$BLOCK_{OOB}$	Interferer frequency 30 MHz ≤ f ≤ 2000 MHz	-5	—	—	dBm
		Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz[4]	-10	—	—	dBm
		Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz	-10	—	—	dBm
		Interferer frequency 3 GHz ≤ f ≤ 6 GHz	-10	—	—	dBm
		Interferer frequency 6 GHz ≤ f ≤ 12.75 GHz	-17	—	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:
1. Receive sensitivity on Bluetooth Low Energy channel 26 is -86 dBm.
2. Interferer max power limited by equipment capabilities and path loss. Minimum specified at 25 °C.
3. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.
4. Except -13 dBm at Desired Frequency - Crystal Frequency.

4.1.9.5 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 66%.

Table 4.16. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude (offset EVM), per 802.15.4-2011, not including 2415 MHz channel[5]	EVM	Average across frequency. Signal is DSSS-OQPSK reference packet[1]	—	5.5	—	% rms
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ± 3.5 MHz, output power at $POUT_{MAX}$	—	-26	—	dBc/ 100kHz
		Absolute, at carrier ± 3.5 MHz, output power at $POUT_{MAX}$[3]	—	-36	—	dBm/ 100kHz
		Per FCC part 15.247, output power at $POUT_{MAX}$	—	-4.2	—	dBm/ 3kHz
		ETSI	—	12	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	—	2.25	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier	—	-45.8	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz	$SPUR_{HRM\_FCC\_NRR}$	Continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz; continuous transmission of modulated carrier	—	-52	—	dBm
		Restricted bands 88-216 MHz; continuous transmission of modulated carrier	—	-62	—	dBm
		Restricted bands 216-960 MHz; continuous transmission of modulated carrier	—	-57	—	dBm
		Restricted bands >960 MHz; continuous transmission of modulated carrier[4]	—	-48	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247, Emissions taken at $POUT_{MAX}$, PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz	$SPUR_{OOB\_FCC\_NR}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328[2]	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW];	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW]; per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440[2]	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies	—	-42	—	dBm
		1G-14G	—	-36	—	dBm

Note:

1. Reference packet is defined as 20 octet PSDU, modulated according to 802.15.4-2011 DSSS-OQPSK in the 2.4GHz band, with pseudo-random packet data content.
2. Specified at maximum power output level of 10 dBm.
3. For 2415 MHz, a maximum duty cycle of 50% is used to achieve this value.
4. For 2480 MHz, a maximum duty cycle of 20% is used to achieve this value.
5. Typical EVM for the 2415 MHz channel is 7.9%.

4.1.9.6 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.17. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal[5]. Packet length is 20 octets.	—	10	—	dBm
Sensitivity, 1% PER[2]	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	—	-99	—	dBm
		Signal is reference signal. Packet length is 20 octets. Without DC-DC converter.	—	-99	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	-2.6	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[6]	ACR_{P1}	Interferer is reference signal at +1 channel-spacing.	—	33.75	—	dB
		Interferer is filtered reference signal[3] at +1 channel-spacing.	—	52.2	—	dB
		Interferer is CW at +1 channel-spacing[4].	—	58.6	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[6]	ACR_{M1}	Interferer is reference signal at -1 channel-spacing.	—	35	—	dB
		Interferer is filtered reference signal[3] at -1 channel-spacing.	—	54.7	—	dB
		Interferer is CW at -1 channel-spacing.	—	60.1	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[6]	ACR_2	Interferer is reference signal at ± 2 channel-spacing	—	45.9	—	dB
		Interferer is filtered reference signal[3] at ± 2 channel-spacing	—	56.8	—	dB
		Interferer is CW at ± 2 channel-spacing	—	65.5	—	dB
Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level[6]	IR	Interferer is CW in image band[4]	—	49.3	—	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level[6]. Interferer is reference signal	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	57.2	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	57.9	—	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz[1]	$BLOCK_{80211G}$	Desired is reference signal at 6dB above reference sensitivity level[6]	—	51.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2003	$RSSI_{LIN}$		—	+/-1	—	dB

Note:

1. This is an IEEE 802.11b/g ERP-PBCC 22 MBit/s signal as defined by the IEEE 802.11 specification and IEEE 802.11g addendum.
2. Receive sensitivity on 802.15.4 channel 14 is -98 dBm
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stop-band rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.
5. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
6. Reference sensitivity level is -85 dBm.

4.1.10 Sub-GHz RF Transceiver Characteristics

4.1.10.1 Sub-GHz RF Transmitter characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 915 MHz.

Table 4.18. Sub-GHz RF Transmitter characteristics for 915 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		902	—	930	MHz
Maximum TX Power[1]	$POUT_{MAX}$	PAVDD connected directly to external 3.3V supply, 20 dBm output power setting	17.7	20.3	24.5	dBm
		PAVDD connected to DC-DC output, 14 dBm output power setting	10.4	13.8	17.6	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-45.5	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected to external supply, T = 25 °C	—	4.8	—	dB
		1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected to DC-DC output, T = 25 °C	—	1.9	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	-40 to +85 °C with PAVDD connected to external supply	—	0.6	1.3	dB
		-40 to +125 °C with PAVDD connected to external supply	—	0.8	1.6	dB
		-40 to +85 °C with PAVDD connected to DC-DC output	—	0.7	1.4	dB
		-40 to +125 °C with PAVDD connected to DC-DC output	—	1.0	1.9	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	PAVDD connected to external supply, T = 25 °C	—	0.2	0.6	dB
		PAVDD connected to DC-DC output, T = 25 °C	—	0.3	0.6	dB
Spurious emissions of harmonics at 20 dBm output power, Conducted measurement, 20dBm match, PAVDD = 3.3V, Test Frequency = 915 MHz	$SPUR_{HARM\_FCC\_20}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-64.6	-47	dBm
		In non-restricted bands, per FCC Part 15.231	—	-64.2	-42	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band at 20 dBm output power, Conducted measurement, 20dBm match, PAVDD = 3.3V, Test Frequency = 915 MHz	$SPUR_{OOB\_FCC\_20}$	In non-restricted bands, per FCC Part 15.231	—	-76.2	-66	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-68.8	-52	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-67.7	-62	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-69.1	-58	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-54.6	-42.4	dBm
Spurious emissions of harmonics at 14 dBm output power, Conducted measurement, 14dBm match, PAVDD connected to DC-DC output, Test Frequency = 915 MHz	$SPUR_{HARM\_FCC\_14}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-75.2	-60	dBm
		In non-restricted bands, per FCC Part 15.231	—	-69	-49	dBc
Spurious emissions out-of-band at 14 dBm output power, Conducted measurement, 14dBm match, PAVDD connected to DC-DC output, Test Frequency = 915 MHz	$SPUR_{OOB\_FCC\_14}$	In non-restricted bands, per FCC Part 15.231	—	-87.5	-66	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-74.2	-52	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-73.1	-67	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-74.3	-58	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-60.2	-49	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.2 Sub-GHz RF Receiver Characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 915 MHz.

Table 4.19. Sub-GHz RF Receiver Characteristics for 915 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		902	—	930	MHz
Max usable input level, 0.1% BER	SAT_{500K}	Desired is reference 500 kbps GFSK signal[4]	—	—	10	dBm
Sensitivity	SENS	Desired is reference 4.8 kbps OOK signal[3], 20% PER, T ≤ 85 °C	—	-104.7	-100.7	dBm
		Desired is reference 4.8 kbps OOK signal[3], 20% PER, T > 85 °C	—	—	-99.5	dBm
		Desired is reference 600 bps GFSK signal[6], 0.1% BER	—	-126.4	—	dBm
		Desired is reference 50 kbps GFSK signal[5], 0.1% BER, T ≤ 85 °C	—	-107.5	-104.2	dBm
		Desired is reference 50 kbps GFSK signal[5], 0.1% BER, T > 85 °C	—	—	-103	dBm
		Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C	—	-105.1	-101.5	dBm
		Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T > 85 °C	—	—	-101.3	dBm
		Desired is reference 500 kbps GFSK signal[4], 0.1% BER, T ≤ 85 °C	—	-97.7	-93.2	dBm
		Desired is reference 500 kbps GFSK signal[4], 0.1% BER, T > 85 °C	—	—	-93	dBm
		Desired is reference 400 kbps GFSK signal[2], 1% PER, T ≤ 85 °C	—	-90.9	-87.5	dBm
		Desired is reference 400 kbps GFSK signal[2], 1% PER, T > 85 °C	—	—	-86.9	dBm
Level above which RFSENSE will trigger[7]	$RFSENSE_{TRIG}$	CW at 915 MHz	—	-25.8	—	dBm
Level below which RFSENSE will not trigger[7]	$RFSENSE_{THRES}$	CW at 915 MHz	—	-50	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing	C/I_1	Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER	—	43.7	—	dB
		Desired is 600 bps GFSK signal[6] at 3dB above sensitivity level, 0.1% BER	—	65.76	—	dB
		Desired is 50 kbps GFSK signal[5] at 3dB above sensitivity level, 0.1% BER	—	48.24	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	51.1	—	dB
		Desired is 500 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	47	—	dB
		Desired is 400 kbps 4GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	35.9	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing	C/I_2	Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER	—	57.2	—	dB
		Desired is 600 bps GFSK signal[6] at 3dB above sensitivity level, 0.1% BER	—	71.76	—	dB
		Desired is 50 kbps GFSK signal[5] at 3dB above sensitivity level, 0.1% BER	—	53.6	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	56.9	—	dB
		Desired is 500 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	53.6	—	dB
		Desired is 400 kbps 4GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	44	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER	—	41.2	—	dB
		Desired is 50 kbps GFSK signal[5] at 3dB above sensitivity level, 0.1% BER	—	52.4	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	50.35	—	dB
		Desired is 500 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	46.2	—	dB
		Desired is 400 kbps 4GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	35.9	—	dB
Blocking selectivity, 0.1% BER. Desired is 100 kbps GFSK signal at 3dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	58.7	—	dB
		Interferer CW at Desired ± 2 MHz	—	60.9	—	dB
		Interferer CW at Desired ± 10 MHz	—	76.4	—	dB
Intermod selectivity, 0.1% BER. CW interferers at 400 kHz and 800 kHz offsets	C/I_{IM}	Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level	—	46.1	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216-960 MHz	—	-77.7	-49.2	dBm
		Above 960 MHz	—	-62.7	-51.7	dBm
Max spurious emissions during active receive mode,per ARIB STD-T108 Section 3.3	$SPUR_{RX\_ARIB}$	Below 710 MHz, RBW=100kHz	—	-77.7	-60	dBm
		710-900 MHz, RBW=1MHz	—	-75.8	-61	dBm
		900-915 MHz, RBW=100kHz	—	-85.4	-61	dBm
		915-930 MHz, RBW=100kHz	—	-85.6	-55	dBm
		930-1000 MHz, RBW=100kHz	—	-85.1	-60	dBm
		Above 1000 MHz, RBW=1MHz	—	-57.9	-47	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 210.4 kHz, channel spacing = 400 kHz.
2. Definition of reference signal is 400 kbps 4GFSK, BT=0.5, inner deviation = 33.3 kHz, RX channel BW = 336.64 kHz, channel spacing = 600 kHz.
3. Definition of reference signal is 4.8 kbps OOK, RX channel BW = 315.6 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 175 kHz, RX channel BW = 2524.8 kHz, channel spacing = 1 MHz.
5. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, Δf = 25 kHz, RX channel BW = 120.229 kHz, channel spacing = 200 kHz.
6. Definition of reference signal is 600 bps 2GFSK, BT=0.5, Δf = 0.3 kHz, RX channel BW = 1262 Hz, channel spacing = 300 kHz.
7. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.3 Sub-GHz RF Transmitter characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 868 MHz.

Table 4.20. Sub-GHz RF Transmitter characteristics for 868 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		863	—	876	MHz
Maximum TX Power[1]	$POUT_{MAX}$	PAVDD connected directly to external 3.3V supply, 20 dBm output power setting, T ≤ 85 °C	16.6	19.6	23	dBm
		PAVDD connected directly to external 3.3V supply, 20 dBm output power setting, T > 85 °C	—	—	23.7	dBm
		PAVDD connected to DC-DC output, 14 dBm output power setting	10	14.7	17.5	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-43.5	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected to external supply, T = 25 °C	—	5	—	dB
		1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected to DC-DC output, T = 25 °C	—	2	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	-40 to +85 °C with PAVDD connected to external supply	—	0.6	0.9	dB
		-40 to +125 °C with PAVDD connected to external supply	—	0.8	1.3	dB
		-40 to +85 °C with PAVDD connected to DC-DC output	—	0.5	1.2	dB
		-40 to +125 °C with PAVDD connected to DC-DC output	—	0.7	1.5	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	PAVDD connected to external supply, T = 25 °C	—	0.2	0.6	dB
		PAVDD connected to DC-DC output, T = 25 °C	—	0.2	0.8	dB
Spurious emissions of harmonics, Conducted measurement, PAVDD connected to DC-DC output, Test Frequency = 868 MHz	$SPUR_{HARM\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1	—	-44	-30	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band, Conducted measurement, PAVDD connected to DC-DC output, Test Frequency = 868 MHz	$SPUR_{OOB\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-61.7	-55.7	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-64.2	-43.5	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-59.9	-30	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.4 Sub-GHz RF Receiver Characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 868 MHz.

Table 4.21. Sub-GHz RF Receiver Characteristics for 868 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		863	—	876	MHz
Max usable input level, 0.1% BER	SAT_{2k4}	Desired is reference 2.4 kbps GFSK signal[1]	—	—	10	dBm
Max usable input level, 0.1% BER	SAT_{38k4}	Desired is reference 38.4 kbps GFSK signal[2]	—	—	10	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER	—	-121.4	-116.5	dBm
		Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C	—	-109.2	-105.4	dBm
		Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T > 85 °C	—	—	-105.2	dBm
		Desired is reference 500 kbps GFSK signal[3], 0.1% BER	—	-95.1	—	dBm
Level above which RFSENSE will trigger[4]	$RFSENSE_{TRIG}$	CW at 868 MHz	—	-25.8	—	dBm
Level below which RFSENSE will not trigger[4]	$RFSENSE_{THRES}$	CW at 868 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing	C/I_1	Desired is 2.4 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	48.5	57.7	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	36.4	44.9	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing	C/I_2	Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	59.1	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	47.7	—	dB
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	47.5	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	47.2	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[1] at 3 dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	71.9	—	dB
		Interferer CW at Desired ± 2 MHz	—	77.9	—	dB
		Interferer CW at Desired ± 10 MHz	—	90.9	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode	$SPUR_{RX}$	30 MHz to 1 GHz	—	-77.1	-69	dBm
		1 GHz to 12 GHz	—	-59.9	-50	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 5.05 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 84.16 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 841.6 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.5 Sub-GHz RF Transmitter characteristics for 490 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 490 MHz.

Table 4.22. Sub-GHz RF Transmitter characteristics for 490 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		470	—	510	MHz
Maximum TX Power[1]	$POUT_{MAX}$	PAVDD connected directly to external 3.3V supply	18.5	21.1	23	dBm
Minimum active TX Power	$POUT_{MIN}$			-44.9	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply, peak to peak	$POUT_{VAR\_V}$	at 20 dBm;1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected directly to external supply, T = 25 °C	—	4.3	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	-40 to +85 °C at 20 dBm	—	0.2	0.9	dB
		-40 to +125 °C at 20 dBm	—	0.3	1.3	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T = 25 °C	—	0.2	0.4	dB
Harmonic emissions, 20 dBm output power setting, 490 MHz	$SPUR_{HARM\_CN}$	Per China SRW Requirement, Section 2.1, frequencies below 1GHz	—	-41.3	-34.9	dBm
		Per China SRW Requirement, Section 2.1, frequencies above 1GHz	—	-47.2	-36	dBm
Spurious emissions, 20 dBm output power setting, 490 MHz	$SPUR_{OOB\_CN}$	Per China SRW Requirement, Section 3 (48.5-72.5MHz, 76-108MHz, 167-223MHz, 470-556MHz, and 606-798MHz)	—	-57.5	—	dBm
		Per China SRW Requirement, Section 2.1 (other frequencies below 1GHz)	—	-58.5	—	dBm
		Per China SRW Requirement, Section 2.1 (frequencies above 1GHz)	—	-47.9	—	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.6 Sub-GHz RF Receiver Characteristics for 490 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 490 MHz.

Table 4.23. Sub-GHz RF Receiver Characteristics for 490 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		470	—	510	dBm
Max usable input level, 0.1% BER	SAT_{2k4}	Desired is reference 2.4 kbps GFSK signal[3]	—	—	10	dBm
Max usable input level, 0.1% BER	SAT_{38k4}	Desired is reference 38.4 kbps GFSK signal[4]	—	—	10	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal[3], 0.1% BER	—	-122.2	—	dBm
		Desired is reference 38.4 kbps GFSK signal[4], 0.1% BER, T ≤ 85 °C	—	-111.7	-108.9	dBm
		Desired is reference 38.4 kbps GFSK signal[4], 0.1% BER, T > 85 °C	—	—	-107.9	dBm
		Desired is reference 10 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C	—	-117.5	-114.8	dBm
		Desired is reference 10 kbps GFSK signal[2], 0.1% BER, T > 85 °C	—	—	-113.9	dBm
		Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C	—	-107.6	-104.7	dBm
		Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T > 85 °C	—	—	-104	dBm
Level above which RFSENSE will trigger[5]	$RFSENSE_{TRIG}$	Desired is reference 100 kbps GFSK signal[1], 0.1% BER	—	-25.8	—	dBm
Level below which RFSENSE will not trigger[5]	$RFSENSE_{THRES}$	CW at 490 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing	C/I_1	Desired is 2.4 kbps GFSK signal[3] at 3dB above sensitivity level, 0.1% BER	48	58.4	—	dB
		Desired is 38.4kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	38.3	47.5	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing	C/I_2	Desired is 2.4kbps GFSK signal[3] at 3dB above sensitivity level, 0.1% BER	—	60.8	—	dB
		Desired is 38.4kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	51.7	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 2.4kbps GFSK signal[3] at 3dB above sensitivity level, 0.1% BER	—	60.9	—	dB
		Desired is 38.4kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	53	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[3] at 3 dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	71.9	—	dB
		Interferer CW at Desired ± 2 MHz	—	74.1	—	dB
		Interferer CW at Desired ± 10 MHz	—	87.9	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode	$SPUR_{RX}$	30 MHz to 1 GHz	—	-84.7	-54	dBm
		1 GHz to 12 GHz	—	-66.8	-54	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 210.4 kHz.
2. Definition of reference signal is 10 kbps 2GFSK, BT=0.5, Δf = 5 kHz, RX channel BW = 21.04 kHz.
3. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 5.05 kHz, channel spacing = 12.5 kHz.
4. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 84.16 kHz, channel spacing = 100 kHz.
5. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.7 Sub-GHz RF Transmitter characteristics for 433 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 433 MHz.

Table 4.24. Sub-GHz RF Transmitter characteristics for 433 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		426	—	445	MHz
Maximum TX Power[1]	$POUT_{MAX}$	PAVDD connected to DCDC output, 14dBm output power	11	14.3	18	dBm
		PAVDD connected to DCDC output, 10dBm output power	7	10.7	14	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-42	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply, peak to peak, Pout = 10dBm	$POUT_{VAR\_V}$	At 10 dBm;1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD = DC-DC output, T = 25 °C	—	1.7	—	dB
Output power variation vs temperature, peak to peak, Pout= 10dBm	$POUT_{VAR\_T}$	-40 to +85C at 10dBm	—	0.5	1.2	dB
		-40 to +125C at 10dBm	—	0.7	1.7	dB
Output power variation vs RF frequency, Pout = 10dBm	$POUT_{VAR\_F}$	T = 25 °C	—	0.2	0.6	dB
Spurious emissions of harmonics FCC, Conducted measurement, 14dBm match, PAVDD connected to DCDC output, Test Frequency = 434 MHz	$SPUR_{HARM\_FCC}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-61.2	-47	dBm
		In non-restricted bands, per FCC Part 15.231	—	-68.5	-26	dBc
Spurious emissions out-of-band FCC, Conducted measurement, 14dBm match, PAVDD connected to DCDC output, Test Frequency = 434 MHz	$SPUR_{OOB\_FCC}$	In non-restricted bands, per FCC Part 15.231	—	-86.2	-26	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-71.9	-52	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-70.2	-62	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-60.5	-54.5	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-57.7	-46	dBm
Spurious emissions of harmonics ETSI, Conducted measurement, 14dBm match, PAVDD connected to DCDC output, Test Frequency = 434 MHz	$SPUR_{HARM\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (frequencies below 1Ghz)	—	-57.3	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1Ghz)	—	-84.5	-36	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band ETSI, Conducted measurement, 14dBm match, PAVDD connected to DCDC output, Test Frequency = 434 MHz	$SPUR_{OOB\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-65.1	-60	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-63.9	-42	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-56.8	-36	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.8 Sub-GHz RF Receiver Characteristics for 433 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 433 MHz.

Table 4.25. Sub-GHz RF Receiver Characteristics for 433 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		426	—	445	MHz
Max usable input level, 0.1% BER	SAT_{2k4}	Desired is reference 2.4 kbps GFSK signal[2]	—	—	10	dBm
Max usable input level, 0.1% BER	SAT_{50k}	Desired is reference 50 kbps GFSK signal[4]	—	—	10	dBm
Sensitivity	SENS	Desired is reference 4.8 kbps OOK signal[3], 20% PER	—	-107	—	dBm
		Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C	—	-107.5	-105	dBm
		Desired is reference 100 kbps GFSK signal[1], 0.1% BER, T > 85 °C	—	—	-104	dBm
		Desired is reference 50 kbps GFSK signal[4], 0.1% BER, T ≤ 85 °C	—	-110	-107.2	dBm
		Desired is reference 50 kbps GFSK signal[4], 0.1% BER, T > 85 °C	—	—	-106.6	dBm
		Desired is reference 2.4 kbps GFSK signal[2], 0.1% BER	—	-122.3	—	dBm
		Desired is reference 9.6 kbps GFSK signal[5], 1% PER, T ≤ 85 °C	—	-109.4	-106.2	dBm
		Desired is reference 9.6 kbps GFSK signal[5], 1% PER, T > 85 °C	—	—	-105.7	dBm
Level above which RFSENSE will trigger[6]	$RFSENSE_{TRIG}$	CW at 433 MHz	—	-25.8	—	dBm
Level below which RFSENSE will not trigger[6]	$RFSENSE_{THRES}$	CW at 433 MHz	—	-50	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing	C/I_1	Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER	—	46	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	24.8	33.4	—	dB
		Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	47	59.1	—	dB
		Desired is 50 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	45.6	50.7	—	dB
		Desired is 9.6 kbps 4GFSK signal[5] at 3dB above sensitivity level, 1% PER	—	31.2	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing	C/I_2	Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER	—	56.8	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	56.2	—	dB
		Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	62.2	—	dB
		Desired is 50 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	57.4	—	dB
		Desired is 9.6 kbps 4GFSK signal[5] at 3dB above sensitivity level, 1% PER	—	47.8	—	dB
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 4.8 kbps OOK signal[3] at 3dB above sensitivity level, 20% PER	—	42.2	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	50	—	dB
		Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	52.3	—	dB
		Desired is 50 kbps GFSK signal[4] at 3dB above sensitivity level, 0.1% BER	—	53	—	dB
		Desired is 9.6 kbps 4GFSK signal[5] at 3dB above sensitivity level, 1% PER	—	45	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	73.8	—	dB
		Interferer CW at Desired ± 2 MHz	—	75.7	—	dB
		Interferer CW at Desired ± 10 MHz	—	89.9	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermod selectivity, 0.1% BER. CW interferers at 12.5 kHz and 25 kHz offsets	C/I_{IM}	Desired is 2.4 kbps GFSK signal[2] at 3dB above sensitivity level	—	59.1	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216-960 MHz	—	-83.5	-57	dBm
		Above 960 MHz	—	-62.5	-52	dBm
Max spurious emissions during active receive mode, per ETSI 300-220 Section 8.6	$SPUR_{RX\_ETSI}$	Below 1000 MHz	—	-84.6	-57	dBm
		Above 1000 MHz	—	-59.7	-52	dBm
Max spurious emissions during active receive mode, per ARIB STD T67 Section 3.3(5)	$SPUR_{RX\_ARIB}$	Below 710 MHz, RBW=100kHz	—	-83.6	-57	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 210.4 kHz, channel spacing = 200 kHz.
2. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 5.05 kHz, channel spacing = 12.5 kHz.
3. Definition of reference signal is 4.8 kbps OOK, RX channel BW = 315.6 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, Δf = 25 kHz, RX channel BW = 120.229 kHz, channel spacing = 200 kHz.
5. Definition of reference signal is 9.6 kbps 4GFSK, BT=0.5, inner deviation = 0.8 kHz, RX channel BW = 9.989 kHz, channel spacing = 12.5 kHz.
6. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.9 Sub-GHz RF Transmitter characteristics for 315 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 315 MHz.

Table 4.26. Sub-GHz RF Transmitter characteristics for 315 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		195	—	358	MHz
Maximum TX Power[1]	$POUT_{MAX}$	PAVDD connected to DC-DC output, T ≤ 85 °C	10.8	15.3	17	dBm
		PAVDD connected to DC-DC output, T > 85 °C	10.5	—	—	dBm
Minimum active TX Power	$POUT_{MIN}$			-43.9	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD = DC-DC output, T = 25 °C	—	1.8	—	dB
Output power variation vs temperature	$POUT_{VAR\_T}$	-40 to +85C	—	0.5	1.2	dB
		-40 to +125C	—	0.7	1.5	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T = 25 °C	—	0.1	0.7	dB
Spurious emissions of harmonics at 14 dBm output power, Conducted measurement, 14dBm match, PAVDD connected to DC-DC output, Test Frequency = 303 MHz	$SPUR_{HARM\_FCC}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-53.8	-47	dBm
		In non-restricted bands, per FCC Part 15.231	—	-63.4	-26	dBc
Spurious emissions out-of-band at 14 dBm output power, Conducted measurement, 14dBm match, PAVDD connected to DC-DC output, Test Frequency = 303 MHz	$SPUR_{OOB\_FCC}$	In non-restricted bands, per FCC Part 15.231	—	-76.6	-26	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-71.8	-51	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-70.2	-61	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-68.2	-57	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-57.5	-46	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.10 Sub-GHz RF Receiver Characteristics for 315 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 315 MHz.

Table 4.27. Sub-GHz RF Receiver Characteristics for 315 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		195	—	358	dBm
Max usable input level, 0.1% BER	SAT_{2k4}	Desired is reference 2.4 kbps GFSK signal[1]	—	—	10	dBm
Max usable input level, 0.1% BER	SAT_{38k4}	Desired is reference 38.4 kbps GFSK signal[2]	—	—	10	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER, T ≤ 85 °C	—	-123.5	-120.7	dBm
		Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER, T > 85 °C	—	—	-120	dBm
		Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C	—	-111.4	-108.6	dBm
		Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T > 85 °C	—	—	-107.9	dBm
		Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T ≤ 85 °C	—	-97.2	-94.6	dBm
		Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T > 85 °C	—	—	-93.9	dBm
Level above which RFSENSE will trigger[4]	$RFSENSE_{TRIG}$	CW at 315 MHz	—	-25.8	—	dBm
Level below which RFSENSE will not trigger[4]	$RFSENSE_{THRES}$	CW at 315 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing	C/I_1	Desired is 2.4 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	54.1	64.2	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	46	50	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing	C/I_2	Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	66	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level[2], 0.1% BER	—	54	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	54.4	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	51.9	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[1] at 3 dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	74.9	—	dB
		Interferer CW at Desired ± 2 MHz	—	76.7	—	dB
		Interferer CW at Desired ± 10 MHz	72.6	93.1	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216-960 MHz	—	-87.4	-55	dBm
		Above 960MHz	—	-76.7	-47	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 5.05 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 84.16 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 841.6 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.11 Sub-GHz RF Transmitter Characteristics for 169 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 169 MHz.

Table 4.28. Sub-GHz RF Transmitter Characteristics for 169 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		169	—	170	MHz
Maximum TX Power[1]	$POUT_{MAX}$	PAVDD connected to external 3.3 V supply	18.4	20.4	23.3	dBm
Minimum active TX Power	$POUT_{MIN}$			-42.6	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply, peak to peak	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, PAVDD connected to external supply, T = 25 °C	—	4.8	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	-40 to +85 °C at 20 dBm	—	0.6	1.2	dB
		-40 to +125 °C at 20 dBm	—	0.8	1.5	dB
Spurious emissions of harmonics, Conducted measurement, PAVDD = 3.3V, Test Frequency = 169 MHz	$SPUR_{HARM\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-49.3	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-58.2	-53	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-38.9	25.4	dBm
Spurious emissions out-of-band, Conducted measurement, PAVDD = 3.3V, Test Frequency = 169 MHz	$SPUR_{OOB\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-61.8	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-62	-54	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-47.6	-41.1	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.12 Sub-GHz RF Receiver Characteristics for 169 MHz Band

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 169 MHz.

Table 4.29. Sub-GHz RF Receiver Characteristics for 169 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		169	—	170	dBm
Max usable input level, 0.1% BER	SAT_{2k4}	Desired is reference 2.4 kbps GFSK signal[1]	—	—	10	dBm
Max usable input level, 0.1% BER	SAT_{38k4}	Desired is reference 38.4 kbps GFSK signal[2]	—	—	10	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal[1], 0.1% BER	—	-124	—	dBm
		Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T ≤ 85 °C	—	-111.9	-108	dBm
		Desired is reference 38.4 kbps GFSK signal[2], 0.1% BER, T > 85 °C	—	—	-108.5	dBm
		Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T ≤ 85 °C	—	-97.7	-94.6	dBm
		Desired is reference 500 kbps GFSK signal[3], 0.1% BER, T > 85 °C	—	—	-94	dBm
Level above which RFSENSE will trigger[4]	$RFSENSE_{TRIG}$	CW at 169 MHz	—	-25.8	—	dBm
Level below which RFSENSE will not trigger[4]	$RFSENSE_{THRES}$	CW at 169 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at ± 1 x channel-spacing	C/I_1	Desired is 2.4 kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	65	—	dB
		Desired is 38.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	43.3	50.4	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 x channel-spacing	C/I_2	Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	67.9	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	55.5	—	dB
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 2.4kbps GFSK signal[1] at 3dB above sensitivity level, 0.1% BER	—	54.6	—	dB
		Desired is 38.4kbps GFSK signal[2] at 3dB above sensitivity level, 0.1% BER	—	51	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal[1] at 3 dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	74.2	—	dB
		Interferer CW at Desired ± 2 MHz	68.7	76	—	dB
		Interferer CW at Desired ± 10 MHz	80	90.6	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-98	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dBm
Max spurious emissions during active receive mode	$SPUR_{RX}$	30 MHz to 1 GHz	—	-83.7	-63	dBm
		1 GHz to 12 GHz	—	-58.8	-50	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 5.05 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 84.16 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 841.6 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.11 Modem

Table 4.30. Modem

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive bandwidth	BW_{RX}	Configurable range with 38.4 MHz crystal	0.1	—	2530	kHz
IF frequency	f_{IF}	Configurable range with 38.4 MHz crystal. Selected steps available.	150	—	1371	kHz
DSSS symbol length	SL_{DSSS}	Configurable in steps of 1 chip	2	—	32	chips
DSSS bits per symbol	BPS_{DSSS}	Configurable	1	—	4	bits/symbol

4.1.12 Oscillators

4.1.12.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.31. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.12.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.32. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	38.4 MHz required for radio trans-ciever operation	38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	9	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	—	300	—	µs
Frequency tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	-40	—	40	ppm

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.12.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.33. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[2] = 1	30.474	32.768	34.243	kHz
		ENVREF[2] = 1, T > 85 °C	30.474	—	39.7	kHz
		ENVREF[2] = 0	30.474	32.768	33.915	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

4.1.12.4 High-Frequency RC Oscillator (HFRCO)

Table 4.34. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 38 MHz	—	204	228	µA
		f_{HFRCO} = 32 MHz	—	171	190	µA
		f_{HFRCO} = 26 MHz	—	147	164	µA
		f_{HFRCO} = 19 MHz	—	126	138	µA
		f_{HFRCO} = 16 MHz	—	110	120	µA
		f_{HFRCO} = 13 MHz	—	100	110	µA
		f_{HFRCO} = 7 MHz	—	81	91	µA
		f_{HFRCO} = 4 MHz	—	33	35	µA
		f_{HFRCO} = 2 MHz	—	31	35	µA
		f_{HFRCO} = 1 MHz	—	30	35	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.12.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.35. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{AUXHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	$t_{AUXHFRCO}$	$f_{AUXHFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{AUXHFRCO} < 19$ MHz	—	1	—	µs
		$f_{AUXHFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	$I_{AUXHFRCO}$	$f_{AUXHFRCO}$ = 38 MHz	—	204	—	µA
		$f_{AUXHFRCO}$ = 32 MHz	—	171	—	µA
		$f_{AUXHFRCO}$ = 26 MHz	—	147	—	µA
		$f_{AUXHFRCO}$ = 19 MHz	—	126	—	µA
		$f_{AUXHFRCO}$ = 16 MHz	—	110	—	µA
		$f_{AUXHFRCO}$ = 13 MHz	—	100	—	µA
		$f_{AUXHFRCO}$ = 7 MHz	—	81	—	µA
		$f_{AUXHFRCO}$ = 4 MHz	—	33	—	µA
		$f_{AUXHFRCO}$ = 2 MHz	—	31	—	µA
		$f_{AUXHFRCO}$ = 1 MHz	—	30	—	µA
Coarse trim step size (% of period)	$SS_{AUXHFRCO\_COARSE}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{AUXHFRCO\_FINE}$		—	0.1	—	%
Period jitter	$PJ_{AUXHFRCO}$		—	0.2	—	% RMS

4.1.12.6 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.36. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.13 Flash Memory Characteristics[5]

Table 4.37. Flash Memory Characteristics[5]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}	Burst write, 128 words, average time per word	20	26	40	µs
		Single word	57	68	82	µs
Page erase time[4]	t_{PERASE}		20	27	40	ms
Mass erase time[1]	t_{MERASE}		20	27	40	ms
Device erase time[2 3]	t_{DERASE}	T ≤ 85 °C	—	60	74	ms
		T ≤ 125 °C	—	60	78	ms
Erase current[6]	I_{ERASE}	Page Erase	—	—	3	mA
		Mass or Device Erase	—	—	5	mA
Write current[6]	I_{WRITE}		—	—	3	mA

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.14 General-Purpose I/O (GPIO)

Table 4.38. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	30	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	50	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—	—	110	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	—	250	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		30	43	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		20	25	35	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:

1. In GPIO_Pn_CTRL register.

4.1.15 Voltage Monitor (VMON)

Table 4.39. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply moni-tored	—	5.8	8.26	μA
		In EM0 or EM1, 4 supplies moni-tored	—	11.8	16.8	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.16 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.40. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[5]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	301	350	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	149	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	91	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	51	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	9	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	117	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	79	—	μA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	345	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	191	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	132	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	102	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	17	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	162	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	123	—	μA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[1]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[4] = NORMAL	—	—	5	μs
		WARMUPMODE[4] = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE[4] = KEEPINSLO-WACC	—	—	1	μs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference[7], differential measurement	58	67	—	dB
		External reference[6], differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Offset error	$V_{ADCOFFSETERR}$		-3	0.25	3	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	3.5	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.
5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.
7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

4.1.17 Analog Comparator (ACMP)

Table 4.41. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL [1]	0	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG[4] ≤ 0x10 or FULLBIAS[4] = 0	1.85	—	$V_{VREGVDD\_MAX}$	V
		0x10 < BIASPROG[4] ≤ 0x20 and FULLBIAS[4] = 1	2.1	—	$V_{VREGVDD\_MAX}$	V
Active current not including voltage reference[2]	I_{ACMP}	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	50	—	nA
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	306	—	nA
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	74	95	µA
Current consumption of internal voltage reference[2]	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	-1.75	0	1.75	mV
		HYSTSEL[5] = HYST1	10	18	26	mV
		HYSTSEL[5] = HYST2	21	32	46	mV
		HYSTSEL[5] = HYST3	27	44	63	mV
		HYSTSEL[5] = HYST4	32	55	80	mV
		HYSTSEL[5] = HYST5	38	65	100	mV
		HYSTSEL[5] = HYST6	43	77	121	mV
		HYSTSEL[5] = HYST7	47	86	148	mV
		HYSTSEL[5] = HYST8	-4	0	4	mV
		HYSTSEL[5] = HYST9	-27	-18	-10	mV
		HYSTSEL[5] = HYST10	-47	-32	-18	mV
		HYSTSEL[5] = HYST11	-64	-43	-27	mV
		HYSTSEL[5] = HYST12	-78	-54	-32	mV
		HYSTSEL[5] = HYST13	-93	-64	-37	mV
		HYSTSEL[5] = HYST14	-113	-74	-42	mV
		HYSTSEL[5] = HYST15	-135	-85	-47	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	-35	—	35	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	2	2.5	2.8	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	102	—	kΩ
		CSRESSEL[6] = 6	—	164	—	kΩ
		CSRESSEL[6] = 7	—	239	—	kΩ

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

4.1.18 Current Digital to Analog Converter (IDAC)

Table 4.42. Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N_{IDAC_RANGES}		—	4	—	ranges
Output current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	steps
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-2	—	2	%
		EM0 or EM1, Across operating temperature range	-18	—	22	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANG-SEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	8.9	13	µA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	12	16	µA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	1.04	—	µA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	1.08	—	µA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	8.9	—	µA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.04	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.02	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.02	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.02	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.18	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.08	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.02	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.19 Pulse Counter (PCNT)

Table 4.43. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quad-rature Modes	—	—	10	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.20 I2C

4.1.20.1 I2C Standard-mode (Sm)[1]

Table 4.44. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	µs
STOP condition set-up time	t_{SU_STO}		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.20.2 I2C Fast-mode (Fm)[1]

Table 4.45. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:
1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.20.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.46. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.21 USART SPI

SPI Master Timing

Table 4.47. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 3 2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1 3]	t_{CS_MO}		-9	—	10	ns
SCLK to MOSI [1 3]	t_{SCLK_MO}		-6	—	6.5	ns
MISO setup time [1 3]	t_{SU_MI}	IOVDD = 1.62 V	60	—	—	ns
		IOVDD = 3.0 V	40	—	—	ns
MISO hold time [1 3]	t_{H_MI}		-13	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

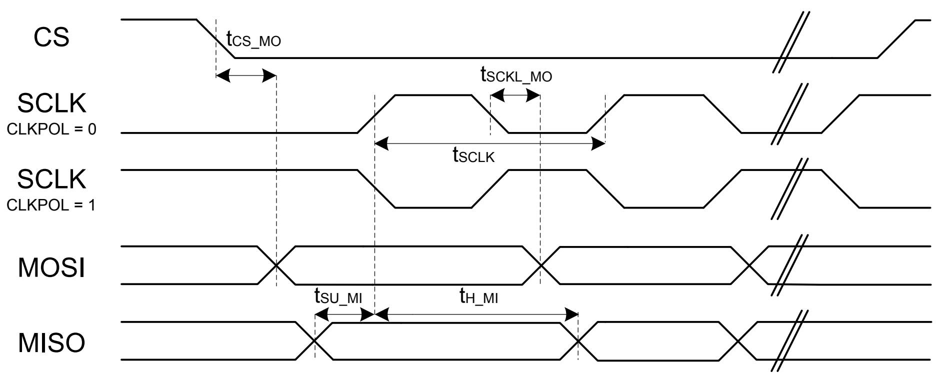


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.48. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 3 2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time[1 3 2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time[1 3 2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1 3]	$t_{CS\_ACT\_MI}$		4	—	70	ns
CS disable to MISO [1 3]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1 3]	t_{SU_MO}		8	—	—	ns
MOSI hold time [1 3 2]	t_{H_MO}		7	—	—	ns
SCLK to MISO [1 3 2]	t_{SCLK_MI}		10 + 1.5 * $t_{HFPERCLK}$	—	65 + 2.5 * $t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

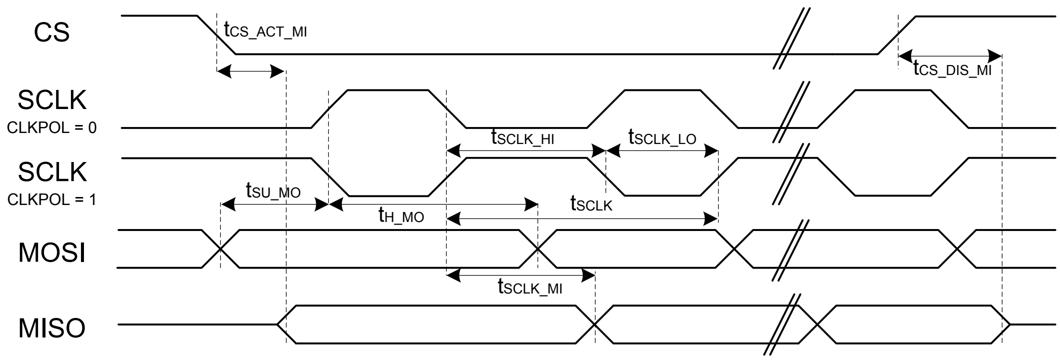


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

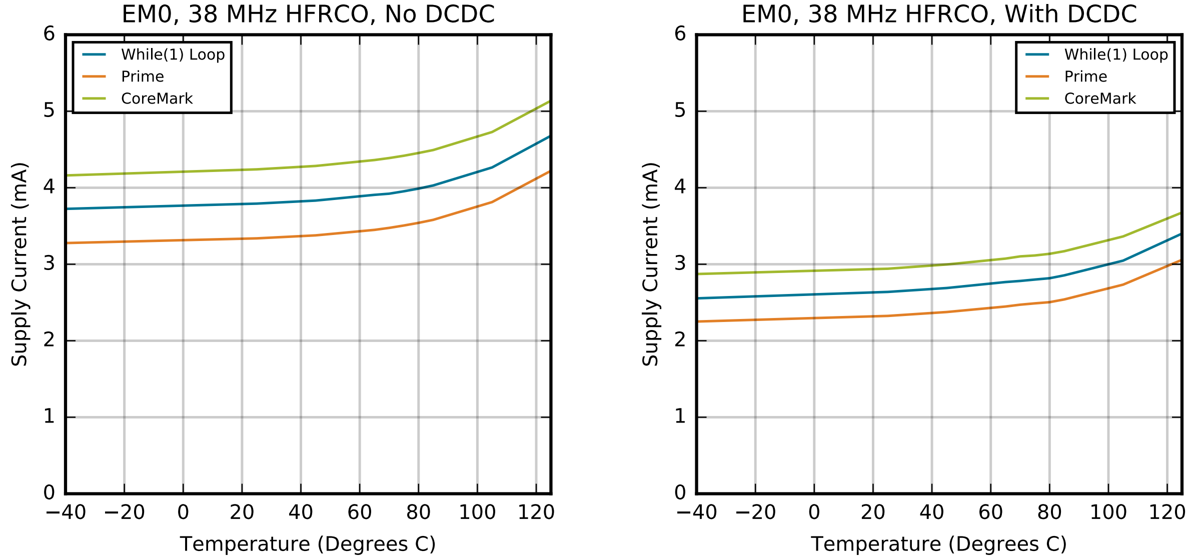


Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

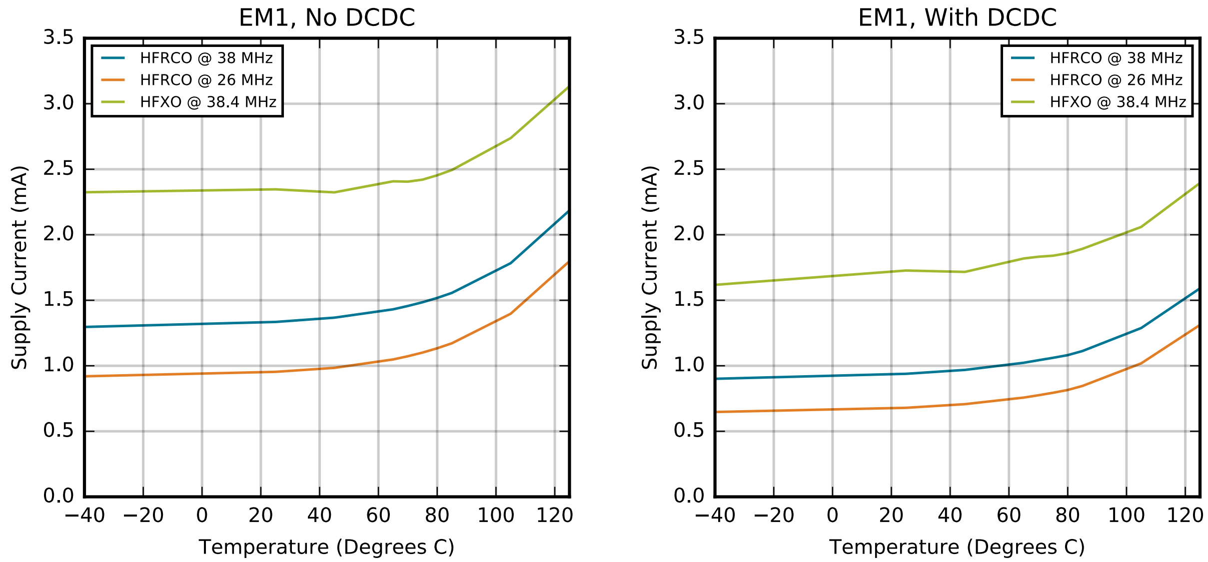


Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

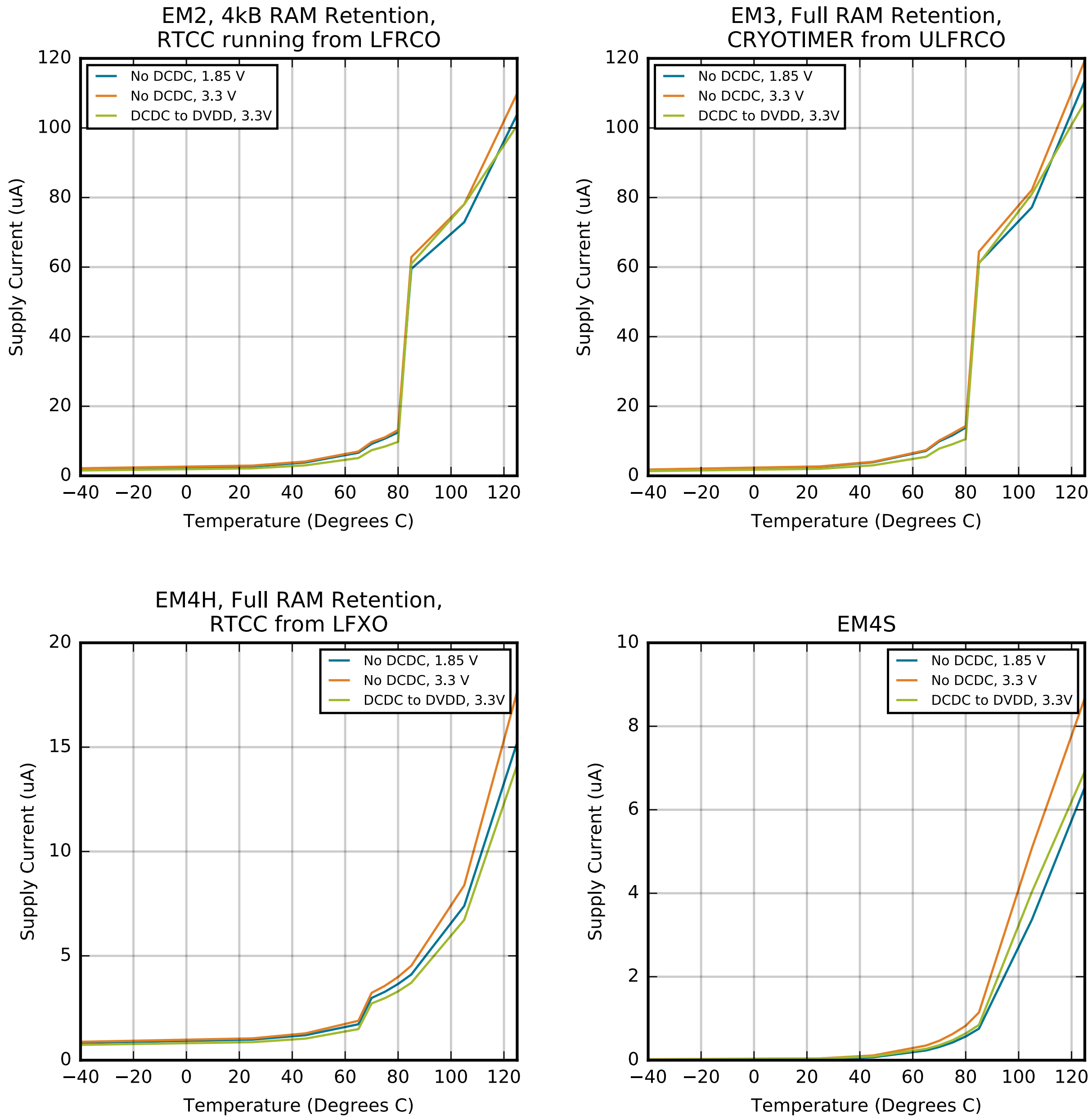


Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 1.0 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

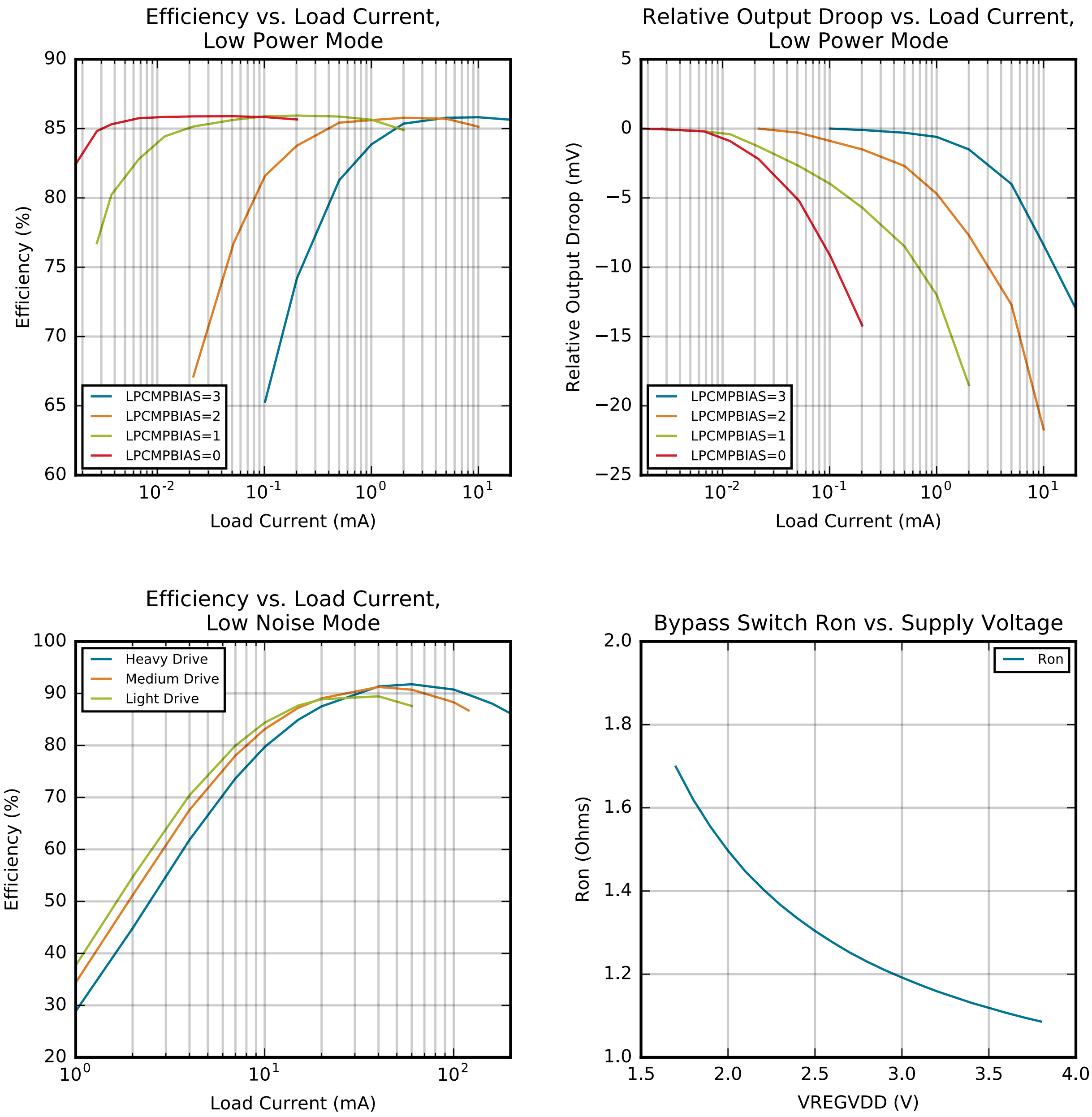


Figure 4.6. DC-DC Converter Typical Performance Characteristics

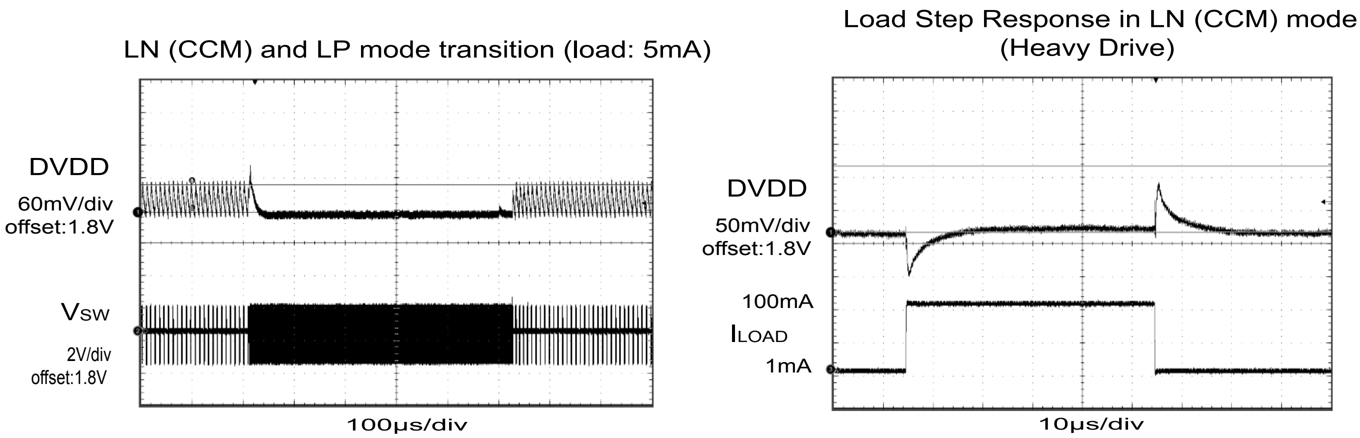


Figure 4.7. DC-DC Converter Transition Waveforms

4.2.3 Internal Oscillators

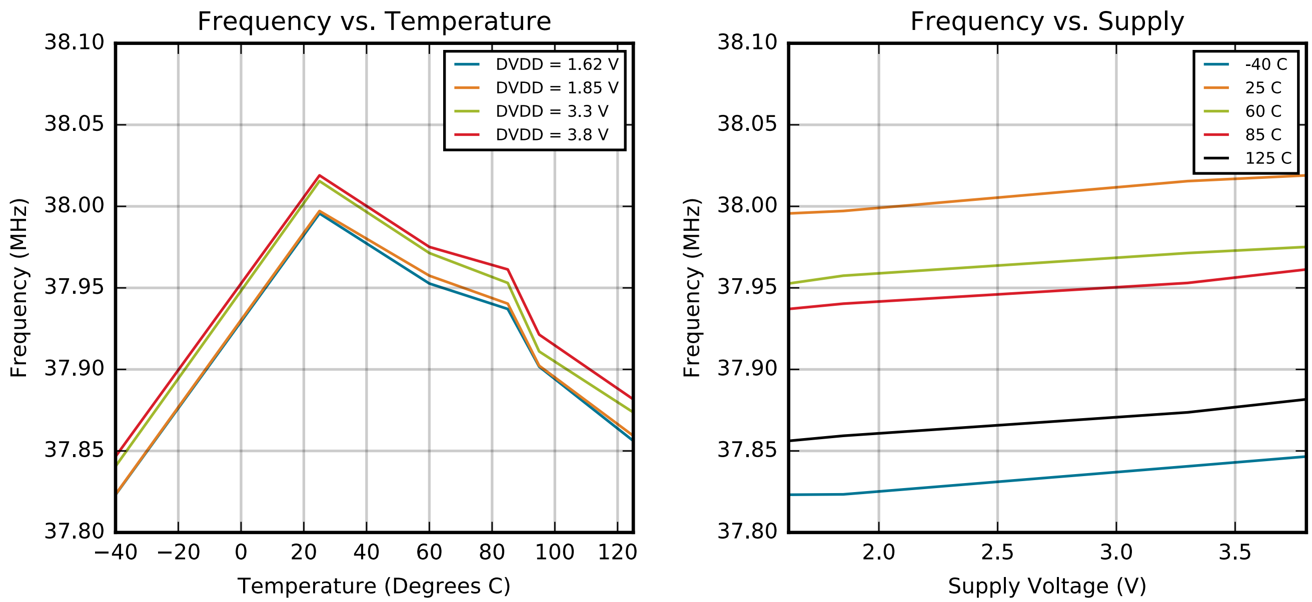


Figure 4.8. HFRCO and AUXHFRCO Typical Performance at 38 MHz

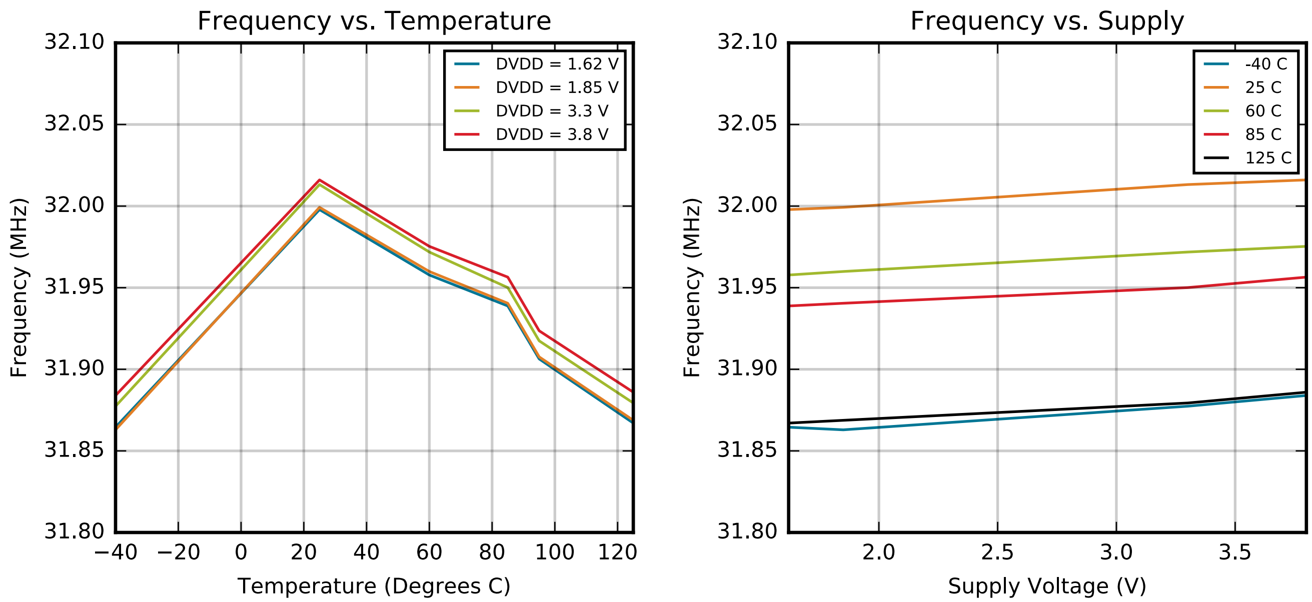


Figure 4.9. HFRCO and AUXHFRCO Typical Performance at 32 MHz

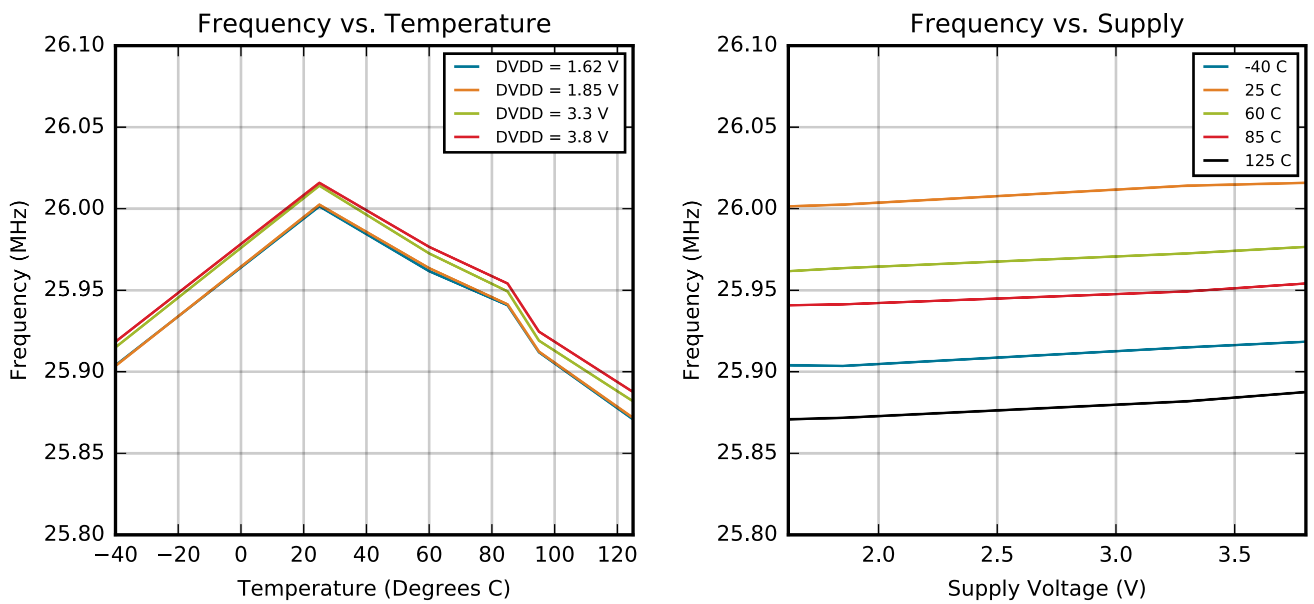


Figure 4.10. HFRCO and AUXHFRCO Typical Performance at 26 MHz

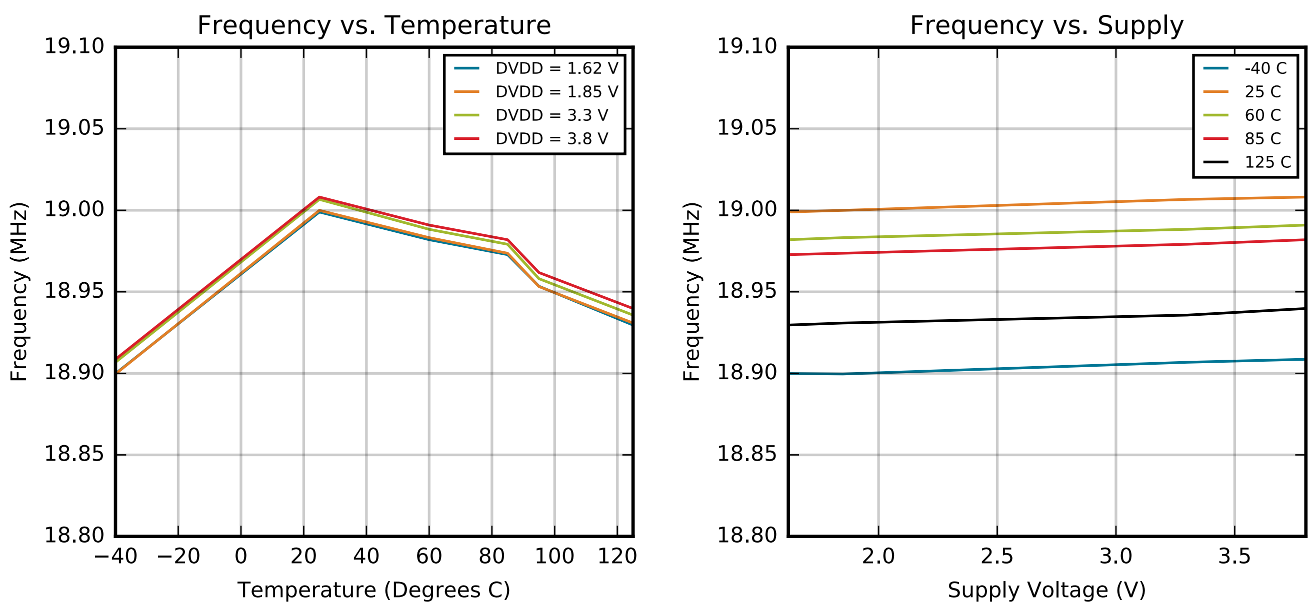


Figure 4.11. HFRCO and AUXHFRCO Typical Performance at 19 MHz

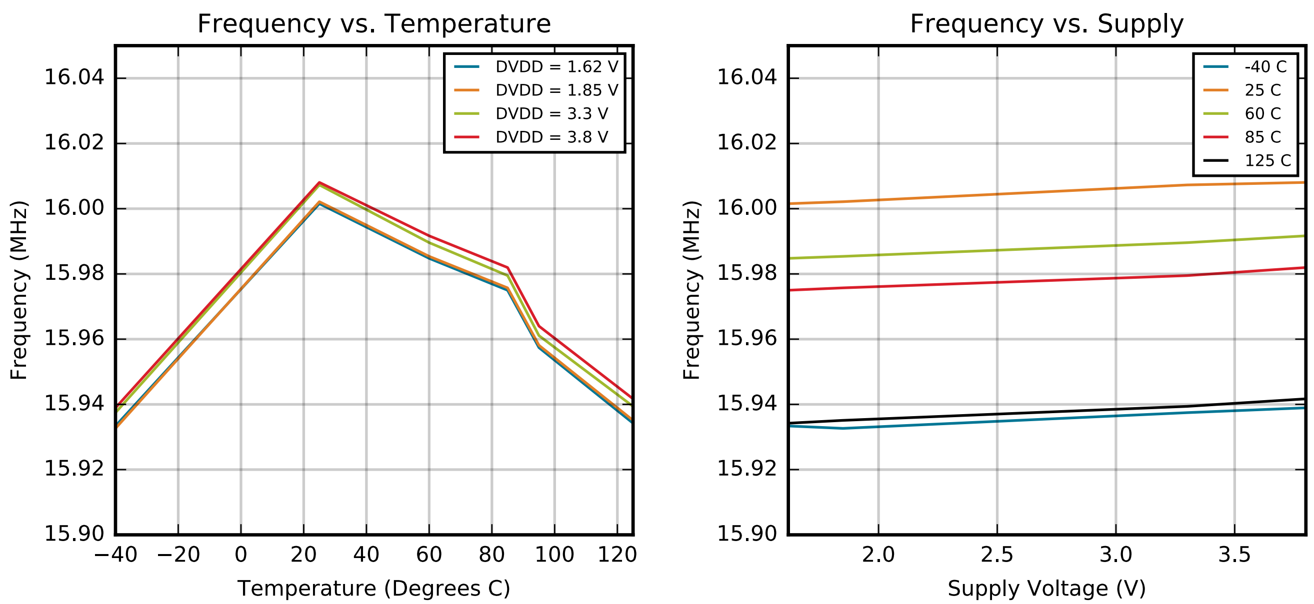


Figure 4.12. HFRCO and AUXHFRCO Typical Performance at 16 MHz

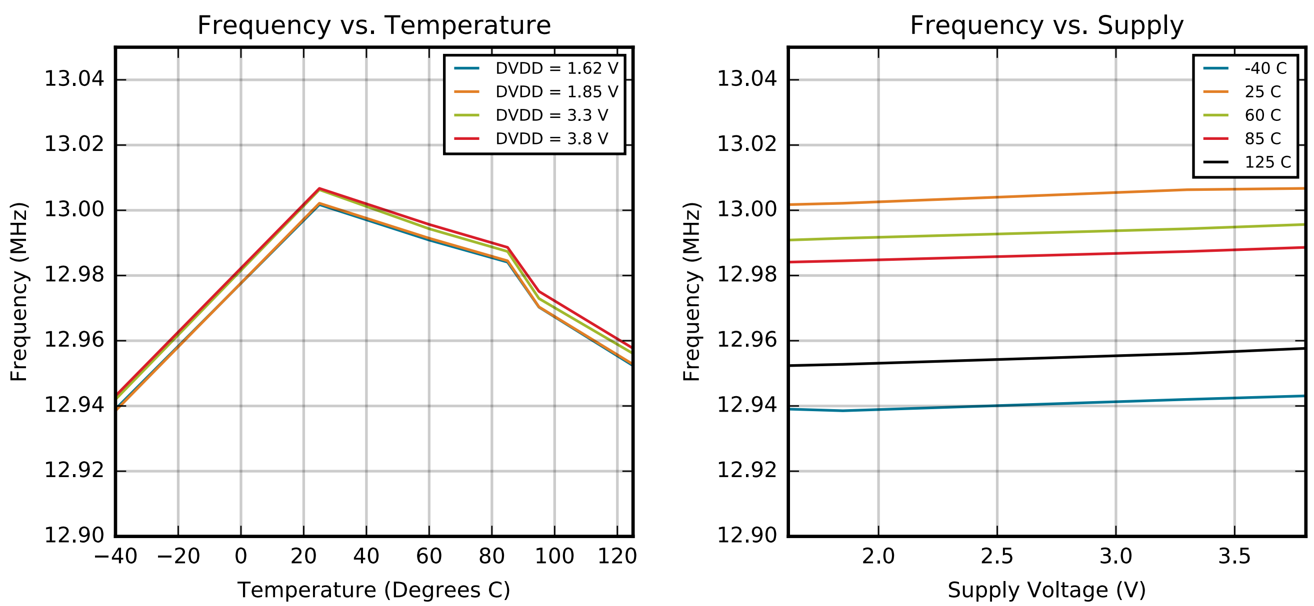


Figure 4.13. HFRCO and AUXHFRCO Typical Performance at 13 MHz

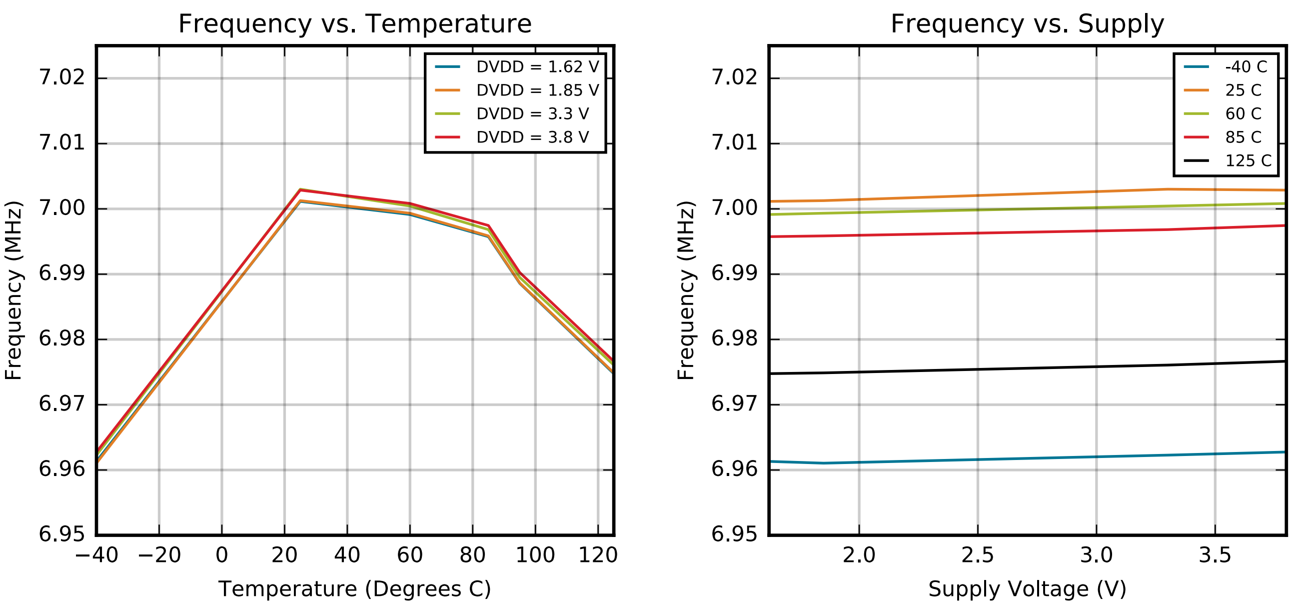


Figure 4.14. HFRCO and AUXHFRCO Typical Performance at 7 MHz

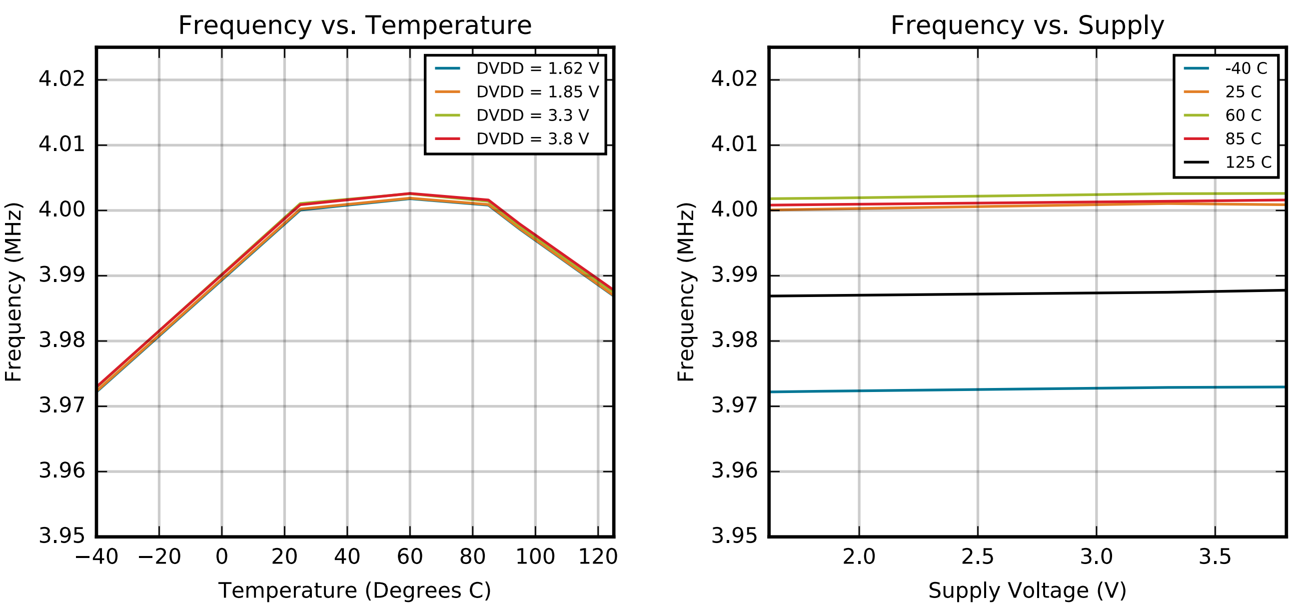


Figure 4.15. HFRCO and AUXHFRCO Typical Performance at 4 MHz

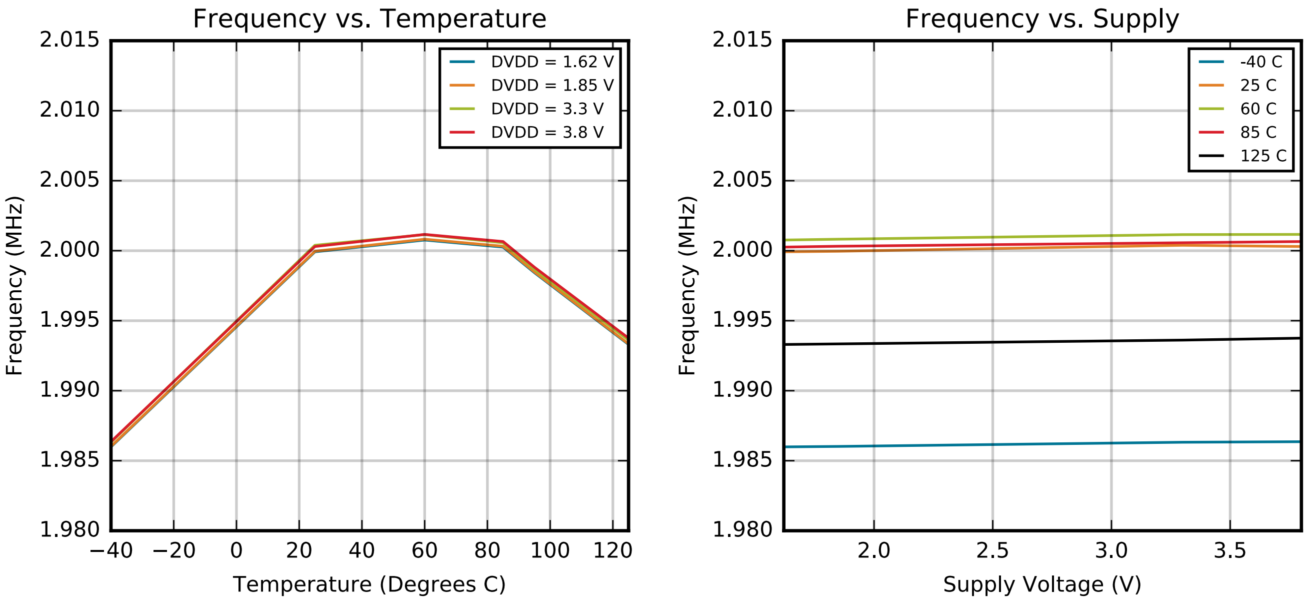


Figure 4.16. HFRCO and AUXHFRCO Typical Performance at 2 MHz

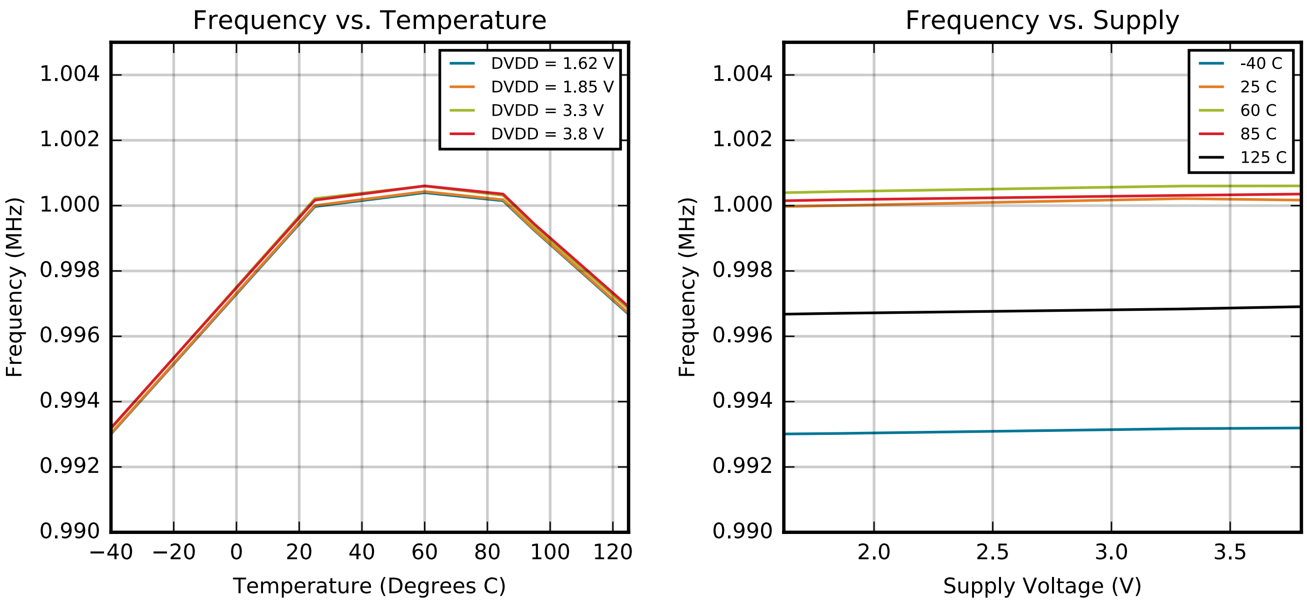


Figure 4.17. HFRCO and AUXHFRCO Typical Performance at 1 MHz

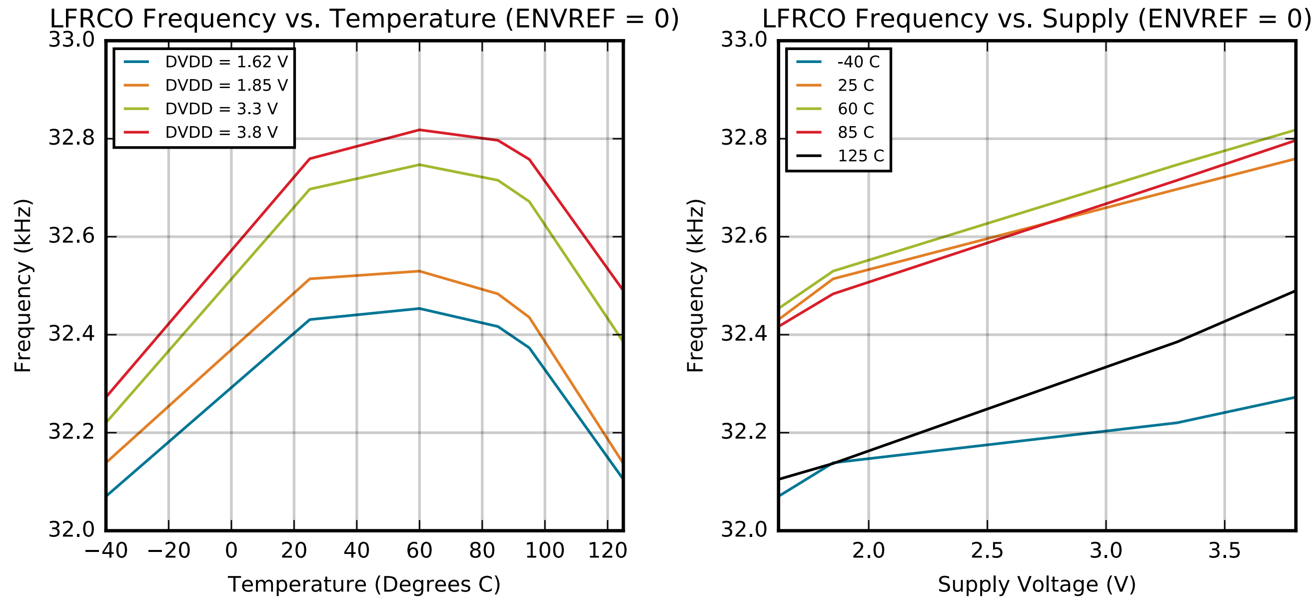


Figure 4.18. LFRCO Typical Performance at 32.768 kHz

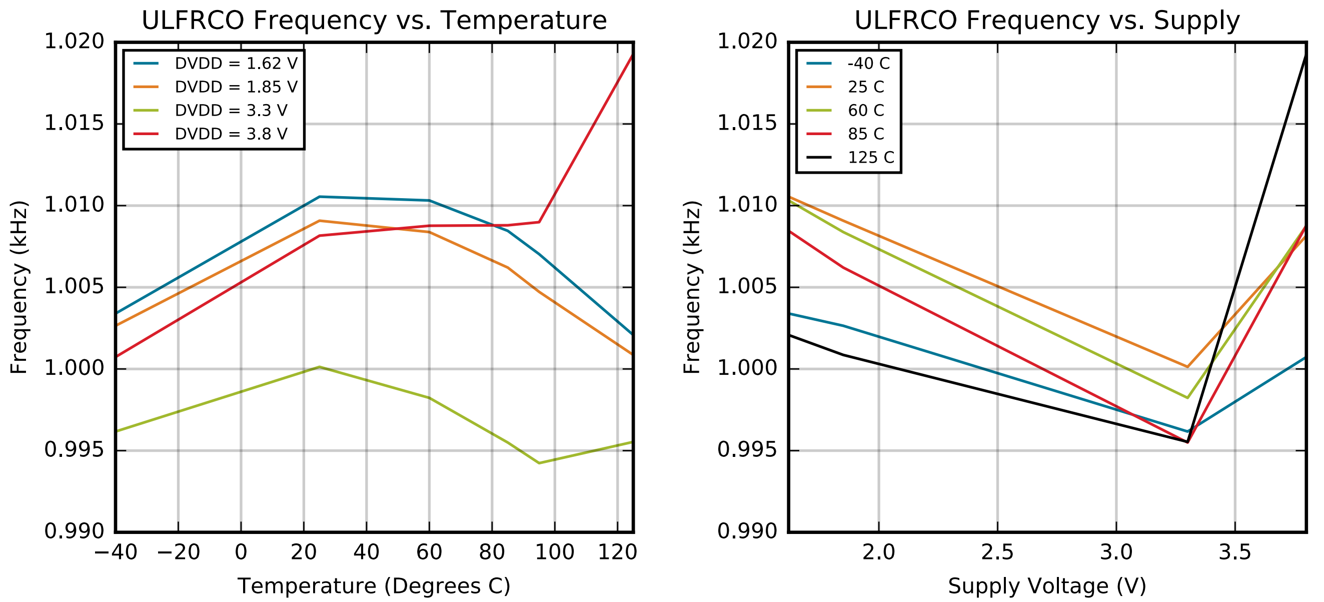


Figure 4.19. ULFRCO Typical Performance at 1 kHz

4.2.4 2.4 GHz Radio

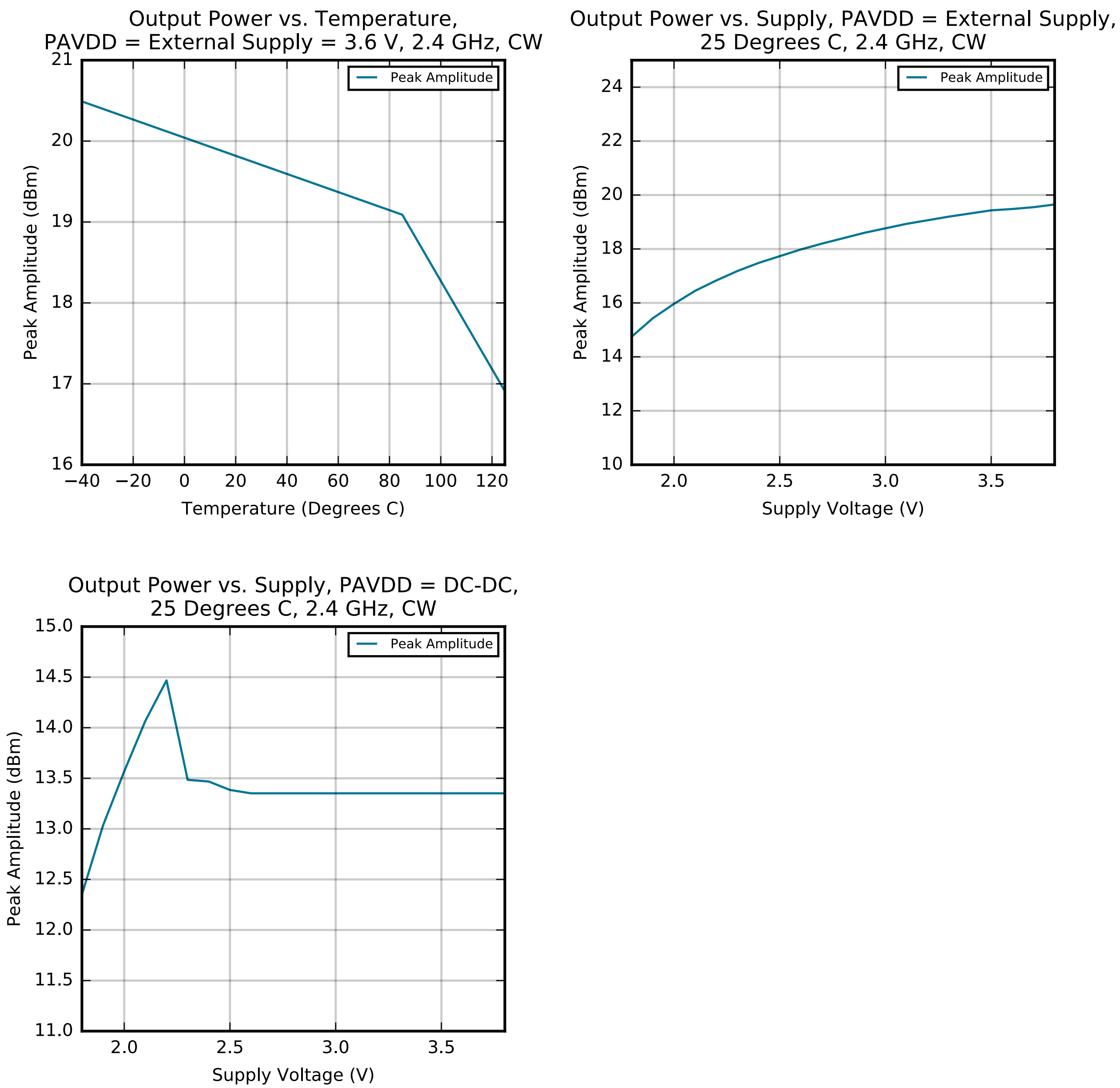


Figure 4.20. 2.4 GHz RF Transmitter Output Power

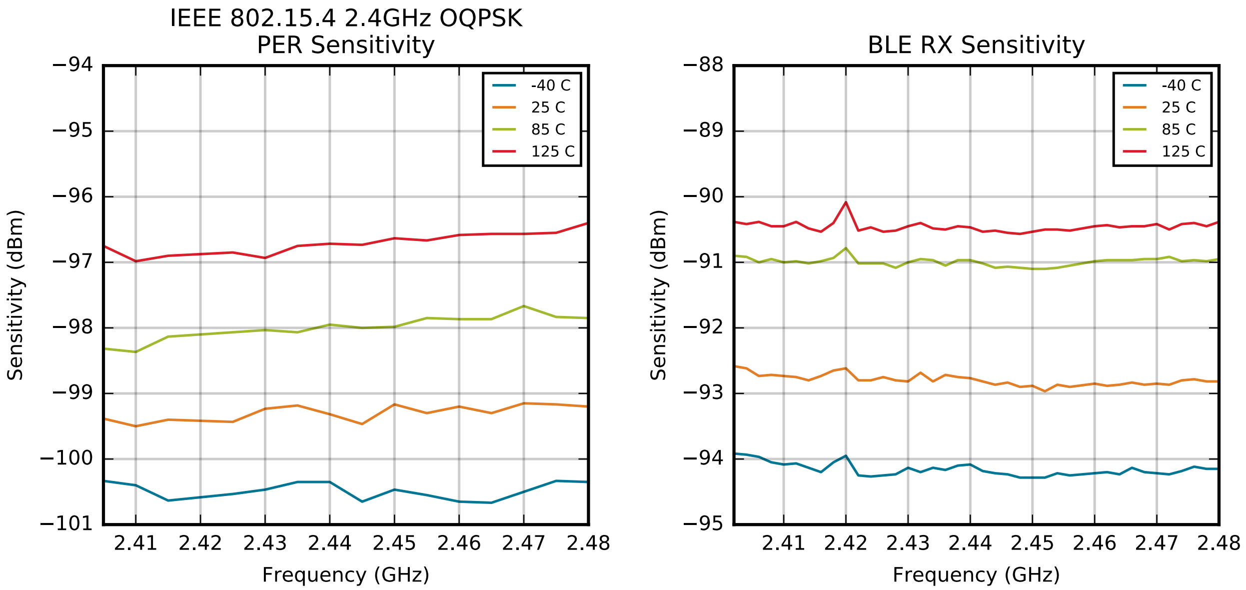


Figure 4.21. 2.4 GHz RF Receiver Sensitivity

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in the following figure.

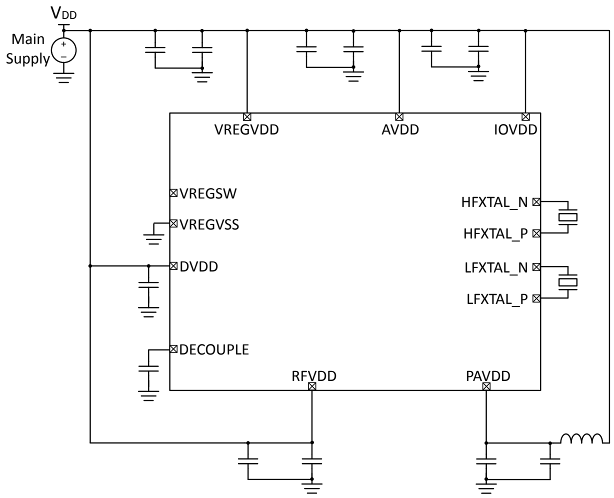


Figure 5.1. EFR32FG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter

Typical power supply circuits using the internal DC-DC converter are shown below. The MCU operates from the DC-DC converter supply. For low RF transmit power applications less than 13dBm, the RF PA may be supplied by the DC-DC converter. For OPNs supporting high power RF transmission, the RF PA must be directly supplied by VDD for RF transmit power greater than 13 dBm.

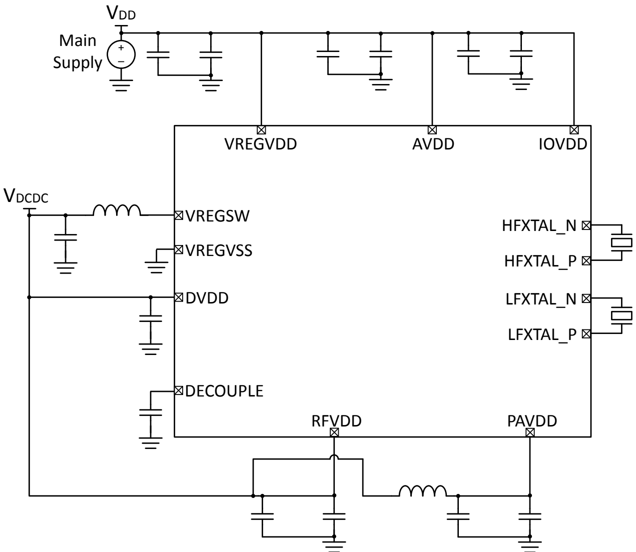


Figure 5.2. EFR32FG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC)

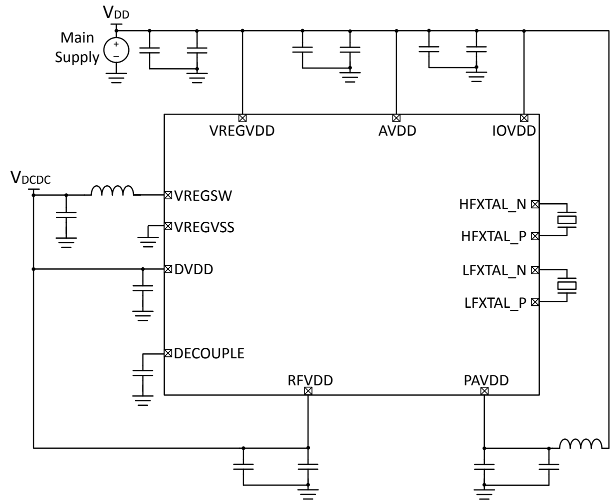


Figure 5.3. EFR32FG1 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDD)

5.2 RF Matching Networks

Typical RF matching network circuit diagrams are shown in Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 102 for applications in the 2.4GHz band, and in Figure 5.5 Typical Sub-GHz RF impedance-matching network circuits on page 102 for applications in the sub-GHz band. Application-specific component values can be found in the EFR32xG1 Reference Manual. For low RF transmit power applications less than 13dBm, the two-element match is recommended. For OPNs supporting high power RF transmission, the four-element match is recommended for high RF transmit power (> 13dBm).

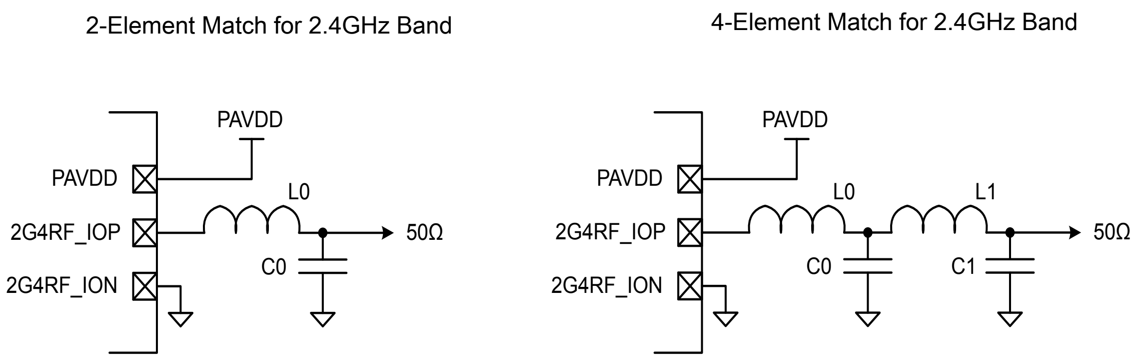


Figure 5.4. Typical 2.4 GHz RF impedance-matching network circuits

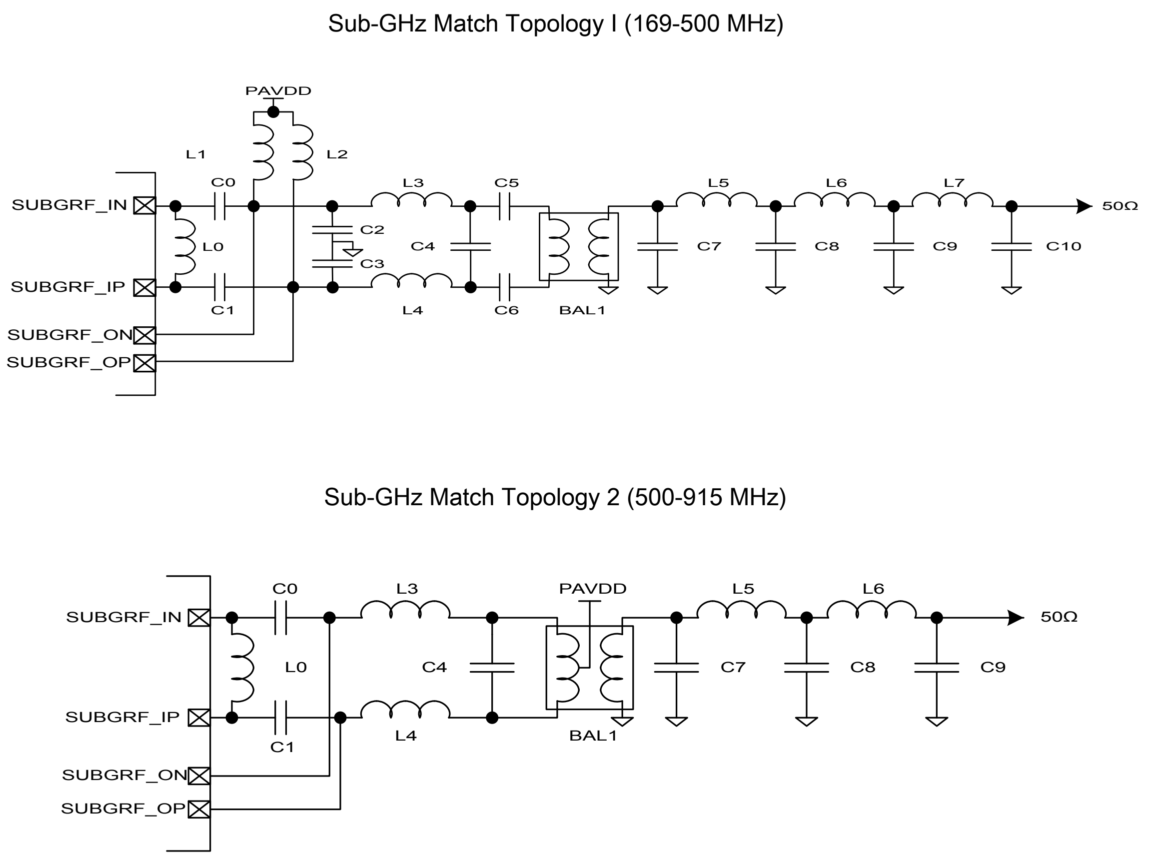


Figure 5.5. Typical Sub-GHz RF impedance-matching network circuits

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN48 2.4 GHz and Sub-GHz Device Pinout

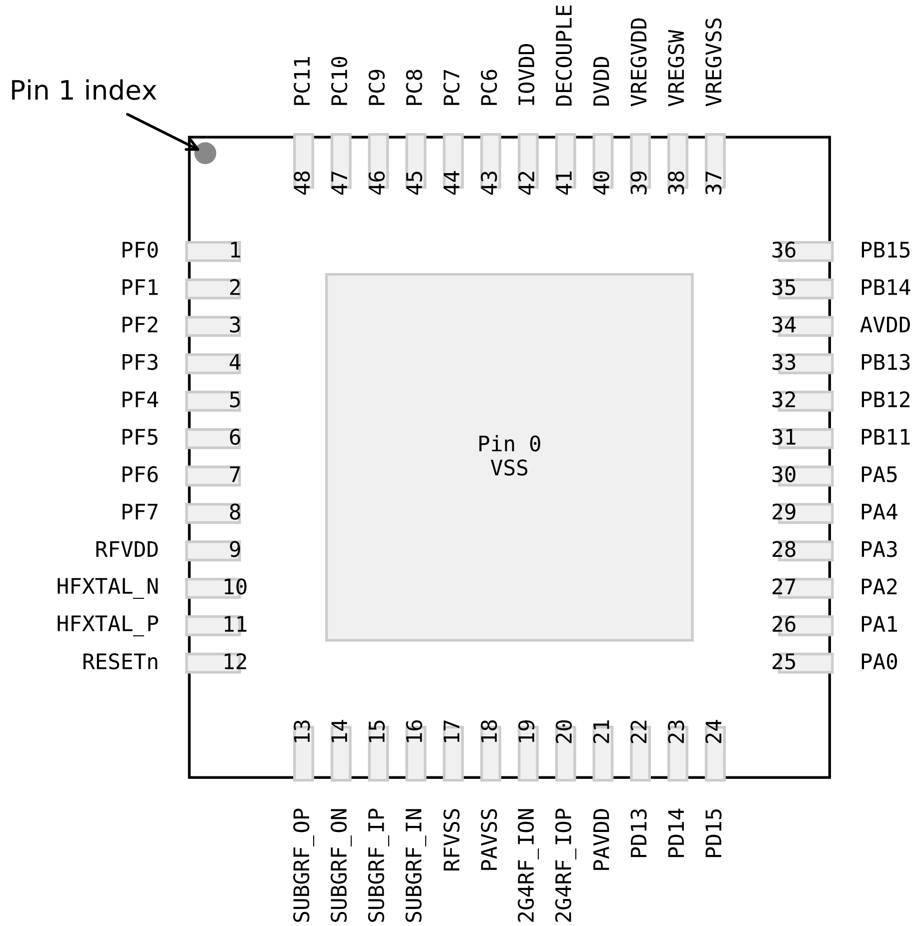


Figure 6.1. QFN48 2.4 GHz and Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 GPIO Functionality Table or 6.7 Alternate Functionality Overview.

Table 6.1. QFN48 2.4 GHz and Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	PF4	5	GPIO (5V)
PF5	6	GPIO (5V)	PF6	7	GPIO (5V)
PF7	8	GPIO (5V)	RFVDD	9	Radio power supply
HFXTAL_N	10	High Frequency Crystal input pin.	HFXTAL_P	11	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	12	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	SUBGRF_OP	13	Sub GHz Differential RF output, positive path.
SUBGRF_ON	14	Sub GHz Differential RF output, negative path.	SUBGRF_IP	15	Sub GHz Differential RF input, positive path.
SUBGRF_IN	16	Sub GHz Differential RF input, negative path.	RFVSS	17	Radio Ground
PAVSS	18	Power Amplifier (PA) voltage regulator VSS	2G4RF_ION	19	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.
2G4RF_IOP	20	2.4 GHz Differential RF input/output, positive path.	PAVDD	21	Power Amplifier (PA) voltage regulator VDD input
PD13	22	GPIO (5V)	PD14	23	GPIO (5V)
PD15	24	GPIO (5V)	PA0	25	GPIO
PA1	26	GPIO	PA2	27	GPIO (5V)
PA3	28	GPIO (5V)	PA4	29	GPIO (5V)
PA5	30	GPIO (5V)	PB11	31	GPIO (5V)
PB12	32	GPIO (5V)	PB13	33	GPIO (5V)
AVDD	34	Analog power supply.	PB14	35	GPIO
PB15	36	GPIO	VREGVSS	37	Voltage regulator VSS
VREGSW	38	DCDC regulator switching node	VREGVDD	39	Voltage regulator VDD input
DVDD	40	Digital power supply.	DECOUPLE	41	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
IOVDD	42	Digital IO power supply.	PC6	43	GPIO (5V)
PC7	44	GPIO (5V)	PC8	45	GPIO (5V)
PC9	46	GPIO (5V)	PC10	47	GPIO (5V)
PC11	48	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PA2, PA3, PA4, PB11, PB12, PB13, PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.2 QFN48 2.4 GHz Device Pinout

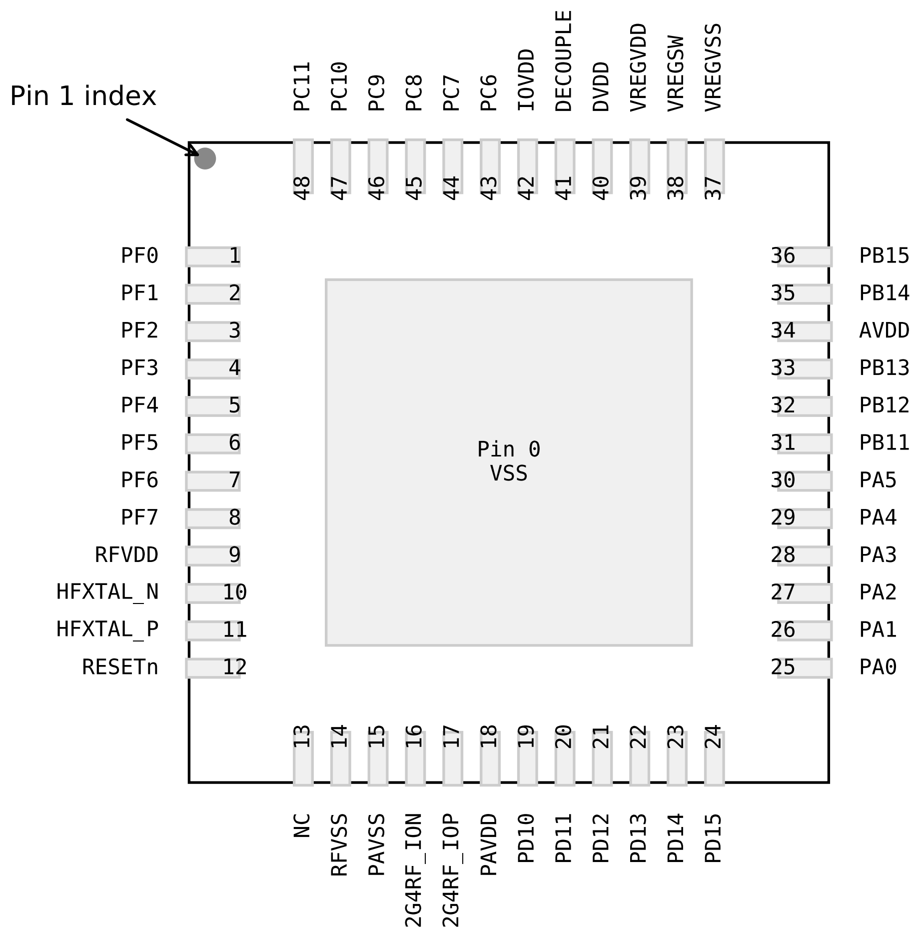


Figure 6.2. QFN48 2.4 GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 GPIO Functionality Table or 6.7 Alternate Functionality Overview.

Table 6.2. QFN48 2.4 GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	PF4	5	GPIO (5V)
PF5	6	GPIO (5V)	PF6	7	GPIO (5V)
PF7	8	GPIO (5V)	RFVDD	9	Radio power supply
HFXTAL_N	10	High Frequency Crystal input pin.	HFXTAL_P	11	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	12	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	NC	13	No Connect.
RFVSS	14	Radio Ground	PAVSS	15	Power Amplifier (PA) voltage regulator VSS
2G4RF_ION	16	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.	2G4RF_IOP	17	2.4 GHz Differential RF input/output, positive path.
PAVDD	18	Power Amplifier (PA) voltage regulator VDD input	PD10	19	GPIO (5V)
PD11	20	GPIO (5V)	PD12	21	GPIO (5V)
PD13	22	GPIO (5V)	PD14	23	GPIO (5V)
PD15	24	GPIO (5V)	PA0	25	GPIO
PA1	26	GPIO	PA2	27	GPIO (5V)
PA3	28	GPIO (5V)	PA4	29	GPIO (5V)
PA5	30	GPIO (5V)	PB11	31	GPIO (5V)
PB12	32	GPIO (5V)	PB13	33	GPIO (5V)
AVDD	34	Analog power supply.	PB14	35	GPIO
PB15	36	GPIO	VREGVSS	37	Voltage regulator VSS
VREGSW	38	DCDC regulator switching node	VREGVDD	39	Voltage regulator VDD input
DVDD	40	Digital power supply.	DECOUPLE	41	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
IOVDD	42	Digital IO power supply.	PC6	43	GPIO (5V)
PC7	44	GPIO (5V)	PC8	45	GPIO (5V)
PC9	46	GPIO (5V)	PC10	47	GPIO (5V)
PC11	48	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PA2, PA3, PA4, PB11, PB12, PB13, PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.3 QFN48 Sub-GHz Device Pinout

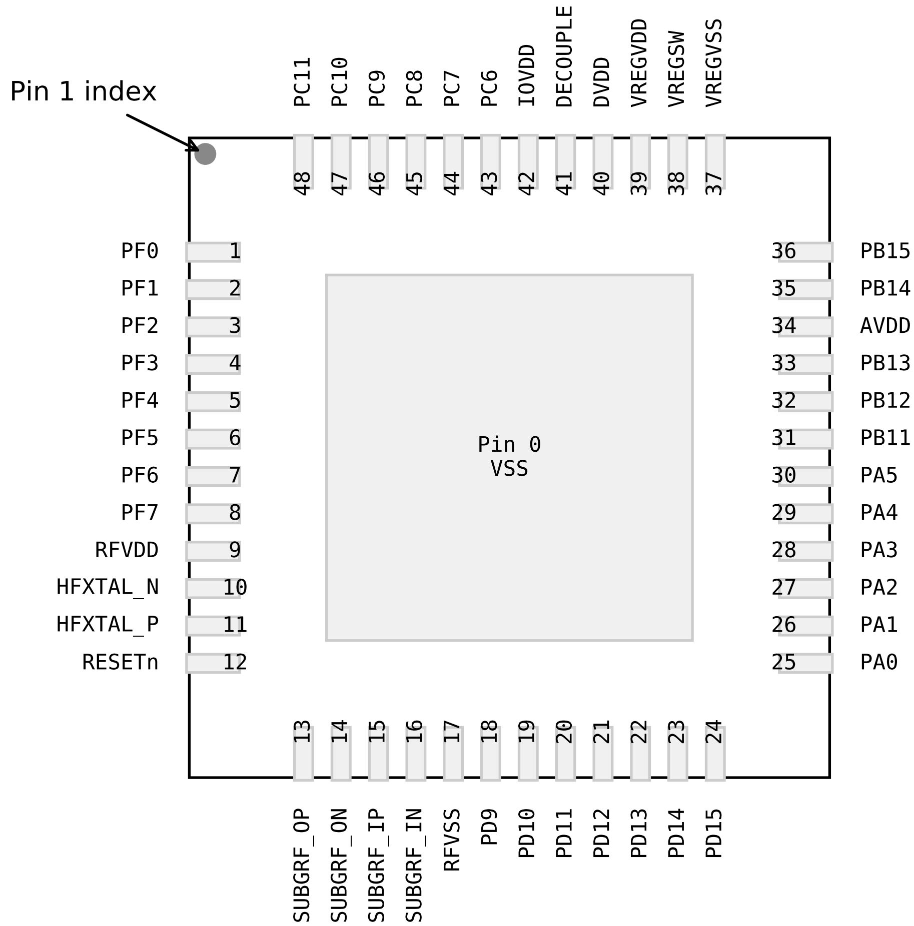


Figure 6.3. QFN48 Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 GPIO Functionality Table or 6.7 Alternate Functionality Overview.

Table 6.3. QFN48 Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	PF4	5	GPIO (5V)
PF5	6	GPIO (5V)	PF6	7	GPIO (5V)
PF7	8	GPIO (5V)	RFVDD	9	Radio power supply
HFXTAL_N	10	High Frequency Crystal input pin.	HFXTAL_P	11	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	12	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	SUBGRF_OP	13	Sub GHz Differential RF output, positive path.
SUBGRF_ON	14	Sub GHz Differential RF output, negative path.	SUBGRF_IP	15	Sub GHz Differential RF input, positive path.
SUBGRF_IN	16	Sub GHz Differential RF input, negative path.	RFVSS	17	Radio Ground
PD9	18	GPIO (5V)	PD10	19	GPIO (5V)
PD11	20	GPIO (5V)	PD12	21	GPIO (5V)
PD13	22	GPIO (5V)	PD14	23	GPIO (5V)
PD15	24	GPIO (5V)	PA0	25	GPIO
PA1	26	GPIO	PA2	27	GPIO (5V)
PA3	28	GPIO (5V)	PA4	29	GPIO (5V)
PA5	30	GPIO (5V)	PB11	31	GPIO (5V)
PB12	32	GPIO (5V)	PB13	33	GPIO (5V)
AVDD	34	Analog power supply.	PB14	35	GPIO
PB15	36	GPIO	VREGVSS	37	Voltage regulator VSS
VREGSW	38	DCDC regulator switching node	VREGVDD	39	Voltage regulator VDD input
DVDD	40	Digital power supply.	DECOUPLE	41	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
IOVDD	42	Digital IO power supply.	PC6	43	GPIO (5V)
PC7	44	GPIO (5V)	PC8	45	GPIO (5V)
PC9	46	GPIO (5V)	PC10	47	GPIO (5V)
PC11	48	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PA2, PA3, PA4, PB11, PB12, PB13, PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.4 QFN32 2.4 GHz Device Pinout

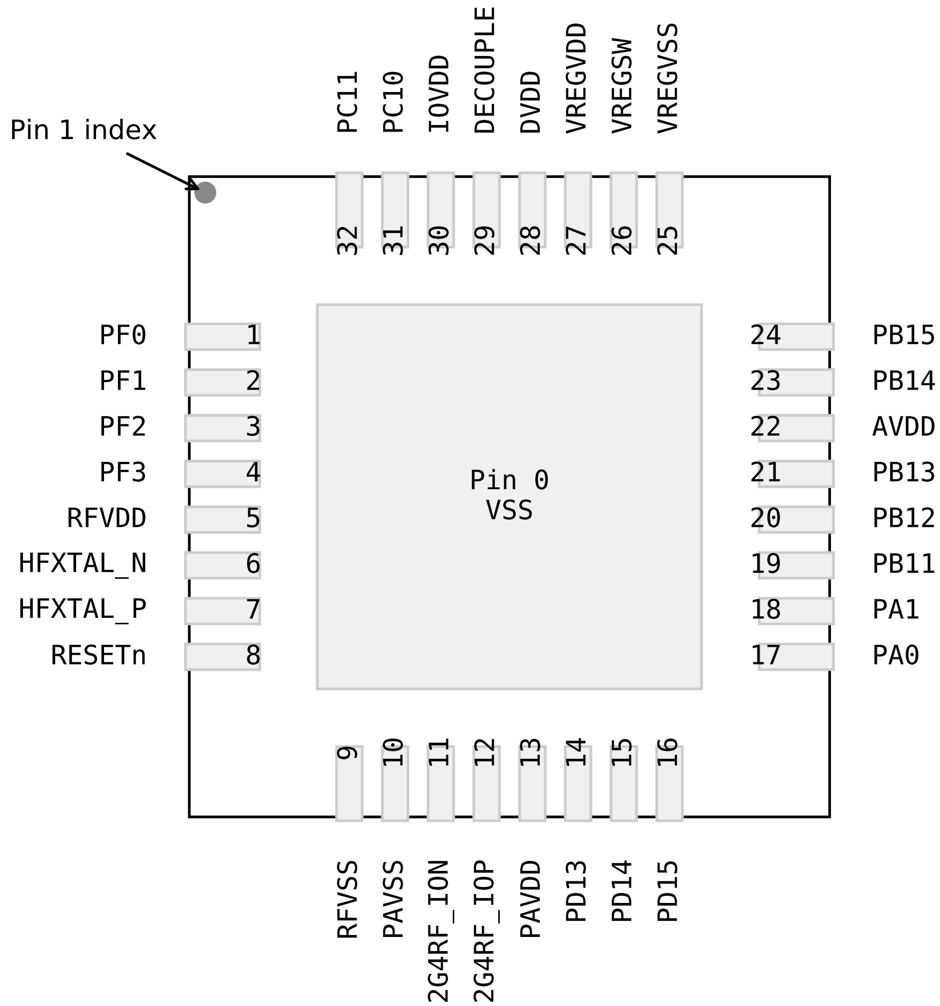


Figure 6.4. QFN32 2.4 GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 GPIO Functionality Table or 6.7 Alternate Functionality Overview.

Table 6.4. QFN32 2.4 GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	RFVDD	5	Radio power supply
HFXTAL_N	6	High Frequency Crystal input pin.	HFXTAL_P	7	High Frequency Crystal output pin.
RESETn	8	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	RFVSS	9	Radio Ground

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PAVSS	10	Power Amplifier (PA) voltage regulator VSS	2G4RF_ION	11	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.
2G4RF_IOP	12	2.4 GHz Differential RF input/output, positive path.	PAVDD	13	Power Amplifier (PA) voltage regulator VDD input
PD13	14	GPIO (5V)	PD14	15	GPIO (5V)
PD15	16	GPIO (5V)	PA0	17	GPIO
PA1	18	GPIO	PB11	19	GPIO (5V)
PB12	20	GPIO (5V)	PB13	21	GPIO (5V)
AVDD	22	Analog power supply.	PB14	23	GPIO
PB15	24	GPIO	VREGVSS	25	Voltage regulator VSS
VREGSW	26	DCDC regulator switching node	VREGVDD	27	Voltage regulator VDD input
DVDD	28	Digital power supply.	DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
IOVDD	30	Digital IO power supply.	PC10	31	GPIO (5V)
PC11	32	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB11, PB12, PB13, PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.5 QFN32 Sub-GHz Device Pinout

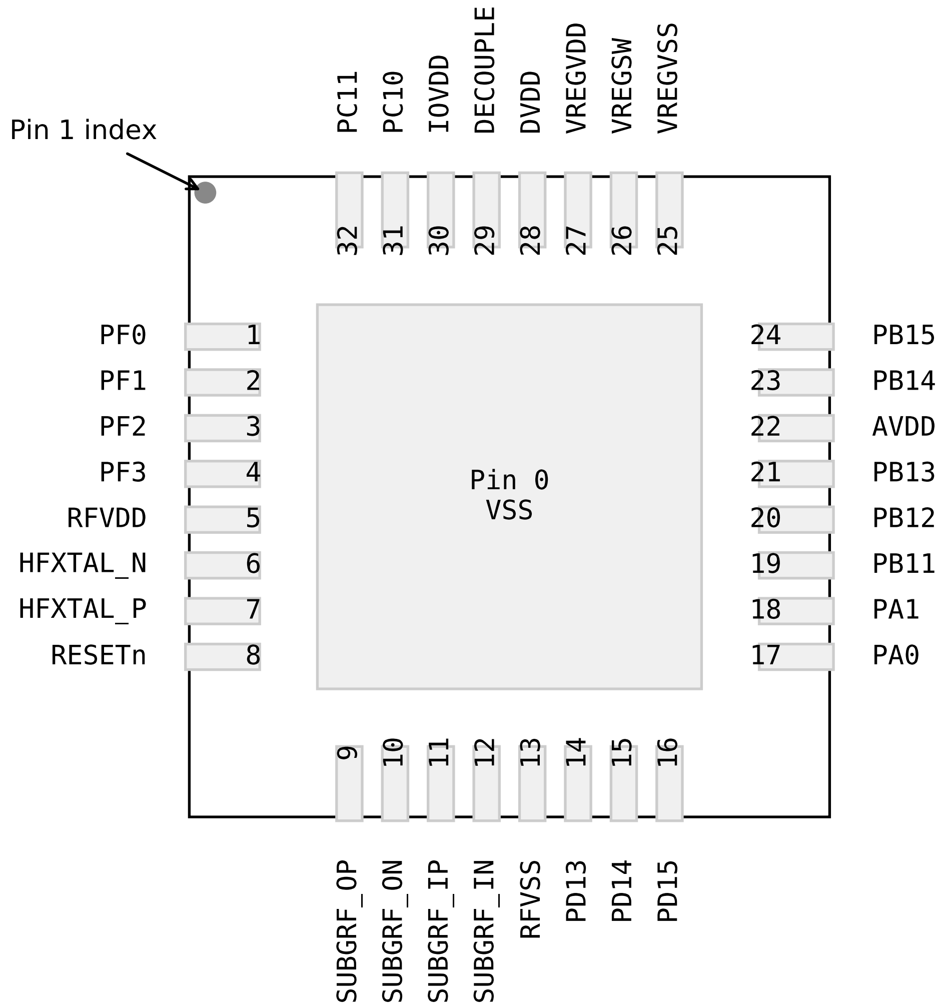


Figure 6.5. QFN32 Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 GPIO Functionality Table or 6.7 Alternate Functionality Overview.

Table 6.5. QFN32 Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	RFVDD	5	Radio power supply
HFXTAL_N	6	High Frequency Crystal input pin.	HFXTAL_P	7	High Frequency Crystal output pin.
RESETn	8	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	SUBGRF_OP	9	Sub GHz Differential RF output, positive path.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
SUBGRF_ON	10	Sub GHz Differential RF output, negative path.	SUBGRF_IP	11	Sub GHz Differential RF input, positive path.
SUBGRF_IN	12	Sub GHz Differential RF input, negative path.	RFVSS	13	Radio Ground
PD13	14	GPIO (5V)	PD14	15	GPIO (5V)
PD15	16	GPIO (5V)	PA0	17	GPIO
PA1	18	GPIO	PB11	19	GPIO (5V)
PB12	20	GPIO (5V)	PB13	21	GPIO (5V)
AVDD	22	Analog power supply.	PB14	23	GPIO
PB15	24	GPIO	VREGVSS	25	Voltage regulator VSS
VREGSW	26	DCDC regulator switching node	VREGVDD	27	Voltage regulator VDD input
DVDD	28	Digital power supply.	DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
IOVDD	30	Digital IO power supply.	PC10	31	GPIO (5V)
PC11	32	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PB11, PB12, PB13, PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.6 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 6.7 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 6.6. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK
PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23 MODEM_ANT0 #22 MODEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS
PF2	BUSBY BUSAX	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24 MODEM_ANT0 #23 MODEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO DBG_SWO #0 GPIO_EM4WU0

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI
PF4	BUSBY BUSAX	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26 MODEM_ANT0 #25 MODEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE- TIM0_OUT0 #29 LE- TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27 MODEM_ANT0 #26 MODEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MODEM_DOUT #28 MODEM_ANT0 #27 MODEM_ANT1 #26	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE- TIM0_OUT0 #31 LE- TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MODEM_DOUT #29 MODEM_ANT0 #28 MODEM_ANT1 #27	CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	FRC_DCLK #17 FRC_DOUT #16 FRC_DFRAME #15 MODEM_DCLK #17 MODEM_DIN #16 MODEM_DOUT #15 MODEM_ANT0 #14 MODEM_ANT1 #13	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD10	BUSDY BUSCX	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE- TIM0_OUT0 #18 LE- TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	FRC_DCLK #18 FRC_DOUT #17 FRC_DFRAME #16 MODEM_DCLK #18 MODEM_DIN #17 MODEM_DOUT #16 MODEM_ANT0 #15 MODEM_ANT1 #14	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18
PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	FRC_DCLK #19 FRC_DOUT #18 FRC_DFRAME #17 MODEM_DCLK #19 MODEM_DIN #18 MODEM_DOUT #17 MODEM_ANT0 #16 MODEM_ANT1 #15	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19
PD12	BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	FRC_DCLK #20 FRC_DOUT #19 FRC_DFRAME #18 MODEM_DCLK #20 MODEM_DIN #19 MODEM_DOUT #18 MODEM_ANT0 #17 MODEM_ANT1 #16	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD13	BUSCY BUSDX	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19 MODEM_ANT0 #18 MODEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
PD14	BUSDY BUSCX	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20 MODEM_ANT0 #19 MODEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4
PD15	BUSCY BUSDX	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21 MODEM_ANT0 #20 MODEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
PA1	BUSCY BUSDX ADC0_EXTP	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
PA2	BUSDY BUSCX	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE-TIM0_OUT0 #2 LE-TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MODEM_ANT1 #30	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2
PA3	BUSCY BUSDX	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE-TIM0_OUT0 #3 LE-TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1 MODEM_ANT0 #0 MODEM_ANT1 #31	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA4	BUSDY BUSCX	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2 MODEM_ANT0 #1 MODEM_ANT1 #0	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4
PA5	BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3 MODEM_ANT0 #2 MODEM_ANT1 #1	PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5
PB11	BUSCY BUSDX	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
PB12	BUSDY BUSCX	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB13	BUSCY BUSDX	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7 MODEM_ANT0 #6 MODEM_ANT1 #5	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9
PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE-TIM0_OUT0 #10 LE-TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8 MODEM_ANT0 #7 MODEM_ANT1 #6	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE- TIM0_OUT0 #11 LE- TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MODEM_DOUT #9 MODEM_ANT0 #8 MODEM_ANT1 #7	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LE- TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MODEM_DOUT #10 MODEM_ANT0 #9 MODEM_ANT1 #8	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
PC8	BUSBY BUSAX	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LE- TIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MODEM_DOUT #11 MODEM_ANT0 #10 MODEM_ANT1 #9	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LE- TIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MODEM_DOUT #12 MODEM_ANT0 #11 MODEM_ANT1 #10	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14
PC10	BUSBY BUSAX	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13 MODEM_ANT0 #12 MODEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14 MODEM_ANT0 #13 MODEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

6.7 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 6.6 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.7. Alternate Functionality Overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin.
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	4: PD9 5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.
MODEM_ANT0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	MODEM antenna control output 1, used for antenna diversity.
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2	8: PD9 9: PD10 10: PD11 11: PD12	12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PD9 1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH5	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15 6: PD9							Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PD9	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

6.8 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 6.6 APORT Connection Diagram on page 131 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

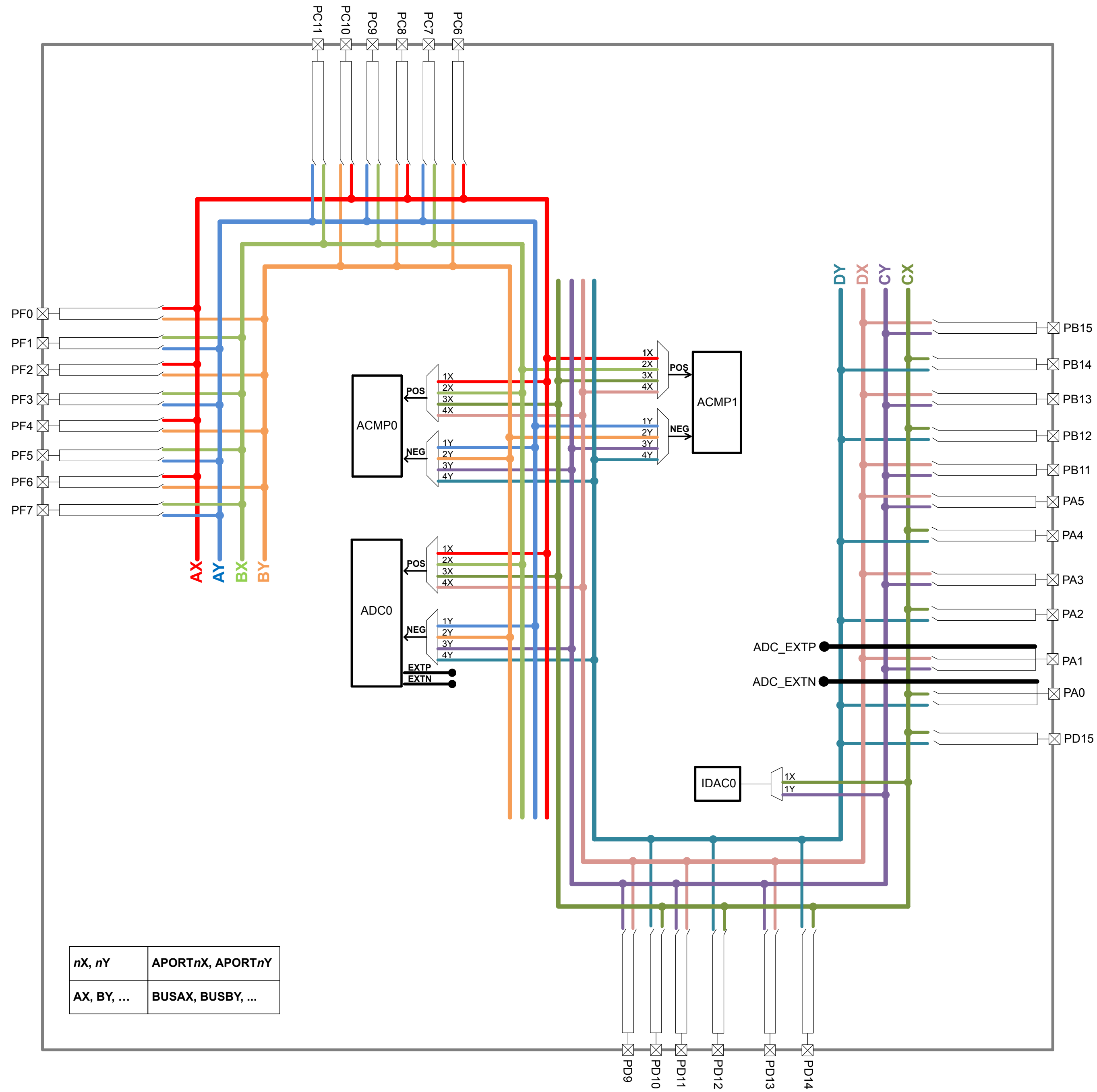


Figure 6.6. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.8. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.9. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.10. ADC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2X	BUSBX									PF7		PF5		PF3		PF1						PC11		PC9		PC7							
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.11. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT1Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	

7. QFN48 Package Specifications

7.1 QFN48 Package Dimensions

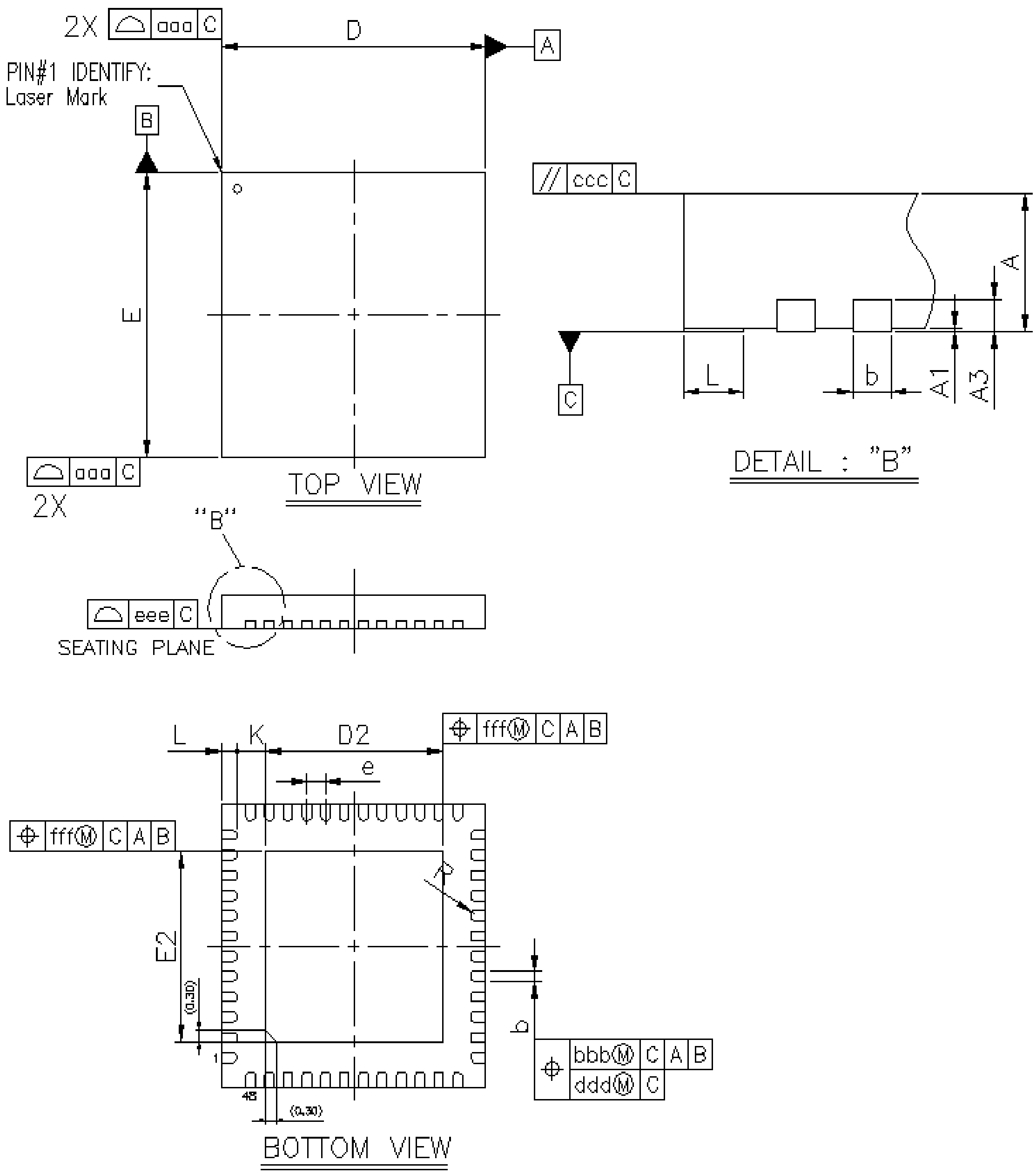


Figure 7.1. QFN48 Package Drawing

Table 7.1. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.60	4.70	4.80
E2	4.60	4.70	4.80
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN48 PCB Land Pattern

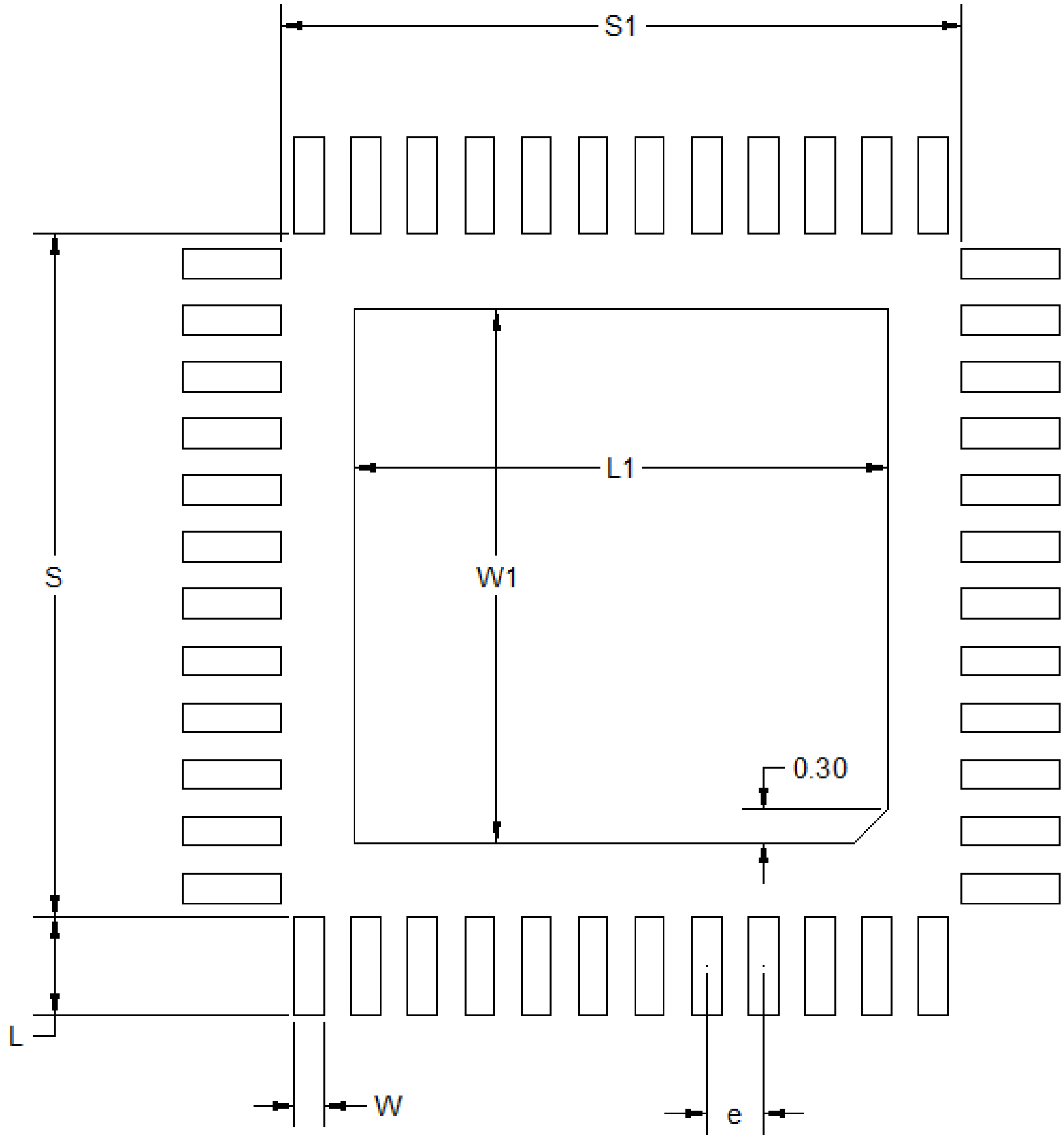


Figure 7.2. QFN48 PCB Land Pattern Drawing

Table 7.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26
L	0.86

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN48 Package Marking

Figure 7.3. QFN48 Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (1, 2,...)
  4. Performance Grade (P | B | V)
  5. Feature Code (1 to 7)
  6. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  7. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
  8. Flash (J = 1024K | H = 512K | G = 256K | F = 128K | E = 64K | D = 32K)
  9. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- # – Bootloader revision number.

8. QFN32 Package Specifications

8.1 QFN32 Package Dimensions

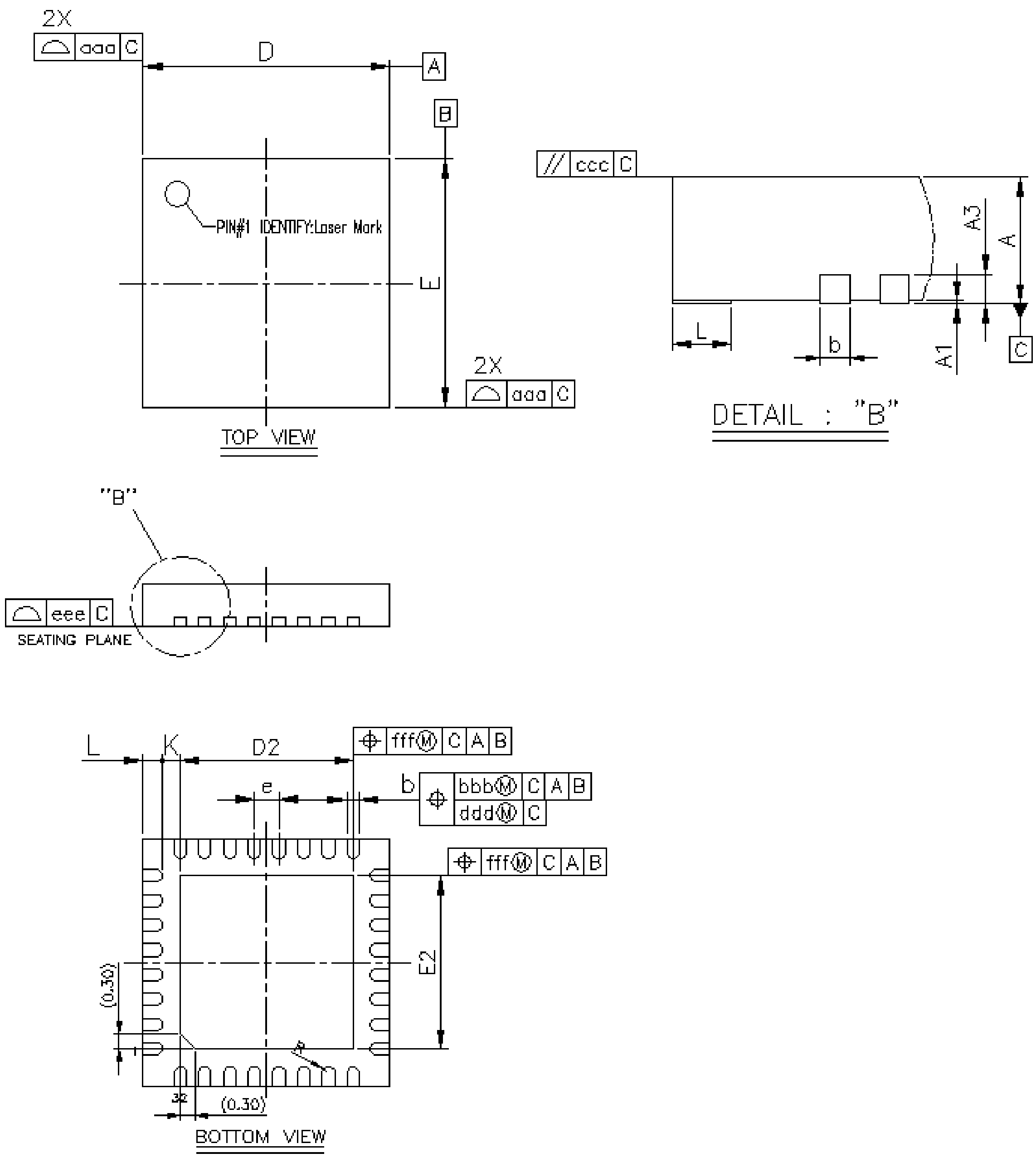


Figure 8.1. QFN32 Package Drawing

Table 8.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN32 PCB Land Pattern

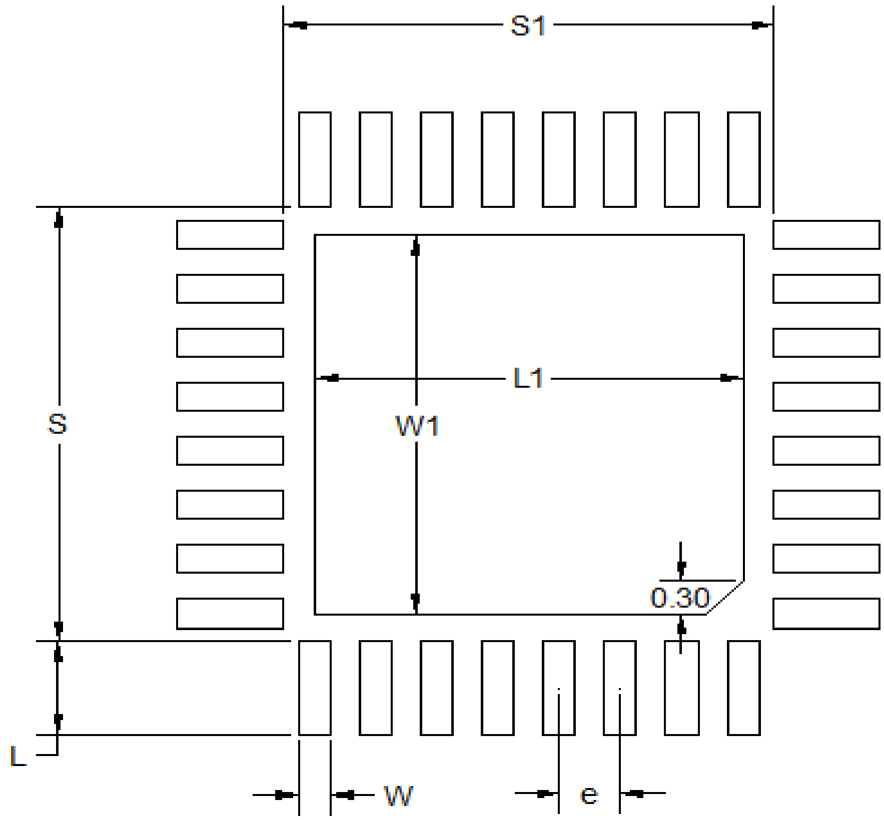


Figure 8.2. QFN32 PCB Land Pattern Drawing

Table 8.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.01
S	4.01
L1	3.50
W1	3.50
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFN32 Package Marking

Figure 8.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Series (1, 2,...)
  4. Performance Grade (P | B | V)
  5. Feature Code (1 to 7)
  6. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  7. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
  8. Flash (J = 1024K | H = 512k | G = 256K | F = 128K | E = 64K | D = 32K)
  9. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

9. Revision History

Revision 1.3

April, 2018

- Table 3.1 Configuration Summary on page 17: Corrected USART1 features (removed IrDA).

Revision 1.2

November, 2017

- Applied latest formatting, style, and sequence guidelines.
- Updated front page with new title and messaging.
- Added high-temperature (-I grade) part numbers and associated sections / specifications.
- Parameter Names, Symbol Names, and Test Conditions throughout electrical specification tables updated for consistency across all EFR32xG1x product families.
- Electrical specification changes not related to formatting consistency, typographical errors, or the addition of high-temperature part numbers are listed below.
  - 4.1.1 Absolute Maximum Ratings:
    - V_{DDMAX}: Min value changed from 0 to -0.3 V.
    - Removed $P_{RFMAXSUBG}$, $V_{MAXDIFFSUBG}$, and DeltaV_{DD} specifications.
    - Split $V_{MAXSUBG}$ into separate line items for SUBGRF_OP/SUBGRF_ON and SUBGRF_IP/SUBGRF_IN.
    - $V_{MAXSUBG}$ for SUBGRF_IP/SUBGRF_IN: Min = -0.3 V, Max = +0.3 V.
    - Added footnotes to clarify V_{DIGPIN} specification for 5V tolerant GPIO.
  - Table 4.2 General Operating Conditions on page 22:
    - Added $C_{DECOUPLE}$ and f_{HFCLK} specifications.
    - Added footnote for additional information on peak current during voltage scaling operations.
  - Table 4.6 Current Consumption 3.3 V using DC-DC Converter on page 27:
    - I_{EM1}: CCM Mode specifications removed from table.
    - Low Power Mode footnote corrected from "LPBIAS=3" to "LPCMPBIAS=0", and "LPCILIMSEL" to "LPCLIMILIMSEL".
    - Typical values for I_{EM2} updated to 2.5 and 2.2 uA per errata CUR_E201.
    - Typical value for I_{EM3} updated to 2.1 uA per errata CUR_E201.
  - Table 4.15 RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate on page 38: typical value for SENS updated to -92.5 dBm.
  - 4.1.9.3 RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate: TXBW Test Condition at 10 dBm added.
  - Table 4.17 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band on page 42:
    - $RSSI_{MAX}$ value placed in Max column and $RSSI_{MIN}$ value placed in Min column.
    - Typical values for SENS updated to -99 dBm per errata RADIO_E208.
  - Table 4.19 Sub-GHz RF Receiver Characteristics for 915 MHz Band on page 47: 100kbps reference signal footnote corrected to show 400 kHz channel spacing instead of 200 kHz.
  - Table 4.34 HFRCO on page 71 and Table 4.35 AUXHFRCO on page 72 tables separated (specifications are identical for this product).
  - Table 4.37 Flash Memory Characteristics[5] on page 73:
    - Added single-word programming time and clarified existing specification as per-word timing for a 128-word burst write.
    - Added footnotes to clarify mass, device, and page erase timing conditions.
  - Table 4.39 Voltage Monitor (VMON) on page 76: I_{VMON} specifications for EM2/3/4 separated into above threshold and below threshold conditions.
  - Table 4.40 Analog to Digital Converter (ADC) on page 77
    - V_{ADCIN} specification changed to reference V_{FS} instead of V_{REF}.
    - Input referred ADC noise specification removed.
    - Footnotes added to clarify internal and external reference configurations.
  - Table 4.41 Analog Comparator (ACMP) on page 79: Text explaining total ACMP current calculation brought into table as a footnote.
  - 4.1.21 USART SPI:
    - SPI Master Timing: Updated with relaxed values.
    - SPI Slave Timing: Corrected t_{SCLK} Min value to "6 * $t_{HFPERCLK}$" from "2 * $t_{HFPERCLK}$".
    - Updated remainder of specifications to match formatting and common specs in all EFR32xG1x product families.
- Added PCNT electrical specifications table: Table 4.43 Pulse Counter (PCNT) on page 83.
- 4.2 Typical Performance Curves: Added data for >85C operation.
- 5.2 RF Matching Networks: Removed redundant paragraph in introduction.

- Added section 5.3 Other Connections.
- Condensed pinout tables and moved detailed GPIO functionality information to 6.6 GPIO Functionality Table.
- Added Figure 6.6 APORT Connection Diagram on page 131.
- Corrected flash designator description in Package Marking sections.

Revision 1.1

2016-Oct-26

- Ordering Information: Removed Encryption column. All products in family include full encryption capabilites. Previously EFR32FG1V devices listed as "AES only".
- System Overview Sections: Minor wording and typographical error fixes.
- Electrical Characteristics: Minor wording and typographical error fixes.
- "Sub-GHz Receiver Characteristics for 433 MHz Band" table in Electrical Characteristics: Corrected Sensitivity spec error where data for 50 kbps and 2.4 kbps were swapped.
- "HFRCO and AUXHFRCO" table in Electrical Characteristics: f_HFRCO symbol changed to f_HFRCO_ACC.
- Pinout tables: APORT channel details removed from "Analog" column. This information is now found in the APORT client map sections.
- Updated APORT client map sections.

Revision 1.0

2016-Jul-22

- Electrical Characteristics: Minimum and maximum value statement changed to cover full operating temperature range.
- Finalized Specification Tables. Tables with condition/min/typ/max or footnote changes include:
  - Absolute Maximum Ratings
  - General Operating Conditions
  - DC-DC Converter
  - Current Consumption Using Radio 3.3V with DC-DC
  - RF Transmitter General Characteristics for 2.4 GHz Band
  - RF Receiver General Characteristics for 2.4 GHz Band
  - RF Receiver Characteristics for 1Mbps 2GFSK in the 2.4 GHz Band
  - RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band
  - RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band
  - Sub-GHz RF Transmitter characteristics for 868 MHz Band
  - Sub-GHz RF Transmitter characteristics for 490 MHz Band
  - Sub-GHz RF Receiver characteristics for 490 MHz Band
  - Sub-GHz RF Receiver characteristics for 433 MHz Band
  - HFRCO and AUXHFRCO
  - ADC
  - IDAC
- Updated Typical Performance Graphs.
- Added external ground note to 2G4RF_ION pin descriptions.
- Added note for 5V tolerance to pinout GPIO Overview sections.
- Updated OPN decoder with latest revision.
- Updated Package Marking text with latest descriptions.

Revision 0.97

2016-06-06

- Added dual-band and sub-GHz OPNs.

Revision 0.951

2016-06-03

- Electrical specification tables updated with additional characterization data.

Revision 0.95

2016-04-11

- All OPNs changed to rev C0. Note the following:
  - All OPNs ending in -B0 are Engineering Samples based on an older revision of silicon and are being removed from the OPN table. These older revisions should be used for evaluation only and will not be supported for production.
  - OPNs ending in -C0 are the Current Revision of Silicon and are intended for production.
- Electrical specification tables updated with latest characterization data and production test limits.

Revision 0.9

2016-01-12

- Updated electrical specifications with latest characterization data.
- Added thermal characteristics table.
- Updated OPN decoder figure to include extended family options.

Revision 0.81

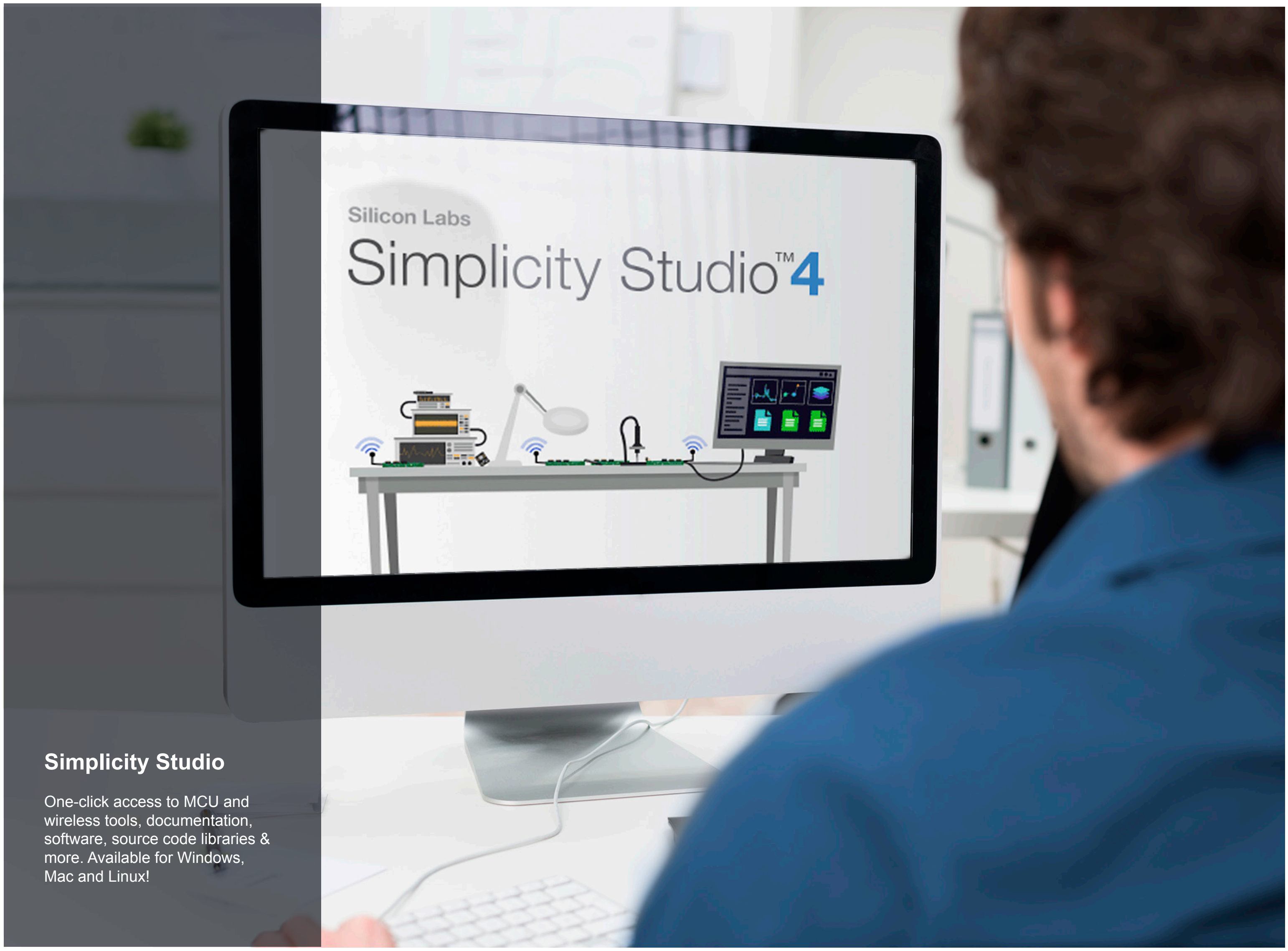
2015-12-01

- Engineering samples note added to ordering information table.

Revision 0.8

2015-11-14

- Initial external release.
- Consolidated individual device datasheets into single-family document.
- Re-formatted ordering information table and OPN decoder.
- Updated block diagrams for front page and system overview.
- Removed extraneous sections from DC-DC and wake-on-radio from system overview.
- Updated table formatting for electrical specifications to tech pubs standards.
- Updated electrcal specifications with latest available data.
- Added I2C and USART SPI timing tables.
- Moved DC-DC graph to typical performance curves.
- Updated APORT tables and APORT references to correct nomenclature.



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