

EFR32FG23 Wireless SoC Family Data Sheet



The EFR32FG23 SoC is an ideal solution for sub-GHz “Internet of Things” for smart home, security, lighting, building automation, and metering. The high-performance sub-GHz radio provides long range and is not susceptible to 2.4 GHz interference from technologies like Wi-Fi.

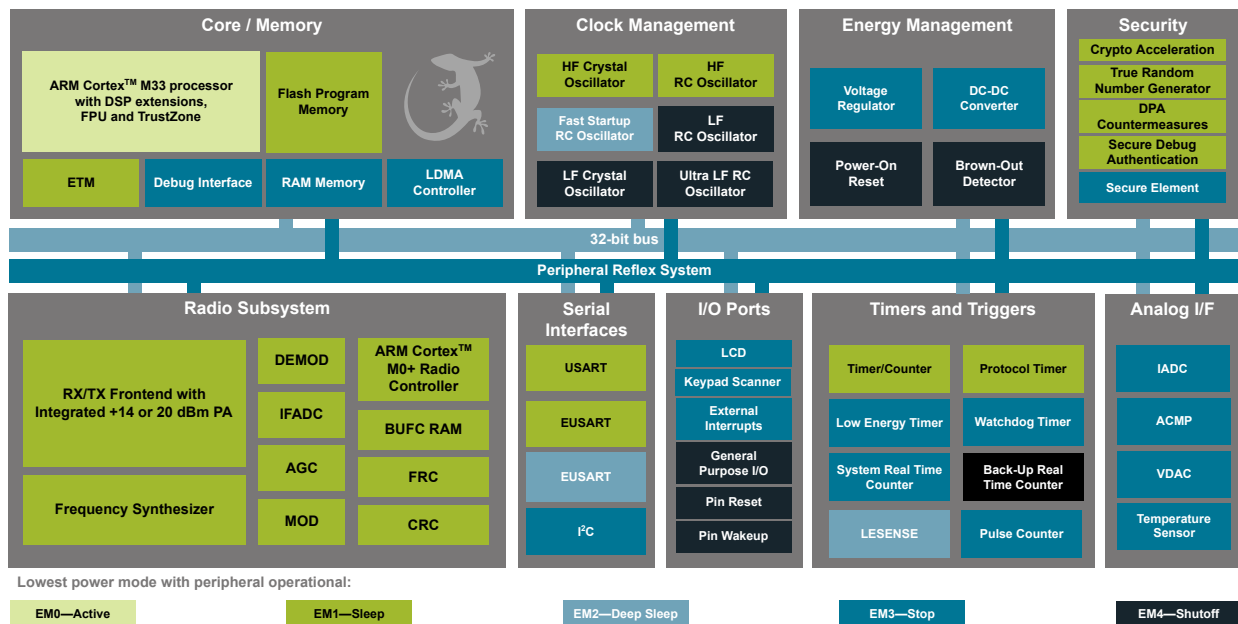
The single die, multi-core solution, provides industry leading security, low power consumption with fast wakeup times, and an integrated power amplifier to enable the next level of secure connectivity for IoT devices.

EFR32FG23 applications include:

- Metering
- Home and Building Automation and Security
- Industrial Automation
- Street Lighting

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 78 MHz maximum operating frequency
- Up to 512 kB of flash and 64 kB of RAM
- Energy-efficient radio core with low active and sleep currents
- Integrated PA with up to 20 dBm (sub-GHz) TX power
- Robust peripheral set and up to 31 GPIO



1. Feature List

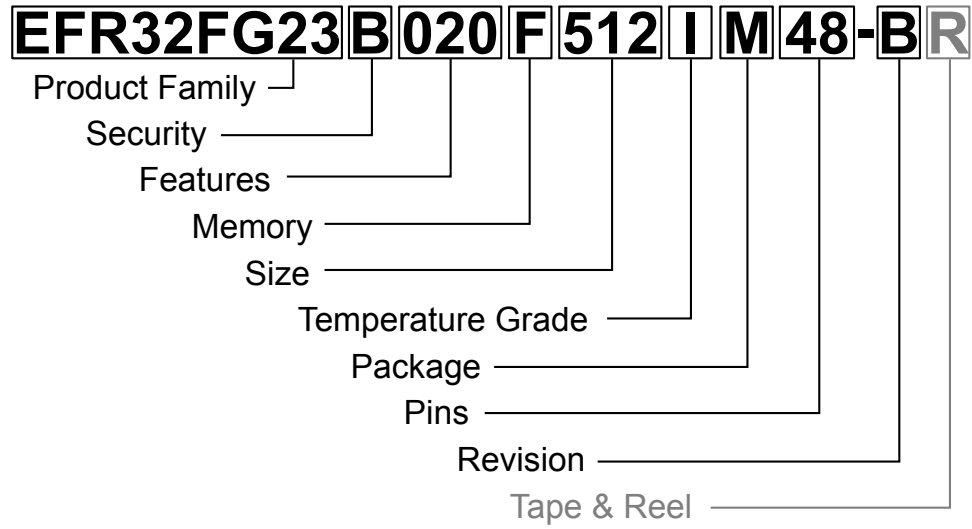
The EFR32FG23 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
 - High Performance 32-bit 78 MHz ARM Cortex[®]-M33 with DSP instruction and floating-point unit for efficient signal processing
 - Up to 512 kB flash program memory
 - Up to 64 kB RAM data memory
 - Sub-GHz radio operation
 - TX power up to +20 dBm
- **Low Energy Consumption**
 - 4.2 mA RX current at 920 MHz (400 kbps 4-FSK)
 - 3.8 mA RX current at 915 MHz (4.8 kbps O-QPSK)
 - 5.1 mA RX current at 915 MHz (2 Mbps GFSK)
 - 3.7 mA RX current at 868 MHz (2.4 kbps GFSK)
 - 3.7 mA RX current at 868 MHz (38.4 kbps FSK)
 - 4.0 mA RX current at 433 MHz (100 kbps 2GFSK)
 - 25 mA TX current @ 14 dBm output power at 915 MHz (14 dBm part numbers)
 - 85.5 mA TX current @ 20 dBm output power at 915 MHz (20 dBm part numbers)
 - 26 μ A/MHz in Active Mode (EM0) at 39.0 MHz
 - 1.5 μ A EM2 DeepSleep current (64 kB RAM retention and RTC running from LFXO)
 - 1.2 μ A EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **High Receiver Performance**
 - -98.6 dBm sensitivity @ 400 kbps 920 MHz 4-GFSK
 - -125.8 dBm sensitivity @ 4.8 kbps 915 MHz O-QPSK
 - -96.9 dBm sensitivity @ 2 Mbps 915 MHz GFSK
 - -125.3 dBm sensitivity @ 2.4 kbps 868 MHz GFSK
 - -111.8 dBm sensitivity @ 38.4 kbps 868 MHz FSK
 - -110.7 dBm sensitivity @ 100 kbps 433 MHz 2GFSK
- **Supported Modulation Format**
 - 2/4 (G)FSK with fully configurable shaping
 - OQPSK DSSS
 - (G)MSK
 - OOK
- **Protocol Support**
 - Proprietary
 - CONNECT
 - Wi-SUN
 - Sidewalk
 - WM-BUS
- **Wide selection of MCU peripherals**
 - Analog to Digital Converter (ADC)
 - 12-bit @ 1 Msps
 - 16-bit @ 76.9 ksps
 - 2 \times Analog Comparator (ACMP)
 - 2-Channel Digital to Analog Converter (VDAC)
 - Low-Energy Sensor Interface (LESENSE)
 - Up to 31 General Purpose I/O pins with output state retention and asynchronous interrupts
 - 8 Channel DMA Controller
 - 12 Channel Peripheral Reflex System (PRS)
 - 4 \times 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
 - 1 \times 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
 - 32-bit Real Time Counter
 - 24-bit Low Energy Timer for waveform generation
 - 16-bit Pulse Counter with asynchronous operation (PCNT)
 - 2 \times Watchdog Timer
 - 3 \times Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)
 - 1 \times Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I²S)
 - 2 \times I²C interface with SMBus support
 - Integrated Low-Energy LCD Controller supporting up to 80 segments
 - Keypad scanner supporting up to 6 \times 8 matrix (KEYSCAN)
 - Die temperature sensor
- **Secure Vault**
 - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
 - True Random Number Generator (TRNG)
 - ARM[®] TrustZone[®]
 - Secure Boot (Root of Trust Secure Loader)
 - Secure Debug Unlock
 - DPA Countermeasures
 - Secure Key Management with PUF
 - Anti-Tamper
 - Secure Attestation
- **Wide Operating Range**
 - 1.71 V to 3.8 V single power supply
 - -40 °C to +125 °C
- **Packages**
 - **QFN40** 5 mm \times 5 mm \times 0.85 mm
 - **QFN48** 6 mm \times 6 mm \times 0.85 mm

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	Flash (kB)	RAM (kB)	Secure Vault	GPIO	LCD	Pack-age	Temp Range
EFR32FG23B020F512IM48-B	Proprietary	20 dBm	512	64	High	31	Yes	QFN48	-40 to 125 °C
EFR32FG23B020F512IM40-B	Proprietary	20 dBm	512	64	High	23	No	QFN40	-40 to 125 °C
EFR32FG23B020F128GM40-B	Proprietary	20 dBm	128	32	High	23	No	QFN40	-40 to 85 °C
EFR32FG23B010F512IM48-B	Proprietary	14 dBm	512	64	High	31	Yes	QFN48	-40 to 125 °C
EFR32FG23B010F512IM40-B	Proprietary	14 dBm	512	64	High	23	No	QFN40	-40 to 125 °C
EFR32FG23B010F128GM40-B	Proprietary	14 dBm	128	32	High	23	No	QFN40	-40 to 85 °C
EFR32FG23A021F512GM40-B	Proprietary	20 dBm	512	64	Mid	22	No	QFN40	-40 to 85 °C
EFR32FG23A020F512GM48-B	Proprietary	20 dBm	512	64	Mid	31	Yes	QFN48	-40 to 85 °C
EFR32FG23A020F512GM40-B	Proprietary	20 dBm	512	64	Mid	23	No	QFN40	-40 to 85 °C
EFR32FG23A020F256GM48-B	Proprietary	20 dBm	256	32	Mid	31	Yes	QFN48	-40 to 85 °C
EFR32FG23A020F256GM40-B	Proprietary	20 dBm	256	32	Mid	23	No	QFN40	-40 to 85 °C
EFR32FG23A011F512GM40-B	Proprietary	14 dBm	512	64	Mid	22	No	QFN40	-40 to 85 °C
EFR32FG23A010F512GM48-B	Proprietary	14 dBm	512	64	Mid	31	Yes	QFN48	-40 to 85 °C
EFR32FG23A010F512GM40-B	Proprietary	14 dBm	512	64	Mid	31	No	QFN40	-40 to 85 °C
EFR32FG23A010F256GM48-B	Proprietary	14 dBm	256	32	Mid	31	Yes	QFN48	-40 to 85 °C
EFR32FG23A010F256GM40-B	Proprietary	14 dBm	256	32	Mid	23	No	QFN40	-40 to 85 °C



Field	Options
Product Family	<ul style="list-style-type: none"> • EFR32FG23: Wireless Gecko Flex 23 Family
Security	<ul style="list-style-type: none"> • A: Secure Vault Mid • B: Secure Vault High
Features [f1][f2][f3]	<ul style="list-style-type: none"> • f1 <ul style="list-style-type: none"> • 0: Unused • f2 <ul style="list-style-type: none"> • 1: 14 dBm PA Transmit Power • 2: 20 dBm PA Transmit Power • f3 <ul style="list-style-type: none"> • 0: Unused • 1: High Quality HFCLKOUT Pin Available
Memory	<ul style="list-style-type: none"> • F: Flash
Size	<ul style="list-style-type: none"> • Memory Size in kBytes
Temperature Grade	<ul style="list-style-type: none"> • G: -40 to +85 °C • I: -40 to +125 °C
Package	<ul style="list-style-type: none"> • M: QFN
Pins	<ul style="list-style-type: none"> • Number of Package Pins
Revision	<ul style="list-style-type: none"> • B: Revision B
Tape & Reel	<ul style="list-style-type: none"> • R: Tape & Reel (optional)

Figure 2.1. Ordering Code Key

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG23 Reference Manual.

A block diagram of the EFR32FG23 family is shown in [Figure 3.1 Detailed EFR32FG23 Block Diagram on page 9](#). The diagram shows a superset of features available on the family, which vary by part number. For more information about specific device features, consult [Ordering Information](#).

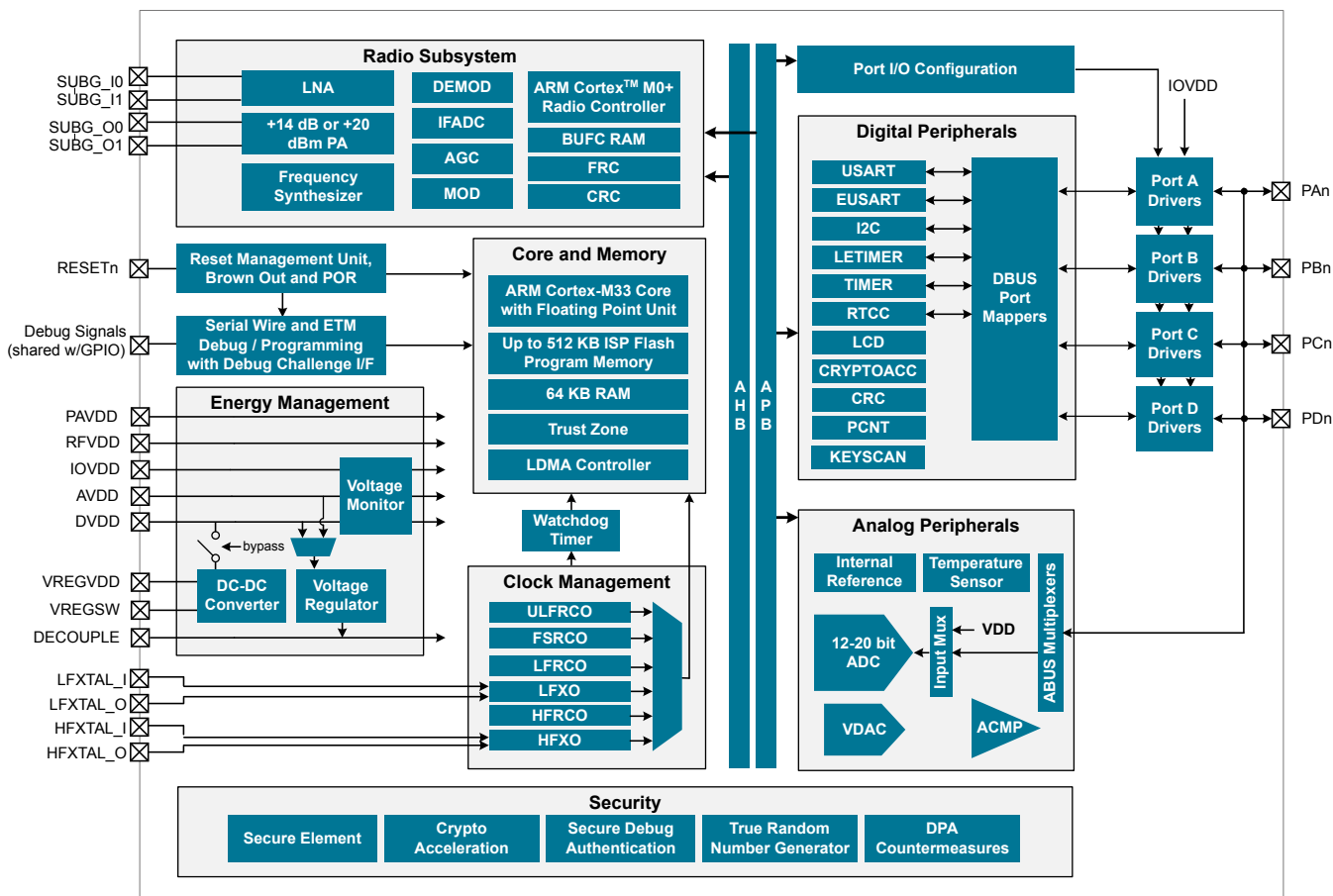


Figure 3.1. Detailed EFR32FG23 Block Diagram

3.2 Radio

The EFR32FG23 family features a radio transceiver supporting proprietary wireless protocols.

3.2.1 Antenna Interface

The sub-GHz antenna interface consists of two single-ended input pins (SUBG_I0 and SUBG_I1) that interface directly to two LNAs and two single-ended output pins that interface directly to two +14 dBm or +20 dBm PA (SUBG_O0 and SUBG_O1). Integrated switches select either SUBG_O0 or SUBG_O1 to be the active path.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32FG23 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 24.8 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32FG23 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32FG23 features integrated support for antenna diversity to improve link budget configuration in the sub-GHz band, using complementary control outputs to an external switch. Internal configurable hardware controls automatic switching between antennae during RF receive detection operations.

3.2.4 Transmitter Architecture

The EFR32FG23 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32FG23. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32FG23 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32FG23 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32FG23. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.3 General Purpose Input/Output (GPIO)

EFR32FG23 has up to 31 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in [6.4 Alternate Function Table](#).

3.4 Keypad Scanner (KEYSCAN)

A low-energy keypad scanner (KEYSCAN) is included, which can scan up to a 6 x 8 matrix of keyboard switches. The KEYSKAN peripheral contains logic for debounce and settling time, allowing it to scan through the switch matrix autonomously in EM0 and EM1, and interrupt the processor when a key press is detected. A wake-on-keypress feature is also supported, allowing for the detection of any key press down to EM3.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32FG23. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32FG23 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 39.0 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

See [3.14 Configuration Summary](#) for information on the feature set of each timer.

3.6.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.6.3 System Real Time Clock with Capture (SYSRTC)

The System Real Time Clock (SYSRTC) is a 32-bit counter providing timekeeping down to EM3. The SYSRTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

3.6.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.6.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.7.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1 the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

3.7.3 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Note that not all instances of I²C are available in all energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Secure Vault Features

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core, and provides several additional security features. The EFR32FG23 family includes devices with Secure Vault High and Secure Vault Mid capabilities, which are summarized in the table below.

Table 3.1. Secure Vault Features

Feature	Secure Vault Mid	Secure Vault High
True Random Number Generator (TRNG)	Yes	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes	Yes
Secure Debug with Lock/Unlock	Yes	Yes
DPA Countermeasures	Yes	Yes
Anti-Tamper		Yes
Secure Attestation		Yes
Secure Key Management		Yes
Symmetric Encryption	<ul style="list-style-type: none"> AES 128 / 192 / 256 bit <ul style="list-style-type: none"> ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC 	<ul style="list-style-type: none"> AES 128 / 192 / 256 bit <ul style="list-style-type: none"> ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC ChaCha20
Public Key Encryption - ECDSA / ECDH / EdDSA	<ul style="list-style-type: none"> p192 and p256 	<ul style="list-style-type: none"> p192, p256, p384 and p521 Curve25519 (ECDH) Ed25519 (EdDSA)
Key Derivation	<ul style="list-style-type: none"> ECJ-PAKE p192 and p256 	<ul style="list-style-type: none"> ECJ-PAKE p192, p256, p384, and p521 PBKDF2 HKDF
Hashes	<ul style="list-style-type: none"> SHA-1 SHA-2/256 	<ul style="list-style-type: none"> SHA-1 SHA-2 256, 384, and 512 Poly1305

3.8.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed and protects Over The Air updates.

More information on this feature can be found in the Application Note *AN1218: Series 2 Secure Boot with RTSL*.

3.8.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.8.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.8.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, Secure Vault High also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

More information on this feature can be found in the Application Note *AN1190: Series 2 Secure Debug*.

3.8.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.8.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by what is called "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of being able to protect a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33 (which includes off-chip storage as well). The symmetric key used for this wrapping and unwrapping must be highly secure as it can expose all other key material in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.8.7 Anti-Tamper

Secure Vault High devices provide internal tamper monitoring the system such as voltage, temperature, and electro-mechanical pulses as well as detecting tamper of the security sub-system itself. There are also 8 external configurable tamper pins for supporting external tamper sources like case tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all the protected key material un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

More information on this feature can be found in the Application Note *AN1247: Anti-Tamper Protection Configuration and Use*.

3.8.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory, and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

This secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

More information on this feature can be found in the Application Note *AN1268: Authenticating Silicon Labs Devices Using Device Certificates*.

3.9 Analog

3.9.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.4 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD with up to 4x20 segments. A voltage boost function enables it to provide the LCD with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD peripheral supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.10 Power

The EFR32FG23 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32FG23 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.10.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.10.2 Voltage Scaling

The EFR32FG23 supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.10.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, providing high efficiency in energy modes EM0, EM1, EM2 and EM3. RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

3.10.4 Power Domains

The EFR32FG23 has five peripheral power domains for operation in EM2 and EM3, as well as the ability to selectively retain configurations for EM0/EM1 peripherals. A small set of peripherals always remain powered on in EM2 and EM3, including all peripherals which are available in EM4. If all of the peripherals in PD0B, PD0C, PD0D, or PD0E are configured as unused, that power domain will be powered off in EM2 or EM3, reducing the overall current consumption of the device. Likewise, if the application can tolerate the setup time to re-configure used EM0/EM1 peripherals on wake, register retention for these peripherals can be disabled to further reduce the EM2 or EM3 current.

Table 3.2. Peripheral Power Subdomains

Always available in EM2/EM3	Power Domain PD0B	Power Domain PD0C	Power Domain PD0D	Power Domain PD0E
SYSRTC	LETIMER0	HFRCOEM23	DEBUG	GPIO
LFRCO ¹	IADC0	HFXO	WDOG0	KEYSCAN
LFXO ¹	PCNT0		WDOG1	PRS
BURTC ¹	ACMP0		EUSART0	
ULFRCO ¹	ACMP1		I2C0	
FSRCO1	LESENSE			
LCD	VDAC0			

Note:

1. Peripheral also available in EM4.

3.11 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32FG23. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.12 Core and Memory

3.12.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 512 kB flash program memory
- Up to 64 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.12.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.12.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.13 Memory Map

The EFR32FG23 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

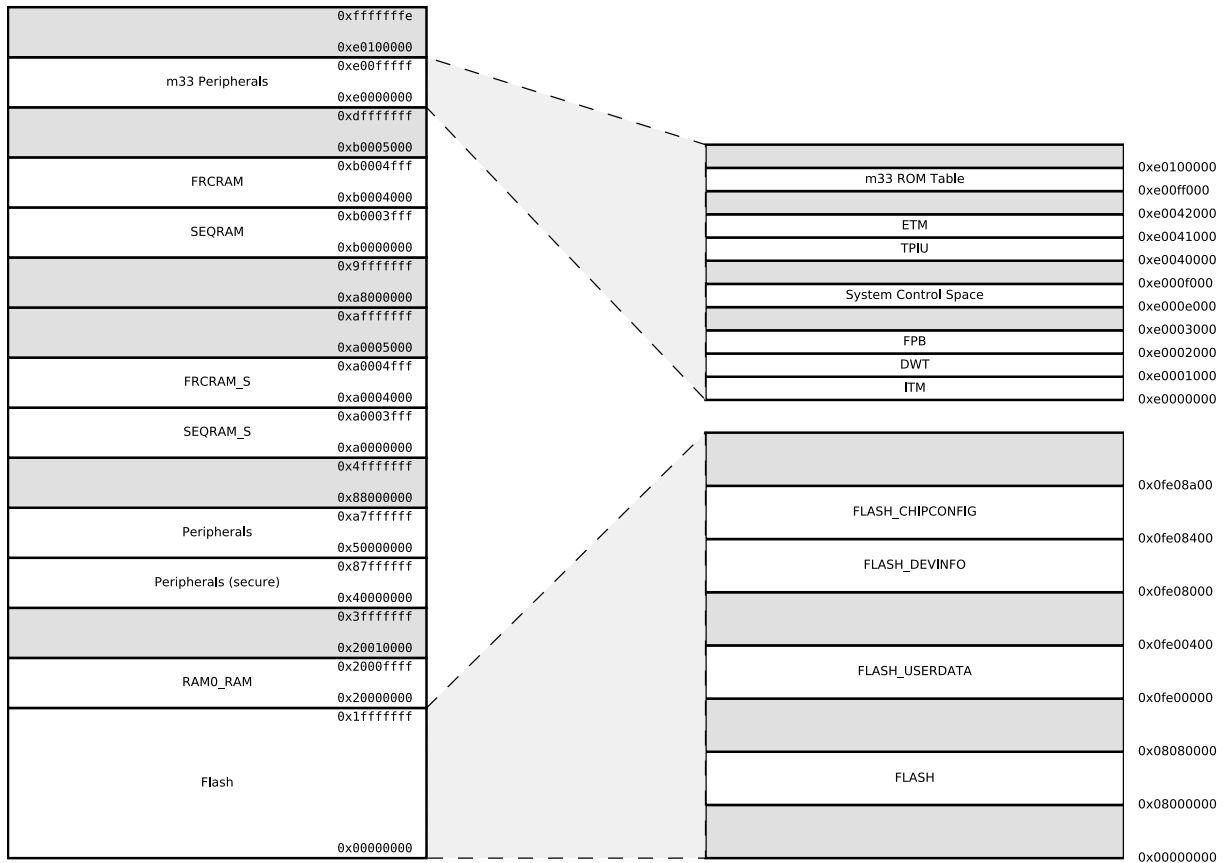


Figure 3.2. EFR32FG23 Memory Map — Core Peripherals and Code Space

3.14 Configuration Summary

The features of the EFR32FG23 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.3. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM2/EM3 ¹	
I2C1	EM1	
IADC0	EM2/EM3	
LETIMER0	EM2/EM3 ¹	
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	16-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUSART0	EM1 - Full high-speed operation EM2 ¹ - Low-energy operation, 9600 Baud	
EUSART1	EM1 - Full high-speed operation	
EUSART2	EM1 - Full high-speed operation	
USART0	EM1	+IrDA, +I2S, +SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_A=25\text{ }^\circ\text{C}$ and all supplies at 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Due to on-chip circuitry (e.g., diodes), some EFR32FG23 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32FG23 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD and DVDD
 - In systems using the DCDC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD ($VREGVDD \geq DVDD$)
 - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB ($VREGVDD=DVDD$)
- AVDD, IOVDD: No dependency with each other or any other supply pin
- $DVDD \geq DECOUPLE$
- $PAVDD \geq RFVDD$

4.2 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <https://www.silabs.com/about-us/corporate-responsibility/commitment-to-quality>.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T _{STG}		-50	—	+150	°C
Voltage on any supply pin	V _{DDMAX}		-0.3	—	3.8	V
Junction temperature	T _{JMAX}	-G grade	—	—	+105	°C
		-I grade	—	—	+125	°C
Voltage ramp rate on any supply pin	V _{DDRAMP} MAX		—	—	1.0	V / μs
Voltage on HFXO pins	V _{HFXOPIN}		-0.3	—	1.2	V
DC voltage on any GPIO pin ¹	V _{DIGPIN}		-0.3	—	V _{IOVDD} + 0.3	V
DC voltage on RESETn pin ²	V _{RESETn}		-0.3	—	3.8	V
Total current into VDD power lines	I _{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I _{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I _{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	I _{IOALLMAX}	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

- When operating as an LCD driver, the output voltage on a GPIO may safely exceed this specification. The pin output voltage may be up to 3.8 V in this case.
- The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade ¹	-40	—	+85	°C
		-I temperature grade ¹	-40	—	+125	°C
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.3	3.8	V
		EM2/3/4 ²	TBD	3.3	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.3	3.8	V
IOVDD operating supply voltage	V_{IOVDD}		1.71	3.3	3.8	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.3	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DCDC in regulation	2.2	3.3	3.8	V
		DCDC in bypass 60 mA load	1.8	3.3	3.8	V
		DCDC in bypass 120 mA load	1.9	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.71	3.3	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.3	V_{PAVDD}	V
DECOUPLE output capacitor ³	$C_{DECOUPLE}$	1.0 μ F \pm 10% X8L capacitor used for performance characterization.	0.75	1.0	2.75	μ F
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	78	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2	—	—	50	MHz
		VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
HCLK Radio frequency ⁴	f_{RHCLK}	VSCALE2 or VSCALE1	—	39.0	40	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
<ol style="list-style-type: none"> 1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. $T_A = T_{JMAX} - (\text{THETA}_{JA} \times \text{PowerDissipation})$. Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and THETA_{JA}. 2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4. 3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias. 4. The recommended radio crystal frequency for the sub-GHz radio is 39.0 MHz. The minimum and maximum RHCLK frequency in this table represent the design timing limits, which are much wider than the typical crystal tolerance. 						

4.4 DC-DC Converter

Test conditions: $L_{DCDC} = 2.2 \mu\text{H}$ (Samsung CIG22H2R2MNE), $C_{DCDC} = 4.7 \mu\text{F}$ (TDK CGA5L3X8R1C475K160AB), $V_{VREGVDD} = 3.3 \text{ V}$, $V_{OUT} = 1.8 \text{ V}$, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin	$V_{VREGVDD}$	DCDC in regulation, $I_{LOAD} = I_{LOAD MAX}^1$, EM0/EM1 mode	2.2	—	3.8	V
		DCDC in regulation, $I_{LOAD} = 5 \text{ mA}$, EM0/EM1 or EM2/EM3 mode	1.8	—	3.8	V
		Bypass Mode, $I_{LOAD} \leq 60 \text{ mA}$	1.8	—	3.8	V
		Bypass Mode, $I_{LOAD} \leq 120 \text{ mA}$	1.9	—	3.8	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD} \geq 2.2 \text{ V}$, Steady state in EM0/EM1 mode or EM2/EM3 mode	TBD	—	TBD	%
Regulation total accuracy	ACC_{TOT}	All error sources (including DC errors, overshoot, undershoot)	-5	—	7	%
Steady-state output ripple	V_R	$I_{LOAD} = 20 \text{ mA}$ in EM0/EM1 mode	—	12	—	mVpp
DC line regulation	V_{REG}	$I_{LOAD} = I_{LOAD MAX}^2$ in EM0/EM1 mode, $V_{VREGVDD} \geq 2.2 \text{ V}$	—	-2.6	—	mV/V
Efficiency	EFF	Load current between 10 μA and 5 mA in EM2/EM3 mode	—	89	—	%
DC load regulation	I_{REG}	Load current between 100 μA and $I_{LOAD MAX}^2$ in EM0/EM1 mode	—	-0.08	—	mV/mA
Output load current	I_{LOAD}	EM0/EM1 mode, DCDC in regulation, DCDC_EM01CTRL0.IPKVAL = 9, Pulse-pairing disabled, Radio not transmitting ²	—	—	60	mA
		EM0/EM1 mode, DCDC in regulation, Radio in receive mode, with pulse-pairing enabled ²	—	—	36	mA
		EM0/EM1 mode, DCDC in regulation, Radio transmitting ¹	—	—	120	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode, $1.8 \text{ V} \leq V_{VREGVDD} \leq 3.8 \text{ V}$	—	—	60	mA
		Bypass mode, $1.9 \text{ V} \leq V_{VREGVDD} \leq 3.8 \text{ V}$	—	—	120	mA
Nominal output capacitor	C_{DCDC}	4.7 $\mu\text{F} \pm 10\%$ X7R capacitor used for performance characterization ³	—	4.7	10	μF
Nominal inductor	L_{DCDC}	$\pm 20\%$ tolerance	—	2.2	—	μH
Nominal input capacitor	C_{IN}		C_{DCDC}	—	—	μF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resistance in bypass mode	R _{BYP}	Bypass switch from VREGVDD to DVDD, V _{VREGVDD} = 1.8 V	—	0.45	TBD	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, V _{VREGVDD} = 1.8 V	—	0.6	TBD	Ω
Supply monitor threshold programming range	V _{CMP_RNG}	Programmable in 0.1 V steps	TBD	—	TBD	V
Supply monitor threshold accuracy	V _{CMP_ACC}	Supply falling edge trip point	TBD	—	TBD	%
Supply monitor threshold hysteresis	V _{CMP_HYST}	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%
Supply monitor response time	t _{CMP_DELAY}	Supply falling edge at -100 mV / μs	—	0.6	—	μs

Note:

1. During radio transmit operations, the RAIL library will place the DCDC into a mode that increases the maximum load current, to support higher TX output power supplied from the DCDC converter.
2. Pulse-pairing is an optional feature to improve performance at radio frequencies below 550 MHz, but has limited output current. It is enabled by default when using RAIL with an IPKVAL setting of 3 or less. Pulse pairing may be disabled from application code by setting IPKVAL > 3. This must be done before RAIL software is initialized.
3. TDK CGA5L3X8R1C475K160AB used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 3.6 μF.

4.5 Thermal Characteristics

Table 4.4. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
40QFN (5x5mm)	JEDEC - High Thermal Cond. (2s2p) ¹	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	26.3	°C/W
		Thermal Resistance, Junction to Board	Θ_{JB}		15.2	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.3	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		10.3	°C/W
	No Board	Thermal Resistance, Junction to Case	Θ_{JC}	Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow.	24.6	°C/W
48QFN (6x6mm)	JEDEC - High Thermal Cond. (2s2p) ¹	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	33.7	°C/W
		Thermal Resistance, Junction to Board	Θ_{JB}		14.6	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.7	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		13.4	°C/W
	No Board	Thermal Resistance, Junction to Case	Θ_{JC}	Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow.	23.0	°C/W

Note:

1. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 Via to top internal plane of PCB.

4.6 Current Consumption

4.6.1 MCU current consumption using DC-DC at 3.3 V input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.3 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU current consumption using DC-DC at 3.3 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	28	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	26	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	36	—	μA/MHz
		39 MHz crystal, CPU running Prime from flash	—	27	—	μA/MHz
		39 MHz crystal, CPU running while loop from flash	—	26	—	μA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	36	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	22	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	24	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	29	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	206	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	17	—	μA/MHz
		39 MHz crystal	—	18	—	μA/MHz
		38 MHz HFRCO	—	14	—	μA/MHz
		26 MHz HFRCO	—	16	—	μA/MHz
		16 MHz HFRCO	—	21	—	μA/MHz
		1 MHz HFRCO	—	197	—	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	64 kB RAM and full Radio RAM retention, RTC running from LFXO	—	1.5	—	μA
		64 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	1.5	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	1.2	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO	—	1.2	—	μA
Current consumption in EM3 mode, VSCALE0	I _{EM3_VS}	64 kB RAM and full Radio RAM retention, RTC running from ULFRCO	—	1.3	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO	—	1.0	—	μA
Current consumption for retained RAM bank in EM2 or EM3	I _{RAM}	Per 16 kB RAM bank	—	0.1	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ¹	I _{PD0B_VS}		—	0.85	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ¹	I _{PD0C_VS}		—	0.13	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ¹	I _{PD0D_VS}		—	0.98	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ¹	I _{PD0E_VS}		—	0.06	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.10.4 Power Domains](#) for a list of the peripherals in each power domain.

4.6.2 MCU current consumption at 3.3 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 3.3 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. MCU current consumption at 3.3 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	45	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	41	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	57	—	μA/MHz
		39 MHz crystal, CPU running Prime from flash	—	44	—	μA/MHz
		39 MHz crystal, CPU running while loop from flash	—	42	—	μA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	58	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	35	TBD	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	38	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	46	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	329	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	27	—	μA/MHz
		39 MHz crystal	—	29	—	μA/MHz
		38 MHz HFRCO	—	22	TBD	μA/MHz
		26 MHz HFRCO	—	25	—	μA/MHz
		16 MHz HFRCO	—	33	—	μA/MHz
		1 MHz HFRCO	—	315	TBD	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	64 kB RAM and full Radio RAM retention, RTC running from LFXO	—	2.4	—	μA
		64 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	2.4	TBD	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	1.92	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO	—	1.93	—	μA
		16 kB RAM retention and RTC running from LFXO, Sequencer RAM and CPU cache not retained	—	1.71	—	μA
		16 kB RAM retention and RTC running from LFXO, Sequencer RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.69	—	μA
		16 kB RAM retention and RTC running from LFXO, Sequencer RAM, FRC RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.62	—	μA
Current consumption in EM3 mode, VSCALE0	I _{EM3_VS}	64 kB RAM and full Radio RAM retention, RTC running from ULFRCO	—	2.0	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO	—	1.59	TBD	μA
Current consumption for retained RAM bank in EM2 or EM3	I _{RAM}	Per 16 kB RAM bank	—	0.14	—	μA
Current consumption in EM4 mode	I _{EM4}	No BURTC, no LF oscillator	—	0.32	TBD	μA
		BURTC with LFXO	—	0.70	—	μA
Current consumption during reset	I _{RST}	Hard pin reset held	—	462	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ¹	I _{PD0B_VS}		—	1.37	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ¹	I _{PD0C_VS}		—	0.20	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ¹	I _{PD0D_VS}		—	1.57	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ¹	I _{PD0E_VS}		—	0.09	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain.						

4.6.3 MCU current consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. MCU current consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	45	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	41	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	57	—	μA/MHz
		39 MHz crystal, CPU running Prime from flash	—	44	—	μA/MHz
		39 MHz crystal, CPU running while loop from flash	—	42	—	μA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	58	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	35	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	38	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	46	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	323	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	26	—	μA/MHz
		39 MHz crystal	—	29	—	μA/MHz
		38 MHz HFRCO	—	22	—	μA/MHz
		26 MHz HFRCO	—	25	—	μA/MHz
		16 MHz HFRCO	—	32	—	μA/MHz
		1 MHz HFRCO	—	309	—	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	64 kB RAM and full Radio RAM retention, RTC running from LFXO	—	2.2	—	μA
		64 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	2.2	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	1.72	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO	—	1.75	—	μA
Current consumption in EM3 mode, VSCALE0	I _{EM3_VS}	64 kB RAM and full Radio RAM retention, RTC running from ULFRCO	—	1.84	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO	—	1.4	—	μA
Current consumption for retained RAM bank in EM2 or EM3	I _{RAM}	Per 16 kB RAM bank	—	0.15	—	μA
Current consumption in EM4 mode	I _{EM4}	No BURTC, no LF oscillator	—	0.16	—	μA
		BURTC with LFXO	—	0.52	—	μA
Current consumption during reset	I _{RST}	Hard pin reset held	—	384	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ¹	I _{PD0B_VS}		—	1.38	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ¹	I _{PD0C_VS}		—	0.21	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ¹	I _{PD0D_VS}		—	1.59	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ¹	I _{PD0E_VS}		—	0.10	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.10.4 Power Domains](#) for a list of the peripherals in each power domain.

4.6.4 Radio current consumption at 3.3 V with DCDC

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.3 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.8. Radio current consumption at 3.3 V with DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P ¹	I _{RX_ACTIVE}	f = 924 MHz, 4-GFSK, 400 kbps	—	4.2	—	mA
		f = 915 MHz, 2-GFSK, 2 Mbps	—	5.1	—	mA
		f = 915 MHz, O-QPSK, 4.8 kbps	—	3.8	—	mA
		f = 915 MHz, FSK, 50 kbps	—	4.0	—	mA
		f = 915 MHz, O-QPSK, 250 kbps	—	5.3	—	mA
		f = 868 MHz, 2-GFSK, 2.4 kbps	—	3.7	—	mA
		f = 868 MHz, 2-GFSK, 38.4 kbps	—	3.7	—	mA
		f = 868 MHz, GMSK, 500 kbps	—	4.3	—	mA
		f = 868 MHz, O-QPSK, 100 kbps	—	4.3	—	mA
		f = 433 MHz, 2-GFSK, 100 kbps	—	4.0	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P ¹	I _{RX_LISTEN}	f = 924 MHz, 4-GFSK, 400 kbps	—	4.2	—	mA
		f = 915 MHz, 2-GFSK, 2 Mbps	—	5.2	—	mA
		f = 915 MHz, O-QPSK, 4.8 kbps	—	3.8	—	mA
		f = 915 MHz, FSK, 50 kbps	—	4.0	—	mA
		f = 915 MHz, O-QPSK, 250 kbps	—	5.7	—	mA
		f = 868 MHz, 2-GFSK, 2.4 kbps	—	3.7	—	mA
		f = 868 MHz, 2-GFSK, 38.4 kbps	—	3.7	—	mA
		f = 868 MHz, GMSK, 500 kbps	—	4.3	—	mA
		f = 868 MHz, O-QPSK, 100 kbps	—	4.3	—	mA
		f = 433 MHz, 2-GFSK, 100 kbps	—	4.0	—	mA
Current consumption in transmit mode, VSCALE2, EM1	I _{TX}	f = 868 MHz, CW, 14 dBm PA, 0 dBm output power ²	—	8.2	—	mA
		f = 868 MHz, CW, 14 dBm PA, +10 dBm output power ²	—	13.2	—	mA
		f = 915 MHz, CW, 14 dBm PA, +14 dBm output power ³	—	25	—	mA
		f = 868.3 MHz, CW, 14 dBm PA, +14 dBm output power ³	—	24.4	—	mA
		f = 915 MHz, CW, 20 dBm PA, +20 dBm output power ⁴ , PAVDD = 3.3V	—	85.5	—	mA
		f = 869.5 MHz, CW, 20 dBm PA, +20 dBm output power ⁴ , PAVDD = 3.3V	—	85.3	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. EM1P operation is 0.22 mA lower than EM1 operation 2. Using the +10 dBm matching network for 868/915/920 MHz Bands. 3. Using the +14 dBm matching network for 868/915/920 MHz Bands. 4. Using the +20 dBm matching network for 868/915/920 MHz Bands.						

4.6.5 Radio current consumption at 3.3V

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.3 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.9. Radio current consumption at 3.3V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P ¹	I _{RX_ACTIVE}	f = 924 MHz, 4-GFSK, 400 kbps	—	7.1	—	mA
		f = 915 MHz, 2-GFSK, 2 Mbps	—	8.5	—	mA
		f = 915 MHz, O-QPSK, 4.8 kbps	—	6.4	—	mA
		f = 915 MHz, FSK, 50 kbps	—	6.8	—	mA
		f = 915 MHz, O-QPSK, 250 kbps	—	8.9	—	mA
		f = 868 MHz, 2-GFSK, 2.4 kbps	—	6.2	—	mA
		f = 868 MHz, 2-GFSK, 38.4 kbps	—	6.3	—	mA
		f = 868 MHz, GMSK, 500 kbps	—	7.1	—	mA
		f = 868 MHz, O-QPSK, 100 kbps	—	7.2	—	mA
		f = 433 MHz, 2-GFSK, 100 kbps	—	6.7	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P ¹	I _{RX_LISTEN}	f = 924 MHz, 4-GFSK, 400 kbps	—	7.1	—	mA
		f = 915 MHz, 2-GFSK, 2 Mbps	—	8.8	—	mA
		f = 915 MHz, O-QPSK, 4.8 kbps	—	6.3	—	mA
		f = 915 MHz, FSK, 50 kbps	—	6.7	—	mA
		f = 915 MHz, O-QPSK, 250 kbps	—	9.5	—	mA
		f = 868 MHz, 2-GFSK, 2.4 kbps	—	6.3	—	mA
		f = 868 MHz, 2-GFSK, 38.4 kbps	—	6.3	—	mA
		f = 868 MHz, GMSK, 500 kbps	—	7.2	—	mA
		f = 868 MHz, O-QPSK, 100 kbps	—	7.2	—	mA
		f = 433 MHz, 2-GFSK, 100 kbps	—	6.7	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode, VSCALE2, EM1	I _{TX}	f = 868 MHz, CW, 14 dBm PA, 0 dBm output power ²	—	13.5	—	mA
		f = 868 MHz, CW, 14 dBm PA, +10 dBm output power ²	—	21.8	—	mA
		f = 915 MHz, CW, 14 dBm PA, +14 dBm output power ³	—	41.3	—	mA
		f = 915 MHz, CW, 20 dBm PA, +14 dBm output power ⁴	—	50.6	—	mA
		f = 868.3 MHz, CW, 14 dBm PA, +14 dBm output power ³	—	40.3	—	mA
		f = 915 MHz, CW, 20 dBm PA, +20 dBm output power ⁴	—	92	—	mA
		f = 869.5 MHz, CW, 20 dBm PA, +14 dBm output power ⁴	—	49.3	—	mA
		f = 869.5 MHz, CW, 20 dBm PA, +20 dBm output power ⁴	—	90.6	—	mA

Note:

1. EM1P operation is 0.35 mA lower than EM1 operation
2. Using the +10 dBm matching network for 868/915/920 MHz Bands.
3. Using the +14 dBm matching network for 868/915/920 MHz Bands.
4. Using the +20 dBm matching network for 868/915/920 MHz Bands.

4.6.6 Radio current consumption at 1.8V

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.10. Radio current consumption at 1.8V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P ¹	I _{RX_ACTIVE}	f = 924 MHz, 4-GFSK, 400 kbps	—	7.0	—	mA
		f = 915 MHz, 2-GFSK, 2 Mbps	—	8.5	—	mA
		f = 915 MHz, O-QPSK, 4.8 kbps	—	6.3	—	mA
		f = 915 MHz, FSK, 50 kbps	—	6.8	—	mA
		f = 915 MHz, O-QPSK, 250 kbps	—	8.9	—	mA
		f = 868 MHz, 2-GFSK, 2.4 kbps	—	6.2	—	mA
		f = 868 MHz, 2-GFSK, 38.4 kbps	—	6.2	—	mA
		f = 868 MHz, GMSK, 500 kbps	—	7.1	—	mA
		f = 868 MHz, O-QPSK, 100 kbps	—	7.2	—	mA
		f = 433 MHz, 2-GFSK, 100 kbps	—	6.7	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P ¹	I _{RX_LISTEN}	f = 924 MHz, 4-GFSK, 400 kbps	—	7.0	—	mA
		f = 915 MHz, 2-GFSK, 2 Mbps	—	8.7	—	mA
		f = 915 MHz, O-QPSK, 4.8 kbps	—	6.3	—	mA
		f = 915 MHz, FSK, 50 kbps	—	6.7	—	mA
		f = 915 MHz, O-QPSK, 250 kbps	—	9.5	—	mA
		f = 868 MHz, 2-GFSK, 2.4 kbps	—	6.2	—	mA
		f = 868 MHz, 2-GFSK, 38.4 kbps	—	6.2	—	mA
		f = 868 MHz, GMSK, 500 kbps	—	7.2	—	mA
		f = 868 MHz, O-QPSK, 100 kbps	—	7.2	—	mA
		f = 433 MHz, 2-GFSK, 100 kbps	—	6.7	—	mA
Current consumption in transmit mode, VSCALE2, EM1	I _{TX}	f = 868 MHz, CW, 14 dBm PA, 0 dBm output power ²	—	13.2	—	mA
		f = 868 MHz, CW, 14 dBm PA, +10 dBm output power ²	—	21.8	—	mA
		f = 915 MHz, CW, 14 dBm PA, +14 dBm output power ³	—	41.3	—	mA
		f = 868.3 MHz, CW, 14 dBm PA, +14 dBm output power ³	—	40.2	—	mA

Note:

- EM1P operation is 0.35 mA lower than EM1 operation
- Using the +10 dBm matching network for 868/915/920 MHz Bands.
- Using the +14 dBm matching network for 868/915/920 MHz Bands.

4.7 Wake Up, Entry, and Exit times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz, with the DPLL disabled.

Table 4.11. Wake Up, Entry, and Exit times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
WakeupTime from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	HCLKs
		Code execution from RAM	—	1.43	—	μ s
WakeupTime from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.7	—	μ s
		Code execution from RAM, No Voltage Scaling	—	5.1	—	μ s
		Voltage scaling up one level ¹	—	37.8	—	μ s
		Voltage scaling up two levels ²	—	51.0	—	μ s
WakeupTime from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.7	—	μ s
		Code execution from RAM, No Voltage Scaling	—	5.1	—	μ s
		Voltage scaling up one level ¹	—	37.8	—	μ s
		Voltage scaling up two levels ²	—	51.0	—	μ s
WakeupTime from EM4	t_{EM4_WU}	Code execution from flash	—	31.0	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.29	—	μ s
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	5.9	—	μ s
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	5.7	—	μ s
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	10.7	—	μ s
Voltage scaling in time in EM0 ³	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	μ s
		Down from VSCALE2 to VSCALE1	—	172	—	μ s

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.8 Flash Characteristics

Table 4.12. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V
Flash data retention ¹	RET_{FLASH}		10	—	—	years
Flash erase cycles before failure ¹	EC_{FLASH}		10,000	—	—	cycles
Program Time	t_{PROG}	one word (32-bits)	41.4	43.5	45.6	μ s
		average per word over 128 words	10.4	10.9	11.4	μ s
Page Erase Time ²	t_{PERASE}		11.7	12.9	14	ms
Mass Erase Time ^{3 4}	t_{MERASE}	512 kB	47.9	50.4	52.8	ms
Program Current	I_{WRITE}	$T_A = 25\text{ }^\circ\text{C}$	—	—	2.4	mA
Page Erase Current	I_{ERASE}	$T_A = 25\text{ }^\circ\text{C}$	—	—	1.9	mA
Mass Erase Current	I_{MERASE}	$T_A = 25\text{ }^\circ\text{C}$	—	—	1.9	mA

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- Page Erase time is measured from setting the ERASEPAGE bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.
- Mass Erase is issued by the CPU and erases all of User space.
- Mass Erase time is measured from setting the ERASEMAIN0 bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.

4.9 Sub-GHz RF Transceiver Characteristics

4.9.1 RF Transmitter Characteristics

4.9.1.1 920 MHz Band +13 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 868/915/920 MHz 14 dBm matching network as shown in the typical connections section. Emissions are measured at 13 dBm and 0 dBm. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 924 MHz.

Table 4.13. 920 MHz Band +13 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		922.3	—	928.1	MHz
Maximum TX Power	$POUT_{MAX}$	PAVDD connected to DC-DC output, 14 dBm devices, 14 dBm match ¹²³	TBD	14.1	TBD	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-22.8	—	dBm
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR_V}$	$2.2\text{ V} < V_{REGVDD} < 3.8\text{ V}$, PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.01	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR_T}$	$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ with PAVDD connected to DC-DC output	—	0.6	1.0	dB
		$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$ with PAVDD connected to DC-DC output	—	0.8	1.4	dB
Output power variation vs RF frequency	$POUT_{VAR_F}$	PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.2	0.4	dB
Adjacent Channel Power 50 kbps GFSK ⁴	$P_{CH_ADJ_50}$	$P_{OUT} = 0\text{ dBm}$ (1 mW), 924 MHz, 200 kHz channel spacing	—	-35.0	-26	dBm
		$P_{OUT} = 13\text{ dBm}$ (20 mW), 924 MHz, 200 kHz channel spacing	—	-21.9	-15	dBm
Adjacent Channel Power 100 kbps GFSK ⁵	$P_{CH_ADJ_100}$	$P_{OUT} = 0\text{ dBm}$ (1 mW), 924 MHz, 400 kHz channel spacing	—	-35.7	-26	dBm
		$P_{OUT} = 13\text{ dBm}$ (20 mW), 924 MHz, 400 kHz channel spacing	—	-22.8	-15	dBm
Max spurious emissions, $P_{OUT} = 0\text{ dBm}$ (1 mW), 916MHz ⁶	$SPUR_{TX_ARIB_0}$	$f \leq 710\text{ MHz}$, RBW = 100 kHz	—	-74.6	-36	dBm
		$710\text{ MHz} < f \leq 900\text{ MHz}$, RBW = 1 MHz	—	-67.2	-55	dBm
		$900\text{ MHz} < f \leq 915\text{ MHz}$, RBW = 100 kHz	—	-77.1	-55	dBm
		$915\text{ MHz} < f \leq 930\text{ MHz}$, RBW = 100 kHz, (except for $ f-f_c \leq (200+100*n)\text{ kHz}$)	—	-49.3	-36	dBm
		$930\text{ MHz} < f \leq 1000\text{ MHz}$, RBW = 100 kHz	—	-78.2	-55	dBm
		$1000\text{ MHz} < f \leq 1215\text{ MHz}$, RBW = 1 MHz	—	-69.5	-45	dBm
		$1215\text{ MHz} < f$, RBW = 1 MHz	—	-46.4	-30	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max spurious emissions, $P_{OUT} = 13$ dBm (20 mW), 924 MHz ⁷	SPUR _{TX_ARIB_13}	$f \leq 710$ MHz, RBW = 100 kHz	—	-66.9	-36	dBm
		710 MHz < $f \leq 900$ MHz, RBW = 1 MHz	—	-55.5	-55	dBm
		900 MHz < $f \leq 915$ MHz, RBW = 100 kHz	—	-66.0	-55	dBm
		915 MHz < $f \leq 930$ MHz, RBW = 100 kHz, (except for $ f-f_c \leq (200+100*n)$ kHz)	—	-37.7	-36	dBm
		930 MHz < $f \leq 1000$ MHz, RBW = 100 kHz	—	-63.9	-55	dBm
		1000 MHz < $f \leq 1215$ MHz, RBW = 1 MHz	—	-57.4	-45	dBm
		1215 MHz < f , RBW = 1 MHz	—	-42.4	-30	dBm

Note:

- Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
- The transmit power for the 922.3 to 928.1 Band MHz is normally limited to +13 dBm (20 mW). For best efficiency at 13 dBm the 14 dBm devices are recommended with the 14 dBm match.
- The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. Emissions for this band are tested with the output power set to 13 dBm (20 mW) and 0 dBm (1mW).
- Measured per ARIB T108, Section 3.3, $f_c = 924$ MHz, 922.3 to 928.1 frequency band, 50 kbps, GFSK, $\Delta f = \pm 25$ kHz, BT=0.5, PN9 sequence, 200 kHz channel spacing, $n = 1$.
- Measured per ARIB T108, Section 3.3, $f_c = 924$ MHz, 922.3 to 928.1 frequency band, 100 kbps, GFSK, $\Delta f = \pm 25$ kHz, PN9 sequence, 400 kHz channel spacing, $n = 2$.
- Measured per ARIB T108, Part 2 Section 3.2, $f_c = 916$ MHz, 915.9 to 916.9 frequency band, 50 kbps, GFSK, $\Delta f = \pm 25$ kHz, PN9 sequence, 200 kHz channel spacing, $n = 1$.
- Measured per ARIB T108, Part 2 Section 3.2, $f_c = 924$ MHz, 922.3 to 928.1 frequency band, 50 kbps, GFSK, $\Delta f = \pm 25$ kHz, PN9 sequence, 200 kHz channel spacing, $n = 1$.

4.9.1.2 915 MHz Band +20 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +20 dBm using the 868/915/920 MHz +20 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = 1.8\text{ V}$ powered from DCDC. $PAVDD = 3.3\text{V}$. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 915 MHz.

Table 4.14. 915 MHz Band +20 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		902	—	928	MHz
Maximum TX Power	$POUT_{\text{MAX}}$	$PAVDD = 3.3\text{V}$, 20 dBm devices, +20 dBm match ^{1 2 3}	TBD	20	TBD	dBm
Minimum active TX Power	$POUT_{\text{MIN}}$		—	-20.6	—	dBm
Output power variation vs supply at $POUT_{\text{MAX}}$	$POUT_{\text{VAR}_V}$	$1.8\text{ V} < V_{PAVDD} < 3.8\text{ V}$, $T = 25\text{ }^\circ\text{C}$	—	4.7	—	dB
Output power variation vs temperature, peak to peak	$POUT_{\text{VAR}_T}$	$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ with $PAVDD = 3.3\text{ V}$	—	0.6	1.0	dB
		$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$ with $PAVDD = 3.3\text{ V}$	—	1.0	1.4	dB
Output power variation vs RF frequency	$POUT_{\text{VAR}_F}$	$PAVDD = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$	—	0.5	0.9	dB
Spurious emissions of harmonics, Conducted measurement, Test Frequency = 915 MHz	$SPUR_{\text{HARM_FCC}}$	In non-restricted bands, per FCC 47 CFR §15.247 ⁴	—	-58.3	-20	dBc
		In restricted bands, per FCC 47 CFR §15.205 & §15.209 ⁵⁶	—	-50.2	-41.2	dBm
Unwanted signal emissions over frequency domain, Conducted measurement, Test Frequency = 915 MHz	$SPUR_{\text{OOB_FCC}}$	In non-restricted bands, per FCC 47 CFR §15.247 ⁴	—	-60.0	-20	dBc
		In restricted bands (30-88 MHz), per FCC 47 CFR §15.205 & §15.209 ^{5 6}	—	-62.7	-55.2	dBm
		In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209 ^{5 6}	—	-60.7	-51.7	dBm
		In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209 ^{5 6}	—	-61.1	-49.2	dBm
		In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209 ^{5 6}	—	-50.6	-41.2	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
<ol style="list-style-type: none"> 1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table. 2. The transmit power for the 902 MHz to 928 Band MHz is normally supports +20 dBm or higher when frequency hopping or DSSS is used. Only the +20 dBm devices are recommended with the +20 dBm match. 3. The 20 dBm match is optimized for best efficiency at maximum power. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 20 dBm. 4. FCC Title 47 CFR Part 15 Section 15.247 Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz. 5. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation. 6. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements. 						

4.9.1.3 915 MHz Band +14 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 868/915/920 MHz 14 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{\text{REGVDD}} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 915 MHz.

Table 4.15. 915 MHz Band +14 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		902	—	928	MHz
Maximum TX Power	$POUT_{\text{MAX}}$	PAVDD connected to DC-DC output, 14 dBm devices, 14 dBm match ^{1 2}	TBD	14.3	TBD	dBm
Minimum active TX Power	$POUT_{\text{MIN}}$		—	-22.7	—	dBm
Output power variation vs supply at $POUT_{\text{MAX}}$	$POUT_{\text{VAR}_V}$	$2.2\text{ V} < V_{\text{REGVDD}} < 3.8\text{ V}$, PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.01	—	dB
Output power variation vs temperature, peak to peak	$POUT_{\text{VAR}_T}$	$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ with PAVDD connected to DC-DC output	—	0.6	0.9	dB
		$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$ with PAVDD connected to DC-DC output	—	0.8	1.4	dB
Output power variation vs RF frequency	$POUT_{\text{VAR}_F}$	PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.6	0.9	dB
Spurious emissions of harmonics, Conducted measurement, Test Frequency = 915 MHz	$SPUR_{\text{HARM}_FCC}$	In non-restricted bands, per FCC 47 CFR §15.247 ³	—	-67.6	-20	dBc
		In restricted bands, per FCC 47 CFR §15.205 & §15.209 ⁴⁵	—	-53.5	-41.2	dBm
Unwanted signal emissions over frequency domain, Conducted measurement, Test Frequency = 915 MHz	$SPUR_{\text{OOB}_FCC}$	In non-restricted bands, per FCC 47 CFR §15.247 ³	—	-68.0	-20	dBc
		In restricted bands (30-88 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5}	—	-68.3	-55.2	dBm
		In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5}	—	-68.3	-51.7	dBm
		In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5}	—	-68.1	-49.2	dBm
		In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209 ^{4 5}	—	-56.4	-41.2	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 14 dBm.
3. FCC Title 47 CFR Part 15 Section 15.247 Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz.
4. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
5. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

4.9.1.4 868 MHz Band +20 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +20 dBm using the 868/915/920 MHz +20 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = 1.8\text{ V}$ powered from DCDC. $PAVDD = 3.3\text{V}$. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 869.5 MHz.

Table 4.16. 868 MHz Band +20 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		869.4	—	869.65	MHz
Maximum TX Power	$POUT_{\text{MAX}}$	$PAVDD = 3.3\text{V}$, 20 dBm devices, +20 dBm match ^{1 2}	TBD	20.3	TBD	dBm
Minimum active TX Power	$POUT_{\text{MIN}}$		—	-20.4	—	dBm
Output power variation vs supply at $POUT_{\text{MAX}}$	$POUT_{\text{VAR}_V}$	$1.8\text{ V} < V_{PAVDD} < 3.8\text{ V}$, $T = 25\text{ }^\circ\text{C}$	—	4.4	—	dB
Output power variation vs temperature, peak to peak	$POUT_{\text{VAR}_T}$	$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$, $PAVDD = 3.3\text{ V}$	—	0.5	0.8	dB
		$T_A = -40\text{ to }+125\text{ }^\circ\text{C}$, $PAVDD = 3.3\text{ V}$	—	0.8	1.2	dB
Output power variation vs RF frequency	$POUT_{\text{VAR}_F}$	$PAVDD = 3.3\text{ V}$, $T = 25\text{ }^\circ\text{C}$	—	0.02	0.08	dB
Spurious emissions of harmonics, +20 dBm match, $P_{\text{OUT}} = +20\text{ dBm}$, 869.5 MHz	$SPUR_{\text{HARM_ETSI}}$	(frequencies above 1 GHz) ³	—	-39.5	-30	dBm
Unwanted emissions in spurious domain, Per ETSI EN 300-220-1 ⁴ , +20 dBm match, $P_{\text{OUT}} = +20\text{ dBm}$, 869.5 MHz	$SPUR_{\text{OOB_ETSI}}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ³	—	-60.3	-54	dBm
		(other frequencies below 1 GHz) ³	—	-56.9	-36	dBm
		(frequencies above 1 GHz) ³	—	-52.1	-30	dBm
Error Vector Magnitude, per 802.15.4-2020	EVM	Signal is 100 kbps DSSS-OQPSK reference packet. Modulated according to 802.15.4-2020 in the 868MHz band, with pseudo-random packet data content. $P_{\text{OUT}} = +20\text{ dBm}$.	—	6.1	35	%

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 20 dBm match is optimized for best efficiency at 20 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 20 dBm.
3. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1

4.9.1.5 868 MHz Band +14 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 868/915/920 MHz +14 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{\text{REGVDD}} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 868.3 MHz.

Table 4.17. 868 MHz Band +14 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		863	—	869.2	MHz
Maximum TX Power	$POUT_{\text{MAX}}$	PAVDD connected to DC-DC output, 14 dBm devices, 14 dBm match ^{1 2}	TBD	14.5	TBD	dBm
Minimum active TX Power	$POUT_{\text{MIN}}$		—	-22.1	—	dBm
Output power variation vs supply at $POUT_{\text{MAX}}$	$POUT_{\text{VAR}_V}$	$2.2\text{ V} < V_{\text{REGVDD}} < 3.8\text{ V}$, PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.01	—	dB
Output power variation vs temperature, peak to peak	$POUT_{\text{VAR}_T}$	$T_A = -40\text{ to }+85\text{ }^\circ\text{C}$ with PAVDD connected to DC-DC output	—	0.4	0.8	dB
Output power variation vs RF frequency	$POUT_{\text{VAR}_F}$	PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.04	0.1	dB
Spurious emissions of harmonics, +14 dBm match, $P_{\text{OUT}} = +14\text{ dBm}$, 868.3 MHz	$SPUR_{\text{HARM_ETSI}}$	(frequencies above 1 GHz) ³	—	-42.5	-30	dBm
Unwanted emissions in spurious domain, Per ETSI EN 300-220-1 ⁴ , +14 dBm match, $P_{\text{OUT}} = +14\text{ dBm}$, 868.3 MHz	$SPUR_{\text{OOB_ETSI}}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ³	—	-67.0	-54	dBm
		(other frequencies below 1 GHz) ³	—	-64.2	-36	dBm
		(frequencies above 1 GHz) ³	—	-58.9	-30	dBm
Error Vector Magnitude, per 802.15.4-2020	EVM	Signal is 100 kbps DSSS-OQPSK reference packet. Modulated according to 802.15.4-2020 in the 868MHz band, with pseudo-random packet data content. $P_{\text{OUT}} = +14\text{ dBm}$.	—	6.0	35	%

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The 14 dBm match is optimized for best efficiency at 14 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 14 dBm.
3. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1

4.9.1.6 470 MHz Band +17 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +17 dBm usnig the 470 MHz Band +17 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = 1.8\text{ V}$ powered from DCDC. $PAVDD = 3.3\text{V}$. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 490 MHz.

Table 4.18. 470 MHz Band +17 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		470	—	510	MHz
Maximum TX Power	$POUT_{MAX}$	$PAVDD = 3.3\text{V}$, 20 dBm devices, +17 dBm match ¹²³	TBD	18.2	TBD	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-16.7	—	dBm
Output power variation vs supply, peak to peak	$POUT_{VAR_V}$	$1.8\text{ V} < V_{PAVDD} < 3.8\text{ V}$, $T = 25\text{ }^\circ\text{C}$	—	4.5	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR_T}$	-40 to +85 °C at 17 dBm	—	0.6	1.0	dB
Output power variation vs RF frequency	$POUT_{VAR_F}$	$T = 25\text{ }^\circ\text{C}$	—	0.7	1.0	dB
Harmonic emissions, +17 dBm Match, $P_{OUT} = +17\text{ dBm}$, 490 MHz	$SPUR_{HARM_CN}$	Per China SRW Requirement, Section 2.1, frequencies below 1GHz	—	-56.5	-36	dBm
		Per China SRW Requirement, Section 2.1, frequencies above 1GHz	—	-47.4	-30	dBm
Spurious emissions, +17 dBm Match, $P_{OUT} = +17\text{ dBm}$, 490 MHz	$SPUR_{OOB_CN}$	Per China SRW Requirement, Section 3 (48.5-72.5MHz, 76-108MHz, 167-223MHz, 470-556MHz, and 606-798MHz)	—	-72.6	-54	dBm
		Per China SRW Requirement, Section 2.1 (other frequencies below 1GHz)	—	-57.0	-36	dBm
		Per China SRW Requirement, Section 2.1 (frequencies above 1GHz)	—	-48.0	-30	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. The +17 dBm match is optimized for best efficiency at +17 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to +17 dBm.
3. Specific regional requirements for this band normally limit the maximum Tx power in this band to +17 dBm or less. Only the 20 dBm part numbers are recommended for this band.

4.9.1.7 433 MHz Band +10 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 433 MHz 10 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{\text{REGVDD}} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 433.92 MHz.

Table 4.19. 433 MHz Band +10 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		433	—	434.79	MHz
Maximum TX Power	$POUT_{\text{MAX}}$	PAVDD connected to DC-DC output, 14 dBm devices, 10dBm match ¹²³	TBD	12.3	TBD	dBm
Minimum active TX Power	$POUT_{\text{MIN}}$		—	-19.1	—	dBm
Output power variation vs supply, peak to peak, $P_{\text{out}} = 10\text{dBm}$	$POUT_{\text{VAR}_V}$	$2.2\text{ V} < V_{\text{REGVDD}} < 3.8\text{ V}$, PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.01	—	dB
Output power variation vs temperature, peak to peak, $P_{\text{out}} = 10\text{dBm}$	$POUT_{\text{VAR}_T}$	-40 to +85C at 10dBm	—	0.5	0.9	dB
Output power variation vs RF frequency, $P_{\text{out}} = 10\text{dBm}$	$POUT_{\text{VAR}_F}$	$T = 25\text{ }^\circ\text{C}$	—	0.06	0.09	dB
Unwanted emissions in spurious domain, Per ETSI EN 300-220-1 ⁴ , +10 dBm match, $P_{\text{OUT}} = +10\text{ dBm}$, 433.92 MHz	$SPUR_{\text{OOB_ETSI}}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ⁵	—	-70.1	-54	dBm
		(other frequencies below 1 GHz) ⁵	—	-69.0	-36	dBm
		(frequencies above 1 GHz) ⁵	—	-45.3	-30	dBm
Spurious emissions of harmonics ETSI, Conducted measurement, +10 dBm match, $P_{\text{OUT}} = +10\text{ dBm}$, 433.92 MHz	$SPUR_{\text{HARM_ETSI}}$	(other frequencies below 1 GHz) ⁵	—	-58	-36	dBm
		(frequencies above 1 GHz) ⁵	—	-48.5	-30	dBm
Spurious emissions of harmonics FCC, Conducted measurement, +10 dBm match, $P_{\text{OUT}} = 10\text{ dBm}$, 433.0 MHz ⁶	$SPUR_{\text{HARM_FCC}}$	Per FCC 47 CFR §15.205 & §15.209 ^{7 8 9}	—	-48.2	-41.2	dBm
Spurious emissions out-of-band FCC, Conducted measurement, +10 dBm match, $P_{\text{OUT}} = 10\text{ dBm}$, 433.0 MHz ⁶	$SPUR_{\text{OOB_FCC}}$	30-88 MHz, per FCC 47 CFR §15.205 & §15.209 ^{7 8 9}	—	-68.8	-55.2	dBm
		88-216 MHz, per FCC 47 CFR §15.205 & §15.209 ^{7 8 9}	—	-69.8	-51.7	dBm
		216-960 MHz, per FCC 47 CFR §15.205 & §15.209 ^{7 8 9}	—	-66.7	-49.2	dBm
		>960 MHz, per FCC 47 CFR §15.205 & §15.209 ^{7 8 9}	—	-75.3	-41.2	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. Using the +10 dBm matching network for the 433 MHz Band. The 10 dBm match is optimized for best efficiency at 10 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 10 dBm.
3. Specific regional requirements for this band normally limit the maximum Tx power in this band to 10 dBm or less. Only the 14 dBm part numbers are recommended for this band.
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1
5. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2
6. FCC emissions are specified at a power level of 10 dBm conducted. A lower power setting may be required to meet the FCC limit specified in μV at 3m.
7. FCC Title 47 CFR Part 15 Section 15.231 Periodic operation in the band 40.66-40.70 MHz and above 70 MHz.
8. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
9. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

4.9.1.8 315 MHz Band +10 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +14 dBm using the 315 MHz +10 dBm matching network as shown in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 315 MHz.

Table 4.20. 315 MHz Band +10 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		314	—	315	MHz
Maximum TX Power	$POUT_{MAX}$	PAVDD connected to DC-DC output, 14 dBm devices, 10dBm match ¹²³	TBD	12.6	TBD	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-20.0	—	dBm
Output power variation vs supply	$POUT_{VAR_V}$	$2.2\text{ V} < V_{REGVDD} < 3.8\text{ V}$, PAVDD connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0.01	—	dB
Output power variation vs temperature	$POUT_{VAR_T}$	-40 to +85C	—	0.4	1.0	dB
Output power variation vs RF frequency	$POUT_{VAR_F}$	$T = 25\text{ }^\circ\text{C}$	—	0.1	0.14	dB
Spurious emissions of harmonics, 10 dBm match, $P_{OUT} = +10\text{ dBm}$, 315.0 MHz ⁴	$SPUR_{HARM_FCC}$	Per FCC 47 CFR §15.205 & §15.209 ^{5 6 7}	—	-48.2	-49.2	dBm
Spurious emissions out-of-band, +10dBm match, $P_{OUT} = +10\text{ dBm}$, 315.0 MHz ⁴	$SPUR_{OOB_FCC}$	30-88 MHz, per FCC 47 CFR §15.205 & §15.209 ^{5 6 7}	—	-68.9	-55.2	dBm
		88-216 MHz, per FCC 47 CFR §15.205 & §15.209 ^{5 6 7}	—	-70.5	-51.7	dBm
		216-960 MHz, per FCC 47 CFR §15.205 & §15.209 ^{5 6 7}	—	-67.5	-49.2	dBm
		>960 MHz, per FCC 47 CFR §15.205 & §15.209 ^{5 6 7}	—	-77.6	-41.2	dBm

Note:

- Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
- Using the +10 dBm matching network for the 315 MHz Band. The 10 dBm match is optimized for best efficiency at 10 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 10 dBm.
- The transmit power for the 314MHz to 316 Band MHz is normally limited to +10 dBm. Only 14 dBm part numbers are recommended for this band.
- FCC emissions are specified at a power level of 10 dBm conducted. A lower power setting may be required to meet the FCC limit specified in μV at 3m.
- FCC Title 47 CFR Part 15 Section 15.231 Periodic operation in the band 40.66-40.70 MHz and above 70 MHz.
- FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
- FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

4.9.1.9 169 MHz Band +20 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +20 dBm using the 169 MHz +20 dBm matching network in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = 1.8\text{ V}$ powered from DCDC. $PAVDD = 3.3\text{V}$. Crystal frequency= 39.0 MHz. RFVDD and PAVDD paths filtered using ferrites. RF center frequency 169.4375 MHz. Conducted emissions.

Table 4.21. 169 MHz Band +20 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		169.4	—	169.475	MHz
Maximum TX Power	$POUT_{MAX}$	$PAVDD = 3.3\text{V}$, 20 dBm devices, +20 dBm match ¹²³ , Min / Max at 25C, 3.3V PAVDD	TBD	21.2	TBD	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-19.9	—	dBm
Output power variation vs supply, peak to peak	$POUT_{VAR_V}$	$1.8\text{ V} < V_{PAVDD} < 3.8\text{ V}$, $T = 25\text{ }^\circ\text{C}$	—	4.5	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR_T}$	-40 to +85 °C at 20 dBm	—	0.5	1.0	dB
Unwanted emissions in spurious domain, Per ETSI EN 300-220-1 ⁴ , $PAVDD = 3.3\text{ V}$, $P_{OUT} = 20\text{ dBm}$, 169.4375 MHz	$SPUR_{OOB_ETSI}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ⁵	—	-60.9	-54	dBm
		(other frequencies below 1 GHz) ⁵	—	-59.6	-36	dBm
		(frequencies above 1 GHz) ⁵	—	-63.5	-30	dBm
Spurious emissions harmonics, Per ETSI EN 300-220-1 ⁴ , $PAVDD = 3.3\text{ V}$, $P_{OUT} = 20\text{ dBm}$, 169.4375 MHz	$SPUR_{HARM_ETSI}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ⁵	—	-68.6	-54	dBm
		(other frequencies below 1 GHz) ⁵	—	-40.7	-36	dBm
		(frequencies above 1 GHz) ⁵	—	-68.3	-30	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. Using the +20 dBm matching network for the 169 MHz Band. The 20 dBm match is optimized for best efficiency at 20 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 20 dBm.
3. The transmit power for the 169.4 MHz to 169.475 Band MHz is normally limited to +27 dBm. Only 20 dBm part numbers are recommended for this band.
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1
5. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2

4.9.1.10 169 MHz Band +10 dBm RF Transmitter Characteristics

This table is for devices with a output power rating of +10 dBm using the 169 MHz +10 dBm matching network in the typical connections section. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = 1.8\text{ V}$ powered from DCDC. $PAVDD = 3.3\text{V}$. Crystal frequency= 39.0 MHz. RFVDD and PAVDD paths filtered using ferrites. RF center frequency 169.7 MHz. Conducted emissions.

Table 4.22. 169 MHz Band +10 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		169.5875	—	169.8125	MHz
Maximum TX Power	$POUT_{MAX}$	$PAVDD = 3.3\text{V}$, 14 dBm devices, +10 dBm match ¹²³	TBD	12.1	TBD	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-18.4	—	dBm
Output power variation vs supply, peak to peak	$POUT_{VAR_V}$	$2.2\text{ V} < V_{VREGVDD} < 3.8\text{ V}$, $PAVDD$ connected to DC-DC output, $T = 25\text{ }^\circ\text{C}$	—	0	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR_T}$	-40 to +85 °C at 10 dBm	—	0.7	0.5	dB
Unwanted emissions in spurious domain, Per ETSI EN 300-220-1 ⁴ , $PAVDD = 3.3\text{ V}$, $P_{OUT} = 10\text{ dBm}$, 169.7 MHz	$SPUR_{OOB_ETSI}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ⁵	—	-70.1	-54	dBm
		(other frequencies below 1 GHz) ⁵	—	-69.6	-36	dBm
		(frequencies above 1 GHz) ⁵	—	-63.5	-30	dBm
Spurious emissions harmonics, Per ETSI EN 300-220-1 ⁴ , $PAVDD = 3.3\text{ V}$, $P_{OUT} = 10\text{ dBm}$, 169.7 MHz	$SPUR_{HARM_ETSI}$	(47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz) ⁵	—	-61.3	-54	dBm
		(other frequencies below 1 GHz) ⁵	—	-51.2	-36	dBm
		(frequencies above 1 GHz) ⁵	—	-72.8	-30	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
2. Using the +10 dBm matching network for the 169 MHz Band. The 10 dBm match is optimized for best efficiency at 10 dBm. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 10 dBm.
3. The transmit power for the 169.5875 MHz to 169.8125 Band MHz is normally limited to +10 dBm. Only 14 dBm part numbers are recommended for this band.
4. Conducted measurement per EN 300-220-1 v3.1.1 5.9.3.3.1
5. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2

4.9.2 RF Receiver Characteristics

4.9.2.1 920 MHz Band RF Receiver Characteristics

Band is 920 to 928 MHz. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 924.0 MHz.

Table 4.23. 920 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		920	—	928	MHz
Max usable input level, PER 10%	SAT_{400K}	Desired is reference 400 kbps 4FSK signal ¹	—	—	10.0	dBm
Sensitivity	SENS	Desired is reference 50 kbps GFSK signal, $\Delta f = \pm 25\text{ kHz}$, PER<10% ²	—	-110.1	-109.2	dBm
		Desired is reference 100 kbps GFSK signal, $\Delta f = \pm 50\text{ kHz}$, PER<10% ³	—	-107.1	-106.2	dBm
		Desired is reference 400 kbps 4FSK signal, $\Delta f_o = \pm 200\text{ kHz}$, PER<10% ¹	—	-98.6	-97.7	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I_1	Desired is 50 kbps GFSK signal ² at 3dB above sensitivity level	—	44.2	—	dB
		Desired is 100 kbps GFSK signal ³ at 3dB above sensitivity level	—	45.6	—	dB
		Desired is reference 400 kbps 4FSK signal, $\Delta f_o = \pm 200\text{ kHz}$ ¹ at 3dB above sensitivity level	—	41.2	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I_2	Desired is 50 kbps GFSK signal ² at 3dB above sensitivity level	—	51.4	—	dB
		Desired is 100 kbps GFSK signal ³ at 3dB above sensitivity level	—	56.7	—	dB
		Desired is reference 400 kbps 4FSK signal, $\Delta f_o = \pm 200\text{ kHz}$, PER<10% ¹	—	51.2	—	dB
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 50 kbps GFSK signal ² at 3dB above sensitivity level	—	44.9	—	dB
		Desired is 100 kbps GFSK signal ³ at 3dB above sensitivity level	—	45.7	—	dB
		Desired is reference 400 kbps 4FSK signal, $\Delta f_o = \pm 200\text{ kHz}$, PER<10% ¹	—	40.5	—	
Blocking selectivity, 10% PER. Desired is 100 kbps GFSK signal at 3dB above sensitivity level	C/I_{BLOCKER}	Interferer CW at Desired $\pm 1\text{ MHz}$	—	59.6	—	dB
		Interferer CW at Desired $\pm 2\text{ MHz}$	—	66.4	—	dB
		Interferer CW at Desired $\pm 10\text{ MHz}$	—	78.3	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermod selectivity, 10% PER. CW interferers at 400 kHz and 800 kHz offsets	C/I_{IM}	Desired is 100 kbps FSK signal ³ at 3dB above sensitivity level	—	45.4	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	10	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-99	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dB
Max spurious emissions during active receive mode, per ARIB STD-T108 Section 3.3	$SPUR_{RX_ARIB}$	Below 710 MHz, RBW=100kHz	—	-84.4	-54	dBm
		710-900 MHz, RBW=1MHz	—	-71.3	-55	dBm
		900-915 MHz, RBW=100kHz	—	-86.3	-55	dBm
		915-930 MHz, RBW=100kHz	—	-86.0	-54	dBm
		930-1000 MHz, RBW=100kHz	—	-85.3	-55	dBm
		Above 1000 MHz, RBW=1MHz	—	-67.3	-47	dBm

Note:

1. Definition of reference signal is 400 kbps 4FSK, $\Delta f_o = \pm 100$ kHz, $\Delta f_i = \pm 33.3$ kHz, Channel Spacing = 600 kHz, PER<10%, Data Whitening, no FEC, Per IEEE 802.15.4g 920 MHz band, mode 4.
2. Definition of reference signal is 50 kbps GFSK, $m_i = 0.5$, BT = 2.0, Channel Spacing = 200 kHz, PER<10%, Data Whitening, no FEC. Per WiSun ECHONET PHY 1.0 standard mode #1b.
3. Definition of reference signal is 100 kbps GFSK, $m_i = 1.0$, BT = 2.0, Channel Spacing = 400 kHz, PER<10%, Data Whitening, no FEC. Per WiSun ECHONET PHY 1.0 standard mode #2b.

4.9.2.2 915 MHz Band RF Receiver Characteristics

Band is 902 to 928 MHz. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 915 MHz.

Table 4.24. 915 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		902	—	928	MHz
Max usable input level, 0.1% BER	SAT_{2M}	Desired is reference 2 Mbps GFSK signal ¹	—	—	10	dBm
Sensitivity	SENS	Desired is reference 4.8 kbps OOK signal ² , PER<20%	—	-113.1	—	dBm
		Desired is reference 50 kbps FSK signal, $\Delta f = \pm 25\text{ kHz}$, PER<10% ³	—	-110.1	—	dBm
		Desired is reference 50 kbps FSK signal, $\Delta f = \pm 25\text{ kHz}$, PER<10% with FEC ⁴	—	-114.2	—	dBm
		Desired is reference 150 kbps FSK signal, $\Delta f = \pm 37.5\text{ kHz}$, PER<10% ⁵	—	-107.5	—	dBm
		Desired is reference 2 Mbps GFSK signal, $\Delta f = \pm 500\text{ kHz}$, BER<0.1% ¹	—	-96.9	—	dBm
		Desired is reference 4.8 kbps OQPSK signal, spreading factor=8, PER<1% ⁶	—	-125.8	—	dBm
		Desired is reference 250 kbps O-QPSK DSSS signal, PER<1% ⁷	—	-103.5	—	dBm
		Desired is reference 120 kbps OOK signal ⁸ , PER<20%	—	-102.6	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I_1	Desired is 4.8 kbps OOK signal ² at 3dB above sensitivity level	—	49.6	—	dB
		Desired is 50 kbps FSK signal ³ at 3dB above sensitivity level	—	44.1	—	dB
		Desired is 150 kbps FSK signal ⁵ at 3dB above sensitivity level	—	43.8	—	dB
		Desired is reference 250 kbps O-QPSK DSSS signal ⁷ at 3dB above sensitivity level	—	46.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 4.8 kbps OOK signal ² at 3dB above sensitivity level	—	64.0	—	dB
		Desired is 50 kbps FSK signal ³ at 3dB above sensitivity level	—	51.5	—	dB
		Desired is 150 kbps FSK signal ⁵ at 3dB above sensitivity level	—	57.7	—	dB
		Desired is reference 250 kbps O-QPSK DSSS signal ⁷ at 3dB above sensitivity level	—	50.7	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 4.8 kbps OOK signal ² at 3dB above sensitivity level	—	43.0	—	dB
		Desired is 50 kbps FSK signal ³ at 3dB above sensitivity level	—	44.0	—	dB
		Desired is 150 kbps FSK signal ⁵ at 3dB above sensitivity level	—	44.5	—	dB
		Desired is reference 250 kbps O-QPSK DSSS signal ⁷ at 3dB above sensitivity level	—	52.3	—	dB
Blocking selectivity, PER < 10%. Desired is 50 kbps GFSK signal at 3dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	63.9	—	dB
		Interferer CW at Desired ± 2 MHz	—	71.3	—	dB
		Interferer CW at Desired ± 10 MHz	—	81.4	—	dB
Intermod selectivity, PER < 10%. CW interferers at 400 kHz and 800 kHz offsets	C/I _{IM}	Desired is 50 kbps GFSK signal ³ at 3dB above sensitivity level	—	48.2	—	dB
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	10.0	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-97.0	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dB
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216-960 MHz	—	-81.7	-49.2	dBm
		Above 960 MHz	—	-78.7	-41.2	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. The modulation bandwidth may not be suitable for regional regulatory requirements in this band. Crystal tolerance = 0 ppm.						
2. Definition of reference signal is 4.8 kbps Manchester-encoded OOK, RX channel BW = 350 kHz, channel spacing = 500 kHz.						
3. Definition of reference signal is 50 kbps filtered FSK, $m_i = 1.0$, $BT = 2.0$, Channel Spacing = 200 kHz, PER<10%, Data Whitening, no FEC. Per WiSun PHY 1.0 standard mode #1b.						
4. Definition of reference signal is 50 kbps filtered FSK, $m_i = 1.0$, $BT = 2.0$, PER<10%, Data Whitening, NRNSC FEC with interleaving. Per IEEE 802.15.4g. Per WiSun FAN PHY 1.0 standard mode #1b.						
5. Definition of reference signal is 150 kbps filtered FSK, $m_i = 0.5$, $BT = 2.0$, Channel Spacing = 400 kHz, PER<10%, Data Whitening, no FEC. Per WiSun FAN PHY 1.0 standard mode #3.						
6. Definition of reference signal is 4.8 kbps O-QPSK DSSS long-range PHY, 38.4 kcps chip rate, chipping code length 32, PER<1%. Crystal tolerance = 0 ppm.						
7. Definition of reference signal is O-QPSK DSSS, Data rate = 250 kbps, 32-chip PN sequence mapping, <1% PER, Channel Spacing = 2 MHz, payload length=20 octets. Crystal tolerance = 0 ppm.						
8. Definition of reference signal is 120 kbps OOK, RX channel BW = 350 kHz, channel spacing = 500 kHz.						

4.9.2.3 868 MHz Band RF Receiver Characteristics

Band is 868 to 870 MHz. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 868.3 MHz.

Table 4.25. 868 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		863	—	870	MHz
Max usable input level, 0.1% BER	SAT_{500k}	Desired is reference 500 kbps GFSK signal ¹	—	—	10.0	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal, $\Delta f = \pm 1.2\text{ kHz}$, BER < 0.1% ²	—	-125.3	—	dBm
		Desired is 38.4 kbps GFSK signal ³ $\Delta f = \pm 20\text{ kHz}$, BER < 0.1%	—	-113.3	—	dBm
		Desired is reference 50 kbps FSK, $\Delta f = \pm 12.5\text{ kHz}$, PER < 10% ⁴	—	-111.8	—	dBm
		Desired is reference 100 kbps FSK, $\Delta f = \pm 25\text{ kHz}$, PER < 10% ⁵	—	-109.2	—	dBm
		Desired is reference 100 kbps O-QPSK DSSS signal, PER < 1% ⁶	—	-110.9	—	dBm
		Desired is reference 500 kbps GFSK signal, $\Delta f = \pm 125\text{ kHz}$ ¹ , BER < 0.1% ⁷	—	-103.2	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I_1	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	-43.9	—	dBm
		Desired is 38.4 kbps GFSK signal ³ at 3dB above sensitivity level	—	45.0	—	dB
		Desired is reference 50 kbps FSK, $\Delta f = \pm 12.5\text{ kHz}$, ⁴ at 3dB above sensitivity level	—	45.1	—	dB
		Desired is reference 100 kbps FSK, $\Delta f = \pm 25\text{ kHz}$, ⁵ at 3dB above sensitivity level	—	44.2	—	dB
		Desired is reference 100 kbps O-QPSK DSSS signal ⁶ at 3dB above sensitivity level	—	57.4	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	-44.4	—	dBm
		Desired is 38.4 kbps GFSK signal ³ at 3dB above sensitivity level	—	37.9	—	dB
		Desired is reference 50 kbps FSK, $\Delta f = \pm 12.5$ kHz, ⁴ at 3dB above sensitivity level	—	44.0	—	dB
		Desired is reference 100 kbps FSK, $\Delta f = \pm 25$ kHz, ⁵ at 3dB above sensitivity level	—	51.2	—	dB
		Desired is reference 100 kbps O-QPSK DSSS signal ⁶ at 3dB above sensitivity level	—	65.7	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	-51.0	—	dBm
		Desired is 38.4 kbps GFSK signal ³ at 3dB above sensitivity level	—	38.0	—	dB
		Desired is reference 50 kbps FSK, $\Delta f = \pm 12.5$ kHz, ⁴ at 3dB above sensitivity level	—	45.4	—	dB
		Desired is reference 100 kbps FSK, $\Delta f = \pm 25$ kHz, ⁵ at 3dB above sensitivity level	—	44.9	—	dB
		Desired is reference 100 kbps O-QPSK DSSS signal ⁶ at 3dB above sensitivity level	—	50.3	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ² at 3 dB above sensitivity level	C/I _{BLOCKER_24}	Interferer CW at Desired ± 2 MHz	—	-17.0	—	dBm
		Interferer CW at Desired ± 10 MHz	—	-6.7	—	dBm
		Interferer CW at Desired ± 43.4 MHz	—	-4.5	—	dBm
Blocking selectivity, 10% PER. Desired is 50 kbps GFSK signal ⁴ at 3 dB above sensitivity level	C/I _{BLOCKER_50}	Interferer CW at Desired ± 1 MHz	—	66.5	—	dB
		Interferer CW at Desired ± 2 MHz	—	73.7	—	dB
		Interferer CW at Desired ± 10 MHz	—	83.1	—	dB
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	10	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-103	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dB
Max spurious emissions during active receive mode	SPUR _{RX}	30 MHz to 1 GHz	—	-81.7	-57	dBm
		1 GHz to 12 GHz	—	-71.7	-47	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. Definition of reference signal is 500 kbps 2GMSK, BT=0.5, $\Delta f = \pm 125$ kHz, RX channel BW = 753.320 kHz. Crystal tolerance = 0 ppm.						
2. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, $\Delta f = \pm 1.2$ kHz, RX channel BW = 10 kHz, channel spacing = 25 kHz.						
3. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, $\Delta f = \pm 20$ kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz. Crystal tolerance = 0 ppm.						
4. Definition of reference signal is 50 kbps filtered FSK, $m_i = 0.5$, BT = 2.0, Channel Spacing = 100 kHz, PER<10%, Data Whitening, no FEC. Per WiSun FAN PHY 1.0 standard mode #1a.						
5. Definition of reference signal is 100 kbps filtered FSK, $m_i = 0.5$, BT = 2.0, Channel Spacing = 200 kHz, PER<10%, Data Whitening, no FEC. Per WiSun FAN PHY 1.0 standard mode #2a.						
6. Definition of reference signal is O-QPSK DSSS per IEEE802.15.4, Data rate = 100 kbps, 4 bit to 16 chip PN sequence mapping, <1% PER, Channel Spacing = 2 MHz, payload length=20 octets.						
7. The modulation bandwidth may not be suitable for regional regulatory requirements in this band. Crystal tolerance = 0 ppm.						

4.9.2.4 470 MHz Band RF Receiver Characteristics

Band is 470 to 510 MHz. Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = External PA Supply. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency=39MHz. RF center frequency 490 MHz.

Table 4.26. 470 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F _{RANGE}		470	—	510	MHz
Max usable input level, 10% PER	SAT _{100k}	Desired is reference 100 kbps FSK signal ¹	—	—	10	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal ² , 0.1% BER	—	-126.7	—	dBm
		Desired is reference 50 kbps FSK signal ³ , 10% PER	—	-111.4	—	dBm
		Desired is reference 100 kbps FSK signal ¹ , 10% PER	—	-110.5	—	dBm
		Desired is reference 4.8 kbps OQPSK signal, spreading factor=8, PER<1% ⁴	—	-126.4	—	dBm
		Desired is reference 9.6 kbps OQPSK signal, spreading factor=8, PER<1% ⁵	—	-123.2	—	dBm
		Desired is reference 10 kbps GFSK signal ⁶ , 0.1% BER	—	-120.6	—	dBm
Adjacent channel selectivity, Interferer is CW at ± 1 × channel-spacing	C/I ₁	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	62.1	—	dB
		Desired is reference 50 kbps FSK signal ³ at 3dB above sensitivity level	—	48.1	—	dB
		Desired is reference 100 kbps FSK signal ¹ at 3dB above sensitivity level	—	46.4	—	dB
Alternate channel selectivity, Interferer is CW at ± 2 × channel-spacing	C/I ₂	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	61.7	—	dB
		Desired is reference 50 kbps FSK signal ³ at 3dB above sensitivity level	—	56.1	—	dB
		Desired is reference 100 kbps FSK signal ¹ at 3dB above sensitivity level	—	55.3	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	53.3	—	dB
		Desired is reference 50 kbps FSK signal ³ at 3dB above sensitivity level	—	47.8	—	dB
		Desired is reference 100 kbps FSK signal ¹ at 3dB above sensitivity level	—	46.7	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ² at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired \pm 1 MHz	—	82.6	—	dB
		Interferer CW at Desired \pm 2 MHz	—	89.0	—	dB
		Interferer CW at Desired \pm 10 MHz	—	94.9	—	dB
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	10.0	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-111.0	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dB
Max spurious emissions during active receive mode	SPUR _{RX}	30 MHz to 1 GHz	—	-82.3	-57	dBm
		1 GHz to 12 GHz	—	-69.7	-47	dBm

Note:

1. Definition of reference signal is 100 kbps 2FSK, $m_i = 0.5$, $BT=2.0$, Channel Spacing = 200 kHz. Per WiSun FAN PHY 1.0 standard mode #2a.
2. Definition of reference signal is 2.4 kbps 2GFSK, $BT=0.5$, $\Delta f = 1.2$ kHz, RX channel BW = 4.798 kHz, Channel Spacing = 12.5 kHz. Crystal tolerance = 0 ppm.
3. Definition of reference signal is 50 kbps 2FSK, $m_i = 1.0$, $BT=2.0$, Channel Spacing = 200 kHz. Per WiSun FAN PHY 1.0 standard mode #1b.
4. Definition of reference signal is 4.8 kbps O-QPSK DSSS long-range PHY, 38.4 kcps chip rate, spreading factor 8, chipping code length 32, 1/2 rate with $K=7$ per IEEE802.15.4g, $PER < 1\%$, crystal tolerance ± 2.5 ppm.
5. Definition of reference signal is 9.6 kbps O-QPSK DSSS long-range PHY, 76.8 kcps chip rate, spreading factor 8, chipping code length 32, 1/2 rate with $K=7$ per IEEE802.15.4g, $PER < 1\%$, crystal tolerance ± 10 ppm.
6. Definition of reference signal is 10 kbps 2GFSK, $BT=0.5$, $\Delta f = 25$ kHz, RX channel BW = 99.2 kHz. Crystal tolerance = 0 ppm.

4.9.2.5 433 MHz Band RF Receiver Characteristics

Band is 433.05 MHz to 434.79 MHz. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 433.92 MHz.

Table 4.27. 433 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		433	—	434.79	MHz
Max usable input level, 0.1% BER	SAT_{100k}	Desired is reference 100 kbps 2GFSK signal ¹ , 0.1% BER	—	—	10	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal ² , 0.1% BER	—	-126.9	—	dBm
		Desired is reference 4.8 kbps OOK signal ³ , 20% PER	—	-114.2	—	dBm
		Desired is reference 100 kbps 2GFSK signal ¹ , 0.1% BER	—	-110.7	—	dBm
		Desired is reference 50 kbps 2GFSK signal ⁴ , 0.1% BER	—	-113.8	—	dBm
		Desired is reference 50 kbps 4GFSK signal ⁵ , 1% PER	—	-112.1	—	dBm
		Desired is reference 460 MHz 4.8 kbps 2FSK signal ⁶ , PER<10%	—	-122.5	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I_1	Desired is 4.8 kbps OOK signal ³ at 3dB above sensitivity level	—	54.7	—	dB
		Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	63.9	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I_2	Desired is 4.8 kbps OOK signal ³ at 3dB above sensitivity level	—	67.5	—	dB
		Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	63.9	—	dB
Image rejection, Interferer is CW at image frequency	C/I_{IMAGE}	Desired is 4.8 kbps OOK signal ³ at 3dB above sensitivity level	—	49.6	—	dB
		Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	73.9	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	$C/I_{BLOCKER}$	Interferer CW at Desired ± 1 MHz	—	84.1	—	dB
		Interferer CW at Desired ± 2 MHz	—	90.6	—	dB
		Interferer CW at Desired ± 10 MHz	—	95.8	—	dB
Intermod selectivity, 0.1% BER. CW interferers at 12.5 kHz and 25 kHz offsets	C/I_{IM}	Desired is 2.4 kbps GFSK signal ² at 3dB above sensitivity level	—	56.1	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	10	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-111.0	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dB
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216-960 MHz	—	-81.0	-49.2	dBm
		Above 960 MHz	—	-79.4	-41.2	dBm
Max spurious emissions during active receive mode, per ETSI 300-220 Section 8.6	SPUR _{RX_ETSI}	Below 1000 MHz	—	-81.4	-57	dBm
		Above 1000 MHz	—	-72.2	-47	dBm
Max spurious emissions during active receive mode, per ARIB STD T67 Section 3.3(5)	SPUR _{RX_ARIB}	Below 710 MHz, RBW=100kHz	—	-84.8	-54	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, $\Delta f = \pm 50$ kHz, RX channel BW = 200 kHz, Crystal tolerance = 0 ppm.
2. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, $\Delta f = \pm 1.2$ kHz, BER<0.1%, BW=4.8 kHz. Channel Spacing = 12.5 kHz.
3. Definition of reference signal is 4.8 kbps Manchester-encoded OOK, RX channel BW = 350 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, $\Delta f = \pm 25$ kHz, RX channel BW = 100 kHz, Crystal tolerance = 0 ppm.
5. Definition of reference signal is 50 kbps 4GFSK, BT=1.0, $\Delta f_o = \pm 25$ kHz, $\Delta f_i = \pm 8.33$ kHz, RX channel BW = 74.98 kHz, Crystal tolerance = 0 ppm.
6. Definition of reference signal is 4.8 kbps 2FSK, $\Delta f = \pm 2.4$ kHz, Channel Spacing = 12.5 kHz, PER<10%, Data Whitening, no FEC, 460 MHz center frequency Per IEEE 802.15.4g 450 MHz band, mode 2.

4.9.2.6 315 MHz Band RF Receiver Characteristics

Band is 314 to 316 MHz. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 315 MHz.

Table 4.28. 315 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		314	—	316	MHz
Max usable input level, 20% PER	SAT_{38k4}	Desired is reference 38.4 kbps GFSK signal ¹	—	—	10	dBm
Sensitivity	SENS	Desired is reference 38.4 kbps GFSK signal ¹ , 0.1% BER	—	-114.5	—	dBm
		Desired is reference 40 kbps OOK signal ² , 20% PER	—	-106.5	—	dBm
		Desired is reference 4.8 kbps OOK signal ³ , 20% PER	—	-114.0	—	dBm
Blocking selectivity, 0.1% BER. Desired is 38.4 kbps GFSK signal ¹ at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	73.4	—	dB
		Interferer CW at Desired ± 2 MHz	—	79.0	—	dB
		Interferer CW at Desired ± 10 MHz	—	80.9	—	dB
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	10	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-115.0	—	—	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dB
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216-960 MHz	—	-82.3	-49.2	dBm
		Above 960MHz	—	-79.2	-41.2	dBm

Note:

1. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, $\Delta f = 20\text{ kHz}$, RX channel BW = 74.809 kHz, channel spacing = 100 kHz. Crystal tolerance = 0 ppm.
2. Definition of reference signal is 40 kbps Manchester-encoded OOK, BW = 350 kHz.
3. Definition of reference signal is 4.8 kbps Manchester-encoded OOK, BW = 350 kHz.

4.9.2.7 169 MHz Band RF Receiver Characteristics

Band is 169.4 to to 169.8125 MHz. Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^\circ\text{C}$, $V_{REGVDD} = 3.3\text{ V}$, $AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8\text{ V}$ powered from DCDC. Crystal frequency= 39.0 MHz. RFVDD and external PA supply paths filtered using ferrites. RF center frequency 169.4MHz.

Table 4.29. 169 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		169.4	—	169.812	MHz
Max usable input level, 0.1% BER	SAT_{9k6}	Desired is reference 9.6 kbps 4FSK signal ¹	—	10	—	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal, $\Delta f = \pm 1.2\text{ kHz}^2$, 0.1% BER	—	-124.5	—	dBm
		Desired is reference 2.4 kbps FSK signal, $\Delta f = \pm 2.4\text{ kHz}^3$, PER<10%	—	-118.7	—	dBm
		Desired is reference 4.8 kbps FSK signal, $\Delta f = \pm 1.2\text{ kHz}^4$, PER<10%	—	-122.8	—	dBm
		Desired is reference 9.6 kbps 4FSK signal, $\Delta f_i = \pm 1.6\text{ kHz}^1$, PER<10%	—	-116.6	—	dBm
Alternate channel selectivity, Interferer is CW at $\pm 1\text{ x}$ channel-spacing	C/I_1	Desired is reference 2.4 kbps GFSK signal, $\Delta f = \pm 1.2\text{ kHz}$ at 3 dB above sensitivity level ²	—	-34.9	—	dBm
		Desired is reference 2.4 kbps FSK signal, $\Delta f = \pm 2.4\text{ kHz}$ at 3 dB above sensitivity level ³	—	33.4	—	dB
		Desired is reference 4.8 kbps FSK signal, $\Delta f = \pm 1.2\text{ kHz}$ at 3 dB above sensitivity level ⁴	—	67.6	—	dB
		Desired is reference 9.6 kbps 4FSK signal, $\Delta f_i = \pm 1.6\text{ kHz}$ at 3 dB above sensitivity level ¹	—	60.9	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2\text{ x}$ channel-spacing	C/I_2	Desired is reference 2.4 kbps GFSK signal, $\Delta f = \pm 1.2\text{ kHz}$ at 3 dB above sensitivity level ²	—	-33.4	—	dBm
		Desired is reference 2.4 kbps FSK signal, $\Delta f = \pm 2.4\text{ kHz}$ at 3 dB above sensitivity level ³	—	64.6	—	dB
		Desired is reference 4.8 kbps FSK signal, $\Delta f = \pm 1.2\text{ kHz}$ at 3 dB above sensitivity level ⁴	—	65.6	—	dB
		Desired is reference 9.6 kbps 4FSK signal, $\Delta f_i = \pm 1.6\text{ kHz}$ at 3 dB above sensitivity level ¹	—	62.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is reference 2.4 kbps GFSK signal, $\Delta f = \pm 1.2$ kHz at 3 dB above sensitivity level ²	—	-40.1	—	dBm
		Desired is reference 2.4 kbps FSK signal, $\Delta f = \pm 2.4$ kHz at 3 dB above sensitivity level ³	—	60.6	—	dB
		Desired is reference 4.8 kbps FSK signal, $\Delta f = \pm 1.2$ kHz at 3 dB above sensitivity level ⁴	—	61.2	—	dB
		Desired is reference 9.6 kbps 4FSK signal, $\Delta f_i = \pm 1.6$ kHz at 3 dB above sensitivity level ¹	—	55.7	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ³ at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 2 MHz	—	-15.4	—	dBm
		Interferer CW at Desired ± 10 MHz	—	-9.9	—	dBm
		Interferer CW at Desired ± 15 MHz	—	-9.2	—	dBm
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	10	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-117.0	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dB
Max spurious emissions during active receive mode	SPUR _{RX}	30 MHz to 1 GHz	—	-76.4	-57	dBm
		1 GHz to 12 GHz	—	-70.0	-47	dBm

Note:

1. Definition of reference signal is 9.6 kbps 4GFSK, BT=2.0, $\Delta f_o = \pm 3.2$ kHz, $\Delta f_i = \pm 1.6$ kHz, RX channel BW = 13.666 kHz, Channel Spacing = 12.5 kHz, PER<10%. Per IEEE802.15.4g 169 MHz band, mode 3.
2. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, $\Delta f = \pm 1.2$ kHz, BER<0.1%, BW=4.8 kHz. Channel Spacing = 12.5 kHz. Crystal tolerance = 0 ppm.
3. Definition of reference signal is 2.4 kbps 2FSK, $\Delta f = \pm 2.4$ kHz, BT=2.0, m = 2.0, PER<10%, Channel Spacing = 12.5kHz. Per IEEE802.15.4g 169 MHz band, mode 2.
4. Definition of reference signal is 4.8 kbps 2FSK, $\Delta f = \pm 2.4$ kHz, BT=2.0, m = 0.5, PER<10%, Channel Spacing = 12.5kHz. Per IEEE802.15.4g 169 MHz band, mode 1.

4.10 Frequency Synthesizer

Table 4.30. Frequency Synthesizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF synthesizer frequency range	f_{RANGE}	742 - 970 MHz	742	—	970	MHz
		557 - 727 MHz	557	—	727	MHz
		372 - 557 MHz	372	—	557	MHz
		223 - 372 MHz	223	—	372	MHz
		110 - 223 MHz	110	—	223	MHz
LO tuning frequency resolution with 39.0 MHz crystal	f_{RES}	742 - 970 MHz	—	—	24.8	Hz
		557 - 727 MHz	—	—	18.6	Hz
		372 - 557 MHz	—	—	12.4	Hz
		223 - 372 MHz	—	—	7.4	Hz
		110 - 223 MHz	—	—	5.0	Hz
Frequency deviation resolution with 39.0 MHz crystal	df_{RES}	742 - 970 MHz	—	—	24.8	Hz
		557 - 727 MHz	—	—	18.6	Hz
		372 - 557 MHz	—	—	12.4	Hz
		223 - 372 MHz	—	—	7.4	Hz
		110 - 223 MHz	—	—	5.0	Hz
Maximum frequency deviation with 39.0 MHz crystal	df_{MAX}	742 - 970 MHz	—	—	617	kHz
		557 - 727 MHz	—	—	463	kHz
		372 - 557 MHz	—	—	308	kHz
		223 - 372 MHz	—	—	185	kHz
		110 - 223 MHz	—	—	116	kHz

4.11 Oscillators

4.11.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.3 V. $T_A = 25\text{ }^\circ\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.31. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{HFXO}	see note ¹	38.0	39.0	40.0	MHz
Supported range of crystal load capacitance ²	$C_{\text{HFXO_LC}}$	39.0 MHz, ESR = 40 ³	—	10	—	pF
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	39.0 MHz, CL = 10 pF ⁴	—	40	60	Ω
Supply Current	I_{HFXO}		—	498	—	μA
Startup Time	T_{STARTUP}	39.0 MHz, ESR=40 Ohm, CL=10 pF	—	178	—	μs
On-chip tuning cap step size ⁵	SS_{HFXO}		—	0.04	—	pF

Note:

1. All sub-GHz RF measurements made using a 39 MHz crystal. Other crystal frequencies supported, but RF performance may vary.
2. Total load capacitance as seen by the crystal.
3. It is recommended to use a crystal with a 10 pF load capacitance rating. Only crystals with a 10 pF load cap rating have been characterized for RF use.
4. The crystal should have a maximum ESR less than or equal to this maximum rating.
5. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.11.2 Low Frequency Crystal Oscillator

Table 4.32. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	TBD	k Ω
		GAIN = 1 to 3	—	—	TBD	k Ω
Supported range of crystal load capacitance ¹	C_{LFXO_CL}	GAIN = 0	TBD	—	TBD	pF
		GAIN = 1	TBD	—	TBD	pF
		GAIN = 2 (see note ²)	TBD	—	TBD	pF
		GAIN = 3 (see note ²)	TBD	—	TBD	pF
Current consumption	I_{CL12p5}	ESR = 70 k Ω , CL = 12.5 pF, GAIN ³ = 2, AGC ⁴ = 1	—	290	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 k Ω , CL = 7 pF, GAIN ³ = 1, AGC ⁴ = 1	—	52	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting ⁵	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting ⁵	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

- Total load capacitance seen by the crystal
- Crystals with a load capacitance of greater than 12 pF require external load capacitors.
- In LFXO_CAL Register
- In LFXO_CFG Register
- The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.11.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.3 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.33. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F _{HFRCO_ACC}	For all production calibrated frequencies	TBD	—	TBD	%
Current consumption on all supplies ¹	I _{HFRCO}	F _{HFRCO} = 4 MHz	—	28	—	μA
		F _{HFRCO} = 5 MHz ²	—	29	—	μA
		F _{HFRCO} = 7 MHz	—	59	—	μA
		F _{HFRCO} = 10 MHz ²	—	63	—	μA
		F _{HFRCO} = 13 MHz	—	77	—	μA
		F _{HFRCO} = 16 MHz	—	87	—	μA
		F _{HFRCO} = 19 MHz	—	90	—	μA
		F _{HFRCO} = 20 MHz ²	—	107	—	μA
		F _{HFRCO} = 26 MHz	—	116	—	μA
		F _{HFRCO} = 32 MHz	—	139	—	μA
		F _{HFRCO} = 38 MHz ³	—	170	—	μA
		F _{HFRCO} = 40 MHz ²	—	172	—	μA
		F _{HFRCO} = 48 MHz ³	—	207	—	μA
		F _{HFRCO} = 56 MHz ³	—	228	—	μA
F _{HFRCO} = 64 MHz ³	—	269	—	μA		
F _{HFRCO} = 80 MHz ³	—	285	—	μA		
Clock out current for HFRCODPLL ⁴	I _{CLKOUT_HFRCODPLL}	FORCEEN bit of HFRCO0_CTRL = 1	—	3.0	—	μA/MHz
Clock Out current for HFRCOEM23 ⁴	I _{CLKOUT_HFRCOEM23}	FORCEEN bit of HFRCOEM23_CTRL = 1	—	1.6	—	μA/MHz
Output clock duty cycle	DUTY _{CYCLE}		TBD	50	TBD	%
Startup Time ⁵	T _{STARTUP}	FREQRANGE = 0 to 7	—	1.2	—	μs
		FREQRANGE = 8 to 15	—	0.6	—	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits ⁶	f _{HFRCO_BAND}	FREQRANGE = 0	TBD	—	TBD	MHz
		FREQRANGE = 1	TBD	—	TBD	MHz
		FREQRANGE = 2	TBD	—	TBD	MHz
		FREQRANGE = 3	TBD	—	TBD	MHz
		FREQRANGE = 4	TBD	—	TBD	MHz
		FREQRANGE = 6	TBD	—	TBD	MHz
		FREQRANGE = 7	TBD	—	TBD	MHz
		FREQRANGE = 8	TBD	—	TBD	MHz
		FREQRANGE = 9	TBD	—	TBD	MHz
		FREQRANGE = 10	TBD	—	TBD	MHz
		FREQRANGE = 11	TBD	—	TBD	MHz
		FREQRANGE = 12	TBD	—	TBD	MHz
		FREQRANGE = 13	TBD	—	TBD	MHz
		FREQRANGE = 14	TBD	—	TBD	MHz
		FREQRANGE = 15	TBD	—	TBD	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. This frequency is calibrated for the HFRCOEM23 only.
3. This frequency is calibrated for the HFRCODPLL only.
4. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
5. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
6. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.11.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.34. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F _{FSRCO}		TBD	20	TBD	MHz

4.11.5 Low Frequency RC Oscillator (LFRCO)**Table 4.35. Low Frequency RC Oscillator (LFRCO)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}		TBD	—	TBD	%
Frequency calibration step	F_{TRIM_STEP}	Typical trim step at mid-scale	—	0.33	—	%
Startup time	$t_{STARTUP}$		—	220	—	μ s
Current consumption	I_{LFRCO}		—	186	—	nA

4.11.6 Ultra Low Frequency RC Oscillator**Table 4.36. Ultra Low Frequency RC Oscillator**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F_{ULFRCO}		TBD	1.0	TBD	kHz

4.12 GPIO Pins (3V GPIO pins)

Table 4.37. GPIO Pins (3V GPIO pins)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I _{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.3 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V T _A = 85 °C	—	—	TBD	nA
		MODEx = DISABLED, IOVDD = 3.8 V T _A = 125 °C	—	—	TBD	nA
		MODEx = INPUT, IOVDD = 3.8 V T _A = 125 °C	—	—	TBD	nA
		LCD segment and common pins, IOVDD = 2.7 V, VLCD = 3.8 V, T _A = 85 °C ¹	—	—	TBD	nA
		LCD Charge Pump Supply (PA06), T _A = 85 °C	—	—	TBD	nA
Input low voltage ²	V _{IL}	Any GPIO pin	—	—	0.3*IOVDD	V
		RESETn	—	—	0.3*DVDD	V
Input high voltage ²	V _{IH}	Any GPIO pin	0.7*IOVDD	—	—	V
		RESETn	0.7*DVDD	—	—	V
Hysteresis of input voltage	V _{HYS}	Any GPIO pin	0.05*IOVDD	—	—	V
		RESETn	0.05*DVDD	—	—	V
Output high voltage	V _{OH}	Sourcing 20mA, IOVDD = 3.3 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.62 V	0.6 * IOVDD	—	—	V
Output low voltage	V _{OL}	Sinking 20mA, IOVDD = 3.3 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.62 V	—	—	0.4 * IOVDD	V
GPIO rise time	T _{GPIO_RISE}	IOVDD = 3.3 V, C _{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.7 V, C _{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T _{GPIO_FALL}	IOVDD = 3.3 V, C _{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.7 V, C _{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pull up/down resistance ³	R _{PULL}	Any GPIO pin. Pull-up to IOVDD: MODE _n = DISABLE DOUT=1. Pull-down to VSS: MODE _n = WIREORPULLDOWN DOUT = 0.	TBD	44	TBD	kΩ
		RESET _n pin. Pull-up to DVDD	TBD	44	TBD	kΩ
Maximum filtered glitch width	T _{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESET _n low time to ensure pin reset	T _{RESET}		100	—	—	ns

Note:

1. MODE_x = DISABLED, LCD pins selected by setting the corresponding bits in the VGPI0_SEG or GPIO_COM register.
2. GPIO input thresholds are proportional to the IOVDD pin. RESET_n input thresholds are proportional to DVDD.
3. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESET_n pull-up connects to DVDD.

4.13 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR=2, unless otherwise indicated.

Table 4.38. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V _{AVDD}	Normal mode	1.71	—	3.8	V
Maximum Input Range ¹	V _{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-Scale Voltage	V _{FS}	Voltage required for Full-Scale measurement	—	V _{REF} / Gain	—	
Input Measurement Range	V _{IN}	Differential Mode - Plus and Minus inputs	-V _{FS}	—	+V _{FS}	V
		Single Ended Mode - One input tied to ground	0	—	V _{FS}	V
Input Sampling Capacitance	C _s	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f _{CLK}	Normal mode, Gain = 1x or 0.5x	—	—	10	MHz
		Normal mode, Gain = 2x	—	—	5	MHz
		Normal mode, Gain = 3x or 4x	—	—	2.5	MHz
Throughput rate	f _{SAMPLE}	Normal mode, f _{CLK} = 10 MHz, OSR = 2x	—	—	1	MspS
		Normal mode, f _{CLK} = 10 MHz, OSR = 32x	—	—	76.9	ksps
Current from all supplies, Continuous operation	I _{ADC_CONT}	Normal Mode, 1 Msps, OSR = 2, f _{CLK} = 10 MHz	—	290	TBD	μA
Current in Standby mode. ADC is not functional but can wake up in 1us.	I _{STBY}	Normal mode	—	16	—	μA
ADC Startup Time	t _{startup}	From power down state	—	5	—	μs
		From standby state	—	1	—	μs
Normal Mode ADC Resolution ²	Resolution	OSR = 2	—	12	—	bits
		OSR = 32	—	16	—	bits
Differential Nonlinearity	DNL	Normal mode. Differential Input. OSR = 2 (No missing codes)	TBD	+/- 0.25	TBD	LSB12
Integral Nonlinearity	INL	Normal mode. Differential Input, OSR = 2	TBD	+/- 0.65	TBD	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Effective number of bits ³	ENOB	Normal Mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V. OSR=2	TBD	11.7	—	bits
		Normal Mode, Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, Internal VREF = 1.21 V.	TBD	13.5	—	bits
		Normal Mode, Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, External VREF = 1.25 V.	TBD	14.3	—	bits
Signal to Noise + Distortion Ratio Normal Mode ³	SNDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	TBD	72.3	—	dB
		Differential Input. Gain=2x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.3	—	dB
		Differential Input. Gain=4x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	68.8	—	dB
		Differential Input. Gain=0.5x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.5	—	dB
		Differential Input. Gain = 1x, OSR = 64, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	83.9	—	dB
Total Harmonic Distortion	THD	Normal mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	-80.8	TBD	dB
Spurious-Free Dynamic Range	SFDR	Normal mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	TBD	86.5	—	dB
Common Mode Rejection Ratio	CMRR	Normal mode. DC to 100 Hz	—	87.0	—	dB
		Normal mode. AC high frequency.	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	Normal mode. DC to 100 Hz	—	80.4	—	dB
		Normal mode. AC high frequency, using internal VBGR	—	33.4	—	dB
		Normal mode. AC high frequency, using VREF pad	—	65.2	—	dB
External reference voltage range ¹	V_{EVREF}		1.0	—	AVDD	V
Offset	OFFSET	GAIN = 1 and 0.5, Differential Input	TBD	0.27	TBD	LSB
		GAIN = 2, Differential Input	TBD	0.27	TBD	LSB
		GAIN = 3, Differential Input	TBD	0.25	TBD	LSB
		GAIN = 4, Differential Input	TBD	0.29	TBD	LSB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Gain Error	GE	GAIN = 1 and 0.5, using external VREF, direct mode.	TBD	0.069	TBD	%
		GAIN = 2, using external VREF, direct mode.	TBD	0.151	TBD	%
		GAIN = 3, using external VREF, direct mode.	TBD	0.186	TBD	%
		GAIN = 4, using external VREF, direct mode.	TBD	0.227	TBD	%
		Internal VREF ⁴ , all GAIN settings	TBD	0.023	TBD	%
Internal Reference voltage	V _{IVREF}		—	1.21	—	V

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR=2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: $ENOB = (SNDR - 1.76) / 6.02$.
4. Includes error from internal VREF drift.

4.14 Analog Comparator (ACMP)

Table 4.39. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ACMP Supply current from AVDD pin	I_{ACMP}	BIAS = 2, HYST = DISABLED	—	520	—	nA
		BIAS = 3, HYST = DISABLED	—	1.9	—	μ A
		BIAS = 4, HYST = DISABLED	—	4.4	—	μ A
		BIAS = 5, HYST = DISABLED	—	9.4	—	μ A
		BIAS = 6, HYST = DISABLED	—	24	—	μ A
		BIAS = 7, HYST = DISABLED	—	46	TBD	μ A
ACMP Supply current from AVDD pin with Hysteresis	I_{ACMP_WHYS}	BIAS = 2, HYST = SYM30MV	—	780	—	nA
		BIAS = 3, HYST = SYM30MV	—	2.8	—	μ A
		BIAS = 4, HYST = SYM30MV	—	6.3	—	μ A
		BIAS = 5, HYST = SYM30MV	—	14	—	μ A
		BIAS = 6, HYST = SYM30MV	—	35	—	μ A
		BIAS = 7, HYST = SYM30MV	—	66	—	μ A
Current consumption from VREFDIV in continuous mode	$I_{VREFDIV}$	NEGSEL = VREFDIVAVDD	—	3.4	—	μ A
		NEGSEL = VREFDIV1V25	—	4.2	—	μ A
		NEGSEL = VREFDIV2V5	—	6.9	—	μ A
Current consumption from VREFDIV in SH mode	$I_{VREFDIV_SH}$	NEGSEL = VREFDIV2V5	—	76	—	nA
		NEGSEL = VREFDIV1V25	—	73	—	nA
		NEGSEL = VREFDIVAVDD	—	72	—	nA
Current consumption from VSENSEDIV in continuous mode	$I_{VSENSEDIV}$	NEGSEL = VSENSE01DIV4	—	1.8	—	μ A
Current consumption from VSENSEDIV in SH mode	$I_{VSENSEDIV_SH}$	NEGSEL = VSENSE01DIV4	—	58	—	nA
Hysteresis (BIAS = 4)	V_{HYST}	HYST = SYM10MV ¹	—	21	—	mV
		HYST = SYM20MV ¹	—	40	—	mV
		HYST = SYM30MV ¹	—	58	—	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V Reference	TBD	1.25	TBD	V
		Internal 2.5 V Reference	TBD	2.5	TBD	V
Input offset voltage	V_{OFFSET}	BIAS = 2, VCM = 0.15 to AVDD - 0.15	TBD	—	TBD	mV
		BIAS = 4, VCM = 0.15 to AVDD - 0.15	TBD	—	TBD	mV
		BIAS = 7, VCM = 0.15 to AVDD - 0.15	TBD	—	TBD	mV
Input Range	V_{IN}	Input Voltage Range	TBD	—	TBD	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparator delay with 100 mV overdrive	T _{DELAY}	BIAS = 2	—	0.87	—	μs
		BIAS = 3	—	0.28	—	μs
		BIAS = 4	—	160	—	ns
		BIAS = 5	—	94	—	ns
		BIAS = 6	—	60	—	ns
		BIAS = 7	—	49	—	ns
Capacitive Sense Oscillator Resistance	R _{CSRESSEL}	CSRESSEL = 0	—	14	—	kΩ
		CSRESSEL = 1	—	24	—	kΩ
		CSRESSEL = 2	—	43	—	kΩ
		CSRESSEL = 3	—	60	—	kΩ
		CSRESSEL = 4	—	80	—	kΩ
		CSRESSEL = 5	—	99	—	kΩ
		CSRESSEL = 6	—	120	—	kΩ
Note: 1. V _{CM} = 1.25 V						

4.15 Digital to Analog Converter (VDAC)

Table 4.40. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}		0	—	VREF	V
Output Current	I_{DACOUT}		-10	—	10	mA
DAC clock frequency	f_{DAC}		—	—	1	MHz
Sample rate	SR_{DAC}	$f_{DAC} = f_{DAC(max)}$	—	—	500	ksps
Resolution	$N_{RESOLUTION}$		—	12	—	bits
Load Capacitance ¹	C_{LOAD}	High Power and Lower Power Modes	—	—	50	pF
		High Capacitance Load Mode	25	—	—	nF
Load Resistance	R_{LOAD}		5	—	—	k Ω
Current consumption, Dynamic, 500 ksps, 1 channel active ²	$I_{DAC_1_500}$	High Power Mode	—	255	—	μ A
		Low Power Mode	—	150	—	μ A
Current consumption, Dynamic, 500 ksps, 2 channels active ²	$I_{DAC_2_500}$	High Power Mode	—	421	—	μ A
		Low Power Mode	—	216	—	μ A
Current consumption, Static, 1 channel active ³	$I_{DAC_1_STAT}$	High Power Mode	—	138	—	μ A
		Low Power Mode	—	33	—	μ A
		High Capacitance Mode	—	44	—	μ A
Current consumption, Static, 2 channels active ³	$I_{DAC_2_STAT}$	High Power Mode	—	267	—	μ A
		Low Power Mode	—	57	—	μ A
		High Capacitance Mode	—	78	—	μ A
Startup time	$t_{DACSTARTUP}$	Enable to 90% full scale output, settling to 10 LSB	—	4.5	TBD	μ s
Settling time	$t_{DACSETTLE}$	High Power Mode, 25% to 75% of full scale, settling to 10 LSB	—	1.1	TBD	μ s
		Low Power Mode, 25% to 75% of full scale, settling to 1%	—	2.7	—	μ s
Output impedance	R_{OUT}	Main Output, High Power Mode	—	2.3	—	Ω
		Main Output, Low Power Mode	—	3.2	—	Ω
Power supply rejection ratio ⁴	PSRR	$V_{out} = 50\%$ full scale, DC output	—	72	—	dB
Signal to noise and distortion ratio	$SNDR_{DAC}$	High Power mode, 500 ksps, internal 2.5V reference, 1 kHz sine wave input, BW limited to 250 kHz	TBD	64.8	—	dB
		High Power mode, 500 ksps, internal 2.5V reference, 1 kHz sine wave input, BW limited to 22 kHz	TBD	67.4	—	dB
Total Harmonic Distortion	THD	High Power Mode, internal 2.5V reference, 1 kHz sine wave input	—	-68.8	TBD	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Integral Non-Linearity	INL _{DAC}	High Power Mode, internal 2.5V reference, T _A = 25 °C	TBD	—	TBD	LSB
		High Power Mode, internal 2.5V reference, T _A = -40 to +85 °C	TBD	—	TBD	LSB
		High Power Mode, internal 2.5V reference, T _A = -40 to +125 °C	TBD	—	TBD	LSB
Differential Non-Linearity ⁵	DNL _{DAC}	High Power Mode, internal 2.5V reference, T _A = 25 °C	TBD	—	TBD	LSB
		High Power Mode, internal 2.5V reference, T _A = -40 to +85 °C	TBD	—	TBD	LSB
		High Power Mode, internal 2.5V reference, T _A = -40 to +125 °C	TBD	—	TBD	LSB
Offset error ⁶	V _{OFFSET}	High Power mode	TBD	—	TBD	mV
		Low Power Mode	TBD	—	TBD	mV
		High Capacitance Load mode	TBD	—	TBD	mV
Gain error ⁶	V _{GAIN}	1.25 V internal reference	TBD	—	TBD	%
		2.5 V internal reference	TBD	—	TBD	%
		External Reference	TBD	—	TBD	%
External Reference Voltage ⁷	V _{EXTREF}		1.1	—	V _{AVDD}	V

Note:

1. Main outputs only.
2. Dynamic current specifications are for VDAC circuitry operating at max clock frequency with the output updated at the specified sampling rate. Output is a 1 kHz sine wave from 10% to 90% full scale. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
3. Static current specifications are for VDAC circuitry operating after a one-time update to a static output at 50% full scale. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
4. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$.
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
7. External reference voltage on VREFP pin or PA00 when used for VREFP

4.16 LCD

Table 4.41. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LCD Temperature Range	T _{RANGE}		-40	—	105	°C
Frame rate	f _{LCDFR}		30	—	100	Hz
LCD supply range ^{1 2}	V _{LCDIN}		1.71	—	3.8	V
LCD output voltage range ²	V _{LCD}	Step-down mode with external LCD capacitor	2.4	—	V _{LCDIN}	V
		Charge pump mode with external LCD capacitor	2.4	—	1.9 * V _{LCDIN}	V
Contrast control step size	STEP _{CONTRAST}	Charge pump or Step-down mode	—	50	—	mV
Contrast control step accuracy ³	ACC _{CONTRAST}		—	+/-1.5	—	%

Note:

1. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.
2. V_{LCDIN} and V_{LCD} should be a maximum of 2 V above V_{IOVDD} to avoid additional leakage through the GPIO pins used for LCD functions.
3. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

4.17 Temperature Sensor

Table 4.42. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range ¹	T _{RANGE}		-40	—	125	°C
Temperature sensor resolution	T _{RESOLUTION}		—	0.25	—	°C
Measurement noise (RMS)	T _{NOISE}	Single measurement	—	0.6	—	°C
		16-sample average (TEMPAVG- NUM = 0)	—	0.17	—	°C
		64-sample average (TEMPAVG- NUM = 1)	—	0.12	—	°C
Temperature offset	T _{OFF}	Mean error of uncorrected output across full temperature range	—	3.7	—	°C
Temperature sensor accuracy ^{2 3}	T _{ACC}	Direct output accuracy after mean error (T _{OFF}) removed	TBD	—	TBD	°C
		After linearization in software, no calibration	TBD	—	TBD	°C
		After linearization in software, with single-temperature calibration at 25 °C ⁴	TBD	—	TBD	°C
Measurement interval	t _{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in °K. All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.18 Brown Out Detectors

4.18.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at $T_A = 25\text{ }^\circ\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.43. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply Rising	—	1.65	TBD	V
		Supply Falling	TBD	1.63	—	V
BOD response time	$t_{DVDD_BOD_DELAY}$	Supply dropping at 100 mV/ μs slew rate ¹	—	0.95	—	μs
BOD hysteresis	$V_{DVDD_BOD_HYS T}$		—	22	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.18.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.44. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD_LE_BOD}$	Supply Falling	TBD	—	TBD	V
BOD response time	$t_{DVDD_LE_BOD_DELAY}$	Supply dropping at 2 mV/ μs slew rate ¹	—	50	—	μs
BOD hysteresis	$V_{DVDD_LE_BOD_HYST}$		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.18.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.45. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	TBD	—	TBD	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV/ μ s slew rate ¹	—	50	—	μ s
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:
 1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.19 Pulse Counter

Table 4.46. Pulse Counter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	1.0	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	TBD	kHz
Setup time in asynchronous external clock mode	$t_{SU_S1N_S0N}$	S1N (data) to S0N (clock)	TBD	—	—	ns

4.20 USART SPI Main Timing

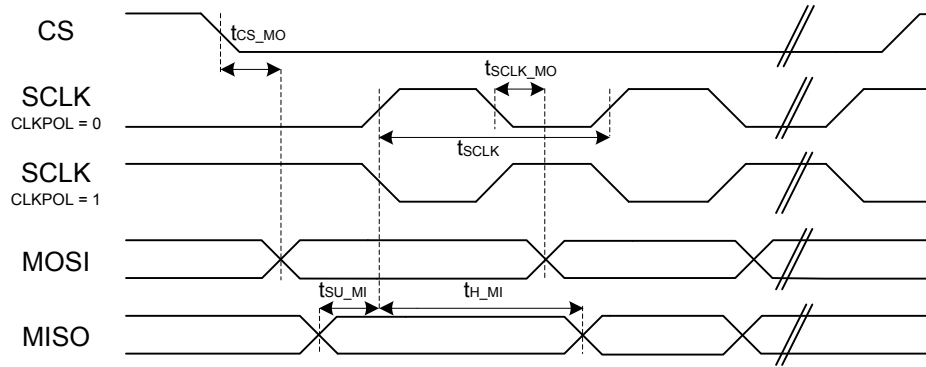


Figure 4.1. SPI Main Timing (SMSDELAY = 0)

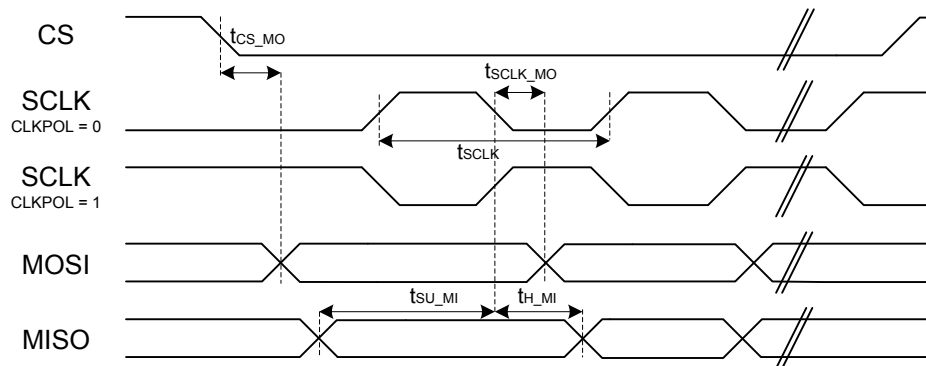


Figure 4.2. SPI Main Timing (SMSDELAY = 1)

4.20.1 USART SPI Main Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.47. USART SPI Main Interface Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		2*t _{PCLK}	—	—	ns
CS to MOSI ^{1 2}	t _{CS_MO}		-17	—	22	ns
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		-12	—	12	ns
MISO setup time ^{1 2}	t _{SU_MI}	IOVDD = 1.62 V	39	—	—	ns
		IOVDD = 3.3 V	28	—	—	ns
MISO hold time ^{1 2}	t _{H_MI}		-10	—	—	ns
Note:						
1. Applies for both CLKPHA = 0 and CLKPHA = 1						
2. Measurement done with 8 pF output loading at 10% and 90% of V _{DD} .						
3. t _{PCLK} is one period of the selected PCLK.						

4.20.2 USART SPI Main Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.48. USART SPI Main Interface Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		2*t _{PCLK}	—	—	ns
CS to MOSI ^{1 2}	t _{CS_MO}		-24	—	32	ns
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		-12	—	20	ns
MISO setup time ^{1 2}	t _{SU_MI}	IOVDD = 1.62 V	47	—	—	ns
		IOVDD = 3.3 V	39	—	—	ns
MISO hold time ^{1 2}	t _{H_MI}		-11	—	—	ns
Note:						
1. Applies for both CLKPHA = 0 and CLKPHA = 1						
2. Measurement done with 8 pF output loading at 10% and 90% of V _{DD} .						
3. t _{PCLK} is one period of the selected PCLK.						

4.21 USART SPI Secondary Timing

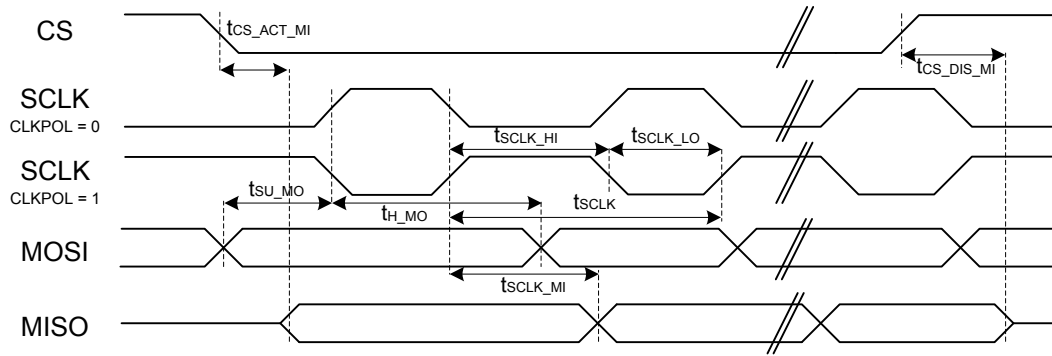


Figure 4.3. SPI Secondary Timing

4.21.1 USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.49. USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		$6 \cdot t_{PCLK}$	—	—	ns
SCLK high time ^{1 2 3}	t_{SCLK_HI}		$2.5 \cdot t_{PCLK}$	—	—	ns
SCLK low time ^{1 2 3}	t_{SCLK_LO}		$2.5 \cdot t_{PCLK}$	—	—	ns
CS active to MISO ^{1 2}	$t_{CS_ACT_MI}$		18	—	75	ns
CS disable to MISO ^{1 2}	$t_{CS_DIS_MI}$		16	—	66	ns
MOSI setup time ^{1 2}	t_{SU_MO}		6	—	—	ns
MOSI hold time ^{1 2 3}	t_{H_MO}		5	—	—	ns
SCLK to MISO ^{1 2 3}	t_{SCLK_MI}		$14 + 1.5 \cdot t_{PCLK}$	—	$29 + 2.5 \cdot t_{PCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. t_{PCLK} is one period of the selected PCLK.

4.21.2 USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.50. USART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		6*t _{PCLK}	—	—	ns
SCLK high time ^{1 2 3}	t _{SCLK_HI}		2.5*t _{PCLK}	—	—	ns
SCLK low time ^{1 2 3}	t _{SCLK_LO}		2.5*t _{PCLK}	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		23	—	102	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		22	—	93	ns
MOSI setup time ^{1 2}	t _{SU_MO}		9	—	—	ns
MOSI hold time ^{1 2 3}	t _{H_MO}		9	—	—	ns
SCLK to MISO ^{1 2 3}	t _{SCLK_MI}		18 + 1.5*t _{PCLK}	—	36 + 2.5*t _{PCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. t_{PCLK} is one period of the selected PCLK.

4.22 EUSART SPI Main Timing

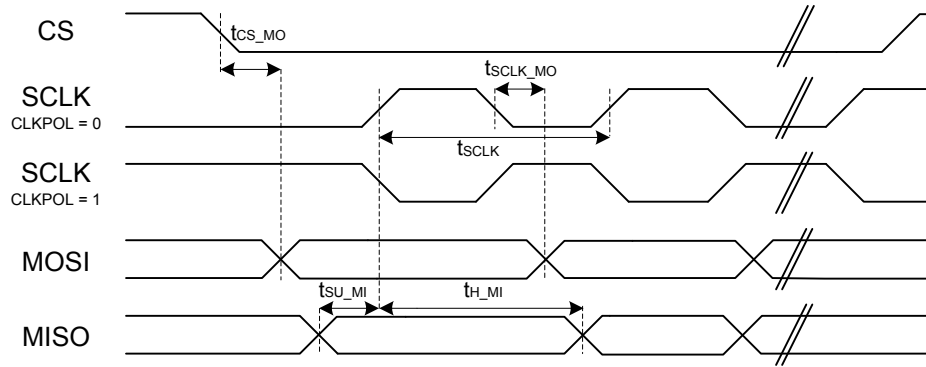


Figure 4.4. SPI Main Timing

4.22.1 EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.51. EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI ^{1 2}	t_{CS_MO}		-10	—	8	ns
SCLK to MOSI ^{1 2}	t_{SCLK_MO}		-3	—	8	ns
MISO setup time ^{1 2}	t_{SU_MI}		7	—	—	ns
MISO hold time ^{1 2}	t_{H_MI}		3	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD} .
3. t_{CLK} is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

4.22.2 EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.52. EUSART SPI Main Interface Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		t _{CLK}	—	—	ns
CS to MOSI ^{1 2}	t _{CS_MO}		-18	—	15	ns
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		-4	—	13	ns
MISO setup time ^{1 2}	t _{SU_MI}		12	—	—	ns
MISO hold time ^{1 2}	t _{H_MI}		3	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD}.
3. t_{CLK} is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

4.23 EUSART SPI Secondary Timing

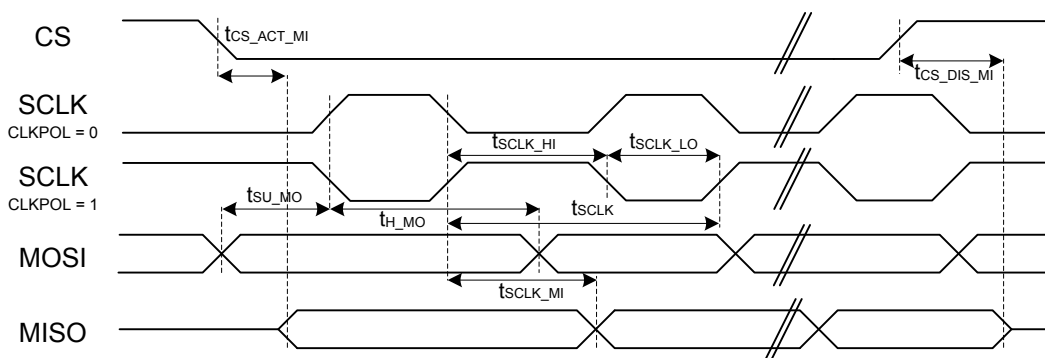


Figure 4.5. SPI Secondary Timing

4.23.1 EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.53. EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time ^{1 2}	t_{SCLK_HI}		50	—	—	ns
SCLK low time ^{1 2}	t_{SCLK_LO}		50	—	—	ns
CS active to MISO ^{1 2}	$t_{CS_ACT_MI}$		5	—	50	ns
CS disable to MISO ^{1 2}	$t_{CS_DIS_MI}$		7	—	40	ns
MOSI setup time ^{1 2}	t_{SU_MO}		5	—	—	ns
MOSI hold time ^{1 2}	t_{H_MO}		6	—	—	ns
SCLK to MISO ^{1 2}	t_{SCLK_MI}	IOVDD = 1.8 V	9	—	40	ns
		IOVDD = 3.3 V	9	—	30	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

4.23.2 EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.54. EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time ^{1 2}	t _{SCLK_HI}		50	—	—	ns
SCLK low time ^{1 2}	t _{SCLK_LO}		50	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		6	—	75	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		6	—	60	ns
MOSI setup time ^{1 2}	t _{SU_MO}		8	—	—	ns
MOSI hold time ^{1 2}	t _{H_MO}		11	—	—	ns
SCLK to MISO ^{1 2}	t _{SCLK_MI}	IOVDD = 1.8 V	10	—	50	ns
		IOVDD = 3.3 V	10	—	42	ns
Note:						
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).						
2. Measurement done with 15 pF output loading at 10% and 90% of V _{DD} (figure shows 50% of V _{DD}).						

4.23.3 EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE0

Timing specifications at VSCALE0 apply to EUSART0 only, routed to DBUSAB on consecutive pins. All GPIO set to slew rate = 6.

Table 4.55. EUSART SPI Secondary Interface Timing, Voltage Scaling = VSCALE0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time ^{1 2}	t _{SCLK_HI}		100	—	—	ns
SCLK low time ^{1 2}	t _{SCLK_LO}		100	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		8	—	112	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		8	—	82	ns
MOSI setup time ^{1 2}	t _{SU_MO}		12	—	—	ns
MOSI hold time ^{1 2}	t _{H_MO}		32	—	—	ns
Note:						
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).						
2. Measurement done with 15 pF output loading at 10% and 90% of V _{DD} (figure shows 50% of V _{DD}).						

4.24 I2C Electrical Specifications

4.24.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.56. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ¹	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	μ s
SCL clock high time	t_{HIGH}		4	—	—	μ s
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	μ s
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	μ s
STOP condition set-up time	t_{SU_STO}		4.0	—	—	μ s
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	μ s

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.24.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.57. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ¹	f _{SCL}		0	—	400	kHz
SCL clock low time	t _{LOW}		1.3	—	—	μs
SCL clock high time	t _{HIGH}		0.6	—	—	μs
SDA set-up time	t _{SU_DAT}		100	—	—	ns
SDA hold time	t _{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.6	—	—	μs
Repeated START condition hold time	t _{HD_STA}		0.6	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		1.3	—	—	μs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.24.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.58. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ¹	f _{SCL}		0	—	1000	kHz
SCL clock low time	t _{LOW}		0.5	—	—	μs
SCL clock high time	t _{HIGH}		0.26	—	—	μs
SDA set-up time	t _{SU_DAT}		50	—	—	ns
SDA hold time	t _{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	—	—	μs
Repeated START condition hold time	t _{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.25 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.25.1 Supply Current

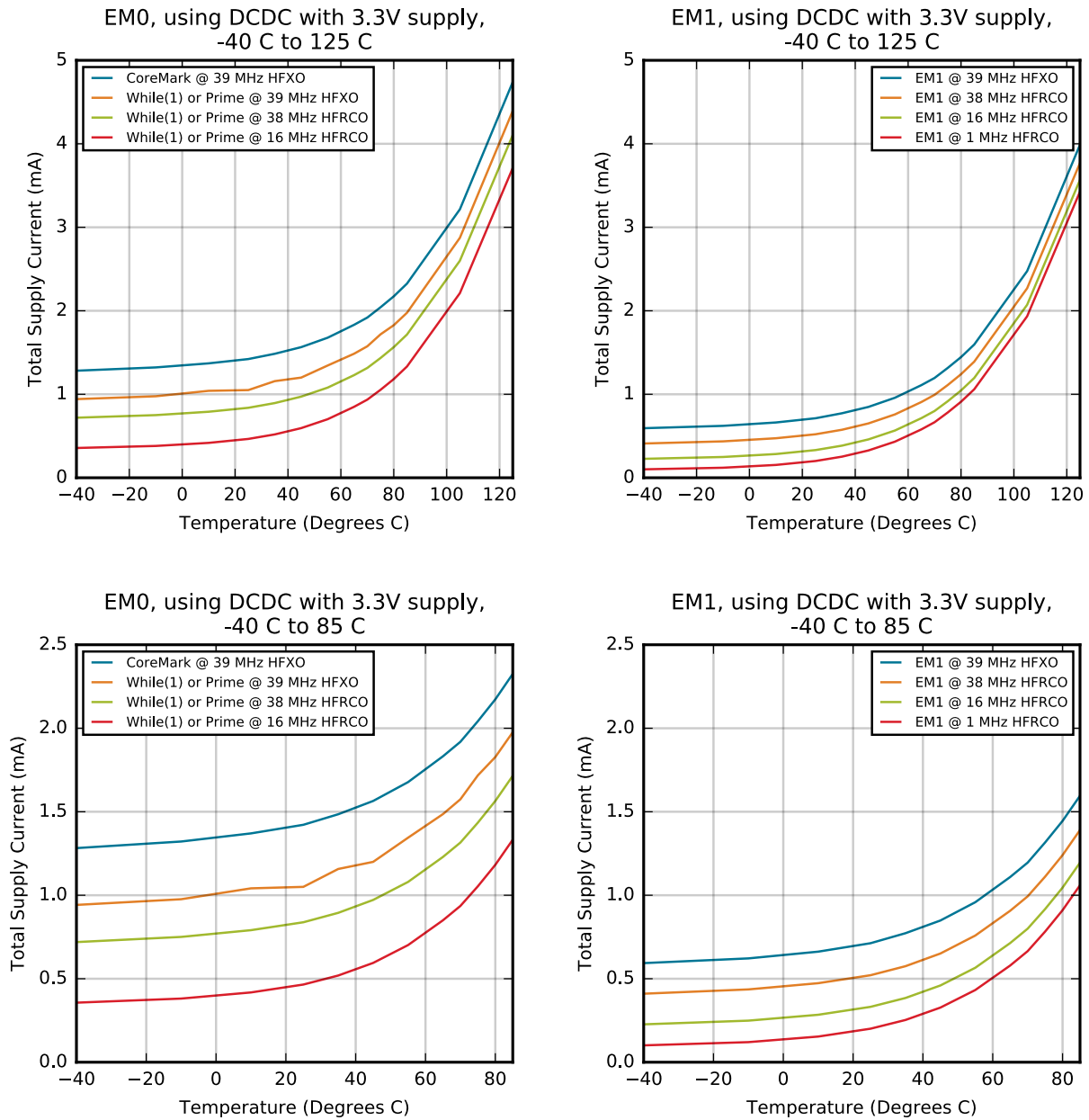


Figure 4.6. EM0 and EM1 Typical Supply Current vs. Temperature

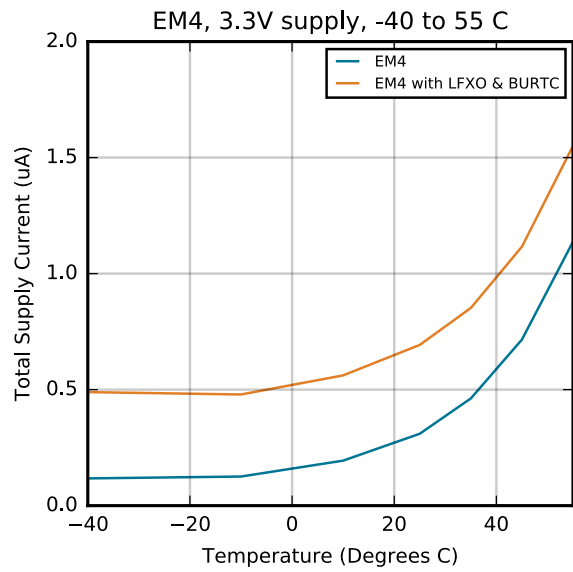
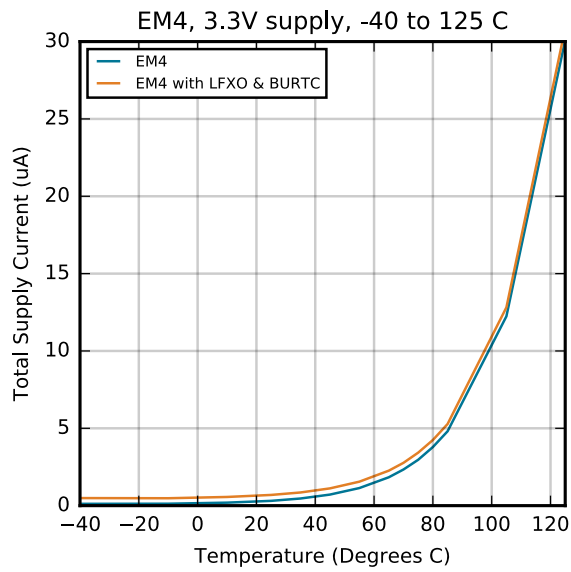
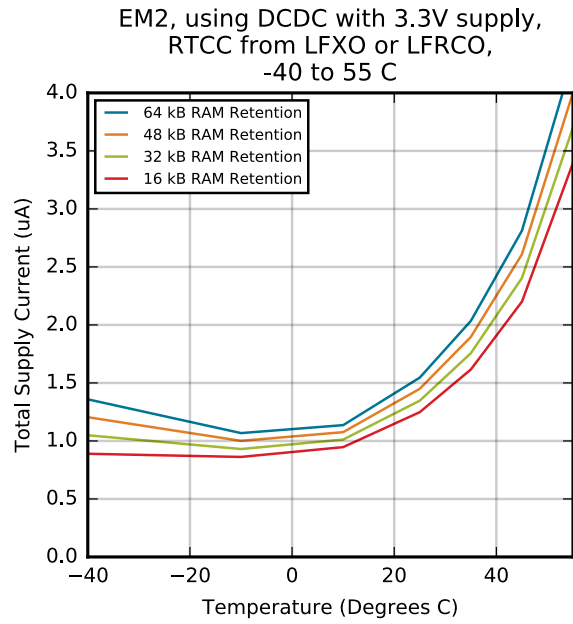
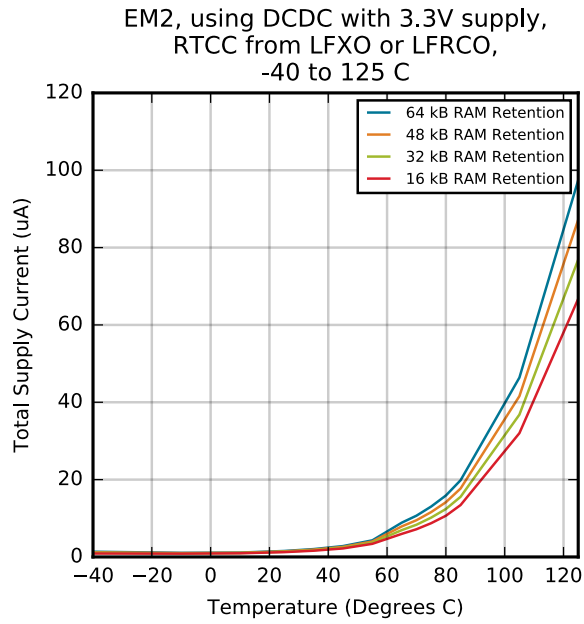


Figure 4.7. EM2 and EM4 Typical Supply Current vs. Temperature

4.25.2 DC-DC Converter

Performance characterized with Samsung CIG22H2R2MNE ($L_{DCDC} = 2.2 \mu\text{H}$) and Samsung CL10B475KQ8NQC ($C_{DCDC} = 4.7 \mu\text{F}$)

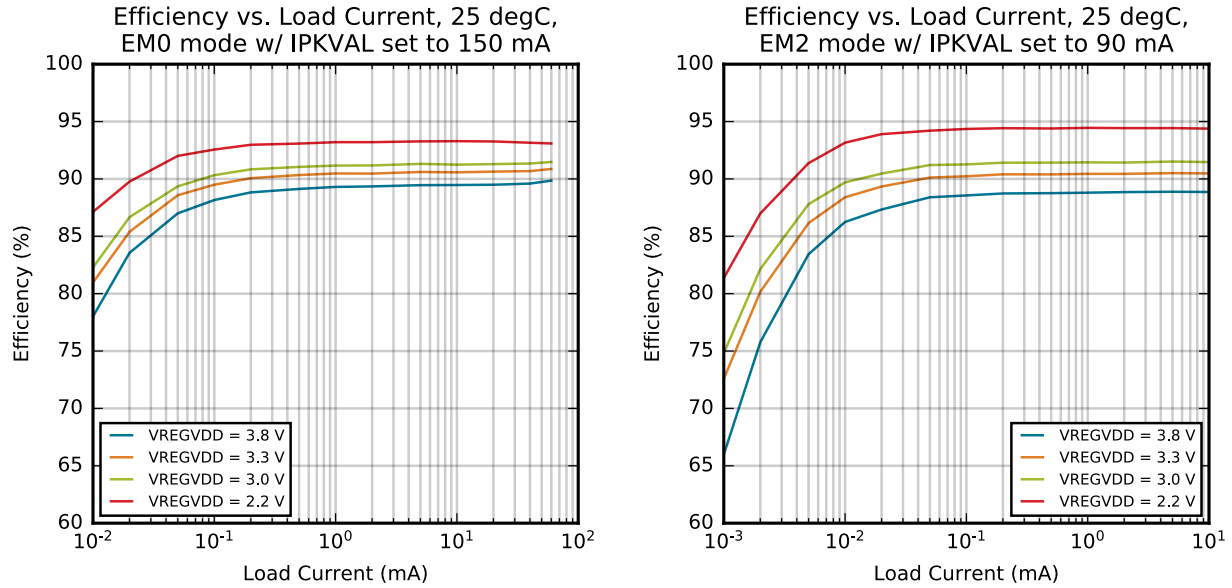


Figure 4.8. DC-DC Efficiency

4.25.3 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

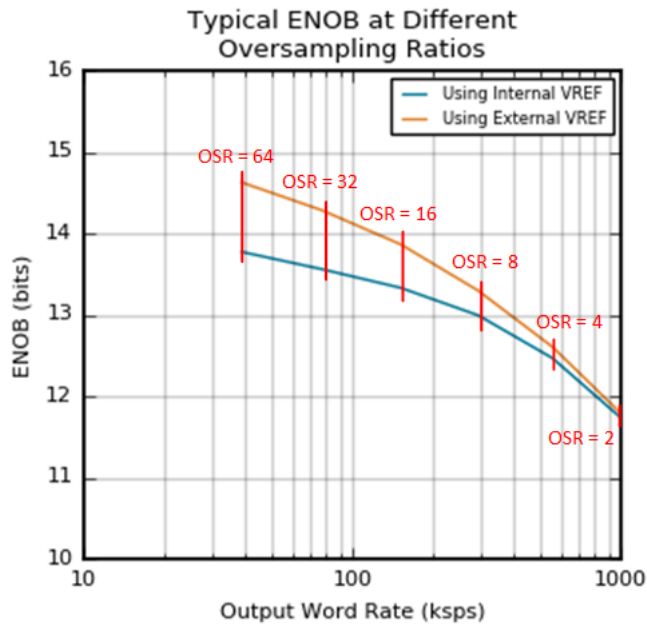


Figure 4.9. Typical ENOB vs. Oversampling Ratio

4.25.4 GPIO

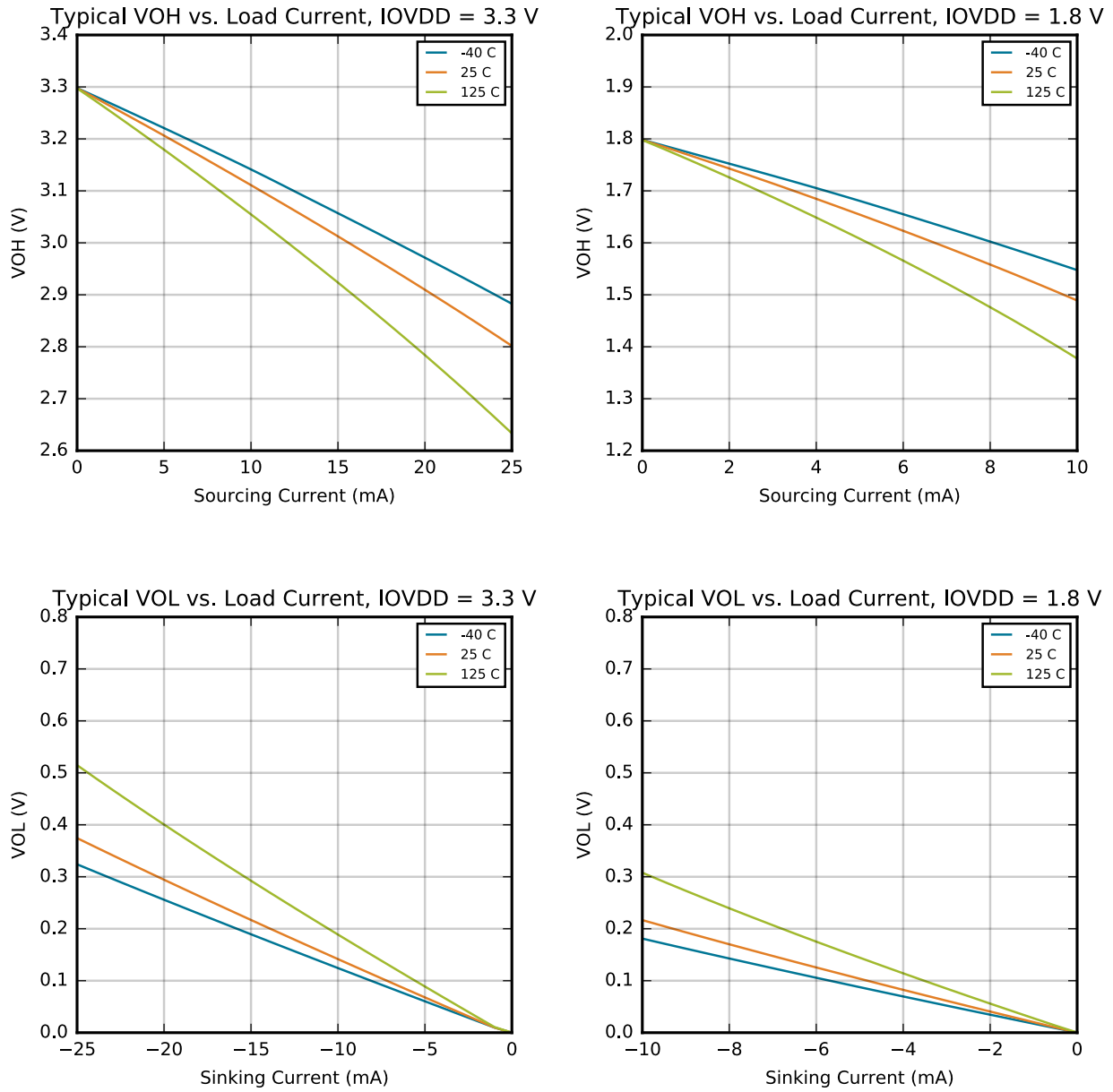


Figure 4.10. VOH and VOL vs. Load Current

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections are shown in the following figures.

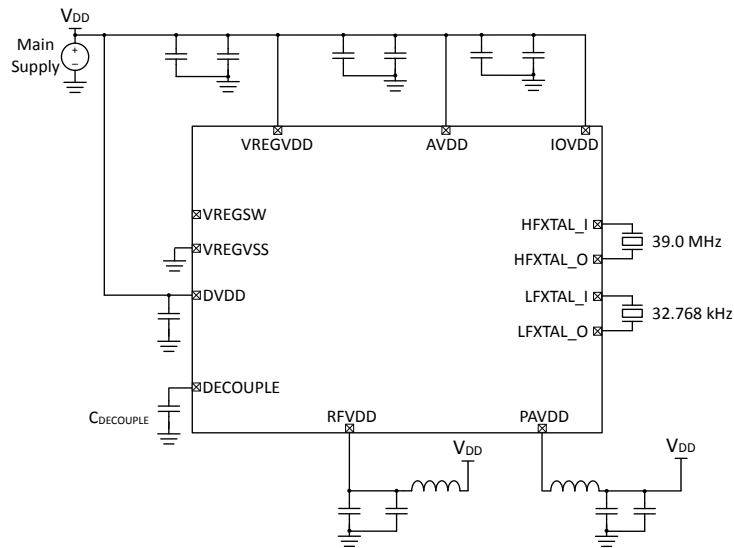


Figure 5.1. EFR32FG23 Typical Application Circuit: Direct Supply Configuration without DCDC

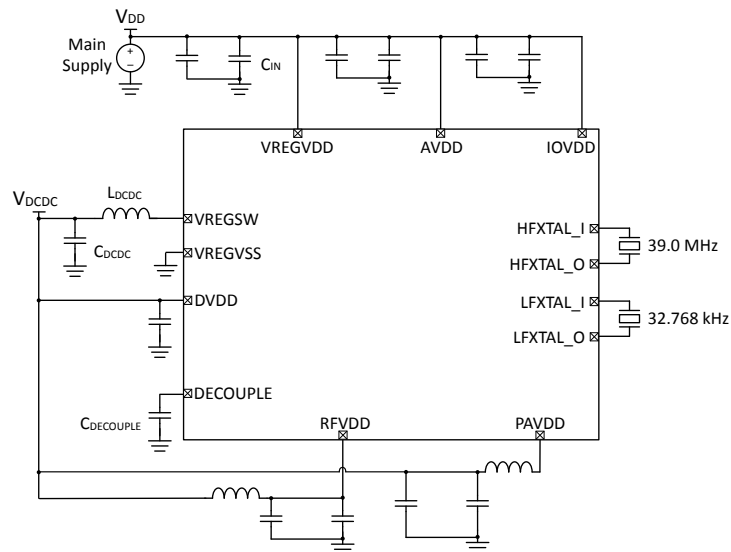


Figure 5.2. EFR32FG23 Typical Application Circuit: DCDC Configuration

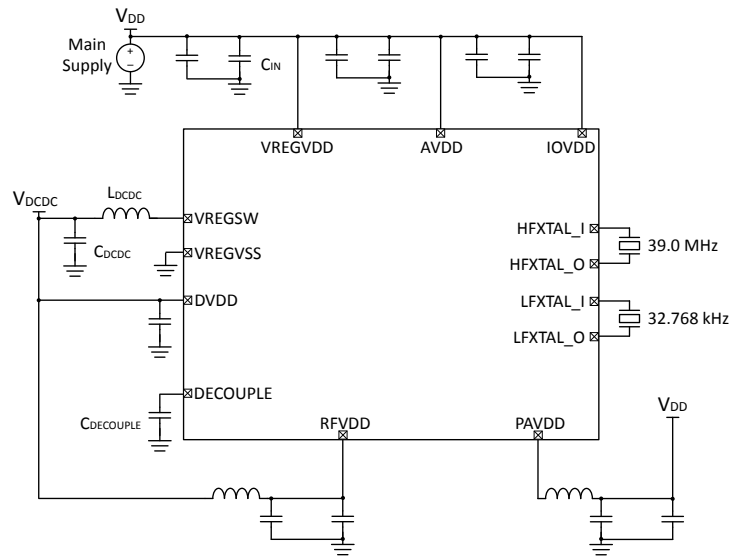


Figure 5.3. EFR32FG23 Typical Application Circuit: DCDC Configuration, PAVDD Powered Separately

5.2 RF Matching Networks

5.2.1 Matching Network for 868 MHz, 915 MHz, and 920 MHz Bands

The recommended RF matching network circuit diagram for the 868 MHz, 915 MHz, and 920 MHz bands at up to +14 dBm TX output power is shown in [Figure 5.4 Typical 868/915/920 MHz RF impedance-matching network circuit, +14 dBm on page 106](#). This supports all frequencies from 868 to 930 MHz. Typical component values are shown in [Table 5.1 868/915/920 MHz Component Values, +14 dBm on page 106](#). Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

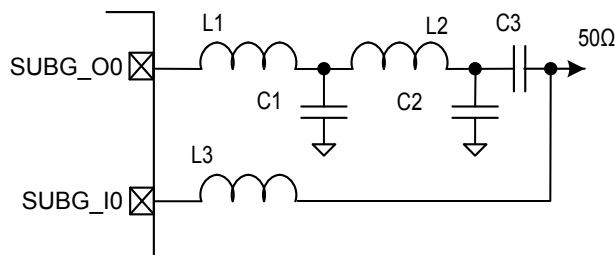


Figure 5.4. Typical 868/915/920 MHz RF impedance-matching network circuit, +14 dBm

Table 5.1. 868/915/920 MHz Component Values, +14 dBm

Designator	Component Value
L1	4.2 nH
C1	5.9 pF
L2	16 nH
C2	2.1 pF
C3	220 pF
L3	18 nH

The recommended RF matching network circuit diagram for the 868 MHz, 915 MHz, and 920 MHz bands at up to +20 dBm TX output power is shown in [Figure 5.5 Typical 868/915/920 MHz RF impedance-matching network circuit, +20 dBm on page 107](#). This supports all frequencies from 868 to 930 MHz. Typical component values are shown in [Table 5.2 868/915/920 MHz Component Values, +20 dBm on page 107](#). Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

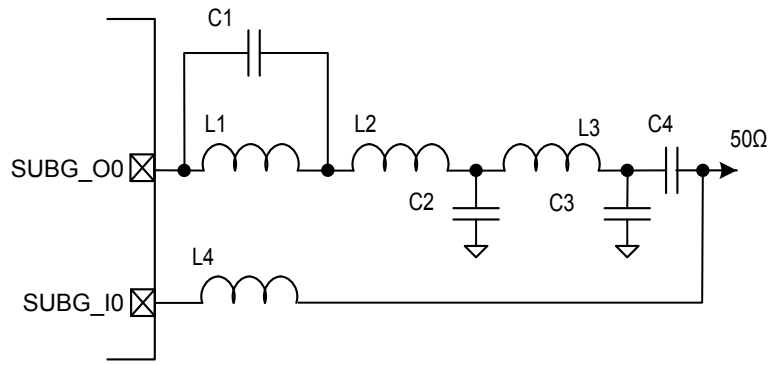


Figure 5.5. Typical 868/915/920 MHz RF impedance-matching network circuit, +20 dBm

Table 5.2. 868/915/920 MHz Component Values, +20 dBm

Designator	Component Value
L1	1.5 nH
C1	1.9 pF
L2	1.3 nH
C2	7.2 pF
L3	13 nH
C3	1.3 pF
C4	220 pF
L4	18 nH

5.2.2 Matching Network for 470 MHz Band

The recommended RF matching network circuit diagram for 470 MHz band applications is shown in [Figure 5.6 Typical 470 MHz Band RF impedance-matching network circuit on page 108](#). This band covers 470 to 510 MHz and is centered at 490 MHz. Typical component values optimized for different power levels are shown in [Table 5.3 470 MHz Band Component Values on page 108](#). Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

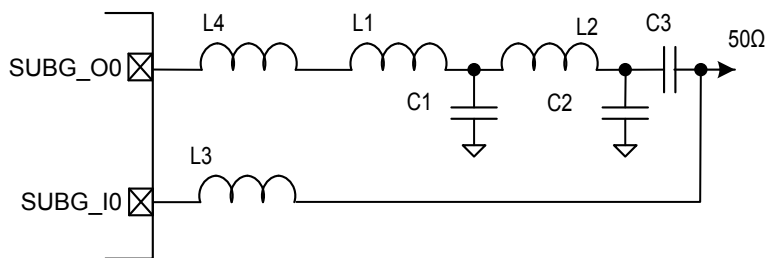


Figure 5.6. Typical 470 MHz Band RF impedance-matching network circuit

Table 5.3. 470 MHz Band Component Values

Designator	Component Value
	+17 dBm
L1	9.1 nH
C1	10 pF
L2	30 nH
C2	7.6 pF
C3	220 pF
L3	68 nH
L4	5.1 nH

5.2.3 Matching Network for 433 MHz Band

The recommended RF matching network circuit diagram for 433 MHz Band applications is shown in [Figure 5.7 Typical 433 MHz Band RF impedance-matching network circuit on page 109](#). Typical component values optimized for different power levels are shown in [Table 5.4 433 MHz Band Component Values on page 109](#). Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

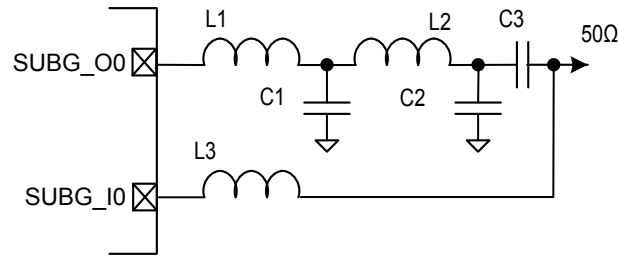


Figure 5.7. Typical 433 MHz Band RF impedance-matching network circuit

Table 5.4. 433 MHz Band Component Values

Designator	Component Value
	+10 dBm
L1	20 nH
C1	8.5 pF
L2	39 nH
C2	4.6 pF
C3	220 pF
L3	82 nH

5.2.4 Matching Network for 315 MHz Band

The recommended RF matching network circuit diagram for 315 MHz Band applications is shown in [Figure 5.8 Typical 315 MHz Band RF impedance-matching network circuit on page 110](#). Typical component values optimized for different power levels are shown in [Table 5.5 315 MHz Band Component Values on page 110](#). Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

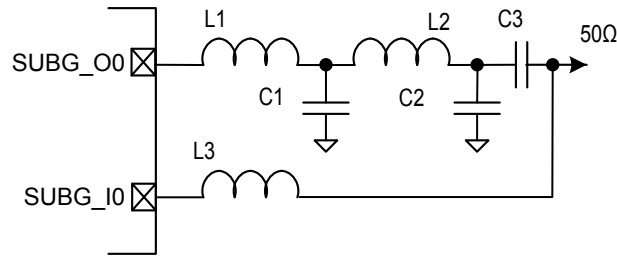


Figure 5.8. Typical 315 MHz Band RF impedance-matching network circuit

Table 5.5. 315 MHz Band Component Values

Designator	Component Value
	+10 dBm
L1	22 nH
C1	15 pF
L2	47 nH
C2	9.2 pF
C3	220 pF
L3	150 nH

5.2.5 Matching Network for 169 MHz Band

The recommended RF matching network circuit diagram for 169 MHz Band applications is shown in [Figure 5.9 Typical 169 MHz Band RF impedance-matching network circuit on page 111](#). Typical component values optimized for different power levels are shown in [Table 5.6 169 MHz Band Component Values on page 111](#). Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

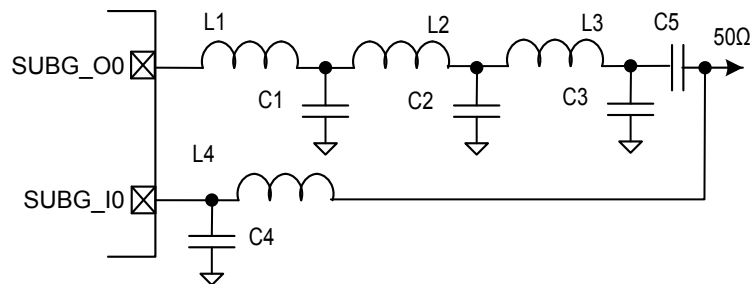


Figure 5.9. Typical 169 MHz Band RF impedance-matching network circuit

Table 5.6. 169 MHz Band Component Values

Designator	Component Value	
	+10 dBm	+20 dBm
L1	22 nH	12 nH
C1	33 pF	62 pF
L2	47 nH	40 nH
C2	27 pF	27 pF
L3	51 nH	51 nH
C3	15 pF	16 pF
L4	220 nH	220 nH
C4	2.6 pF	2.6 pF
C5	220 pF	220 pF

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2: "EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN40 Device Pinout

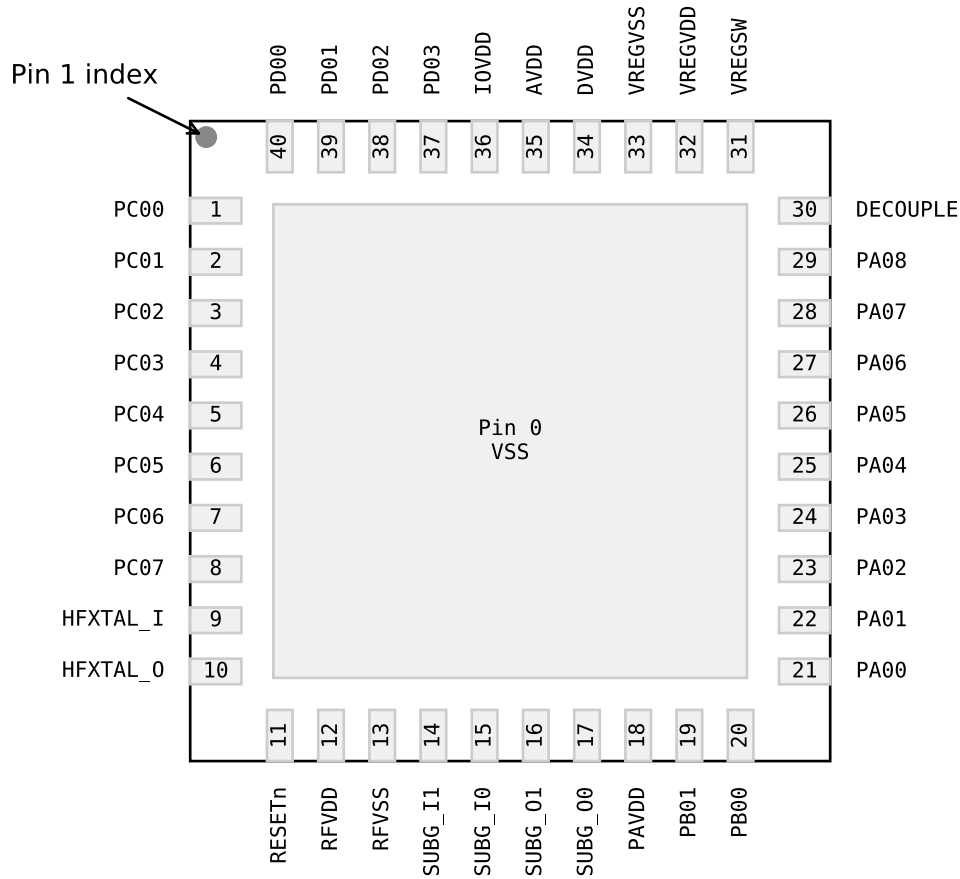


Figure 6.1. QFN40 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.4 Alternate Function Table](#), [6.5 Analog Peripheral Connectivity](#), and [6.6 Digital Peripheral Connectivity](#).

Table 6.1. QFN40 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency XTAL input pin	HFXTAL_O	10	High Frequency XTAL output pin

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	11	Reset pin (active low)	RFVDD	12	RF VDD supply pin
RFVSS	13	RF VSS ground pin	SUBG_I1	14	Sub-GHz Input 1
SUBG_I0	15	Sub-GHz Input 0	SUBG_O1	16	Sub-GHz Output 1
SUBG_O0	17	Sub-GHz Output 0	PAVDD	18	PA VDD supply pin
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decoupling Capacitor pin
VREGSW	31	DCDC output (Inductor) pin	VREGVDD	32	DCDC input supply pin
VREGVSS	33	DCDC ground pin	DVDD	34	Digital VDD supply pin
AVDD	35	Analog VDD supply pin	IOVDD	36	IO VDD supply pin
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.2 QFN48 Device Pinout

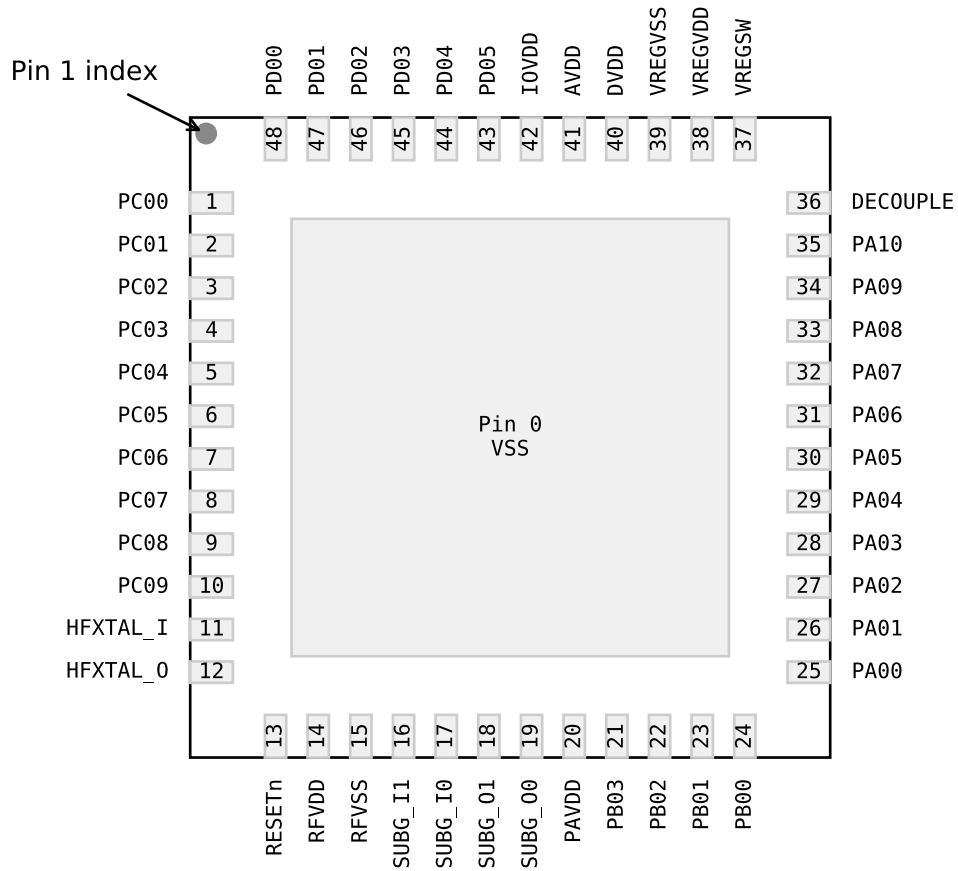


Figure 6.2. QFN48 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.4 Alternate Function Table](#), [6.5 Analog Peripheral Connectivity](#), and [6.6 Digital Peripheral Connectivity](#).

Table 6.2. QFN48 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
PC08	9	GPIO	PC09	10	GPIO
HFXTAL_I	11	High Frequency XTAL input pin	HFXTAL_O	12	High Frequency XTAL output pin
RESETn	13	Reset pin (active low)	RFVDD	14	RF VDD supply pin

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RFVSS	15	RF VSS ground pin	SUBG_I1	16	Sub-GHz Input 1
SUBG_I0	17	Sub-GHz Input 0	SUBG_O1	18	Sub-GHz Output 1
SUBG_O0	19	Sub-GHz Output 0	PAVDD	20	PA VDD supply pin
PB03	21	GPIO	PB02	22	GPIO
PB01	23	GPIO	PB00	24	GPIO
PA00	25	GPIO	PA01	26	GPIO
PA02	27	GPIO	PA03	28	GPIO
PA04	29	GPIO	PA05	30	GPIO
PA06	31	GPIO	PA07	32	GPIO
PA08	33	GPIO	PA09	34	GPIO
PA10	35	GPIO	DECOUPLE	36	Decoupling Capacitor pin
VREGSW	37	DCDC output (Inductor) pin	VREGVDD	38	DCDC input supply pin
VREGVSS	39	DCDC ground pin	DVDD	40	Digital VDD supply pin
AVDD	41	Analog VDD supply pin	IOVDD	42	IO VDD supply pin
PD05	43	GPIO	PD04	44	GPIO
PD03	45	GPIO	PD02	46	GPIO
PD01	47	GPIO	PD00	48	GPIO

6.3 QFN40 with HFCLKOUT Device Pinout

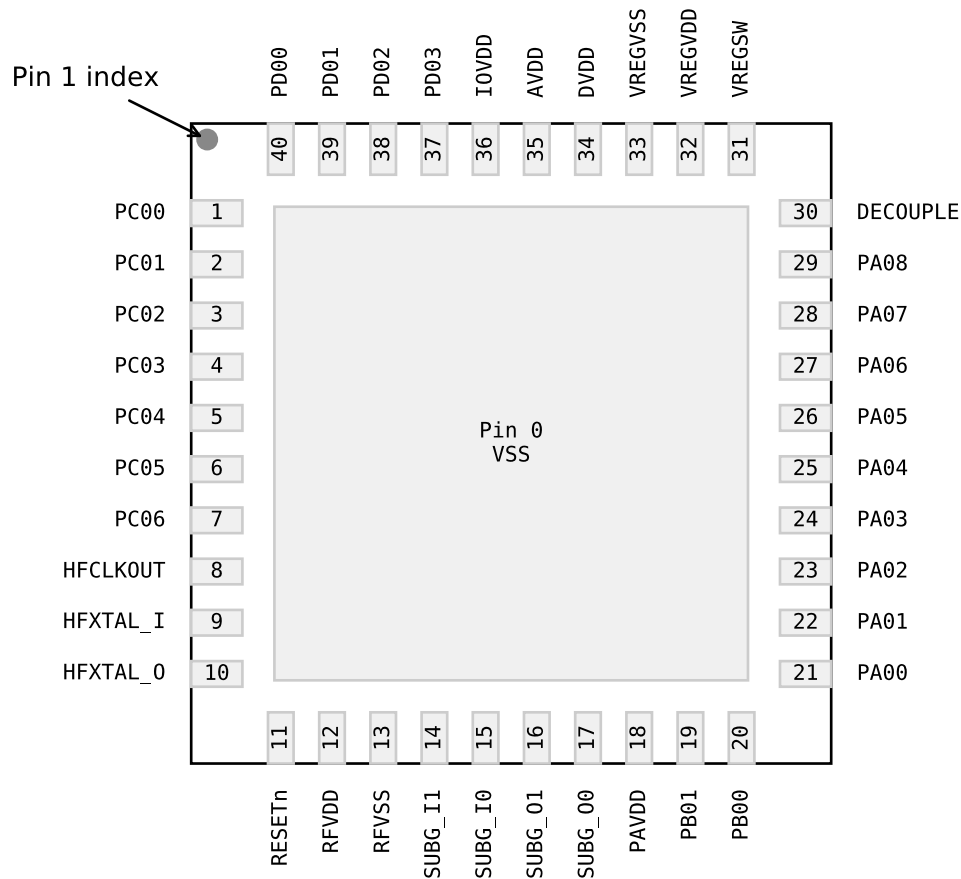


Figure 6.3. QFN40 with HFCLKOUT Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.4 Alternate Function Table](#), [6.5 Analog Peripheral Connectivity](#), and [6.6 Digital Peripheral Connectivity](#).

Table 6.3. QFN40 with HFCLKOUT Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	HFCLKOUT	8	High Frequency clock out pin
HFXTAL_I	9	High Frequency XTAL input pin	HFXTAL_O	10	High Frequency XTAL output pin
RESETn	11	Reset pin (active low)	RFVDD	12	RF VDD supply pin
RFVSS	13	RF VSS ground pin	SUBG_I1	14	Sub-GHz Input 1

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
SUBG_I0	15	Sub-GHz Input 0	SUBG_O1	16	Sub-GHz Output 1
SUBG_O0	17	Sub-GHz Output 0	PAVDD	18	PA VDD supply pin
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decoupling Capacitor pin
VREGSW	31	DCDC output (Inductor) pin	VREGVDD	32	DCDC input supply pin
VREGVSS	33	DCDC ground pin	DVDD	34	Digital VDD supply pin
AVDD	35	Analog VDD supply pin	IOVDD	36	IO VDD supply pin
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.4 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows what functions are available on each device pin.

Table 6.4. GPIO Alternate Function Table

GPIO	Alternate Functions			
PC00	GPIO.EM4WU6		LCD.SEG0	
PC01			LCD.SEG1	
PC02			LCD.SEG2	
PC03			LCD.SEG3	
PC04			LCD.SEG4	
PC05	GPIO.EM4WU7		LCD.SEG5	
PC06			LCD.SEG6	
PC07	GPIO.EM4WU8		LCD.SEG7	
PC08			LCD.SEG18	
PC09	GPIO.THMSW_EN		LCD.SEG19	
PB03	GPIO.EM4WU4		LCD.SEG17	
PB02			LCD.SEG16	
PB01	GPIO.EM4WU3	VDAC0.CH1_MAIN_OUT	LCD.SEG15	
PB00		VDAC0.CH0_MAIN_OUT	LCD.SEG14	
PA00		IADC0.VREFP	LCD.SEG8	
PA01	GPIO.SWCLK		LCD.SEG9	
PA02	GPIO.SWDIO			
PA03	GPIO.SWV	LESENSE.EN_0		
	GPIO.TDO			
	GPIO.TRACEDATA0			
PA04	GPIO.TDI	LESENSE.EN_1	LCD.SEG10	
	GPIO.TRACECLK			
PA05	GPIO.TRACEDATA1	LESENSE.EN_2	LCD.SEG11	
	GPIO.EM4WU0			
PA06	GPIO.TRACEDATA2		LCD.LCD_CP	
PA07	GPIO.TRACEDATA3		LCD.SEG12	
PA08			LCD.SEG13	
PD05	GPIO.EM4WU10		LCD.COM3	
PD04			LCD.COM2	
PD03			LCD.COM1	
PD02	GPIO.EM4WU9		LCD.COM0	

GPIO	Alternate Functions			
PD01		LFXO.LFXTAL_I		
		LFXO.LF_EXTCLK		
PD00		LFXO.LFXTAL_O		

6.5 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Table 6.5. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	CH0_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.6 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 6.6. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
EUSART2.CS			Available	Available
EUSART2.CTS			Available	Available
EUSART2.RTS			Available	Available
EUSART2.RX			Available	Available
EUSART2.SCLK			Available	Available
EUSART2.TX			Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available		
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
I2C1.SDA			Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4	Available	Available	Available	Available
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LESENSE.CH0OUT	Available	Available		
LESENSE.CH1OUT	Available	Available		
LESENSE.CH2OUT	Available	Available		
LESENSE.CH3OUT	Available	Available		
LESENSE.CH4OUT	Available	Available		
LESENSE.CH5OUT	Available	Available		
LESENSE.CH6OUT	Available	Available		
LESENSE.CH7OUT	Available	Available		
LESENSE.CH8OUT	Available	Available		
LESENSE.CH9OUT	Available	Available		
LESENSE.CH10OUT	Available	Available		
LESENSE.CH11OUT	Available	Available		
LESENSE.CH12OUT	Available	Available		
LESENSE.CH13OUT	Available	Available		
LESENSE.CH14OUT	Available	Available		
LESENSE.CH15OUT	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available

7. QFN40 Package Specifications

7.1 QFN40 Package Dimensions

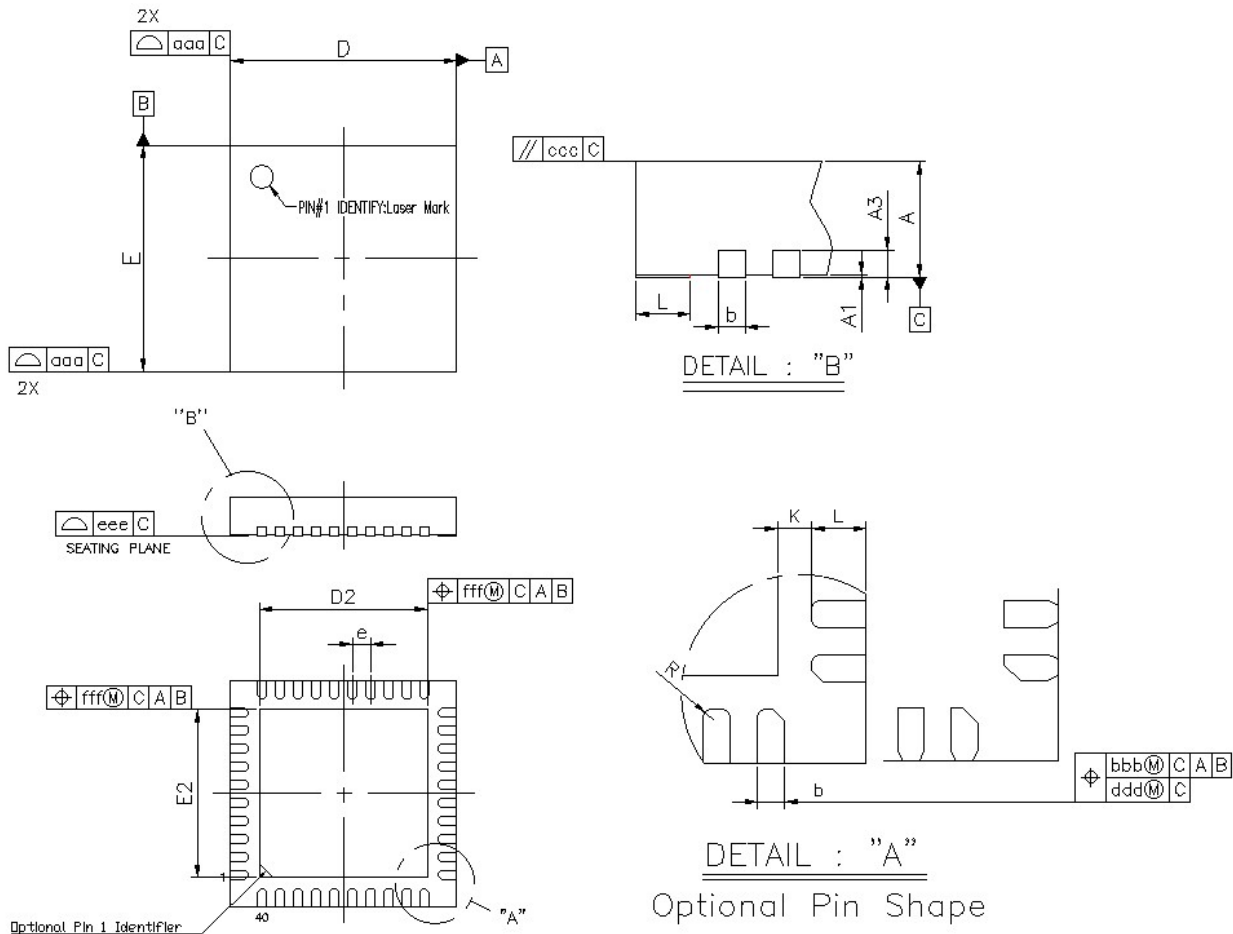


Figure 7.1. QFN40 Package Drawing

Table 7.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

7.2 QFN40 PCB Land Pattern

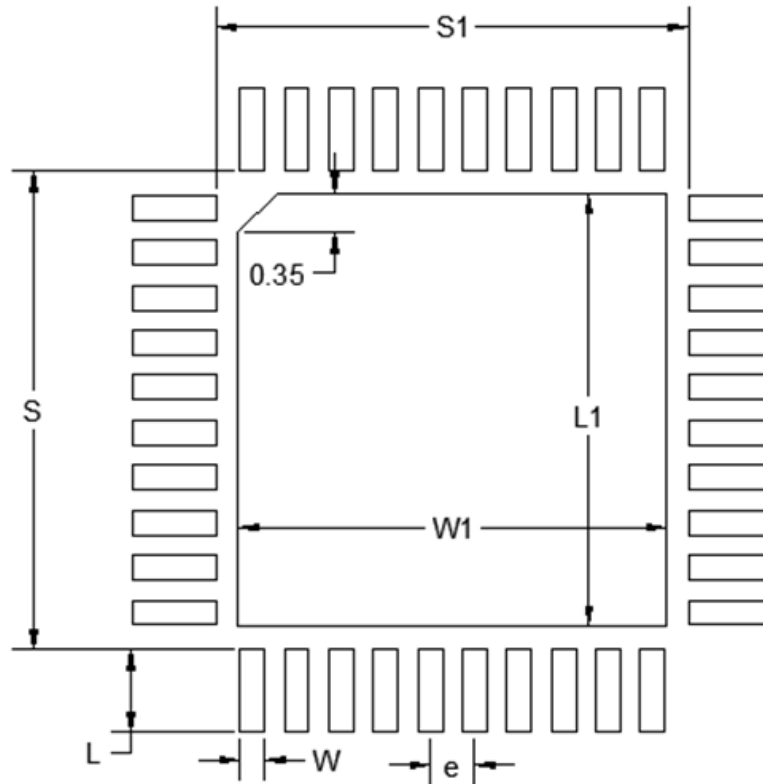


Figure 7.2. QFN40 PCB Land Pattern Drawing

Table 7.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. **Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.**

7.3 QFN40 Package Marking

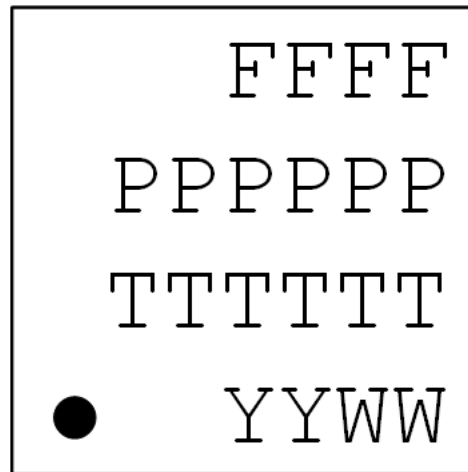


Figure 7.3. QFN40 Package Marking

The package marking consists of:

- FFFF – The product family codes.
 1. Family Code (F | Z)
 2. G (Gecko)
 3. Series (2)
 4. Device Configuration (3)
- PPPPPP – The product option codes.
 - 1. Security (A = Secure Vault Mid | B = Secure Vault High)
 - 2-4. Product Feature Codes
 - 5. Flash (H = 512k | G = 256k | F = 128k)
 - 6. Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. QFN48 Package Specifications

8.1 QFN48 Package Dimensions

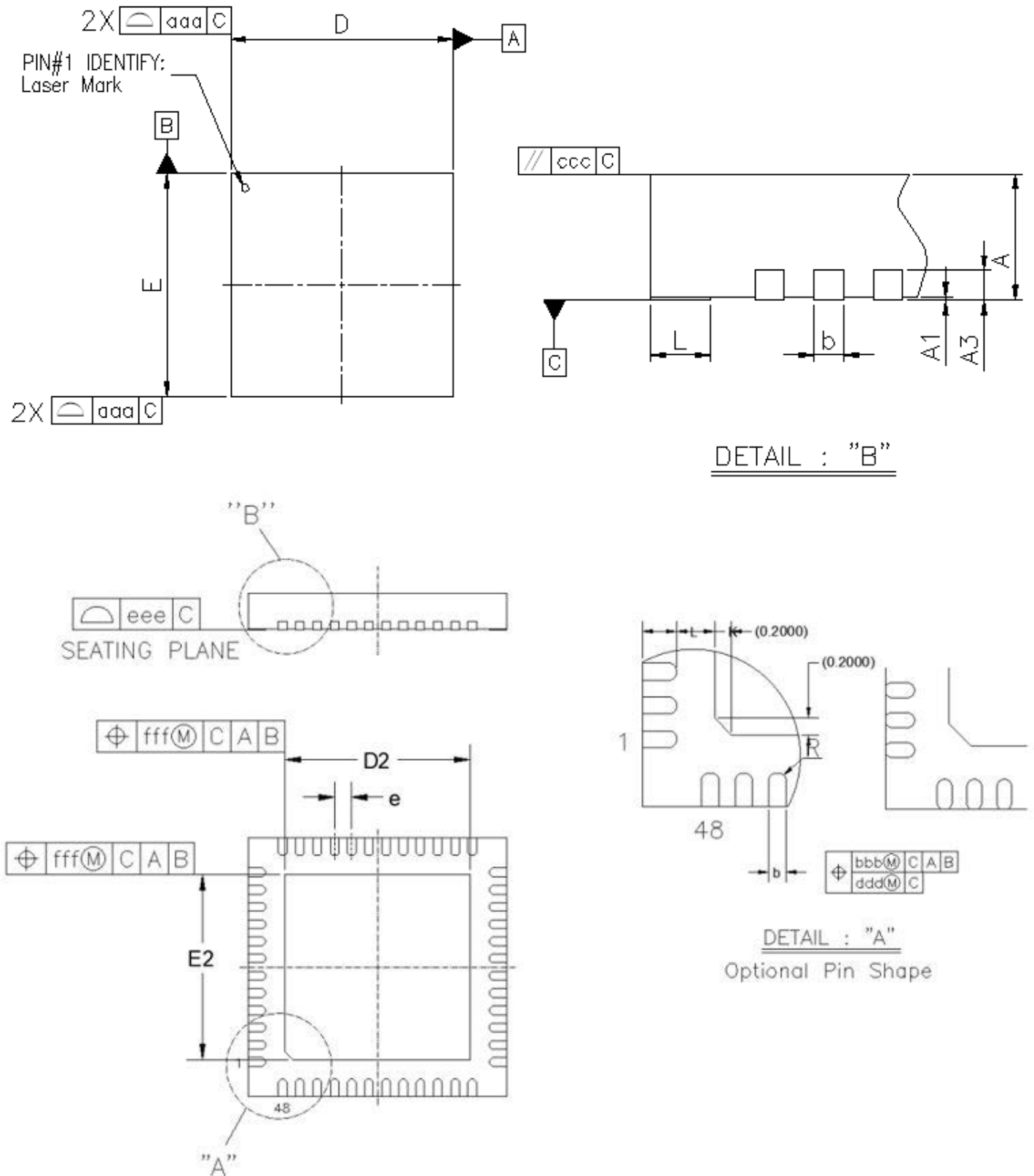


Figure 8.1. QFN48 Package Drawing

Table 8.1. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.2	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e	0.40 BSC		
D2	4.15	4.30	4.45
E2	4.15	4.30	4.45
L	0.30	0.4	0.50
K	0.20	—	—
R	0.075	—	—
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

8.2 QFN48 PCB Land Pattern

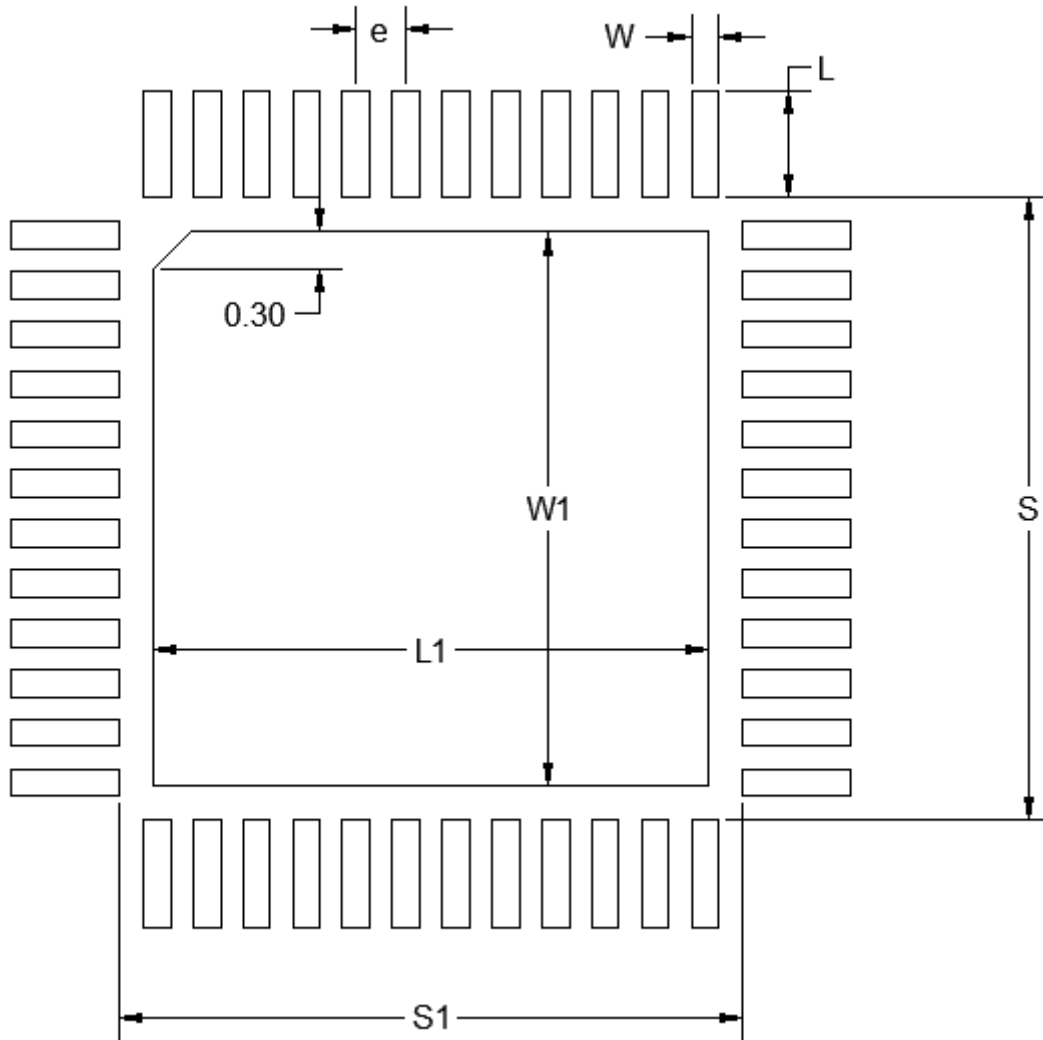


Figure 8.2. QFN48 PCB Land Pattern Drawing

Table 8.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
L	0.86
W	0.22
e	0.40
S	5.01
S1	5.01
L1	4.45
W1	4.45

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 1.10mm x 1.10mm openings on 1.30mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. **Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.**

8.3 QFN48 Package Marking

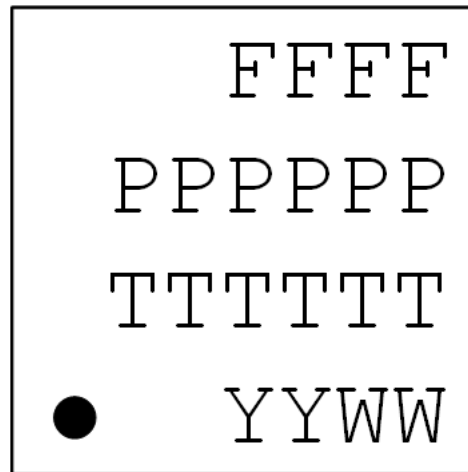


Figure 8.3. QFN48 Package Marking

The package marking consists of:

- FFFF – The product family codes.
 1. Family Code (F | Z)
 2. G (Gecko)
 3. Series (2)
 4. Device Configuration (3)
- PPPPPP – The product option codes.
 - 1. Security (A = Secure Vault Mid | B = Secure Vault High)
 - 2-4. Product Feature Codes
 - 5. Flash (H = 512k | G = 256k | F = 128k)
 - 6. Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

9. Revision History

Revision 0.5

Aug, 2021

- [4.1 Electrical Characteristics](#): Updated specification tables with latest characterization and production test parameters.
- [5.1 Power](#): Corrected typical power supply connections to show proper ferrite placement on PAVDD.
- [Table 5.3 470 MHz Band Component Values on page 108](#): Corrected value C2 to 7.6 pF.
- [Table 5.2 868/915/920 MHz Component Values, +20 dBm on page 107](#): Corrected value L4 to 18 nH.
- Package marking specifications updated.

Revision 0.3

June, 2021

- Updated with latest part numbers.
- Updated terms used in document according to Inclusive Lexicon initiative.
- Added details about Secure Vault High feature set.
- Added specifications for +125 C operation to specification tables.

Revision 0.2

December, 2020

- [Table 3.2 Peripheral Power Subdomains on page 17](#) : Table information corrected, and cross-references to table through document repaired.
- [3.13 Memory Map](#) : Memory map figure corrected.
- [4.1 Electrical Characteristics](#) : Additional characterization data populated, where available.
- Added section: [4.25 Typical Performance Curves](#).
- [Table 6.4 GPIO Alternate Function Table on page 118](#) : Corrected signal names for LESENSE module to remove duplicate "LE-SENSE" text.

Revision 0.1

September, 2020

Initial release.

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