EiceDRIVER™

High voltage gate driver IC

Evaluation Board

EVAL-1EDI60I12AF

Application Note

Revision 1.0, 2014-07-25

Industrial Power Control

Edition 2014-08-05

Published by
Infineon Technologies AG
81726 Munich, Germany

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History: 2014-06 Rev.1.0	
Page or Item	**Subjects (major changes since last revision)**
Revision 1.00	

Table of Contents

Warnings

The described board is an evaluation board dedicated for laboratory environment only. It operates at high voltages. This board must be operated by qualified, skilled personnel familiar with all applicable safety standards.

1 Introduction

The gate driver evaluation board EVAL-1EDI60I12AF was developed to demonstrate the functionalities and key features of Infineon's IGBT gate driver 1EDI60I12AF.

The board is available from Infineon in sampling quantities. Main features of this board are described in the datasheet chapter of this document, whereas the remaining paragraphs provide information intended to enable the customer to copy, modify and qualify the design for production, according to their own specific requirements.

The design of the EVAL-1EDI60I12AF was performed with respect to the environmental conditions described in this document. The design was tested as described in this document, but not qualified regarding manufacturing, lifetime or over the full range of ambient operating conditions.

The boards provided by Infineon are subjected to functional testing only.

Due to their purpose Evaluation Boards are not subjected to the same procedures regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Discontinuation (PD) as regular products. The Evaluation Boards are intended for development support only and should not be used directly as reference designs for volume production.

See Legal Disclaimer and Warnings for further restrictions on Infineon's warranty and liability.

2 Design features

This chapter provides an overview of the main features, the main specifications and pin assignments as well as mechanical dimensions.

2.1 Main features

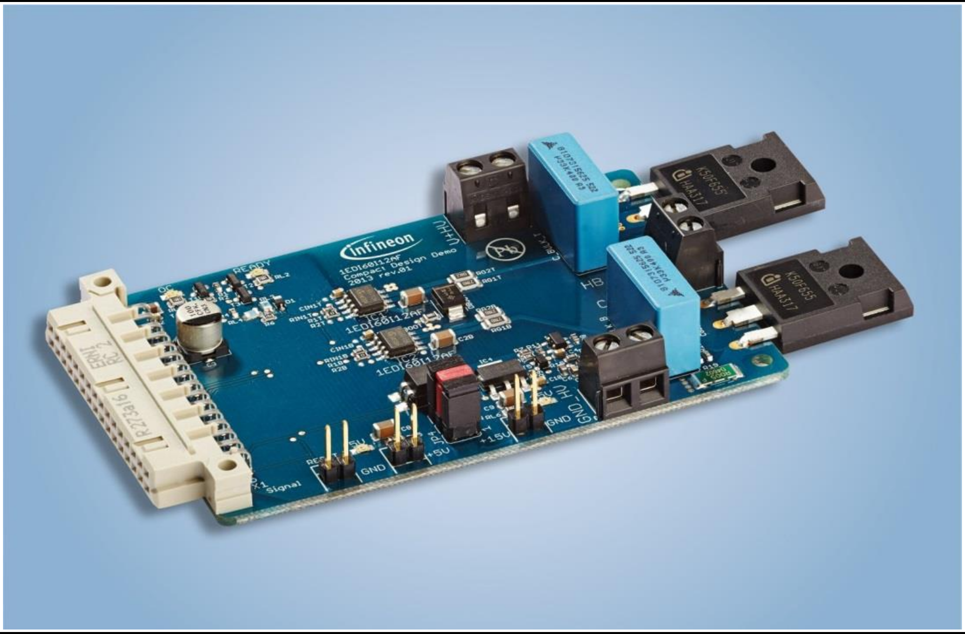


Figure 2-1: Top view of the EVAL-1EDI60I12AF

The EVAL-1EDI60I12AF contains two Infineon 1EDI60I12AF single channel IGBT gate driver ICs and two Infineon IGBTs IKW50N65F5.

The major features of the evaluation board are:

- Short circuit protection
- Current measurement
- Under voltage lock-out
- Bootstrap functionality for the high side gate driver
- Possibility of separating input and output side

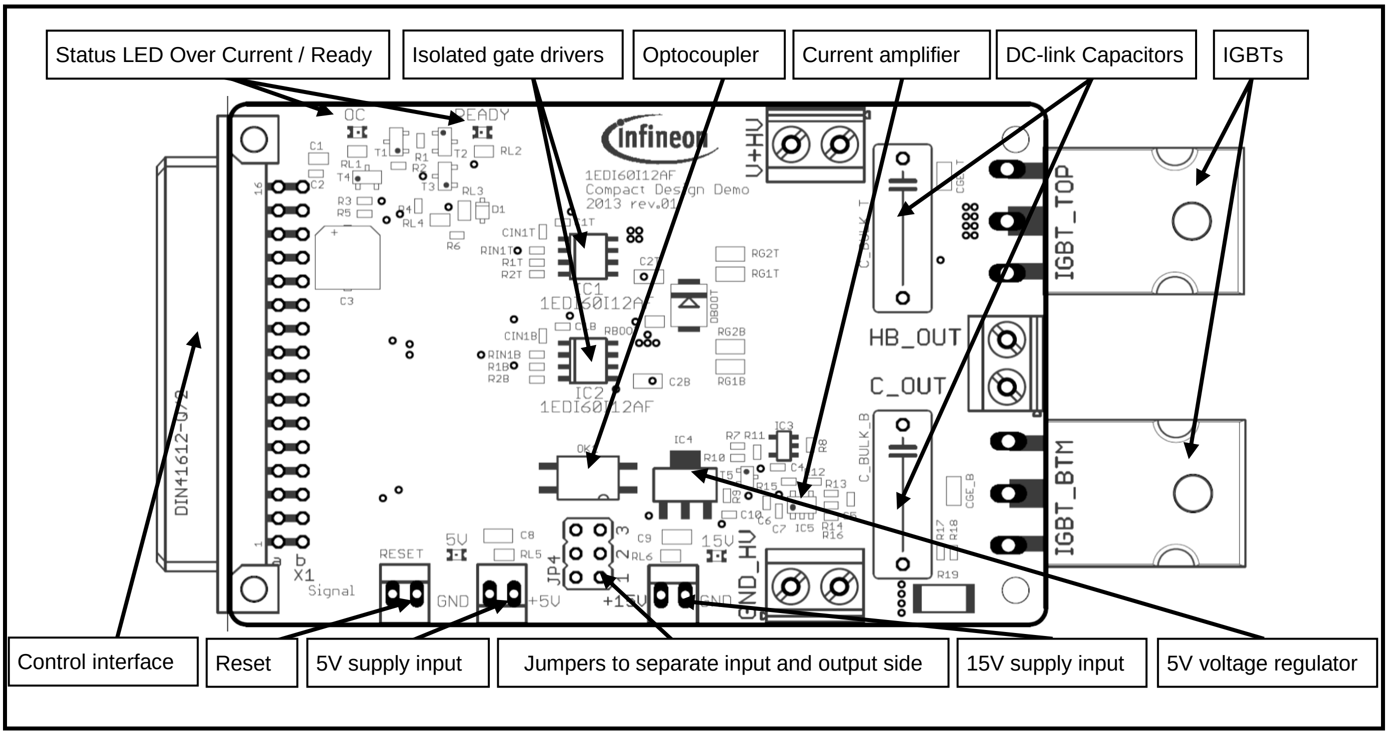


Figure 2-2: PCB overview

2.2 Main specifications

All values listed in the table below are values determined at an ambient temperature of 25°C.

Table 2-1

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CC}	15V supply	13.2	15	17.5	V
V_{DC}	High voltage supply*		400	500	V
$I_{Out,pk}$	Single pulse peak output current	-	-	40	A
$I_{Out,rms}$	RMS output current**	-	-	10	A
f_p	Switching frequency	-	50	100	kHz

Note: Please make sure, never to exceed the maximum rated values. Also the performance and quality cannot be guaranteed when using the board with all parameters at maximum rated values at the same time.

* High voltage supply is limited by the IGBTs used and the DC link capacitors. If higher supply voltage is required, these parts should be replaced by parts with a higher voltage rating. The gate drivers are capable of operating up to peak voltage levels of 1200V. However, note that the board's layout was not tested for voltages exceeding 600V.

** Use of an appropriate heat sink for IGBT devices should be considered in case of continuous operation with currents higher than approximately $2A_{rms}$.

2.3 Pin assignment

Table 2-2 summarizes the connections and pins of the board with all references correlated to the overview given in Figure 2-2.

Table 2-2

Connector name	Pin Position	Pin name	Description
RESET	Left terminal	/RST	same as X1-B1
	Right terminal	GND	same as X1-A16
+5V (VCC1)	Right terminal	+5V	positive 5V supply
	Left terminal	GND	5V power supply necessary if input and output side are separated
+15V (VCC2)	Left terminal	+15V	positive 15V supply
	Right terminal	GND	
X1	A16	GND	reference for power supplies and input signals
	B1	/RST	Reset input, 0V for circuit reset
	B2	/FLT	Over current output; OC, 0V / 5V
	B7	IN_T	non-inverting input high-side IGBT; 0V off; 5V on
	B8	IN_B	non-inverting input low-side IGBT; 0V off; 5V on
	B16	VCC	positive 5V supply
GND_HV			reference for high voltage supply Power-GND internally connected to GND
V+HV			positive high voltage supply up to 500V referenced to GND_HV
HB_OUT			Output HV half bridge related to GND_HV
C_OUT			Output filter bulk capacitors center tap

3 Electrical features

3.1 +5V and +15V supply voltages

The driver's high side voltage has to be supplied externally. The 5V supply voltage, required for on board circuits, is generated internally by an Infineon voltage regulator. The evaluation board does not provide an over voltage supply monitoring, therefore the user has to ensure, that the voltages remain within the correct range. Voltages exceeding the maximum values may lead to damage of the IGBT drivers and other circuitries.

The +5V supply is generated on the board by using the Infineon voltage regulator TLE4264G. The regulator is used to supply input as well as output circuits of the evaluation board. In case a complete input to output separation is required, the supply voltage must be provided externally.

The availability of the supply voltages is individually indicated for both power supplies via the green status LEDs. For proper operation of the evaluation board, care has to be taken that both power supplies are available and stable.

The output part of the high-side gate driver is supplied by bootstrap using an external ultra-fast diode. To ensure that the bootstrap capacitor is charged before the high side IGBT is switched on, the low side IGBT has to be switched on for at least 250µs.

3.2 Under voltage lockout

The +15V supply as well as the +5V supply are monitored by the 1EDI60I12AF gate drivers. In case of an under voltage, the driver's output is switched off until both input voltages are higher than the required thresholds.

The thresholds for the +5V supply typically are V_{CCUV+} = 2.85 V on a positive slope and V_{CCUV-} = 2.75 V on a negative slope.
The thresholds for the +15V supply typically are V_{BSUV+} = 12 V on a positive slope and V_{BSUV-} = 11.1 V on a negative slope.

3.3 Short circuit detection

The 1EDI60I12AF evaluation board provides short circuit detection by measuring the voltage drop across a 5mΩ shunt as depicted in Figure 3-1. This voltage drop is compared to a fixed voltage level of 254.5mV by the comparator circuit sketched in Figure 3-2. If the current reaches a value of typ. 50A, a short circuit is detected and the gate driver inputs HIN and LIN are disabled. IN– inputs are pulled high which means that PWM signals at IN+ have no effect and the driver outputs are switched off. This state is reported by the OC LED. The OC event is latched by the on-board flip-flop circuit as given in Figure 3-3 and must be reset by switching the RESET signal to ground. As can be seen in Figure 3-2, the fault signal is fed from the output part of the board to the input part utilizing an optocoupler. This allows operating the over-current protection circuit even if the input to output separation of the board is used.

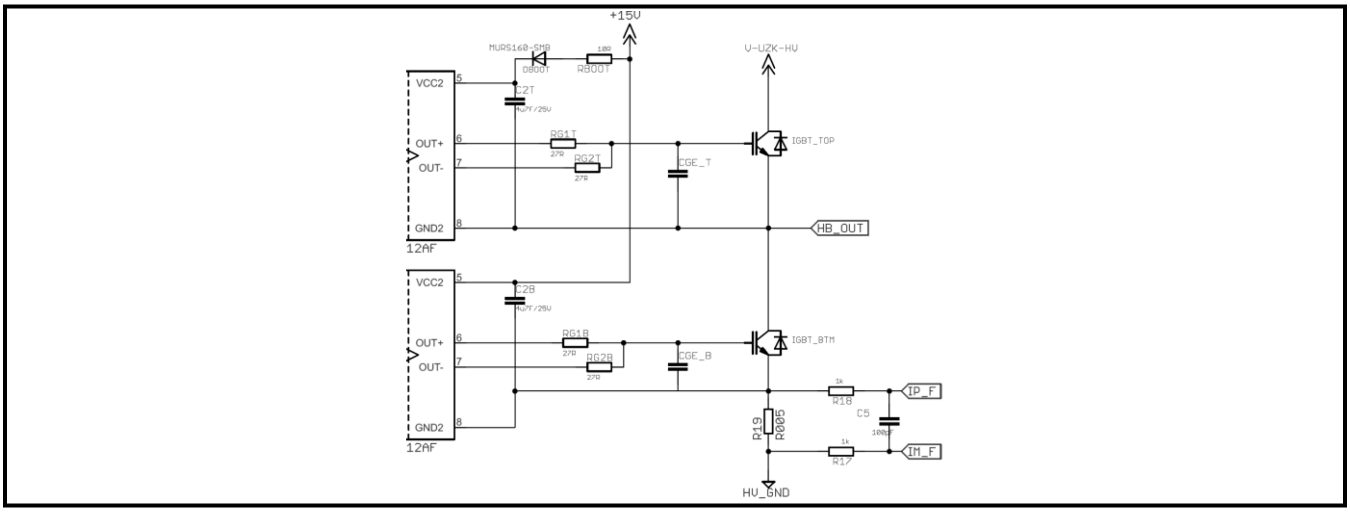


Figure 3-1: Shunt - R19- connection in the power circuit

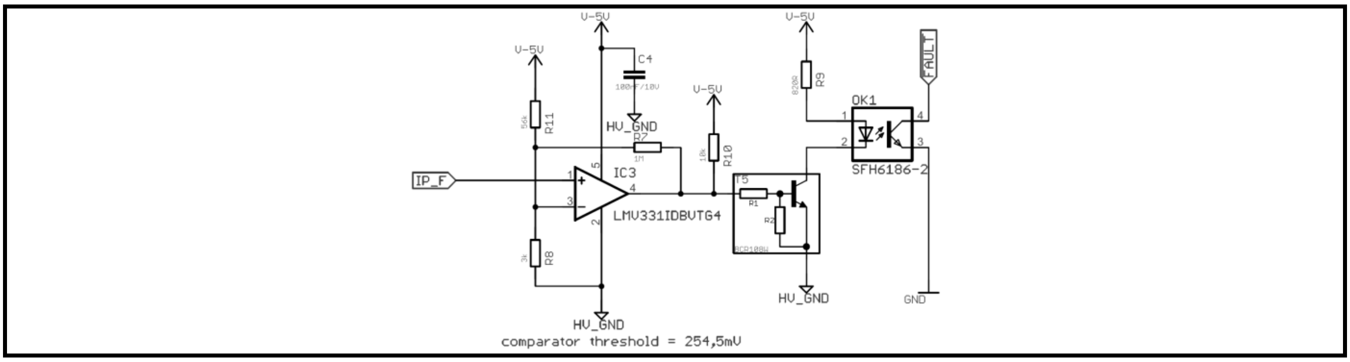


Figure 3-2: Over current comparator circuit and Error signaling

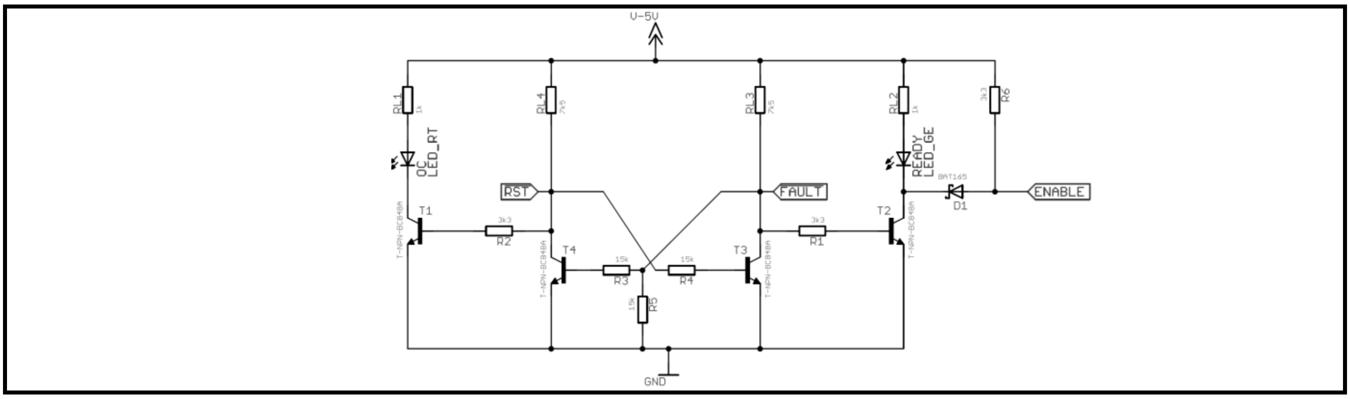


Figure 3-3: Fault flip-flop latch circuit

Figure 3-4 includes the signals of the low-side driver along with current and voltages for the IGBT during short circuit with 20µH inductor connected between HB_OUT and V+HV.

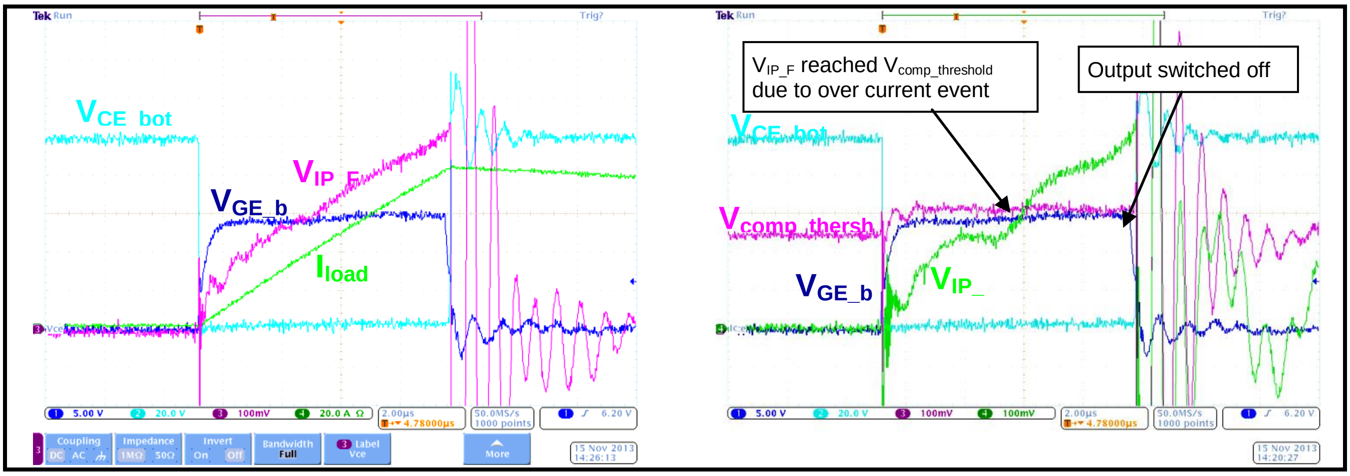


Figure 3-4: Detection signals, IGBT collector current, Gate- and Collector-Emitter voltage during short circuit event

The experiment reveals a delay of approximately 2.8µs between the overcurrent detection and the output being switch off. During this delay time, the current continues to rise until the IGBT switches off. Depending on the inductance of the short circuit loop, the current may rise to rather high values which should be considered when using the test board in connection with sensitive loads, respectively other external circuits.

3.4 Current sense amplifier

The EVAL-1EDI60I12AF provides an operational amplifier which amplifies the voltage drop across the shunt with a gain of 11. The amplified voltage is available to the user at connector X1 pins A9 and B9. Figure 3-5 holds the schematic details of the amplifier setup.

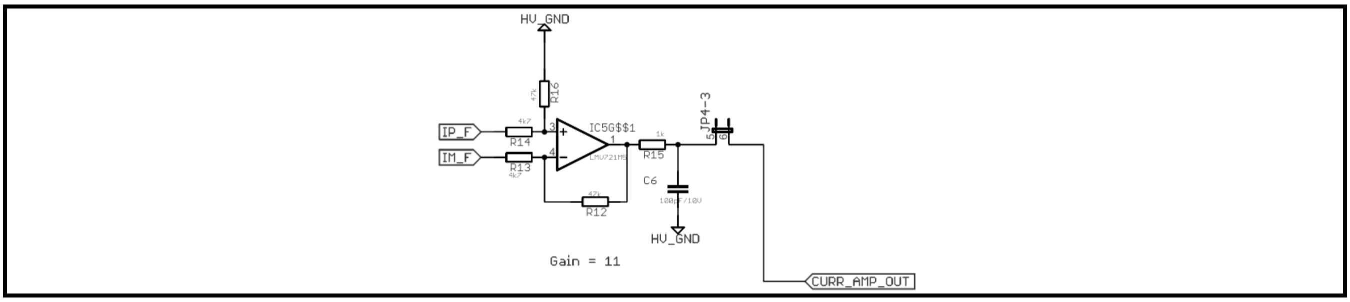


Figure 3-5: Current sense amplifier

The amplified voltage as a function of load current results to be:

$$V_{current\_amp\_out} = R_{shunt} \cdot I_{shunt} \cdot 11 .$$

The scope plot in Figure 3-6 gives an insight to the amplifier's output.

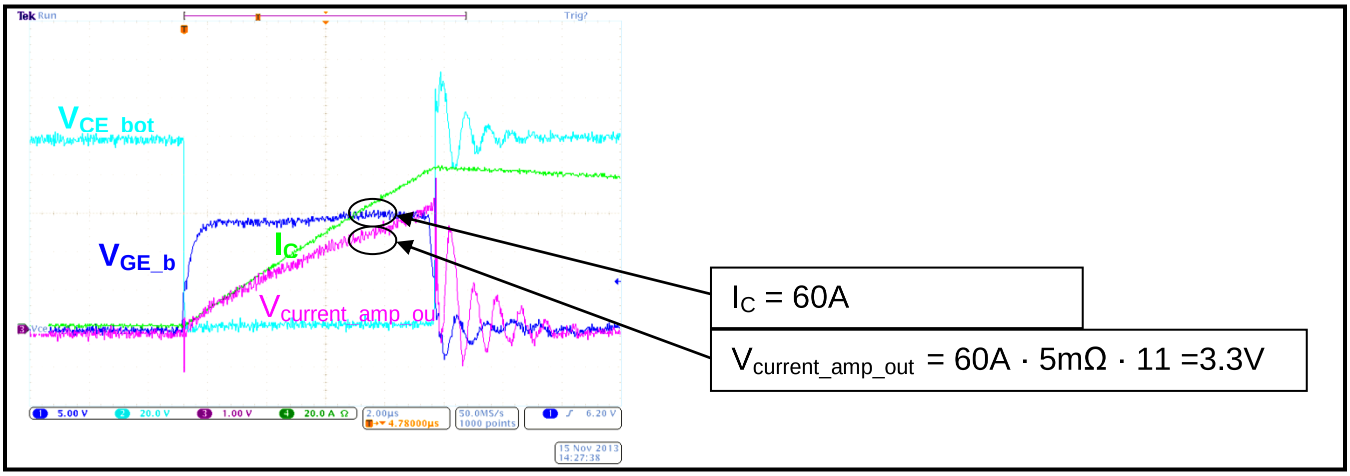
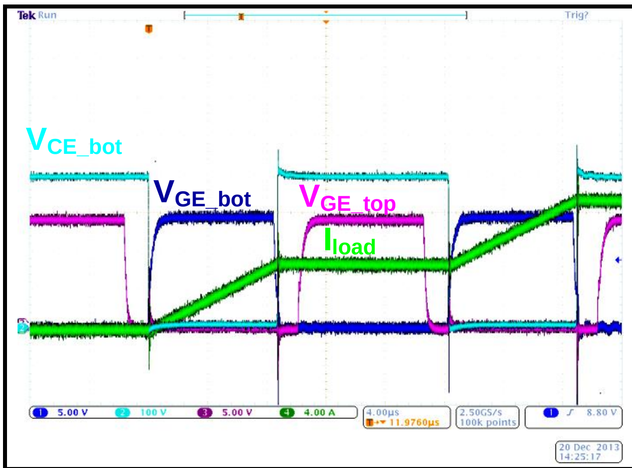


Figure 3-6: Current sense amplifier output and corresponding load current

3.5 IGBT turn – on / off

The 1EDI60I12AF provides separate driver source output and driver sink output signals. These allow independent control of IGBT turn-on respectively turn-off behavior. It can be seen in Figure 3-1Figure 3-7 that the evaluation board is equipped with independent gate resistors RG1B, RG1T, RG2B and RG2T. The resistors used in default configuration have a value of 27Ω. The values can be modified by the user in order to obtain a required switching behavior. It should be noted that the deviation from the default values may result in increased switching noise or higher switching losses. Examples of switching transients with default gate resistors determined in a double pulse test are depicted in Figure 3-7.



Switching sequence with 2 pulses:
Supply Input: 400V
Switching frequency = 50 kHz
Duty cycle = 50%
Dead time = 1.5 µs
500µH inductor connected between HB_OUT and V+HV

CH1 V_{GE_bot} 5V/div **CH2 V_{CE_bot} 100V/div**
CH3 V_{GE_top} 5V/div **CH4 I_{load} 4A/div**
Time 4µs/div

Figure 3-7: Example of waveforms during double pulse switching sequence

A more detailed view to the transient switching behavior is given in Figure 3-8.

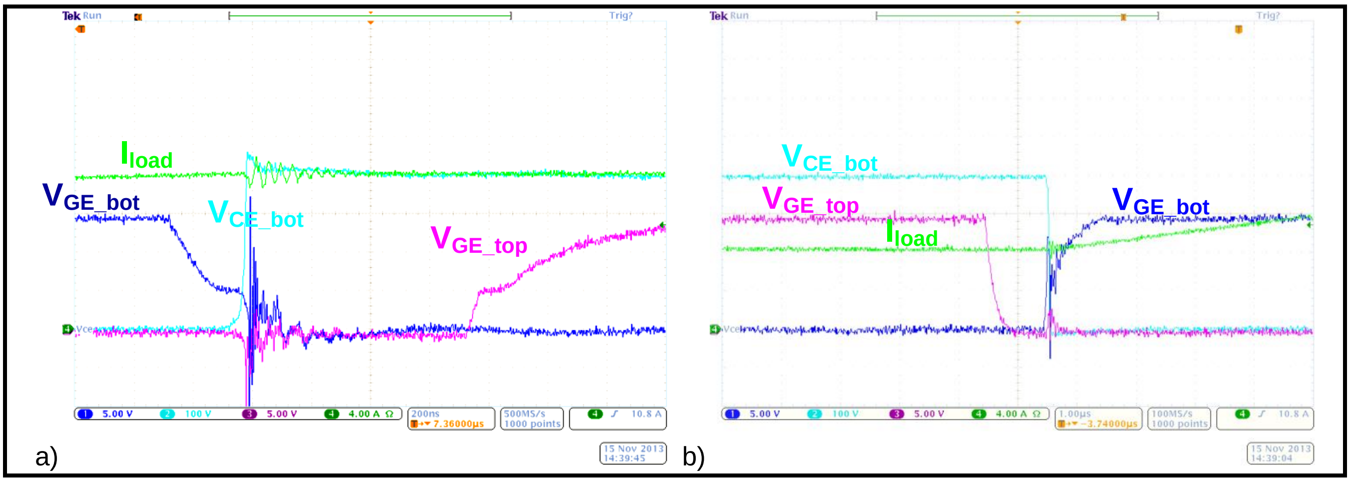


Figure 3-8: Switching transients; a) turning off the low-side IGBT and turning on the high-side IGBT b) vice versa, time scale is 200 ns/div

3.6 DC-Link capacitors

The evaluation board provides a split DC-Link capacitor in order to enable connection of loads which require ac voltages and bi-directional currents. In such a case, the load can be connected between HB_OUT and C_OUT output which enables voltage inversion across the load. An example of possible bi-directional waveforms is displayed in Figure 3-9. It should be noted, that in case of operation with bi-directional currents, the current amplifier output only provides information about the current through the low-side IGBT. In addition to that, the overcurrent protection circuit may not work properly in case of large negative current shifts. In case of symmetrical current waveforms, the overcurrent protection should not be affected but it should be noted that an overcurrent would be detected only on the positive part of the current waveform.

Due to the available space, only rather small DC-Link capacitors of 330nF are available on the board. If a larger DC-Link capacity is necessary, it has to be connected to the connectors V+HV, GND_HV and C_OUT externally.

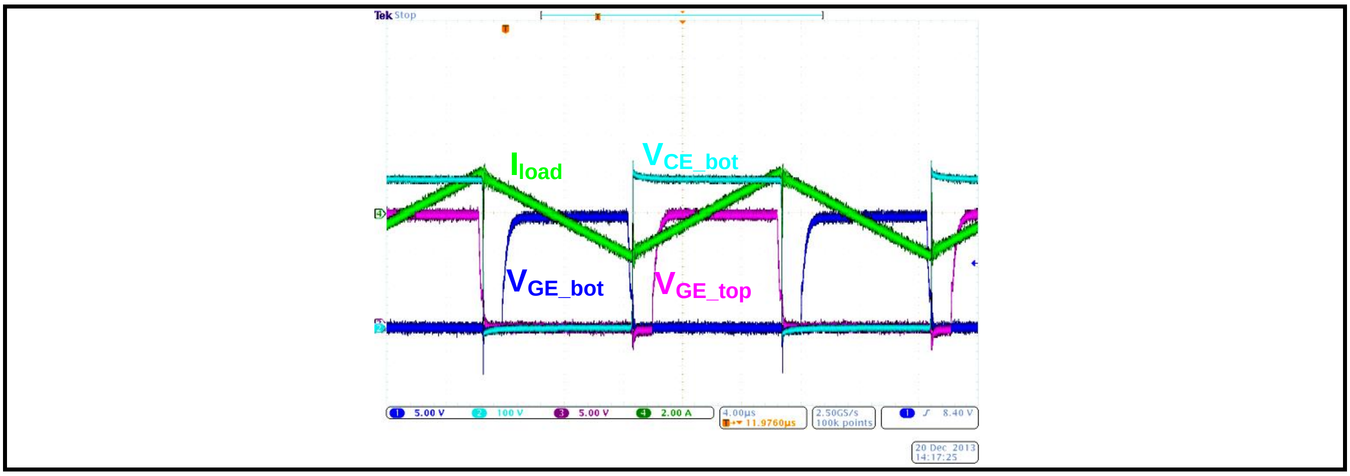


Figure 3-9: Example of an operation with bi-directional load current

3.7 Input PWM-Signals

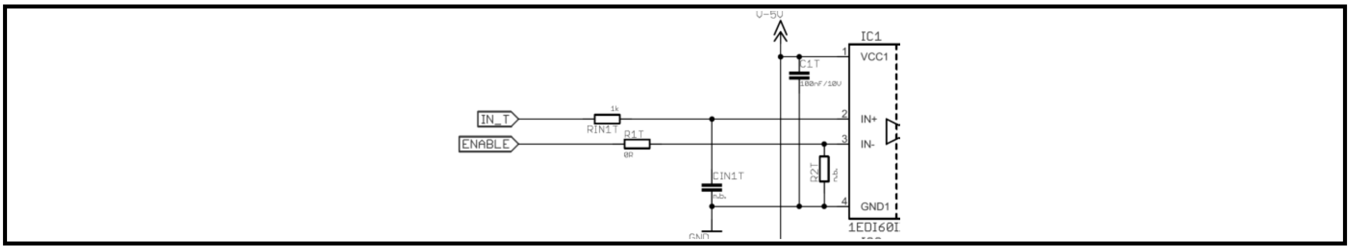


Figure 3-10: Details of the 1EDI60I12AF gate driver input schematic

There is a possibility to use low-pass filters inside the PWM input signals to avoid a turn-on of an IGBT by noise. This feature is not used in this evaluation board due to internal signal filtering of the driver's inputs which are sufficient in most applications. However, there is the possibility to test this feature by changing the resistors RIN1T, RIN1B and using a suitable capacitance value for the capacitors CIN1T, CIN1B as seen in Figure 3-10.

3.8 Separation between input and output side

The 1EDI60I12AF gate driver offers an input to output isolation capability of 1200V. The evaluation board takes advantage of this feature by offering a possibility of input to output separation. This can be done by removing the jumpers marked JP4 on the board as indicated in Figure 3-11. This removes all conductive connections between the input and output side and therefore completely separates the two sides. This procedure also opens the connection between the 5V onboard voltage regulator and the input side circuits. Thus, the +5V for the input side must be supplied from an external, isolated source. In addition to that, the removal of the jumpers opens the connection between the current amplifier output and the connector X1 and therefore the information about the current is not available in case of isolated operation. The overcurrent protection remains functional since the fault signal is fed back to the input side via an optocoupler.

It should be noted that in case of operation without this separation and all jumpers in place, the board requires the +15V supply only.

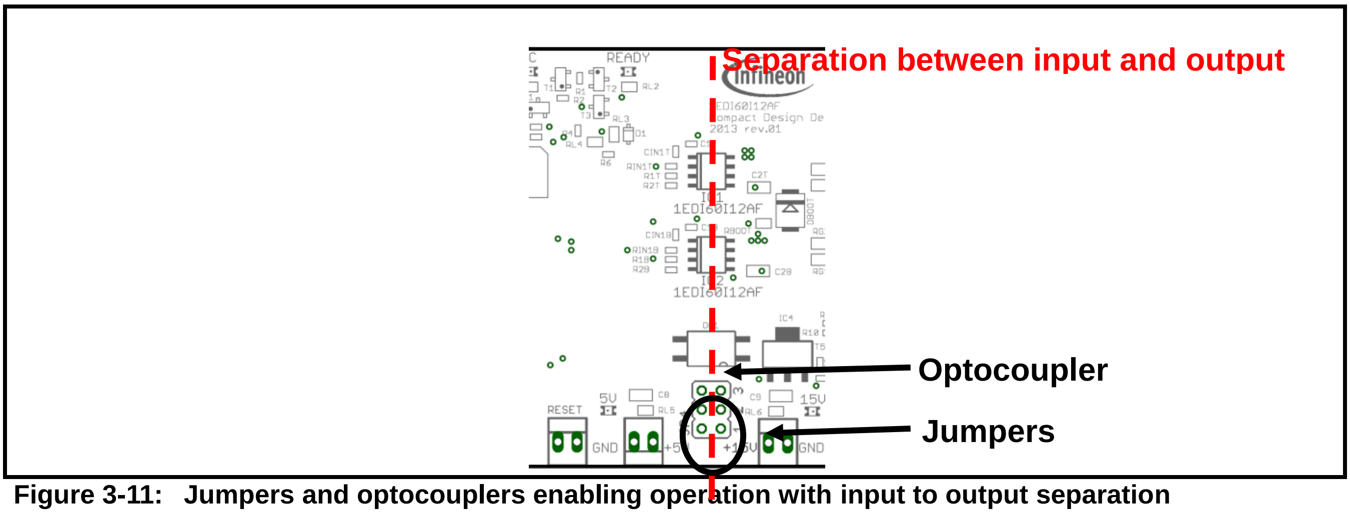


Figure 3-11: Jumpers and optocouplers enabling operation with input to output separation

4 Schematics

To ease reproduction of the board for further use, Figure 4-1 to Figure 4-7 display the detailed schematic of the evaluation board.

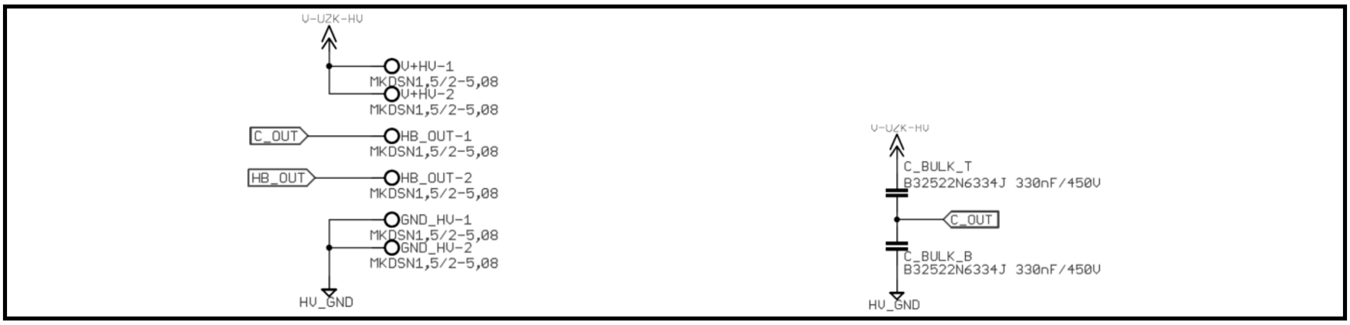


Figure 4-1: HV supply input and DC-Link capacitors

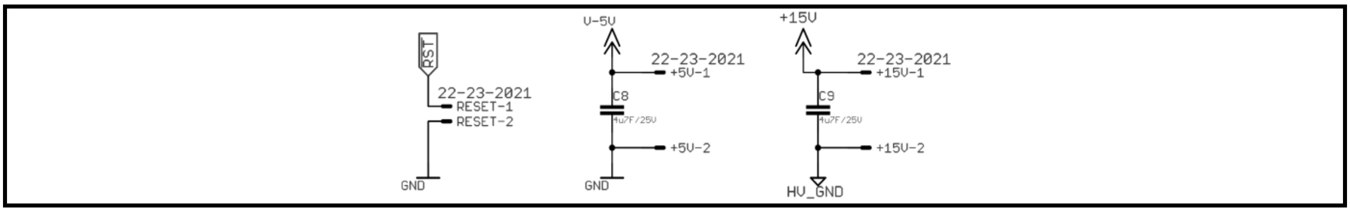


Figure 4-2: LV Supplies and Reset Input

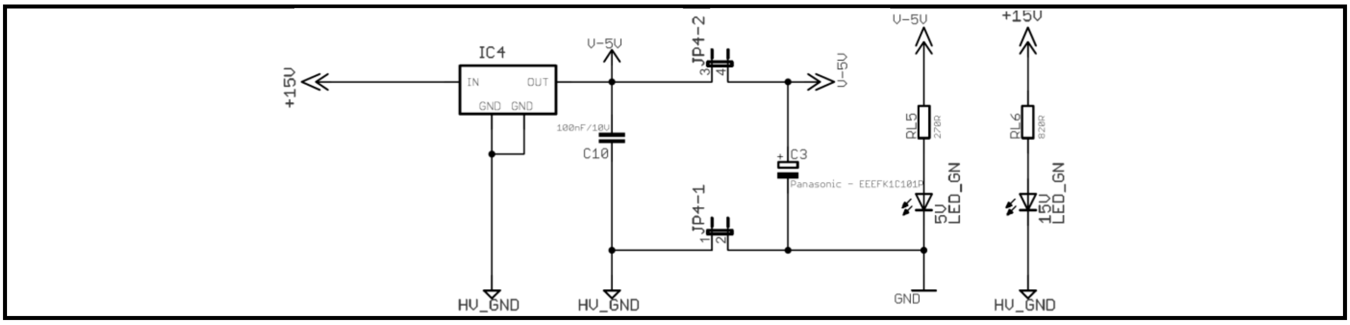


Figure 4-3: 5V voltage regulator and power supply status LEDs

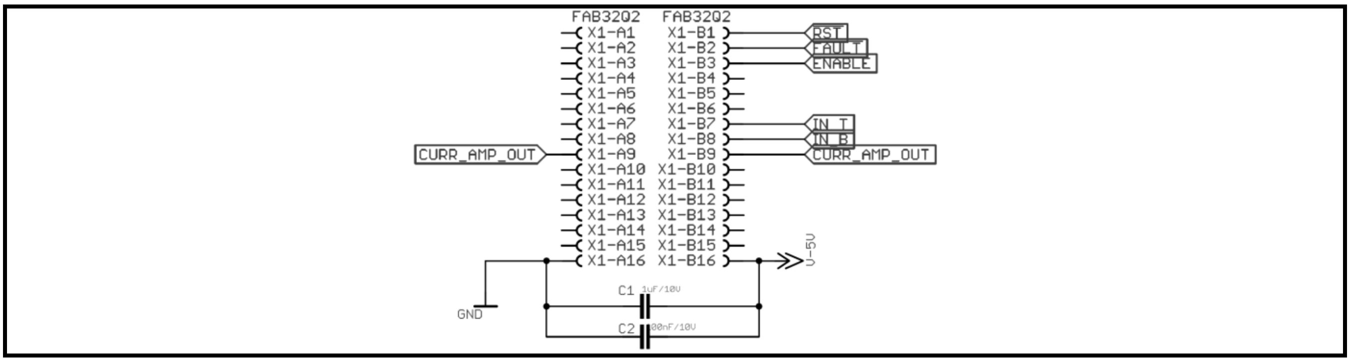


Figure 4-4: Communication interface – connector X1

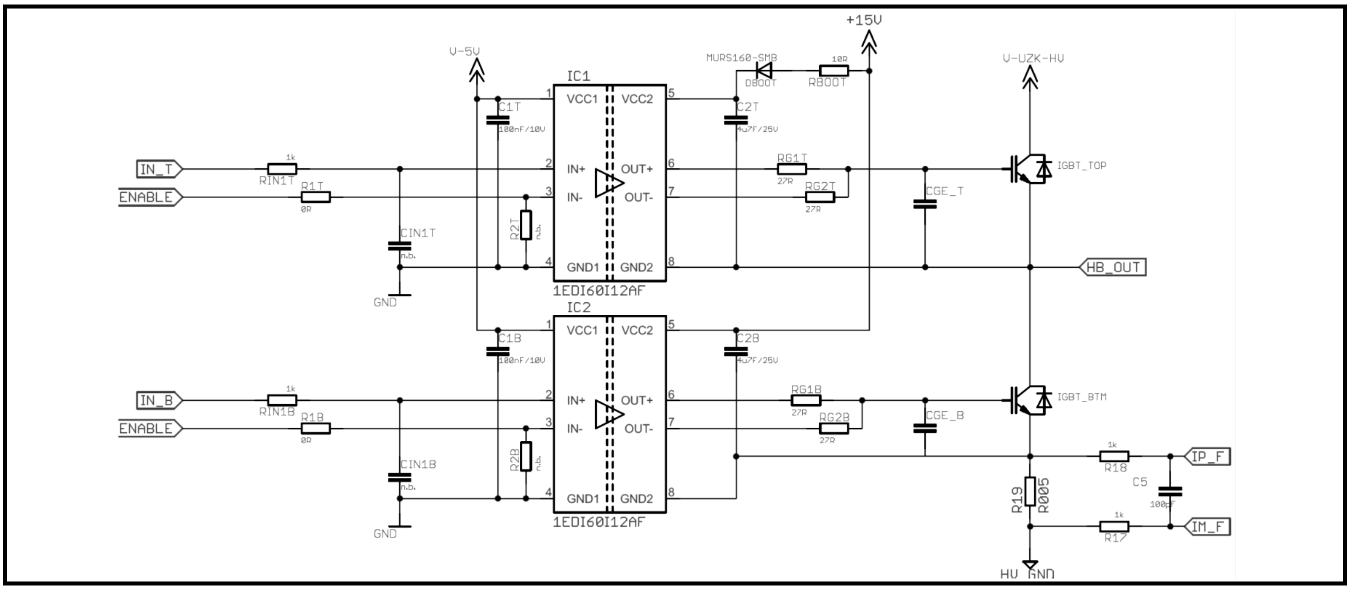


Figure 4-5: Infineon gate drivers 1EDI60I12AF with necessary external components

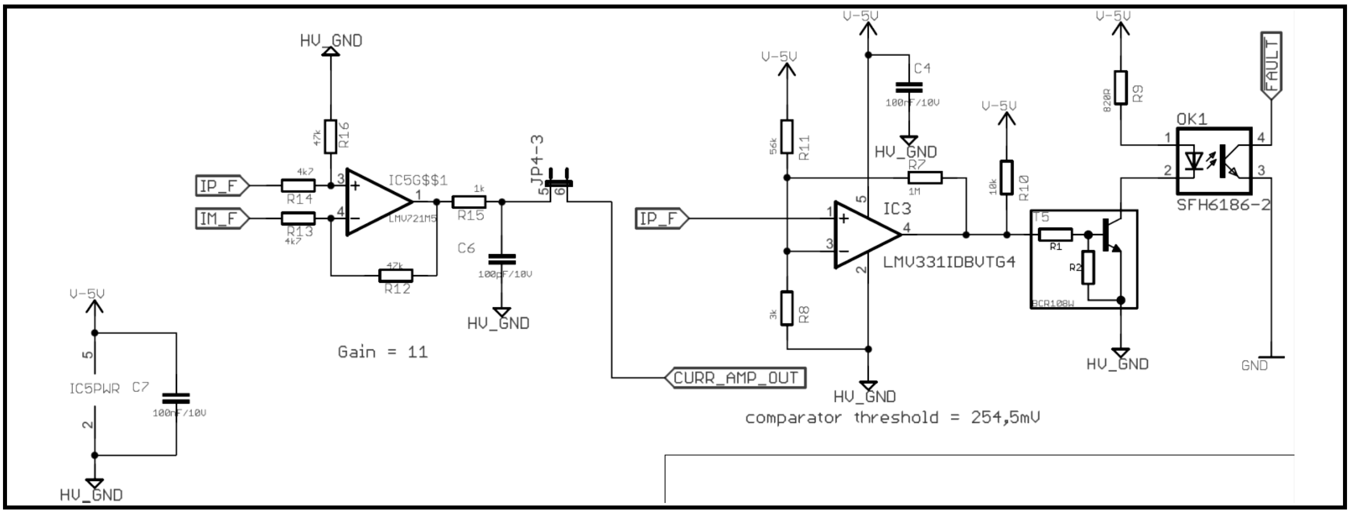


Figure 4-6: Current sense amplifier and over current comparator

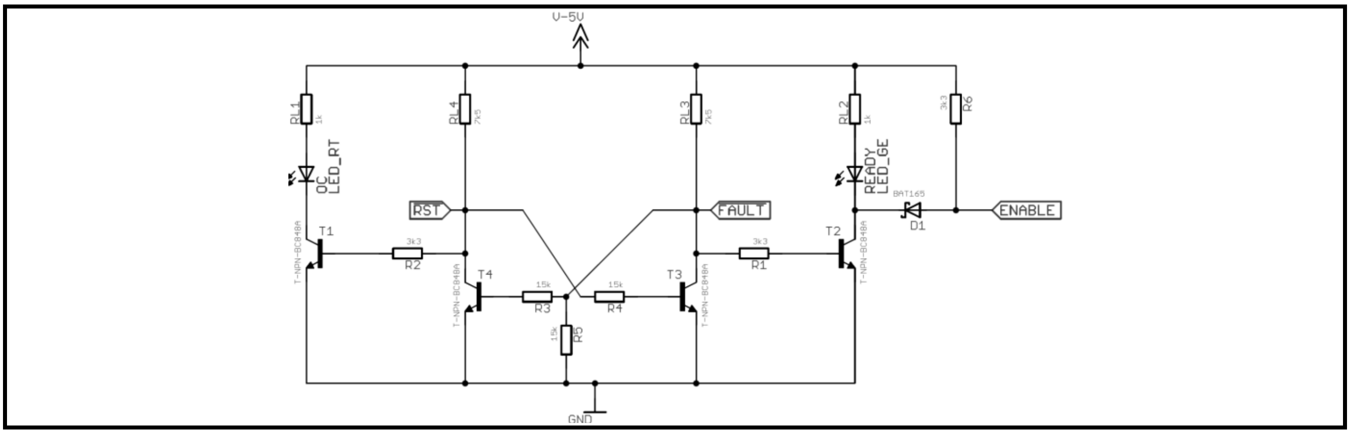


Figure 4-7: OC and READY LEDs, FAULT and over current logic

5 Layout

As a basis to start a dedicated development, Figure 5-1 to Figure 5-3 include the layout of the PCB-layers and the component placement view.

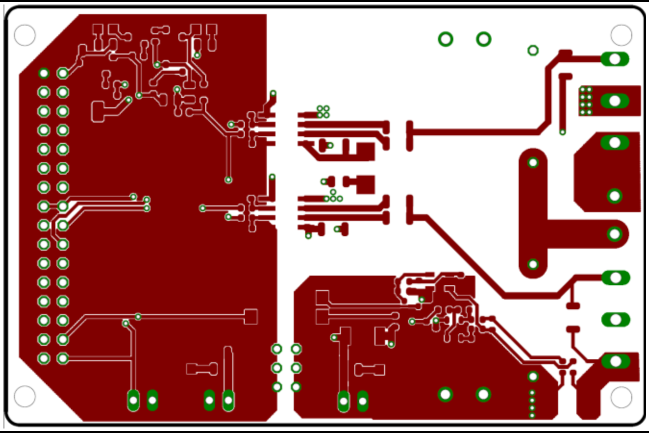


Figure 5-1: Top-Layer of the EVAL-1EDI60I12AF Layout bottom

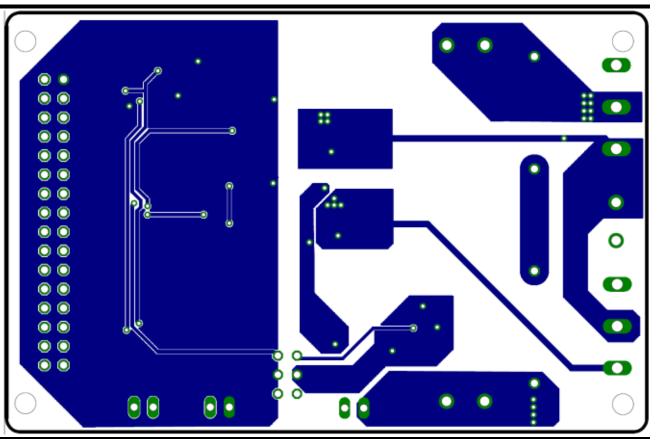


Figure 5-2: Bottom Layer of the EVAL-1EDI60I12AF

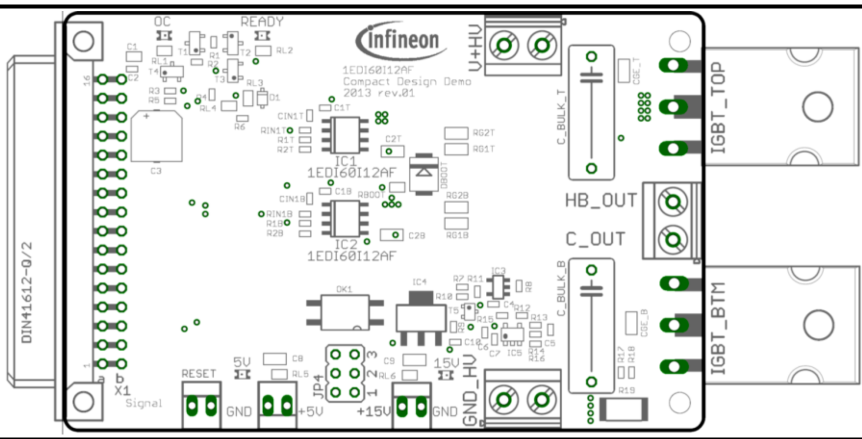


Figure 5-3: Top placement view of the EVAL-1EDI60I12AF

6 Bill of material

Table 6-1

Part	Value	Package
+5V, +15V, RESET	22-23-2021	22-23-2021
GND_HV, HB_OUT,C_OUT, V+HV	MKDSN1,5/2-5,08	MKDSN1,5/2-5,08
5V, 15V	LED_GN	CHIPLED_0805
OC	LED_RT	CHIPLED_0805
READY	LED_GE	CHIPLED_0805
X1	FAB32Q2	FAB32Q2
JP1, JP2, JP3	JP1	Jumper
R2B, R2T	n.a.	SMD0603
R1B, R1T	0R	SMD0603
R9	820R	SMD0603
R15, R17, R18, RIN1B, RIN1T	1k	SMD0603
R8	3k	SMD0603
R1, R2, R6	3k3	SMD0603
R13, R14	4k7	SMD0603
R10	10k	SMD0603
R3, R4, R5	15k	SMD0603
R12, R16	47k	SMD0603
R11	56k	SMD0603
R7	1M	SMD0603
RL5	270R	SMD0805
RL6	820R	SMD0805
RL1, RL2	1k	SMD0805
RL3, RL4	7k5	SMD0805
RG2B, RG2T	3R3	SMD1206
RG1B, RG1T, RBOOT	10R	SMD1206
R19	R005	R2512
CIN1B, CIN1T	n.a.	SMD0603
C5, C6	100pF/10V	SMD0603
C1B, C1T, C2, C4, C7,C10	100nF/10V	SMD0603
C1	1uF/10V	SMD0805
C2B, C2T, C8, C9	4u7F/25V	SMD1206
CGE_B, CGE_T	n.a.	SMD1206
C3	100uF/16V	EEEFK1C101P
C_BULK_B, C_BULK_T	B32522N6334J	330nF/450V
D1	BAT165	SOD323F
DBOOT	MURS160	SMB
IC1, IC2	1EDI60I12AF	SO08
IC3	LMV331IDBVTG4	SOT23-5
IC4	TLE4264G	SOT223
IC5	LMV721M5	SOT23-5
OK1	SFH6186-2	SMD4-7
IGBT_BTM, IGBT_TOP	IKW50N65F5	TO247BH
T1, T2, T3, T4	BC848A	SOT23
T5	BCR108W	SOT323

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG