| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Update drawing to reflect current requirements. Editorial changes throughout. - gap | 01-03-09 | Raymond Monnin |
| B | Boilerplate update and part of five year review. tcr | 06-10-03 | Raymond Monnin |
| | | | |

| REV STATUS OF SHEETS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | B | B | B | B | B | B | B | B | B | B | B | B | B | B |
| SHEET | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
William J. Johnson

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-01-18

REVISION LEVEL
B

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 512K X 8-BIT UVEPROM, MONOLITHIC SILICON

| SIZE | CAGE CODE | 5962-91752 |
|---|---|---|
| A | **67268** | |

SHEET 1 OF 14

DSCC FORM 2233
APR 97

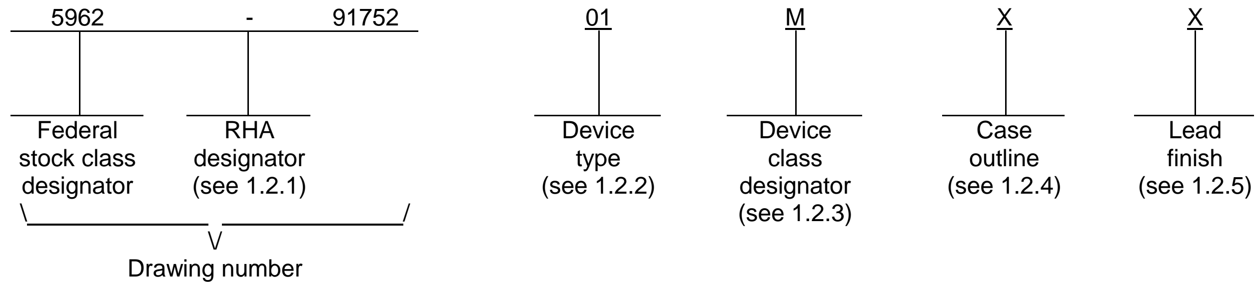
5962-E601-06

Downloaded from Arrow.com.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function | Access time |
|---|---|---|---|
| 01 | 27C040 | (512K x 8) UVEPROM | 250 ns |
| 02 | 27C040 | (512K x 8) UVEPROM | 200 ns |
| 03 | 27C040 | (512K x 8) UVEPROM | 170 ns |
| 04 | 27C040 | (512K x 8) UVEPROM | 150 ns |
| 05 | 27C040 | (512K x 8) UVEPROM | 120 ns |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| X | CDIP2-T32 or GDIP1-T32 | 32 | Dual-in-line package 1/ |
| Y | CQCC1-N32 | 32 | Rectangular leadless chip carrier 1/ |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Lid shall be transparent to permit ultraviolet light erasure.


Downloaded from Arrow.com.

1.3 Absolute maximum ratings. 1/

| | |
|---|---|
| Storage temperature range | -65°C to +150°C |
| All input or output voltage with respect to ground | -0.6 V dc to $V_{CC}$ +0.5 V dc |
| Voltage on A9 with respect to ground | -0.6 V dc to +13.0 V dc |
| $V_{PP}$ supply voltage range with respect to ground during programming | -0.6 V dc to +13.5 V dc |
| $V_{CC}$ supply voltage range with respect to ground | -0.6 V dc to +7.0 V dc |
| Maximum power dissipation ($P_D$) | 330 mW |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$): | |
| Case X and Y | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +150°C 2/ |
| Endurance | 50 cycles/byte, minimum |
| Data retention | 10 years, minimum |

1.4 Recommended operating conditions.

| | |
|---|---|
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Supply voltage ($V_{CC}$) | 4.5 V dc to 5.5 V dc |

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.



Downloaded from Arrow.com.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2) group A, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test with a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be specified by an altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.


Downloaded from Arrow.com.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROMS. All testing requirements and quality assurance provisions herein, shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified by the manufacturer.

3.11.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified by the manufacturer.

3.11.3 Verification of programmed or erased EPROMs. When specified, devices shall be verified as either programmed to a specified program, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.12 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.



Downloaded from Arrow.com.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input load current | $I_{LI}$ | $V_{IN}$ = 0 V to 5.5 V | 1, 2, 3 | All | -10 | +10 | μA |
| Output leakage current | $I_{LO}$ | $V_{OUT}$ = 0 V to 5.5 V | 1, 2, 3 | All | -10 | +10 | μA |
| $V_{PP}$ load current read | $I_{PP1}$ | $V_{PP}$ = 5.5 V | 1, 2, 3 | All | | 100 | μA |
| $V_{CC}$ active current | $I_{CC1}$ | $\overline{CE}$ = $V_{IL}$, $I_{OUT}$ = 0 mA, $V_{CC}$ = $V_{PP}$ = 5.5 V, f = 1/$t_{AVQV}$ | 1, 2, 3 | All | | 60 | mA |
| $V_{CC}$ standby current (TTL) | $I_{CC2}$ | $\overline{CE}$ = $V_{IH}$, $V_{CC}$ = 5.5 V | 1, 2, 3 | All | | 1 | mA |
| $V_{CC}$ super standby current (CMOS) | $I_{CC3}$ | $\overline{CE}$ = $V_{CC}$ ±0.3 V, $V_{CC}$ = 5.5 V | 1, 2, 3 | All | | 100 | μA |
| Input low voltage | $V_{IL}$ | | 1, 2, 3 | All | -0.1 1/ | 0.8 | V |
| Input high voltage | $V_{IH}$ | | 1, 2, 3 | All | 2.0 | $V_{CC}$ +0.5V 1/ | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2.1 mA, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1, 2, 3 | All | | 0.45 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -400 μA, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2.0 V | 1, 2, 3 | All | 2.4 | | V |
| Input capacitance 1/, 2/ | $C_{IN}$ | $T_A$ = +25°C, f = 1 MHz, $V_{IN}$ = 0 V, see 4.4.1c | 4 | All | | 12 | pF |
| Output capacitance 1/, 2/ | $C_{OUT}$ | $T_A$ = +25°C, f = 1 MHz, $V_{OUT}$ = 0 V, see 4.4.1c | 4 | All | | 15 | pF |
| Functional tests | | See 4.4.1d | 7, 8 | All | | | |

See footnotes at end of table.



Downloaded from Arrow.com.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions<br>$-55°C \le T_C \le +125°C$<br>$4.5\ V \le V_{CC} \le 5.5\ V$<br>unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Address to output delay | $t_{AVQV}$ | $\overline{CE} = \overline{OE} = V_{IL}$, see figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 250 | ns |
| | | | | 02 | | 200 | |
| | | | | 03 | | 170 | |
| | | | | 04 | | 150 | |
| | | | | 05 | | 120 | |
| $\overline{CE}$ to output delay | $t_{ELQV}$ | $\overline{OE} = V_{IL}$, see figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 250 | ns |
| | | | | 02 | | 200 | |
| | | | | 03 | | 170 | |
| | | | | 04 | | 150 | |
| | | | | 05 | | 120 | |
| $\overline{OE}$ to output delay | $t_{OLQV}$ | $\overline{CE} = V_{IL}$, see figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 100 | ns |
| | | | | 02 | | 75 | |
| | | | | 03 | | 65 | |
| | | | | 04 | | 65 | |
| | | | | 05 | | 50 | |
| $\overline{CE}$ or $\overline{OE}$ high to output float | $t_{EHQZ}$<br>$t_{OHQZ}$<br>3/ | $\overline{CE}$ or $\overline{OE} = V_{IL}$, see figures 3 and 4 as applicable | 9, 10, 11 | 01 | | 60 | ns |
| | | | | 02 | | 60 | |
| | | | | 03 | | 50 | |
| | | | | 04 | | 50 | |
| | | | | 05 | | 50 | |
| Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first | $t_{AXQX}$<br>3/ | see figures 3 and 4 as applicable | 9, 10,11 | All | 0 | | ns |

1/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
2/ All pins not being tested shall be grounded.
3/ May not be tested, but shall be guaranteed to the limits specified in table I.



Downloaded from Arrow.com.

| Device types | All |
|---|---|
| Case outlines | X and Y |
| Terminal number | Terminal symbol |
| 1 | $V_{PP}$ |
| 2 | $A_{16}$ |
| 3 | $A_{15}$ |
| 4 | $A_{12}$ |
| 5 | $A_7$ |
| 6 | $A_6$ |
| 7 | $A_5$ |
| 8 | $A_4$ |
| 9 | $A_3$ |
| 10 | $A_2$ |
| 11 | $A_1$ |
| 12 | $A_0$ |
| 13 | $I/0_0$ |
| 14 | $I/0_1$ |
| 15 | $I/0_2$ |
| 16 | GND |
| 17 | $I/0_3$ |
| 18 | $I/0_4$ |
| 19 | $I/0_5$ |
| 20 | $I/0_6$ |
| 21 | $I/0_7$ |
| 22 | $\overline{CE}/(\overline{E})$ |
| 23 | $A_{10}$ |
| 24 | $\overline{OE}/(\overline{G})$ |
| 25 | $A_{11}$ |
| 26 | $A_9$ |
| 27 | $A_8$ |
| 28 | $A_{13}$ |
| 29 | $A_{14}$ |
| 30 | $A_{17}$ |
| 31 | $A_{18}$ |
| 32 | $V_{CC}$ |

FIGURE 1. Terminal connections.

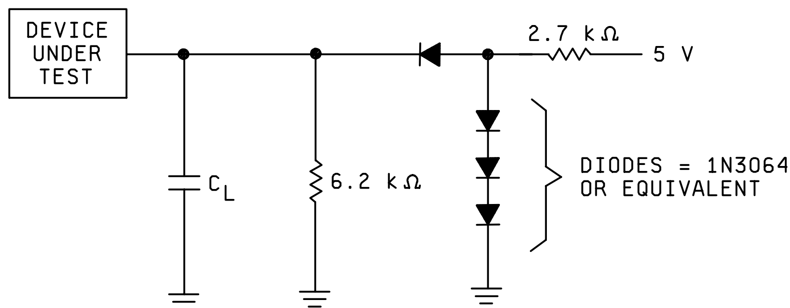


Downloaded from Arrow.com.

| Mode | | Pins | | | | | |
|---|---|---|---|---|---|---|---|
| | | $\overline{CE}$ | $\overline{OE}$ | $A_0$ | $A_9$ | $V_{PP}$ | Outputs |
| Read | | $V_{IL}$ | $V_{IL}$ | X | X | $V_{CC}$ | $D_{OUT}$ |
| Standby (TTL) | | $V_{IH}$ | X | X | X | $V_{CC}$ | Hi-Z |
| Standby (CMOS) | | $V_{CC}$ ±0.3 V | X | X | X | $V_{CC}$ | Hi-Z |
| Output disable | | $V_{IL}$ | $V_{IH}$ | X | X | $V_{CC}$ | Hi-Z |
| Program | | $V_{IL}$ | $V_{IH}$ | X | X | $V_{PP}$ | $D_{IN}$ |
| Program verify | | $V_{IH}$ | $V_{IL}$ | X | X | $V_{PP}$ | $D_{OUT}$ |
| Program inhibit | | $V_{IH}$ | $V_{IH}$ | X | X | $V_{PP}$ | Hi-Z |
| Auto select | Manufacturer code | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | $V_H$ | $V_{CC}$ | |
| (see notes 1 and 3) | Device | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_H$ | $V_{CC}$ | |

NOTES:
1. $V_H$ = HIGH voltage +12.0 ±0.5 V.
2. X = either $V_{IH}$ or $V_{IL}$.
3. $A_1$ - $A_8$ = $A_{10}$ - $A_{18}$ = $V_{IL}$.
4. $V_{PP}$ = see 4.5.

FIGURE 2. Truth table.

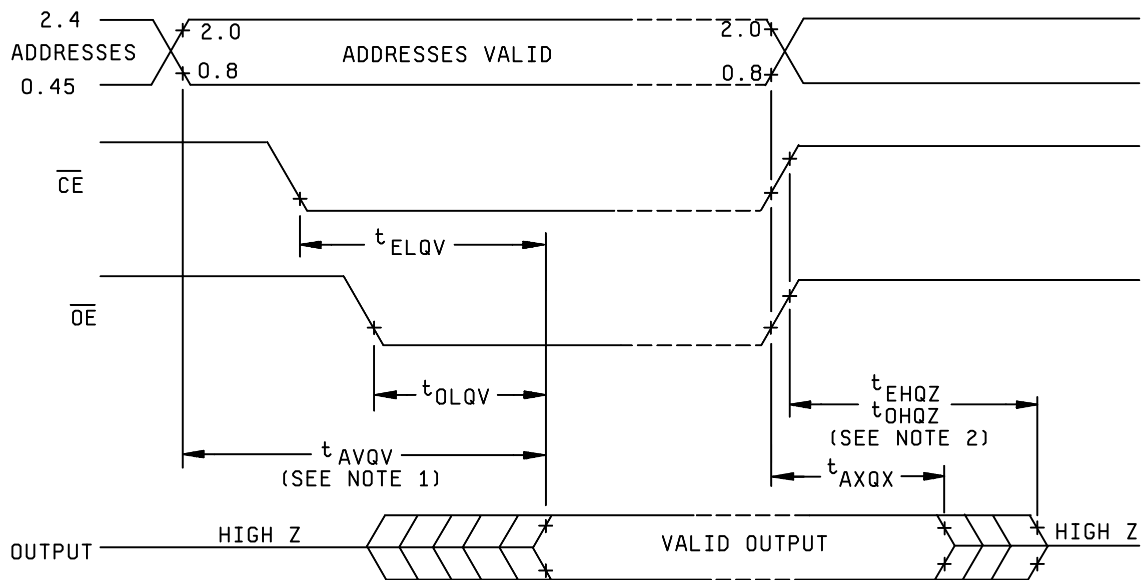



NOTE:
1. Alternate equivalent switching time test circuit may be used.

FIGURE 3. Switching time test circuit.



Downloaded from Arrow.com.




NOTES:

1. $\overline{OE}$ may be delayed up to $t_{ELQV}$ - $t_{OLQV}$ after the falling edge of $\overline{CE}$ without impact on $t_{ELQV}$.
2. $t_{EHQZ}$ or $t_{OHQZ}$ is specified from $\overline{OE}$ or $\overline{CE}$ , whichever occurs first.
3. Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

FIGURE 4. Read cycle waveforms.



Downloaded from Arrow.com.

## 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).



Downloaded from Arrow.com.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method

c. Subgroup 4 ($C_{IN}$ and $C_{OUT}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

f. All devices selected for testing shall be programmed with a checkerboard pattern, or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.


Downloaded from Arrow.com.

TABLE IIA. Electrical test requirements. 1/, 2/, 3/, 4/, 5/, 6/

| Line No. | Test Requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (per MIL-PRF-38535, table III) | |
|---|---|---|---|---|
| | | Device class M | Device class Q | Device class V |
| 1 | Interim electrical parameters (see 4.2) | | | 1, 7, 9 |
| 2 | Static burn-in I method 1015 | Not required | Not required | Required |
| 3 | Same as line 1 | | | 1*, 7* Δ |
| 4 | Dynamic burn-in (method 1015) | Required | Required | Required |
| 5 | Same as line 1 | | | 1*, 7* Δ |
| 6 | Final electrical parameters (programmed devices) | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 | 1*, 2, 3, 7*, 8A, 8B, 9, 10, 11 |
| 6A | Final electrical parameters (unprogrammed devices) | 1*, 2, 3, 7*, 8A, 8B | 1*, 2, 3, 7*, 8A, 8B | 1*, 2, 3, 7*, 8A, 8B |
| 7 | Group A test requirements | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 | 1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11 |
| 8 | Group C end-point electrical parameters | 2, 3, 7, 8A, 8B | 1, 2, 3, 7, 8A, 8B Δ | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ |
| 9 | Group D end-point electrical parameters | 2, 3, 8A, 8B | 2, 3, 8A, 8B | 2, 3, 8A, 8B |
| 10 | Group E end-point electrical parameters | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ * indicates PDA applies to subgroup 1 and 7.
4/ ** see 4.4.1c.
5/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).
6/ See 4.4.1e.

TABLE IIB. Delta limits at +25°C.

| Test 1/ | Device types |
|---|---|
| | All |
| $I_{CC3}$ standby | ±10 percent of specified value in table I |
| $I_{LI}$ | ±10 percent of specified value in table I |
| $I_{LO}$ | ±10 percent of specified value in table I |

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.



Downloaded from Arrow.com.

4.6 Delta measurements for device class Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331 and as follows:

$C_{IN}$ .................................................... Input terminal capacitance.
$C_{OUT}$ .................................................. Output terminal capacitance.
GND ................................................. Ground zero voltage potential.
$I_{CC}$ ..................................................... Supply current.
$I_{LI}$ ...................................................... Input load current.
$T_C$ ..................................................... Case temperature.
$V_{CC}$ ................................................... Positive supply voltage.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.


Downloaded from Arrow.com.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-10-03

Approved sources of supply for SMD 5962-91752 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9175201MXA | 0C7V7 | AT27C040-25DM/883 |
| | 3/ | Am27C040-250/BXA |
| 5962-9175201MYA | 0C7V7 | AT27C040-25LM/883 |
| | 3/ | Am27C040-250/BUA |
| 5962-9175202MXA | 0C7V7 | AT27C040-20DM/883 |
| | 3/ | Am27C040-200/BXA |
| | 3/ | MD27C040-20/B |
| 5962-9175202MYA | 0C7V7 | AT27C040-20LM/883 |
| | 3/ | Am27C040-200/BUA |
| 5962-9175203MXA | 0C7V7 | AT27C040-17DM/883 |
| | 3/ | MD27C040-17/B |
| 5962-9175203MYA | 0C7V7 | AT27C040-17LM/883 |
| 5962-9175204MXA | 0EU86 | SMJ27C040-15JM |
| | 0C7V7 | AT27C040-15DM/883 |
| | 3/ | Am27C040-150/BXA |
| | 3/ | MD27C040-15/B |
| 5962-9175204MYA | 0C7V7 | AT27C040-15LM/883 |
| | 3/ | Am27C040-150/BUA |
| 5962-9175205MXA | 0EU86 | SMJ27C040-12JM |
| | 0C7V7 | AT27C040-12DM/883 |
| 5962-9175205MYA | 0C7V7 | AT27C040-12LM/883 |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0EU86 | Austin Semiconductor<br>8701 Cross Park Dr.<br>Austin, TX 78754-4566 |
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

Downloaded from Arrow.com.