# STL190N4F7AG

## Automotive-grade N-channel 40 V, 1.68 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

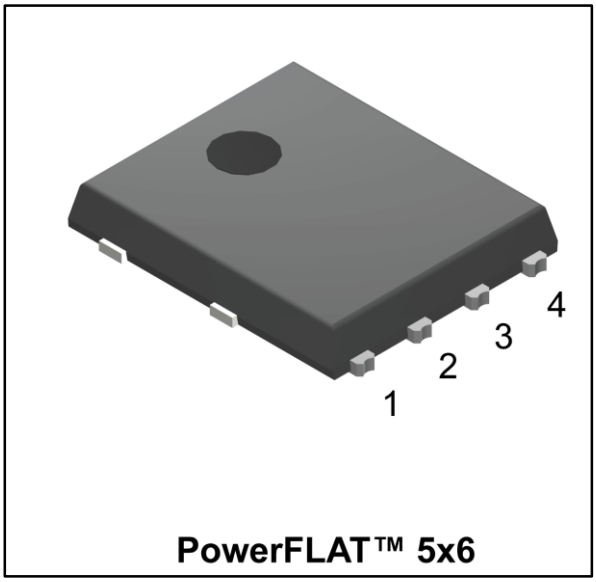
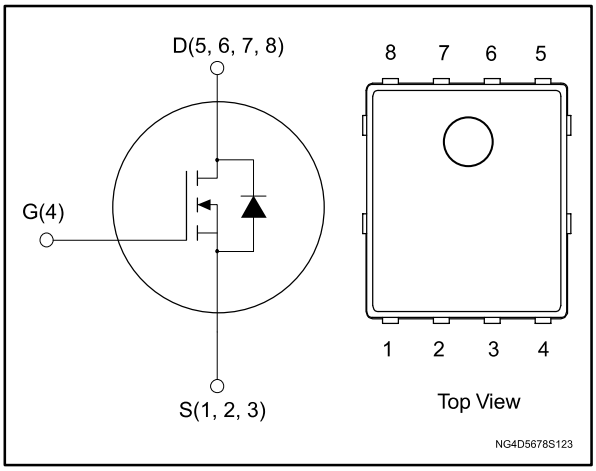



**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL190N4F7AG | 40 V | 2.00 mΩ | 120 A |

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low $C_{rss}/C_{iss}$ ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

## Applications

- Switching applications

## Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

**Table 1: Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL190N4F7AG | 190N4F7 | PowerFLAT™ 5x6 | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 40 | V |
| $V_{GS}$ | Gate-source voltage | ±20 | V |
| $I_D$(1) | Drain current (continuous) at $T_C$ = 25 °C | 120 | A |
| $I_D$(1) | Drain current (continuous) at $T_C$ = 100 °C | 120 | A |
| $I_{DM}$(1)(2) | Drain current (pulsed) | 480 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 127 | W |
| $I_{AV}$ | Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature) | 35 | A |
| $E_{AS}$ | Single pulse avalanche energy ($T_J$ = 25 °C, $I_D$ = 17.5 A, $V_{DD}$ = 22 V) | 300 | mJ |
| $T_j$ | Operating junction temperature range | -55 to 175 | °C |
| $T_{stg}$ | Storage temperature range | | |

**Notes:**

(1)Drain current is limited by package, the current capability of the silicon is 183 A at 25 °C.

(2)Pulse width limited by safe operating area

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb | 31.3 | °C/W |
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 1.18 | °C/W |

**Notes:**

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4: On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$= 250 µA | 40 | | | V |
| $I_{DSS}$ | Zero gate voltagedrain current | $V_{GS}$ = 0 V<br>$V_{DS}$= 40 V | | | 1 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 17.5 A | | 1.68 | 2.00 | mΩ |

**Table 5: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$= 0 V | - | 3000 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 850 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 70 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 20 V, $I_D$ = 35 A, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*) | - | 41 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 15 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 7 | - | nC |

**Table 6: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 20 V, $I_D$ = 17.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*) | - | 19 | - | ns |
| $t_r$ | Rise time | | - | 6.4 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 25 | - | ns |
| $t_f$ | Fall time | | - | 6.5 | - | ns |

**Table 7: Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ (1) | Forward on voltage | $I_{SD}$ = 35 A, $V_{GS}$ = 0 V | - | | 1.2 | V |
| $t_{rr}$ | Reverse recovery time | $I_D$ = 35 A, di/dt = 100 A/µs $V_{DD}$ = 32 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*) | - | 43 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 43 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 2 | | A |

**Notes:**

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

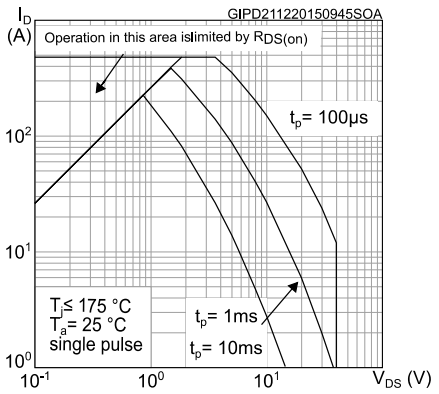



**Figure 3: Thermal impedance**

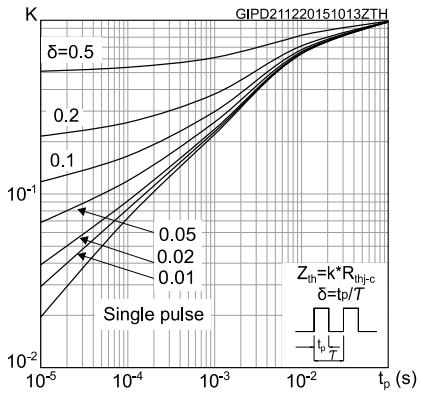



**Figure 4: Output characteristics**

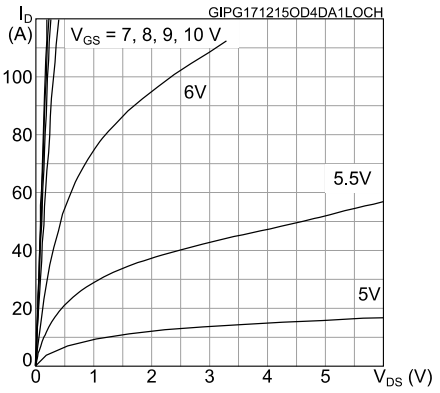



**Figure 5: Transfer characteristics**

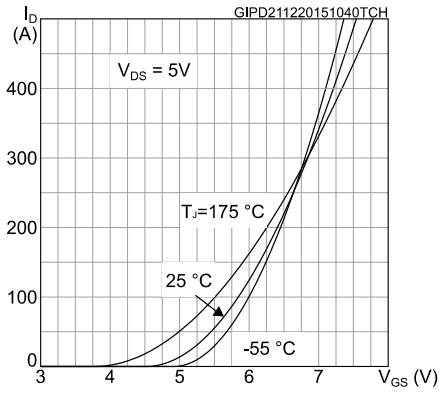



**Figure 6: Gate charge vs gate-source voltage**

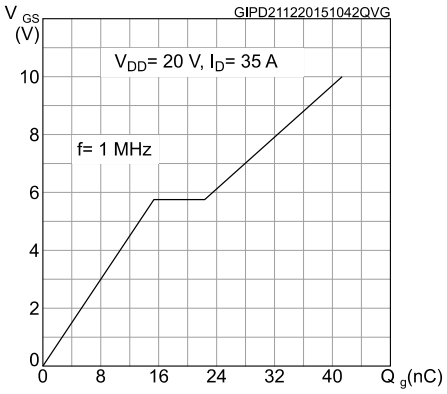



**Figure 7: Static drain-source on-resistance**

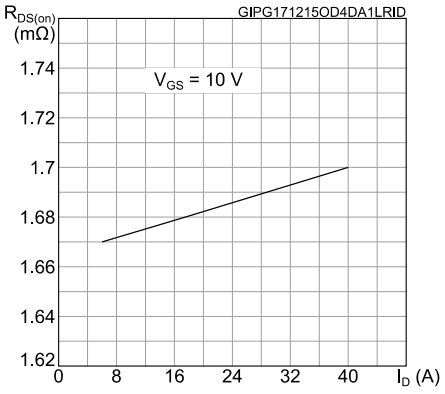


**Figure 8: Capacitance variations**

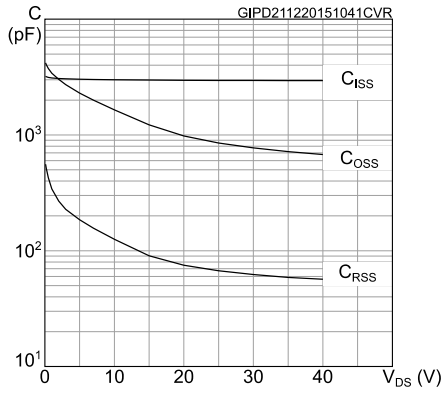



**Figure 9: Normalized on-resistance vs temperature**

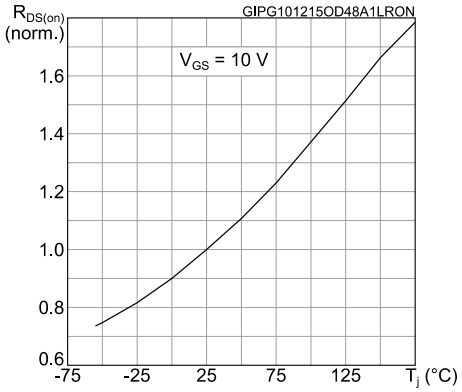



**Figure 10: Normalized V(BR)DSS vs temperature**

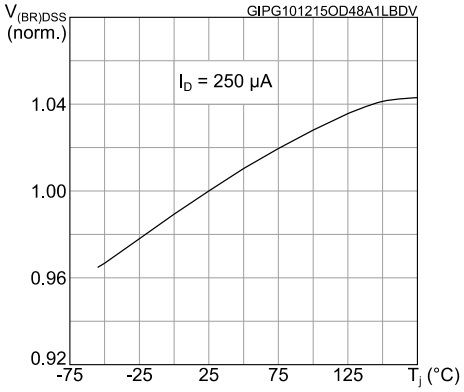



**Figure 11: Normalized gate threshold voltage vs temperature**

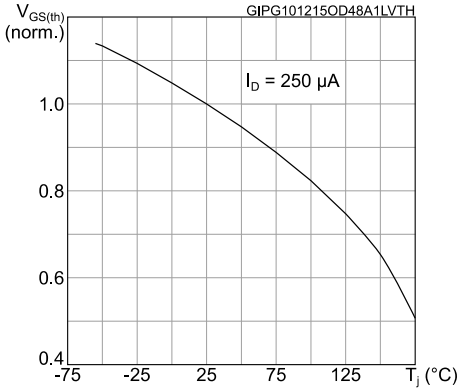
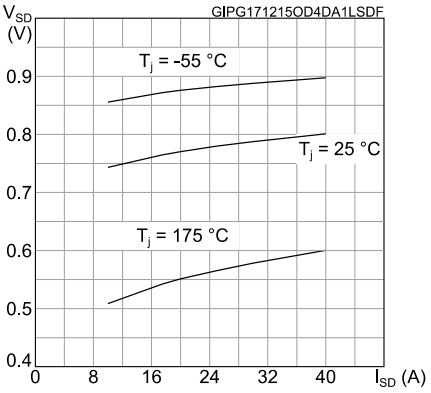



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**

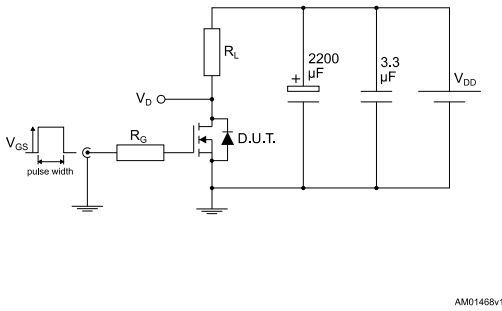



**Figure 14: Test circuit for gate charge behavior**

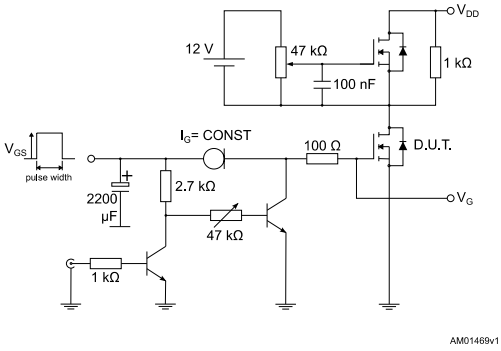



**Figure 15: Test circuit for inductive load switching and diode recovery times**

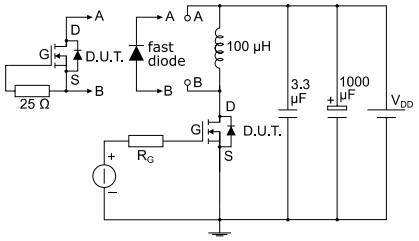



**Figure 16: Unclamped inductive load test circuit**

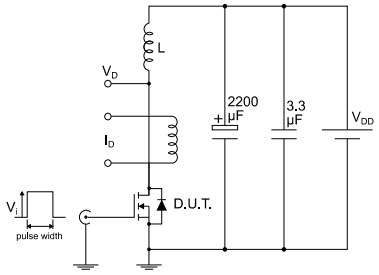



**Figure 17: Unclamped inductive waveform**

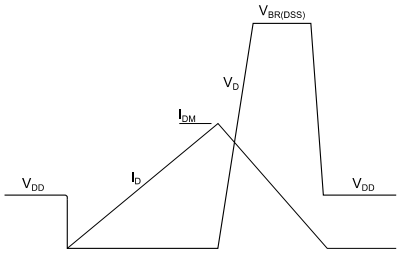
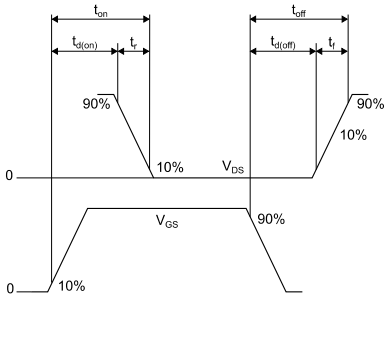



**Figure 18: Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 5x6 WF type C package information

**Figure 19: PowerFLAT™ 5x6 WF type C package outline**

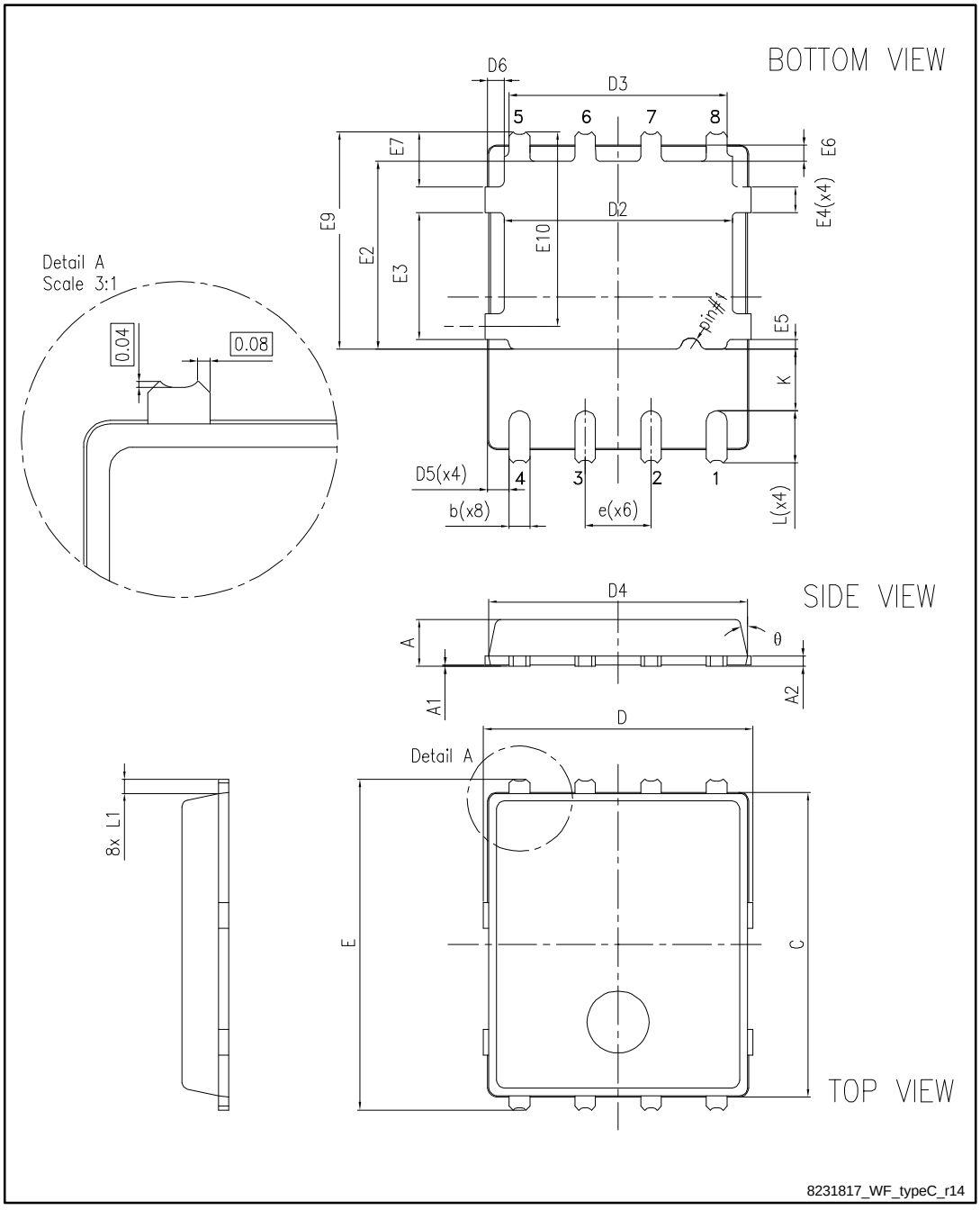
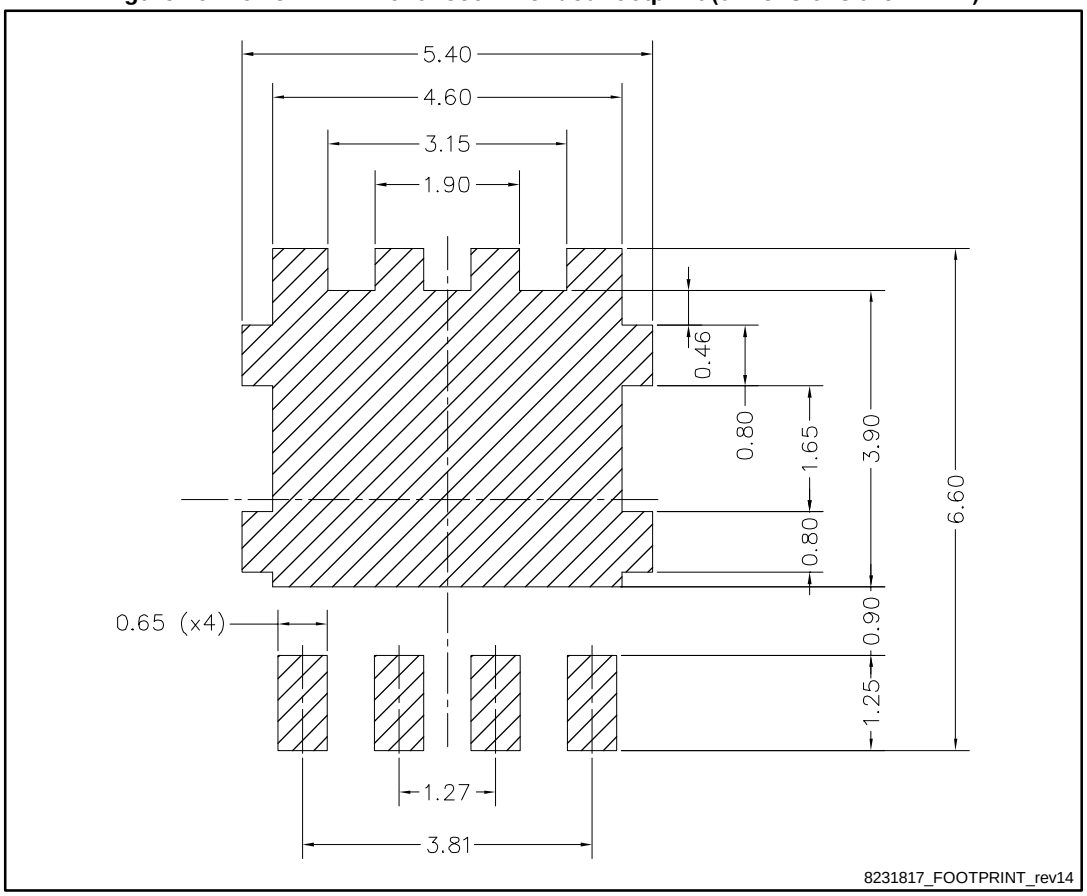


Table 8: PowerFLAT™ 5x6 WF type C mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| C | 5.80 | 6.00 | 6.10 |
| D | 5.00 | 5.20 | 5.40 |
| D2 | 4.15 | | 4.45 |
| D3 | 4.05 | 4.20 | 4.35 |
| D4 | 4.80 | 5.00 | 5.10 |
| D5 | 0.25 | 0.40 | 0.55 |
| D6 | 0.15 | 0.30 | 0.45 |
| e | | 1.27 | |
| E | 6.20 | 6.40 | 6.60 |
| E2 | 3.50 | | 3.70 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |
| E6 | 0.20 | 0.325 | 0.45 |
| E7 | 0.85 | 1.00 | 1.15 |
| E9 | 4.00 | 4.20 | 4.40 |
| E10 | 3.55 | 3.70 | 3.85 |
| K | 1.05 | | 1.35 |
| L | 0.90 | 1.00 | 1.10 |
| L1 | 0.175 | 0.275 | 0.375 |
| θ | 0° | | 12° |

**Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)**



## 4.2 PowerFLAT™ 5x6 packing information

**Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)**

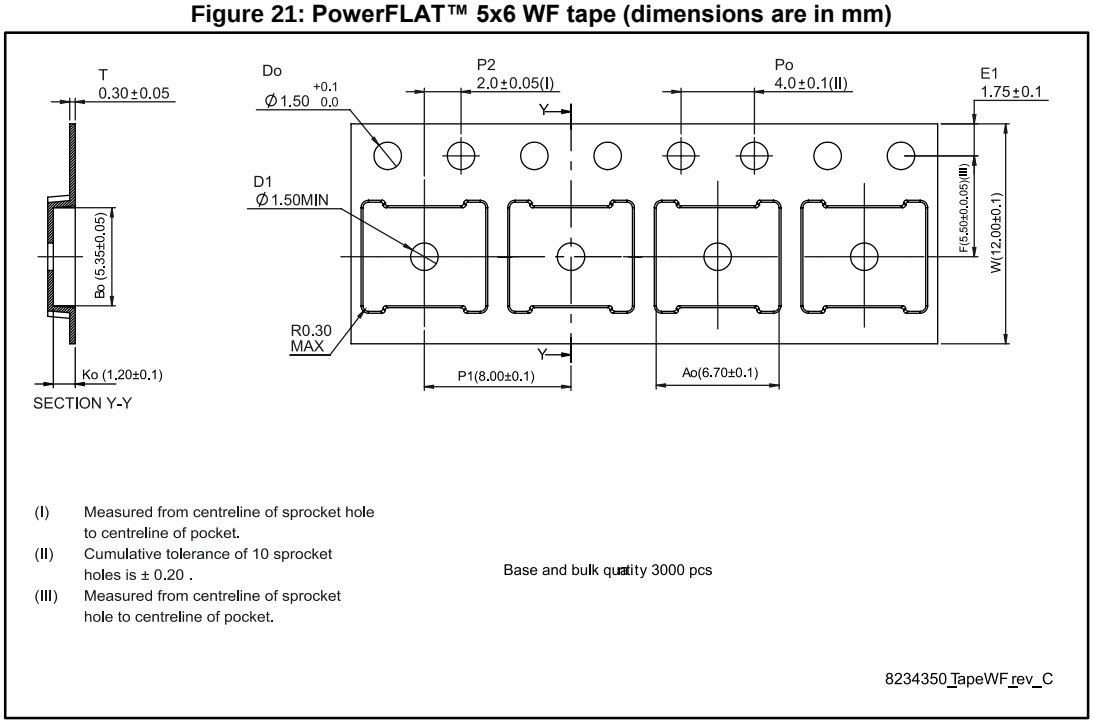



**Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape**

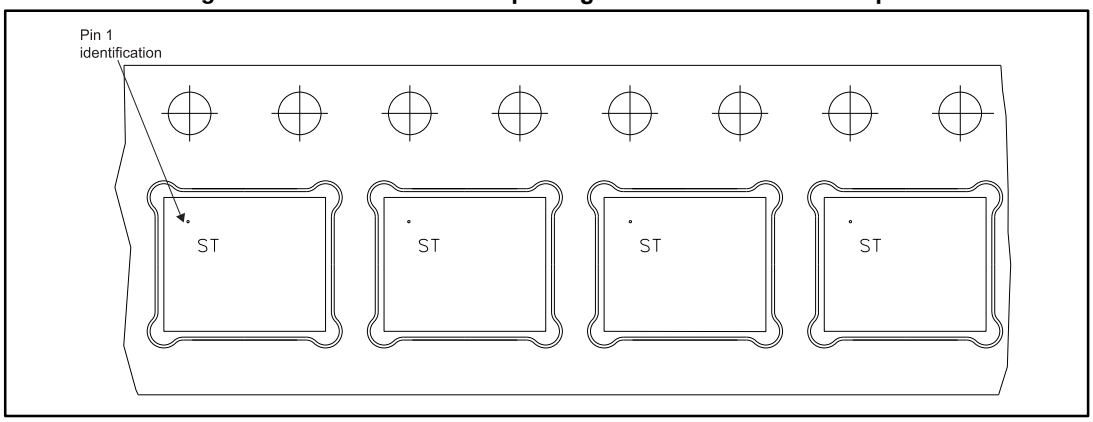
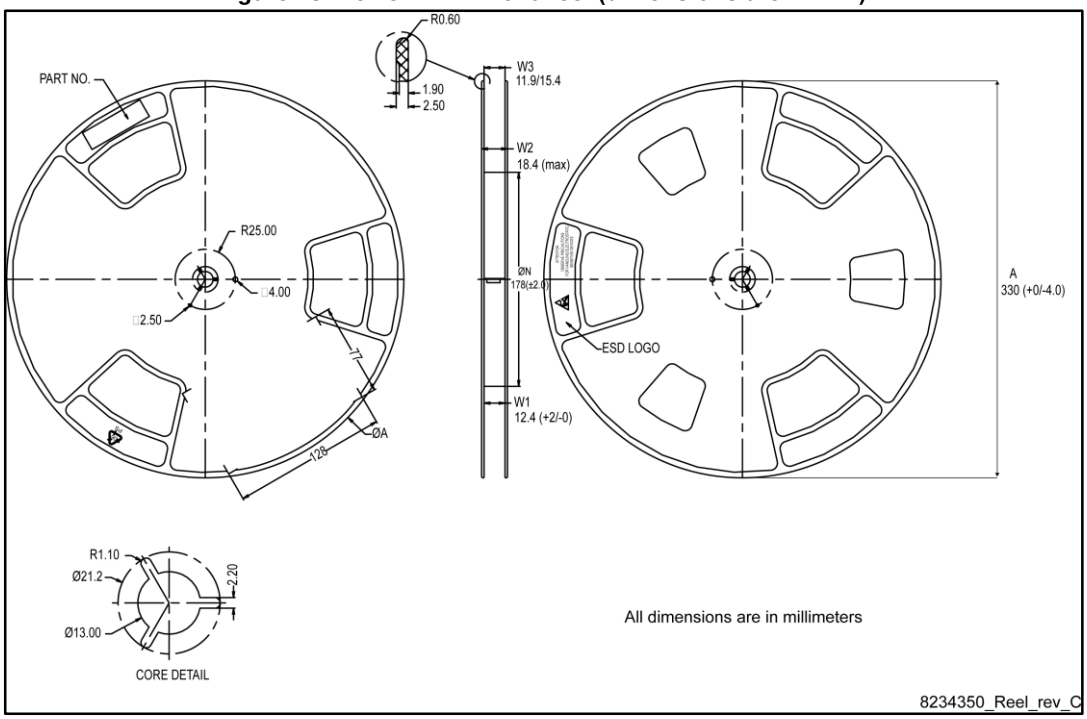


**Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)**



# 5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 07-Jan-2016 | 1 | First release. |
| 23-Jun-2016 | 2 | Updated package silhouette and *Figure 1: "Internal schematic diagram"* in cover page.<br>Updated *Section 6.1: "PowerFLAT™ 5x6 WF type C package information"*.<br>Minor text changes. |

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