DN2470

N-Channel, Depletion-Mode, Vertical DMOS FET

Features

- High-input impedance
- Low-input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

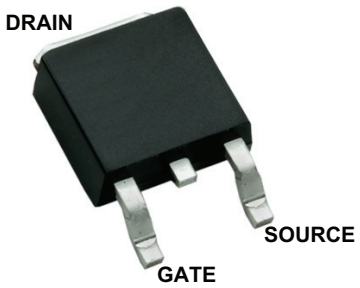
- Normally-on switches
- Solid state relays
- Converters
- Linear amplifiers
- Constant current sources
- Battery operated systems
- Telecom

Description

This low threshold, depletion-mode, normally-on, transistor utilizes an advanced vertical Diffusion Metal Oxide Semiconductor (DMOS) structure and a well proven silicon-gate manufacturing process. This combination produces a device with the power-handling capabilities of bipolar transistors, plus the high-input impedance and positive-temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where a very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type



TO-252 (D-PAK)

See Table 2-1 for pin information

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Drain-to-source voltage ..... BV_{DSX}
Drain-to-gate voltage ..... BV_{DGX}
Gate-to-source voltage ..... ±20V
Operating and storage temperature ..... -55°C to +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC AND AC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J$ = +25°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC Parameters (**Note 1**, unless otherwise stated)						
Drain-to-source breakdown voltage	BV_{DSX}	700	–	–	V	V_{GS} = -5.0V, I_D= 100µA
Gate-to-source off voltage	$V_{GS(OFF)}$	-1.5	–	-3.5	V	V_{DS} = 25V, I_D= 10µA
Change in $V_{GS(OFF)}$ with temperature	$\Delta V_{GS(OFF)}$	–	–	-4.5	mV/°C	V_{DS} = 25V, I_D= 10µA ((**Note 2**)
Gate body leakage current	I_{GSS}	–	–	100	nA	V_{GS} = ±20V, V_{DS}= 0V
Drain-to-source leakage current	$I_{D(OFF)}$	–	–	1.0	µA	V_{DS} = BV_{DSX}, V_{GS} = -10V
		–	–	1.0	mA	V_{DS} = 0.8 BV_{DSX}, V_{GS} = -10V, T_A= 125°C ((**Note 2**)
Saturated drain-to-source current	I_{DSS}	–	500	-	mA	V_{GS} = 0V, V_{DS}= 25V
Static drain-to-source on-state resistance	$R_{DS(ON)}$	–	–	42	Ω	V_{GS} = 0V, I_D= 100mA
Change in $R_{DS(ON)}$ with temperature	$\Delta R_{DS(ON)}$	–	–	1.1	%/°C	V_{GS}= 0V, I_D= 100mA (**Note 2**)
AC Parameters (**Note 2**)						
Forward transconductance	G_{FS}	100	–	–	mmho	V_{DS}= 10V, I_D= 100mA
Input capacitance	C_{ISS}	–	–	540	pF	V_{GS}= -10V, V_{DS}= 25V, f = 1.0 MHz
Common source output capacitance	C_{OSS}	–	–	60		
Reverse transfer capacitance	C_{RSS}	–	–	25		
Turn-on delay time	$t_{d(ON)}$	–	–	30	ns	V_{DD}= 25V, I_D= 100mA, R_{GEN}= 25Ω,
Rise time	t_r	–	–	45		
Turn-off delay time	$t_{d(OFF)}$	–	–	45		
Fall time	t_f	–	–	60		
Diode Parameters						
Diode forward voltage drop	V_{SD}	–	–	1.8	V	V_{GS}= -5.0V, I_{SD}= 200mA (**Note 1**)
Reverse recovery time	t_{rr}	–	800	–	ns	V_{GS}= -5.0V, I_{SD}= 200mA (**Note 2**)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, for all specifications $T_A = T_J$ = +25°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating and Storage temperature		-55	–	150	°C	
Package Thermal Resistances						
Thermal Resistance, TO-252 (D-PAK)	θ_{ja}	–	132	–	°C/W	

TABLE 1-1: THERMAL CHARACTERISTICS

Package	I_D[1] continuous (mA)	I_D pulsed (mA)	Power Dissipation @T_A = 25°C (W)	I_{DR}[1] (mA)	I_{DRM} (mA)
TO-252 (D-PAK)	170	500	2.5[2]	170	500

1. I_D continuous is limited by max rated T_j
2. Mounted on FR4 board, 25mm x 25mm x 1.57 mm

2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Type.

TABLE 2-1: PIN DESCRIPTION

Pin # TO-252	Function
1	GATE
3	SOURCE
2,4	DRAIN

3.0 APPLICATION INFORMATION

Figure 3-1 shows the switching waveform and test circuit for DN2450.

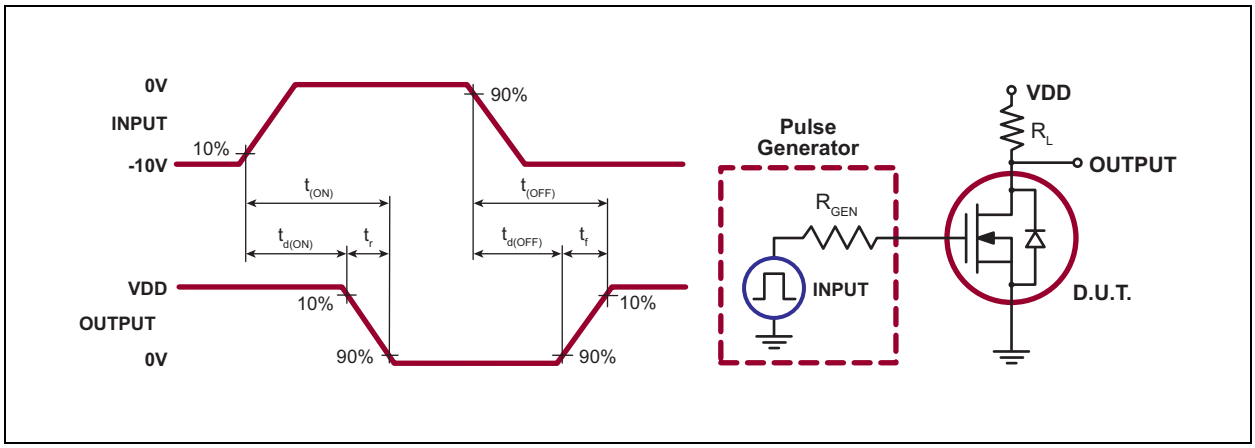


FIGURE 3-1: *Switching Waveforms and Test Circuit*

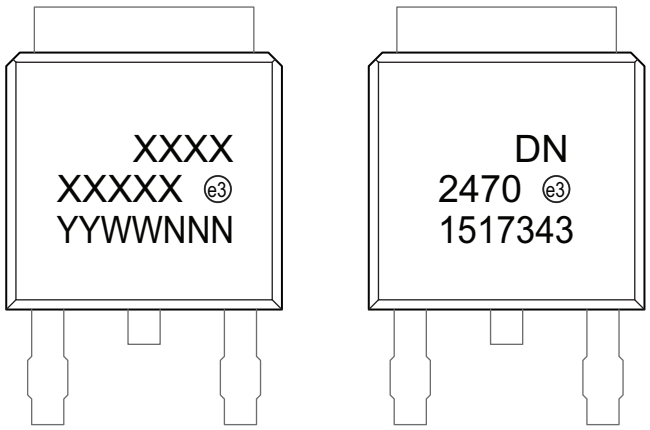
Product Summary

BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max) (Ω)	I_{DSS} (typ) (mA)
700	42	500

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

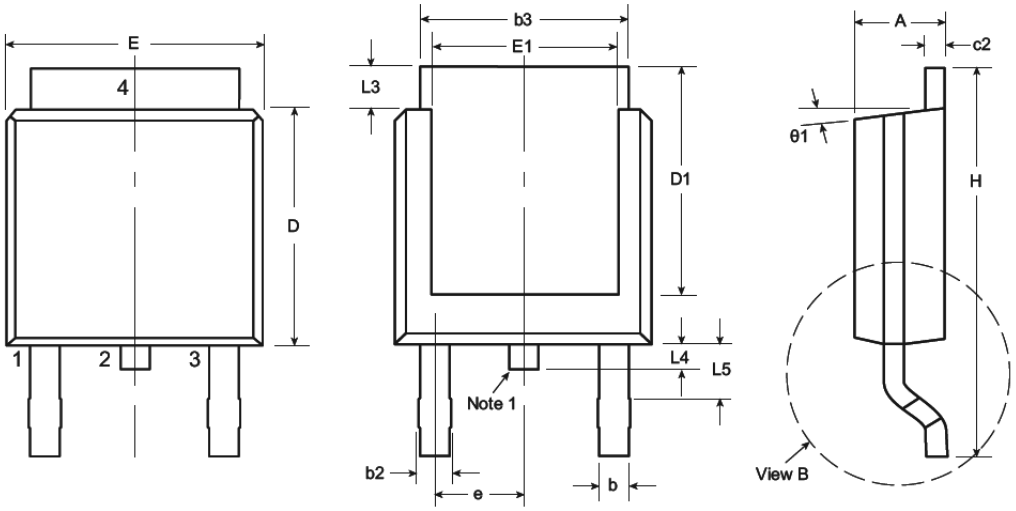
TO-252 (D-PAK) Example



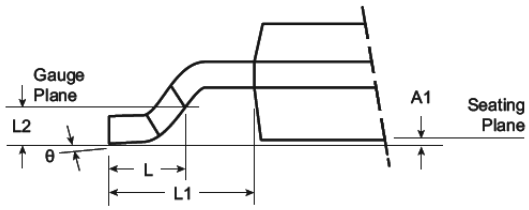
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-252 (D-PAK) Package Outline (K4)



Front View **Rear View** **Side View**



View B

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimension (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.035†	0°	0°
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10°	15°

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2015)

- Updated file to new format. Released data sheet in the Microchip system.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	DN2470	=	N-Channel, Depletion-Mode, vertical DMOS FET
Package:	K4	=	TO-252 (D-PAK)
Environmental	G	=	Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank)	=	2000/Reel

Examples:

a) DN2470K4-G TO-252 package, 2000/reel

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