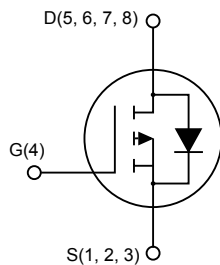
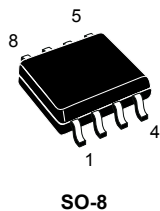


## P-channel -40 V, 12.5 mΩ typ., -10 A STripFET F6 Power MOSFET in SO-8 package



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STS10P4LLF6	-40 V	15 mΩ	-10 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low  $R_{DS(on)}$  in all packages.



#### Product status link

[STS10P4LLF6](#)

#### Product summary

<b>Order code</b>	STS10P4LLF6
<b>Marking</b>	10P4L
<b>Package</b>	SO-8
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	-40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	-10	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	-5.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	-40	A
$P_{TOT}$	Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.7	W
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	47	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu.,  $t \leq 10$  sec.

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 3. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -250\text{ }\mu\text{A}$	-40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = -40\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -40\text{ V}, T_C = 125\text{ }^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = -10\text{ V}, I_D = -3\text{ A}$		12.5	15	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -3\text{ A}$		17	20	

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = -25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	3525	-	pF
$C_{oss}$	Output capacitance		-	344	-	pF
$C_{rss}$	Reverse transfer capacitance		-	238.5	-	pF
$Q_g$	Total gate charge	$V_{DD} = -20\text{ V}, I_D = -10\text{ A}, V_{GS} = -4.5\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	34	-	nC
$Q_{gs}$	Gate-source charge		-	11.3	-	nC
$Q_{gd}$	Gate-drain charge		-	13.8	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -20\text{ V}, I_D = -5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = -10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times)	-	49.4	-	ns
$t_r$	Rise time		-	60.6	-	ns
$t_{d(off)}$	Turn-off-delay time		-	170	-	ns
$t_f$	Fall time		-	20	-	ns

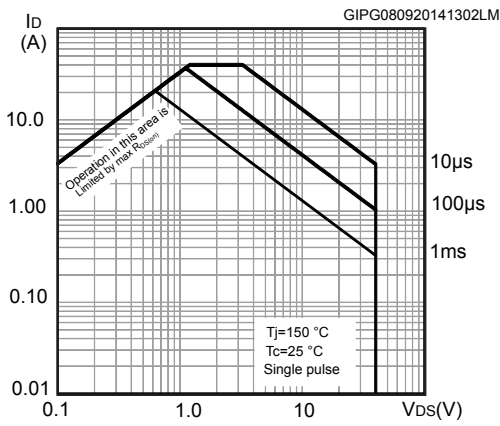
**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}, I_{SD} = -3\text{ A}$	-		-1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = -5\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = -32\text{ V}, T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	29		ns
$Q_{rr}$	Reverse recovery charge		-	27.6		nC
$I_{RRM}$	Reverse recovery current		-	-1.9		A

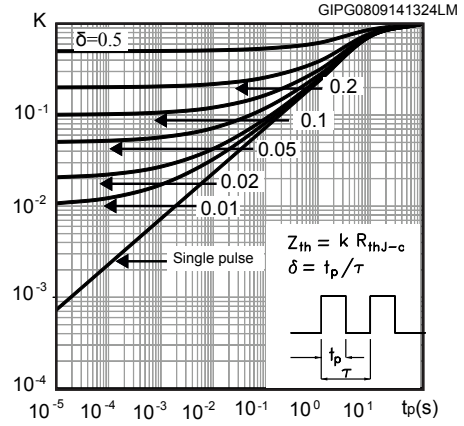
1. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

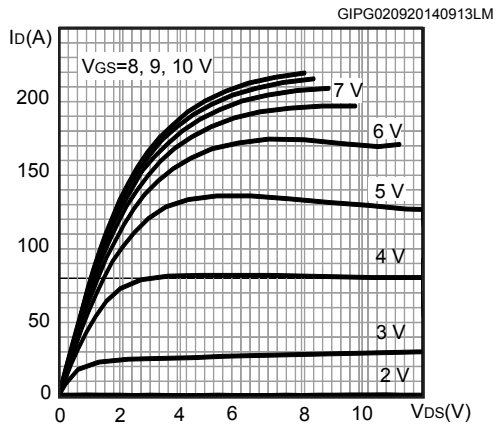
**Figure 1. Safe operating area**



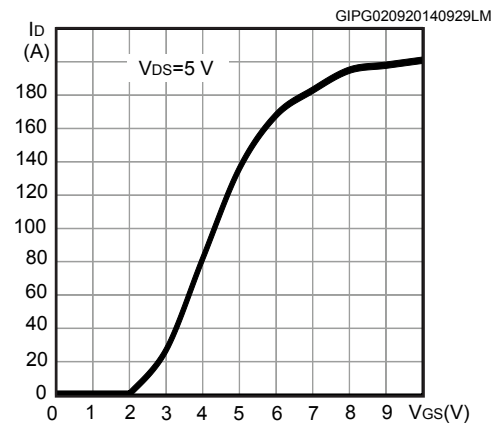
**Figure 2. Thermal impedance**



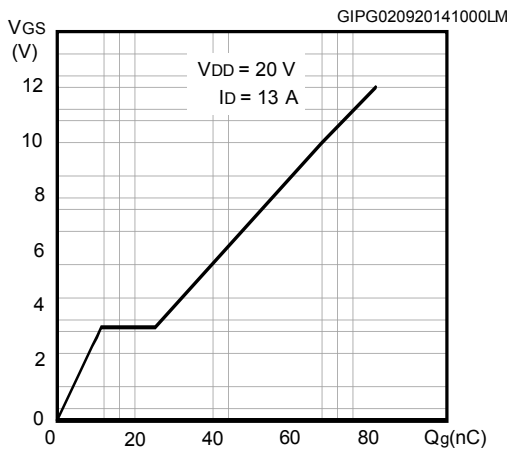
**Figure 3. Output characteristics**



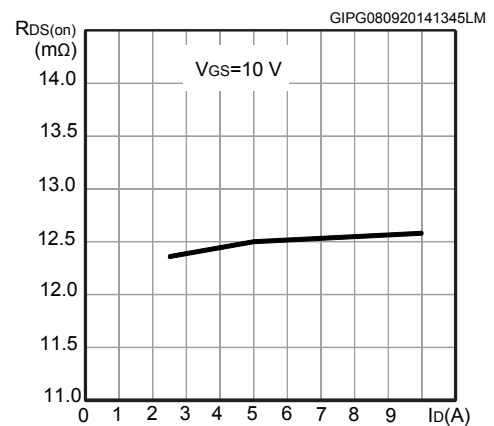
**Figure 4. Transfer characteristics**



**Figure 5. Gate charge vs gate-source voltage**

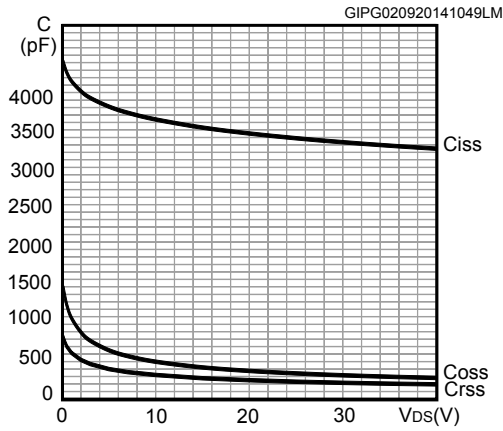


**Figure 6. Static drain-source on-resistance**

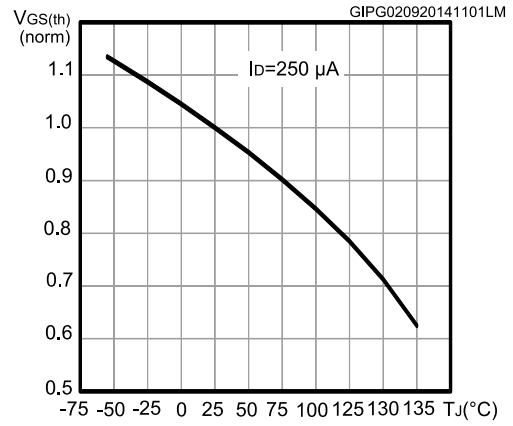


**Note:** For the P-channel Power MOSFET, current and voltage polarities are reversed.

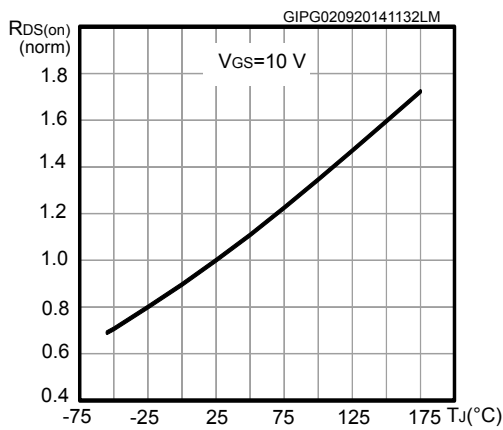
**Figure 7. Capacitance variation**



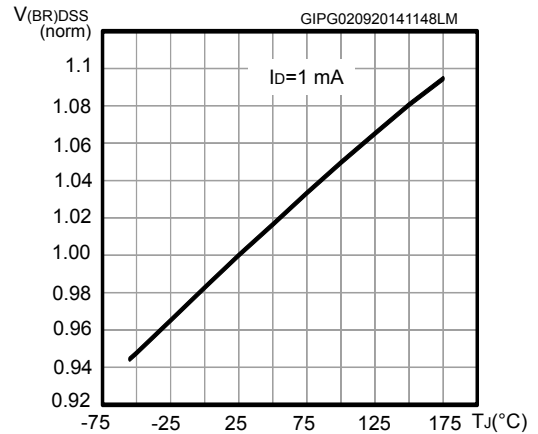
**Figure 8. Normalized gate threshold voltage vs temperature**



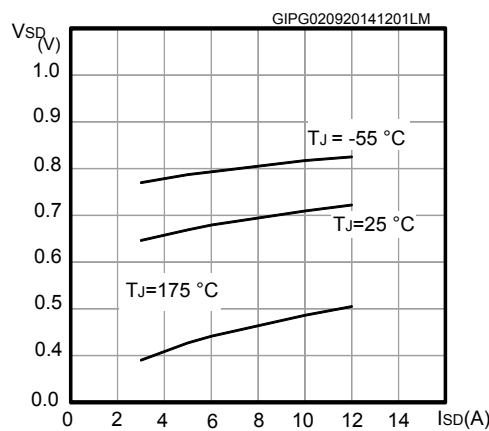
**Figure 9. Normalized on-resistance vs temperature**



**Figure 10. Normalized VBR(DSS) vs temperature**



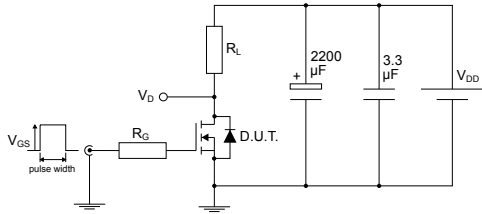
**Figure 11. Source-drain diode forward characteristics**



*Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.*

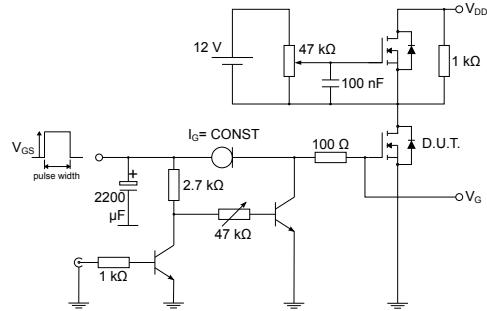
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**



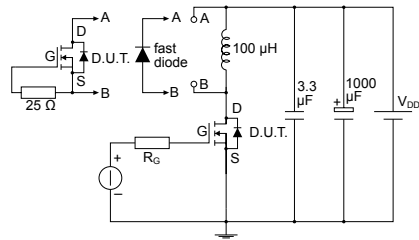
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**Figure 13. Test circuit for gate charge behavior**



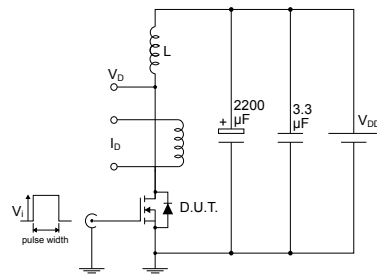
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**Figure 14. Test circuit for inductive load switching and diode recovery times**



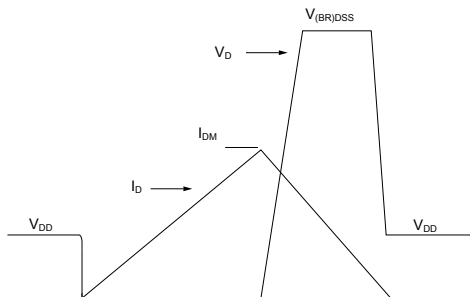
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**Figure 15. Unclamped inductive load test circuit**



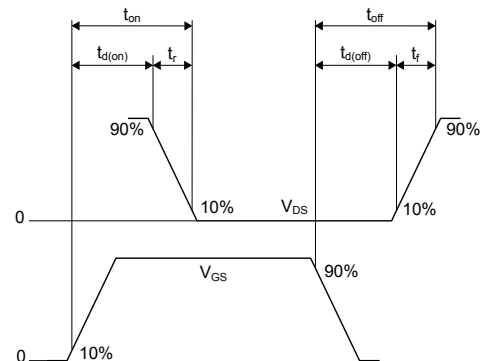
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**Figure 16. Unclamped inductive waveform**



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**Figure 17. Switching time waveform**



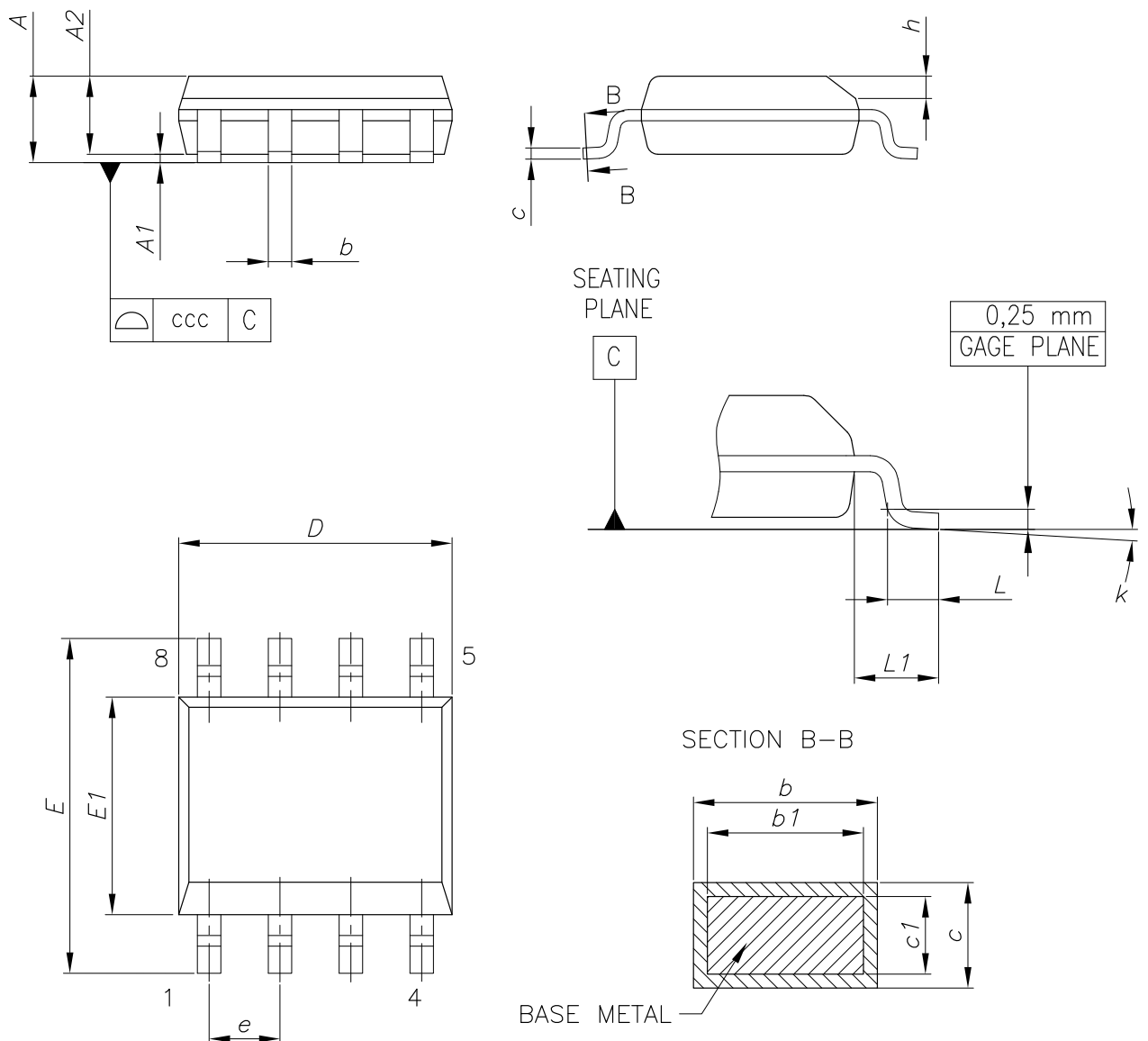
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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 SO-8 package information

Figure 18. SO-8 package outline

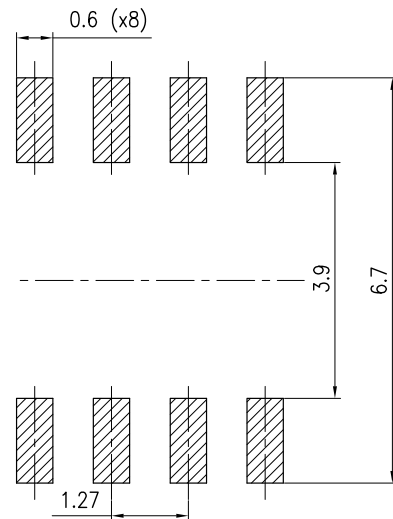


0016023\_So-807\_fig2\_Rev10

**Table 7. SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

**Figure 19. SO-8 recommended footprint (dimensions are in mm)**



0016023\_So-807\_footprint\_Rev10



## 4.2 SO-8 packing information

Figure 20. SO-8 tape and reel dimensions

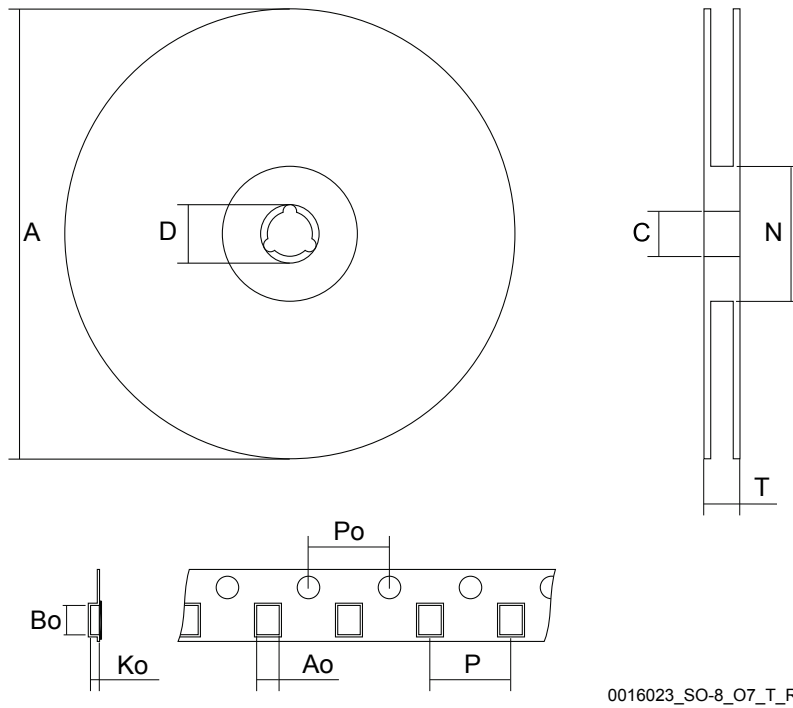
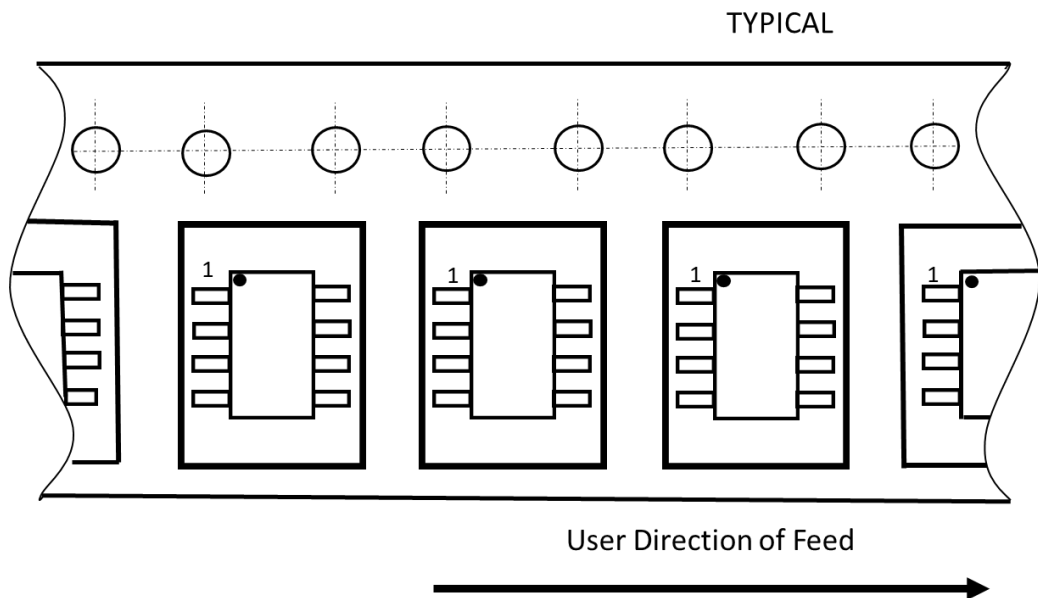


Figure 21. Tape orientation



**Table 8. SO-8 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5	-	6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-Jan-2014	1	First revision.
09-Sep-2014	2	<p>Changed the title.</p> <p>Updated <i>Section "Features" and Section "Description"</i>.</p> <p>Updated <i>Table 4: "On/off states", Table 5: "Dynamic", Table 6: "Switching times", Table 7: "Source-drain diode"</i>.</p> <p>Added <i>Section 3: "Electrical characteristics (curves)"</i>.</p>
16-Dec-2014	3	<p>Document status promoted from preliminary data to production data.</p> <p>Minor text changes.</p>
09-Dec-2020	4	<p>Updated title and features in cover page.</p> <p>Updated <i>Section 1 Electrical ratings and Section 2 Electrical characteristics</i>.</p> <p>Minor text changes.</p>
21-Jan-2021	5	<p>Updated <a href="#">Internal schematic</a>.</p> <p>Minor text changes.</p>

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