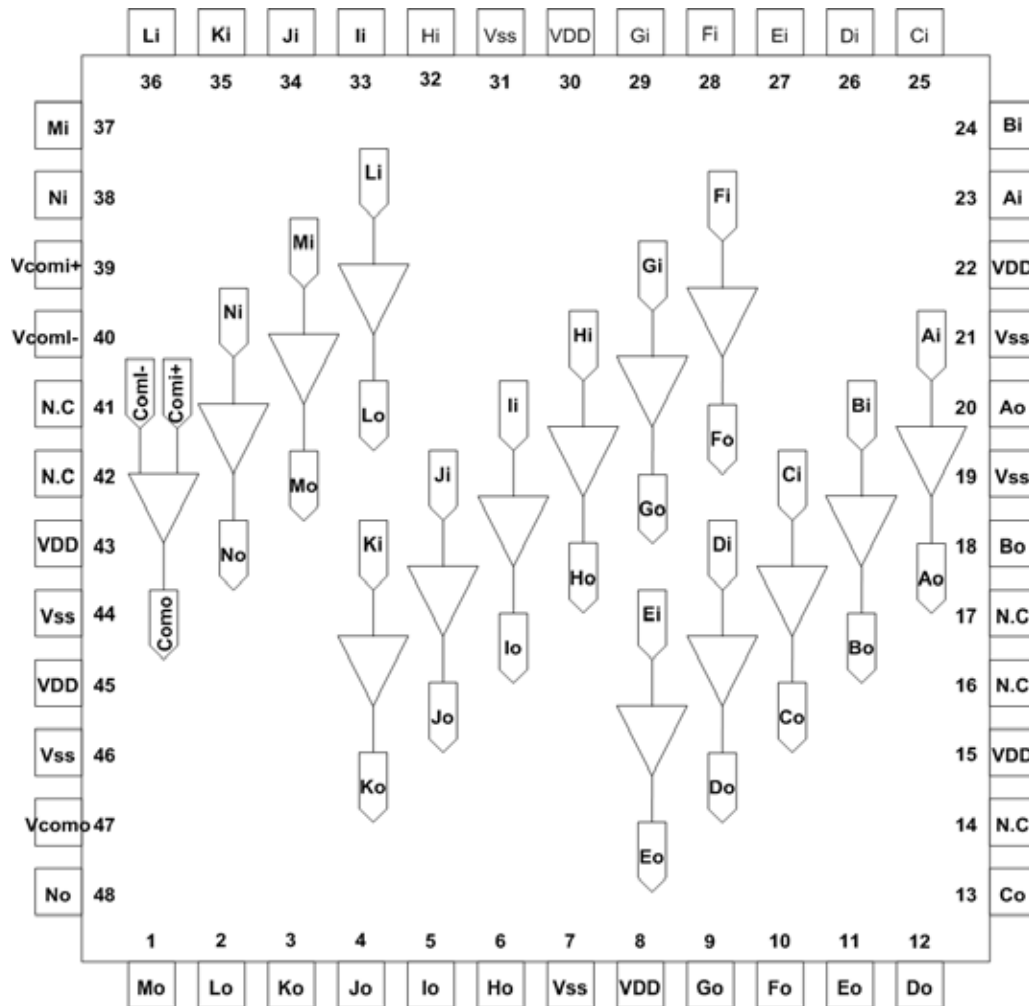




# 14+1 Channel Voltage Buffers for TFT LCD

## ■ PIN ASSIGNMENT ( E2 Type )



## ■ Ordering Information

Part No.	Top Mark	Package	Description
EC5575-F	AS15-F	TQFP48	14+1 lead-free
EC5575-G	AS15-G	TQFP48	14+1 Green Package
EC5575-FR	AS15-F	TQFP48	14+1 lead-free; (R) : Tape & reel
EC5575-GR	AS15-G	TQFP48	14+1 Green Package; (R) : Tape & reel
EC5575-HF	AS15-HF	TQFP48	14+1 lead-free ( H )
EC5575-HG	AS15-HG	TQFP48	14+1 Green Package ( H )
EC5575E2-F	AS15E2-F	TQFP48	14+1 (pin40 is Vcom-) lead-free
EC5575E2-G	AS15E2-G	TQFP48	14 channel (pin40 is Vcom-)Green Package
EC5575E2-HF	AS15E2-HF	TQFP48	14+1 (pin40 is Vcom-) lead-free ( H )
EC5575E2-HG	AS15E2-HG	TQFP48	14 channel (pin40 is Vcom-)Green Package (H)

Note: (H): Exposed pad (3.05x3.05 mm) ; (R) : Tape & reel

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## ■ ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)

Values beyond absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional device operation is not implied. Exposure to AMR conditions for extended periods may affect device reliability.

Supply Voltage between V <sub>S+</sub> and V <sub>S-</sub>	+18V	Storage Temperature	-65°C to +150°C
Input Voltage (For rail-to-rail )	V <sub>S-</sub> - 0.5V, V <sub>S+</sub> + 0.5V	Operating Temperature	-20°C to +85°C
Maximum Continuous Output Current (A ~ N offers)	30mA	Lead Temperature	260°C
Maximum Continuous Output Current(Com Buffer)	100mA	ESD Voltage	2kV
Maximum Die Temperature	+150°C		

### Important Note:

All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>

## ■ ELECTRICAL CHARACTERISTICS

V<sub>S+</sub> = +5V, V<sub>S-</sub> = -5V, R<sub>L</sub> = 10kΩ and C<sub>L</sub> = 10pF to 0V, T<sub>A</sub> = 25°C unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Units
<b>Input Characteristics</b>						
V <sub>OS</sub>	Input Offset Voltage	V <sub>CM</sub> = 0V		2	12	mV
TCV <sub>OS</sub>	Average Offset Voltage Drift	[1]		5		μV/°C
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = 0V		2	50	nA
R <sub>IN</sub>	Input Impedance			1		G
C <sub>IN</sub>	Input Capacitance			1.35		pF
<b>Output Characteristics</b>						
V <sub>OL</sub>	Output Swing Low	I <sub>L</sub> = -5mA (A, B, M, N rail-to-rail Buffers)		-4.92	-4.85	V
V <sub>OH</sub>	Output Swing High	I <sub>L</sub> = 5mA (A, B, M, N rail-to-rail Buffers)	4.85	4.92		V
V <sub>OL</sub>	Output Swing Low	I <sub>L</sub> = -5mA (C ~ L Buffers)	-3.5			V
V <sub>OH</sub>	Output Swing High	I <sub>L</sub> = 5mA (C ~ L Buffers)	3.5			V
I <sub>SC</sub>	Short Circuit Current	(A ~ N Buffers)		±120		mA
I <sub>OUT</sub>	Output Current	(A ~ N Buffers)		±30		mA
I <sub>SC(Com)</sub>	Short Circuit Current	(Com Buffer)		±300		mA
I <sub>OUT(Com)</sub>	Output Current	(Com Buffer)		±100		mA
<b>Power Supply Performance</b>						
PSRR	Power Supply Rejection Ratio	V <sub>S</sub> is moved from ±3.25V to ±7.75V	60	80		dB
I <sub>S</sub>	Supply Current (Per Amplifier)	No Load (A ~ N Buffers)		500	750	μA
I <sub>S(Com)</sub>	Supply Current	(Com Buffer)		5		mA
<b>Dynamic Performance</b>						
SR	Slew Rate [2]	-4.0V V <sub>OUT</sub> 4.0V, 20% to 80%		1		V/μs
t <sub>s</sub>	Settling to +0.1% (AV = +1)	(AV = +1), V <sub>O</sub> = 2V Step		5		μs
BW	-3dB Bandwidth	R <sub>L</sub> = 10K , C <sub>L</sub> = 10PF		2		MHz
PM	Phase Margin	R <sub>L</sub> = 10K , C <sub>L</sub> = 10PF		60		Degrees
CS	Channel Separation	f = 1 MHz		75		dB
1. Measured over operating temperature range 2. Slew rate is measured on rising and falling edges						

■ TYPICAL PERFORMANCE CURVES

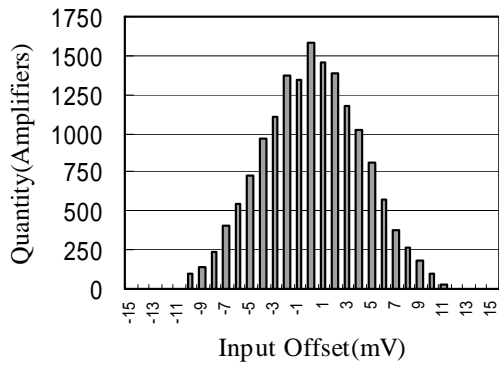


Figure (a) Input Offset Voltage Distribution

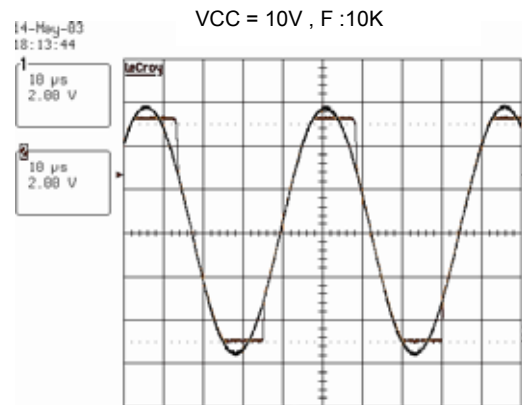


Figure (b) Input beyond the rails

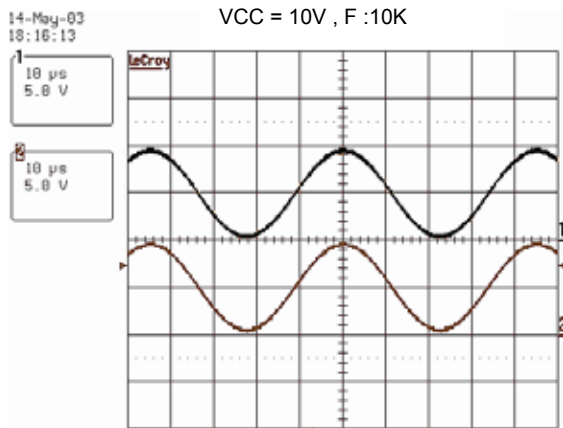


Figure (c) Rail to Rail Capability

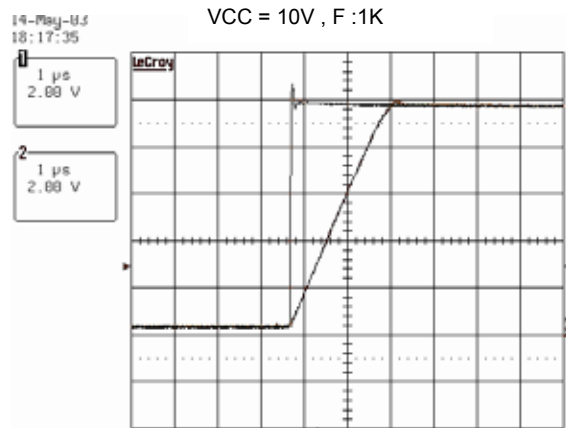


Figure (d) Large Signal Transient Response

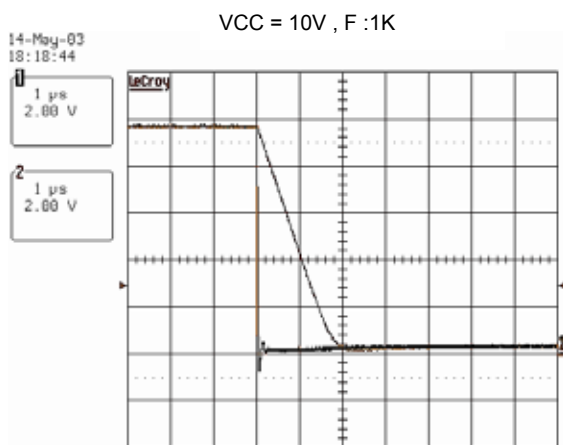


Figure (e) Large Signal Transient Response

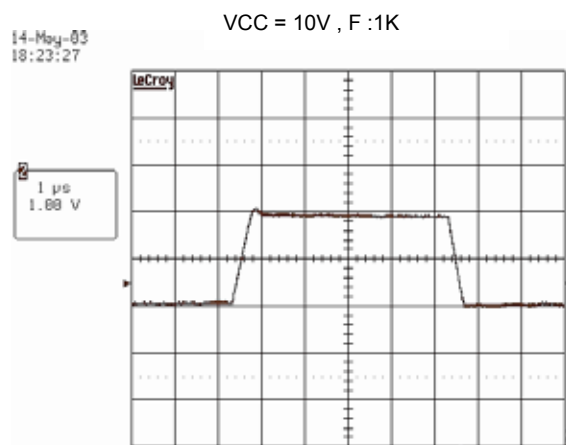


Figure (f) Small Signal Transient Response

■ TYPICAL PERFORMANCE CURVES

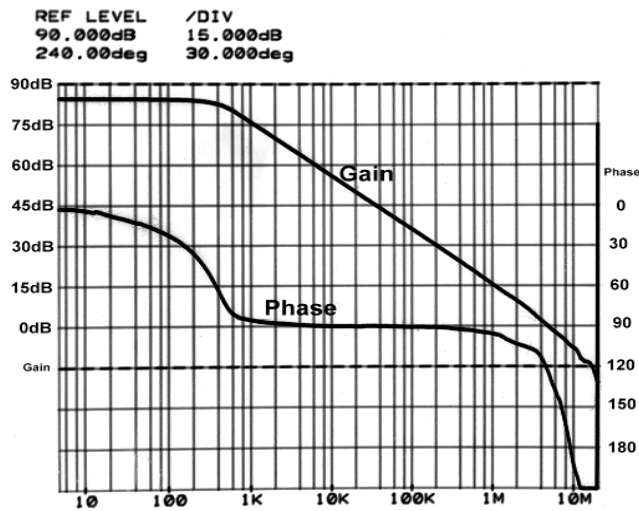


Figure (g) Open Loop Gain & Phase vs. Frequency

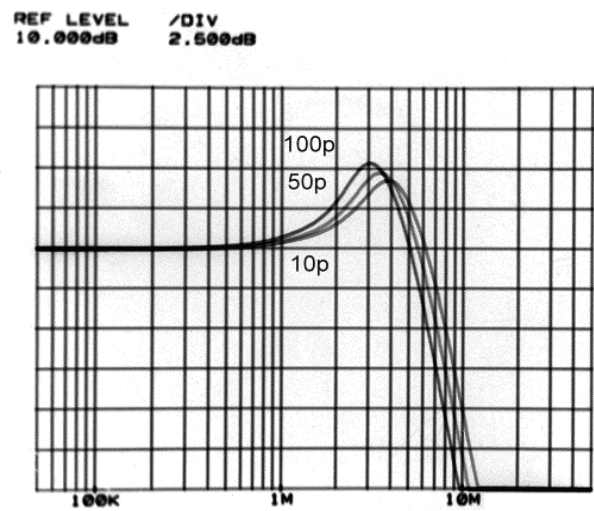


Figure (h) Frequency Response for Various  $C_L$

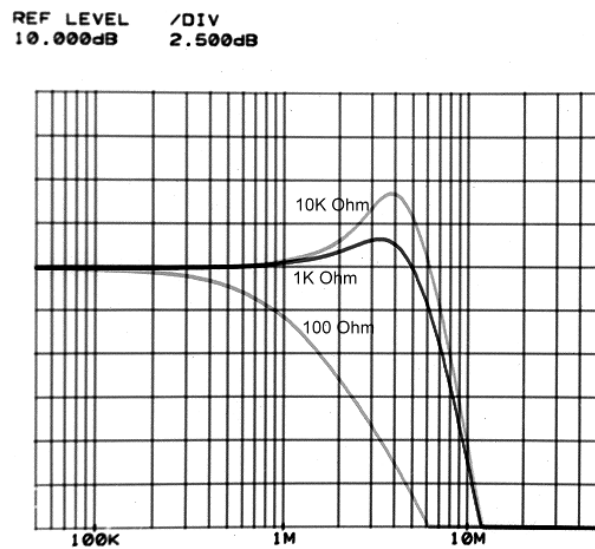


Figure (h) Frequency Response for Various  $R_L$

## ■ APPLICATIONS INFORMATION

### Product Description

The EC5575 rail-to-rail quad channels amplifier is built on an advanced high voltage CMOS process. It's beyond rails input capability and full swing of output range made itself an ideal amplifier for use in a wide range of general-purpose applications. The features of 1 $\mu$ S high slew rate, fast settling time, 2MHz of GBWP as well as high output driving capability have proven the EC5575 a good voltage reference buffer in TFT-LCD for grayscale reference applications. High phase margin and extremely low power consumption (500 $\mu$ A per amplifier) make the EC5575 ideal for Connected in voltage follower mode for low power high drive applications

### Supply Voltage, Input Range and Output Swing

The EC5575 can be operated with a single nominal wide supply voltage ranging from 6.5V to 18V with stable performance over operating temperatures of -20 °C to +85 °C.

With 500mV greater than rail-to-rail input common mode voltage range and 75dB of Common Mode Rejection Ratio, the EC5575 allows a wide range sensing among many applications without having any concerns over exceeding the range and no compromise in accuracy. The output swings of the EC5575 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. The output voltage swing can be even closer to the supply rails by merely decreasing the load current. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. The amplifier is operated under  $\pm$ 5V supply with a 10k $\Omega$  load connected to GND. The input is a 10Vp-p sinusoid. An approximately 9.985 Vp-p of output voltage swing can be easily achieved.

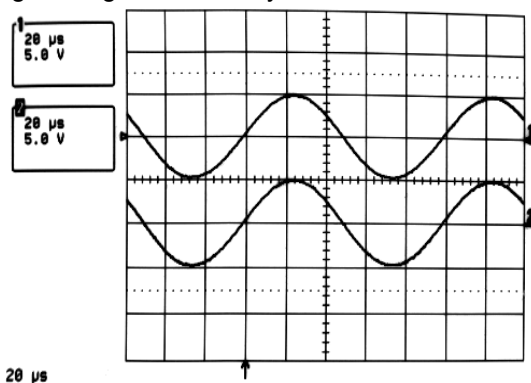


Figure 1. Operation with Rail-to-Rail Input and Output

### Output Short Circuit Current Limit

A  $\pm$ 120mA short circuit current will be limited by the EC5575 if the output is directly shorted to the positive or the negative supply. For an indefinitely output short circuit, the power dissipation could easily increase such that the device may be damaged. The internal

metal interconnections are well designed to prevent the output continuous current from exceeding  $\pm$ 30 mA such that the maximum reliability can be well maintained.

### Output Phase Reversal

The EC5575 is designed to prevent its output from being phase reversal as long as the input voltage is limited from  $V_{S-} - 0.5V$  to  $V_{S+} + 0.5V$ . Figure 2 shows a photo of the device output with its input voltage driven beyond the supply rails. Although the phase of the device's output will not be reversed, the input's over-voltage should be avoided. An improper input voltage exceeds supply range by more than 0.6V may result in an over stress damage.

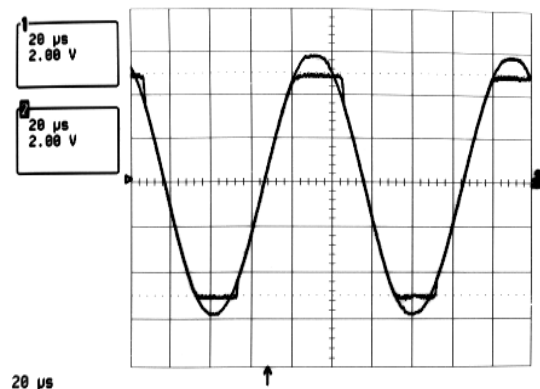


Figure 2. Operation with Beyond-the Rails Input

### Power Dissipation

The EC5575 is designed for maximum output current capability. Even though momentary output shorted to ground causes little damage to the device.

For the high drive amplifier EC5575, it is possible to exceed the 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area. The maximum power dissipation allowed in a package is determined according to:

$$P_{Dmax} = \frac{T_{Jmax} - T_{Amax}}{\Theta_{JA}}$$

Where:

$T_{Jmax}$  = Maximum Junction Temperature

$T_{Amax}$  = Maximum Ambient Temperature

$\Theta_{JA}$  = Thermal Resistance of the Package



## 14+1 Channel Voltage Buffers for TFT LCD

$P_{Dmax}$  = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_{S+} - V_O) * I_L]$$

When sourcing, and

$$P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_O - V_{S-}) * I_L]$$

When sinking.

Where:

$i = 1$  to 4

$V_S$  = Total Supply Voltage

$I_{Smax}$  = Maximum Supply Current Per Amplifier

$V_O$  = Maximum Output Voltage of the Application

$I_L$  = Load current

$R_L$  = Load Resistance =  $(V_{S+} - V_O) / I_L = (V_O - V_{S-}) / I_L$

A calculation for  $R_L$  to prevent device from overheat can be easily solved by setting the two  $P_{Dmax}$  equations equal to each other.

Pin Count	$\Theta_{ja}$ (oC/W)	$\Theta_{jc}$ (C/W)	
TQFP-48	67	31	Normal
TQFP-48	31	15	EXPOSED PAD

### Driving Capacitive Loads

The EC5575 is designed to drive a wide range of capacitive loads. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features make the EC5575 ideally for applications such as TFT LCD panel grayscale reference voltage buffers, ADC input amplifiers, etc.

As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The amplifiers drive 10pF loads in parallel with 10K  $\Omega$  with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5  $\Omega$  and 50  $\Omega$ ) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150  $\Omega$  and 10nF are typical. The advantage of a snubber is that it improves the settling and overshooting performance

while does not draw any DC load current or reduce the gain.

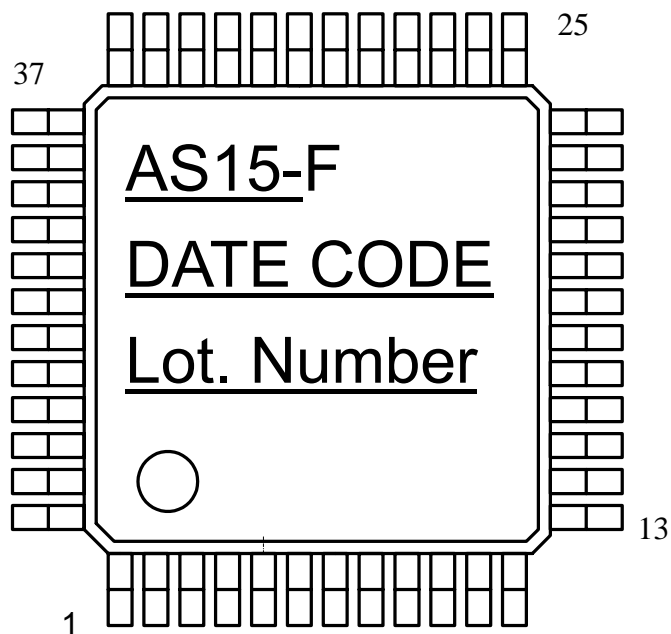
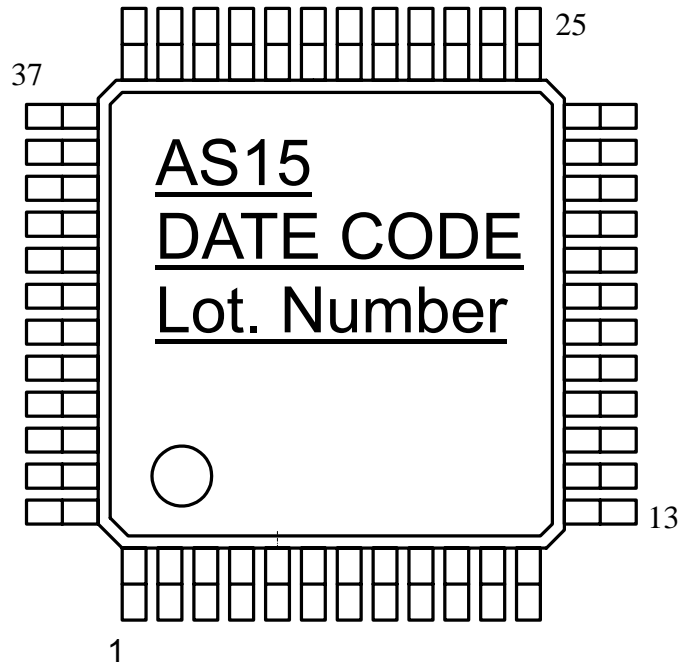
### Power Supply Bypassing and Printed Circuit Board Layout

With high phase margin, the EC5575 performs stable gain at high frequency. Like any high-frequency device, good layout of the printed circuit board usually comes with optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the  $V_{S-}$  pin is connected to ground, a 0.1  $\mu$ F ceramic capacitor should be placed from  $V_{S+}$  pin to  $V_{S-}$  pin as a bypassing capacitor. A 4.7 $\mu$ F tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7 $\mu$ F capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

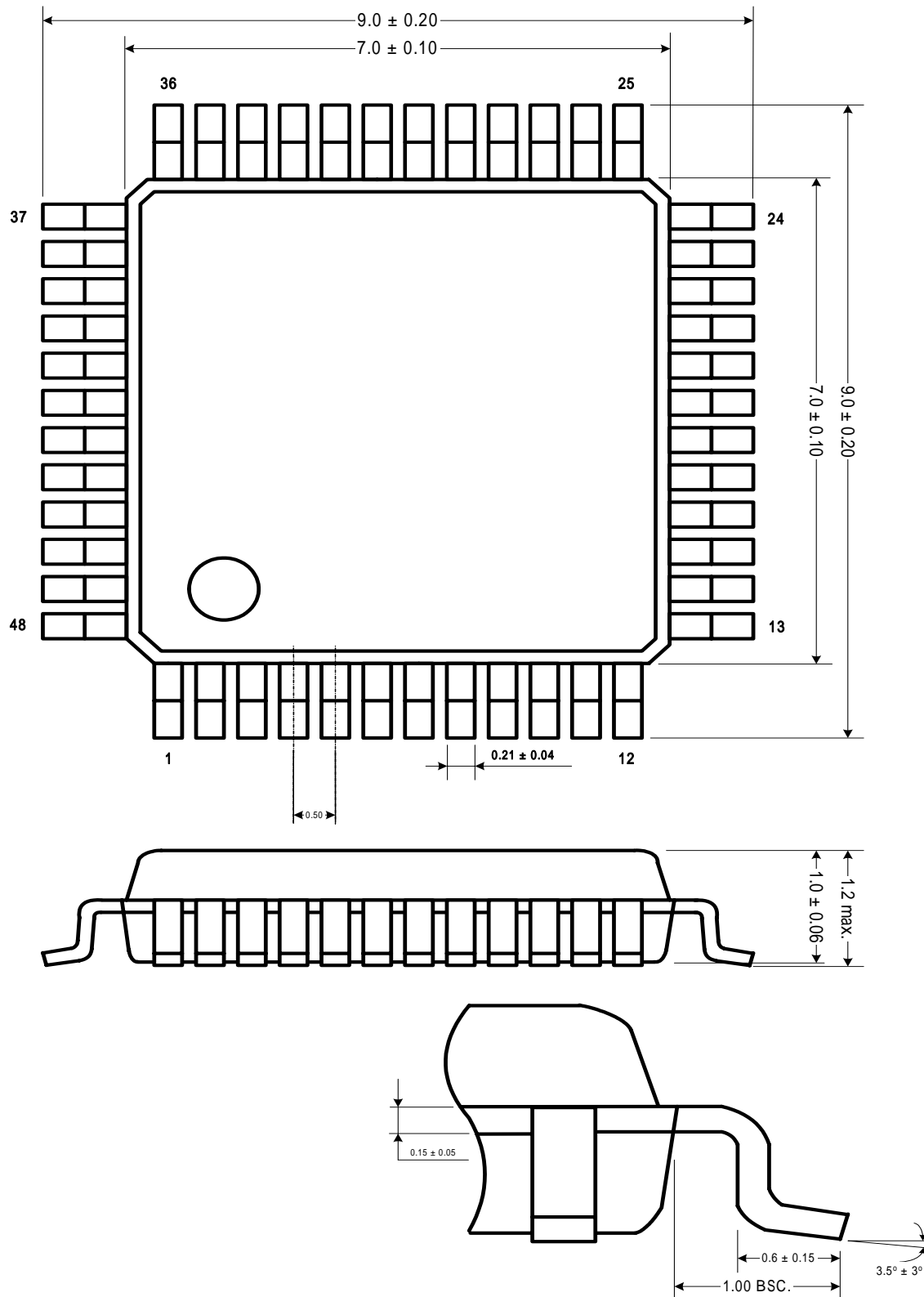




■ PACKAGE MARKING INDICATION (PACKAGE TYPE TQFP 48)



LEAD FREE TQFP48 ( MAKING )

**OUTLINE DIMENSIONS** (Dimensions shown in millimeters)




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