STP200N3LL

N-channel 30 V, 2.15 mΩ typ., 120 A Power MOSFET in a TO-220 package

Datasheet - production data

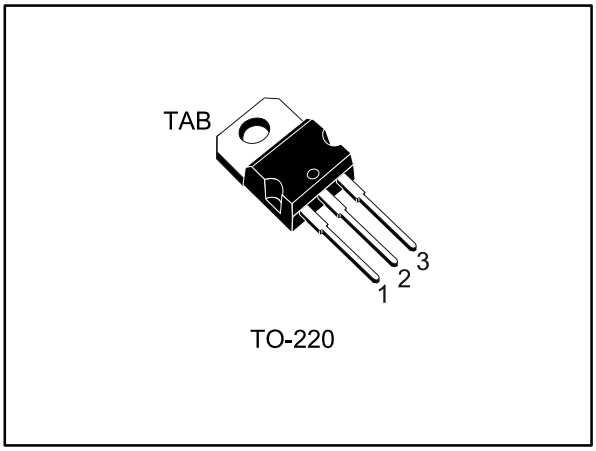
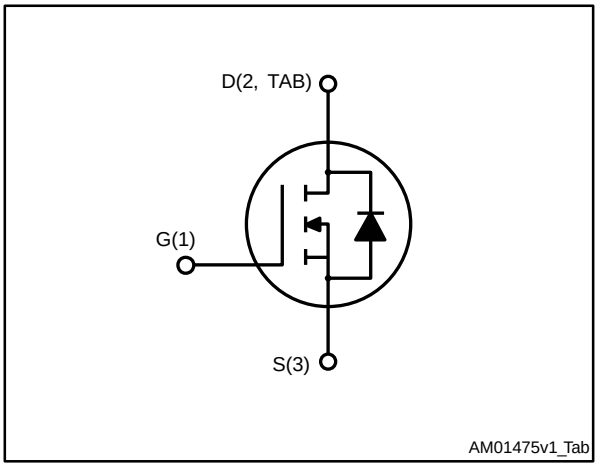


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP200N3LL	30 V	2.4 mΩ	120 A	176.5 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET with very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STP200N3LL	200N3LL	TO-220	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±20	
I_D	Drain current (continuous) at T_{case} = 25 °C (silicon limited)	200	A
I_D(1)	Drain current (continuous) at T_{case} = 25 °C	120	
I_D	Drain current (continuous) at T_{case} = 100 °C	120	
I_{DM}(2)	Drain current (pulsed)	480	
P_{TOT}	Total dissipation at T_{case} = 25 °C	176.5	W
E_{AS}(3)	Single pulse avalanche energy	300	mJ
T_{stg}	Storage temperature range	–55 to 175	°C
T_j	Operating junction temperature range		

Notes:

(1) Current is limited by package.

(2) Pulse width is limited by safe operating area.

(3) starting T_j = 25 °C, I_D = 68 A

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.85	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_{case} = 125 °C(1)			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		2.15	2.4	mΩ
		V_{GS} = 4.5 V, I_D = 60 A		2.5	3.1	

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	5200	-	pF
C_{oss}	Output capacitance		-	640	-	
C_{rss}	Reverse transfer capacitance		-	510	-	
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 120 A, V_{GS} = 4.5 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	53	-	nC
Q_{gs}	Gate-source charge		-	13	-	
Q_{gd}	Gate-drain charge		-	27	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A, gate DC bias = 0 V, magnitude of alternative signal = 20 mV	-	1.1	-	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 60 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	18	-	ns
t_r	Rise time		-	183	-	
$t_{d(off)}$	Turn-off delay time		-	90	-	
t_f	Fall time		-	108	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 60 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD} = 24 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	35		ns
Q_{rr}	Reverse recovery charge		-	34		nC
I_{RRM}	Reverse recovery current		-	2		A

Notes:

(1) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

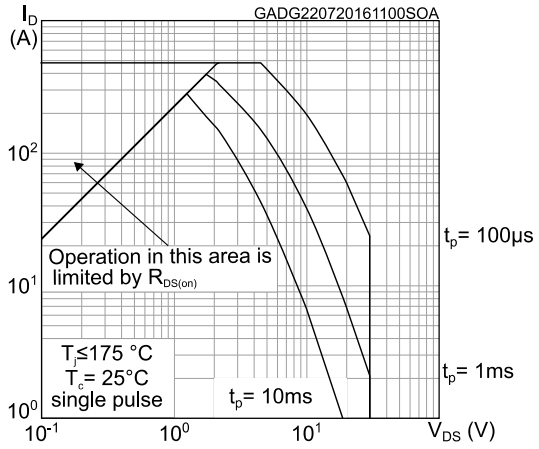


Figure 3: Thermal impedance

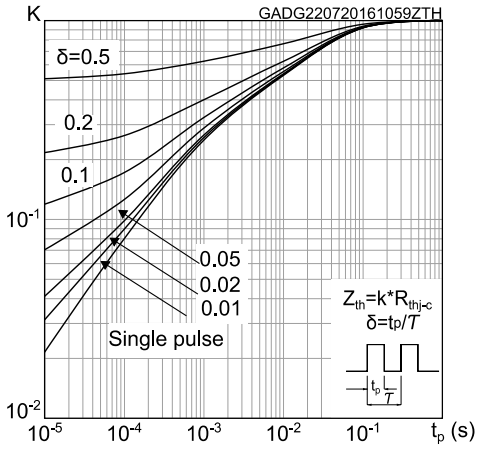


Figure 4: Output characteristics

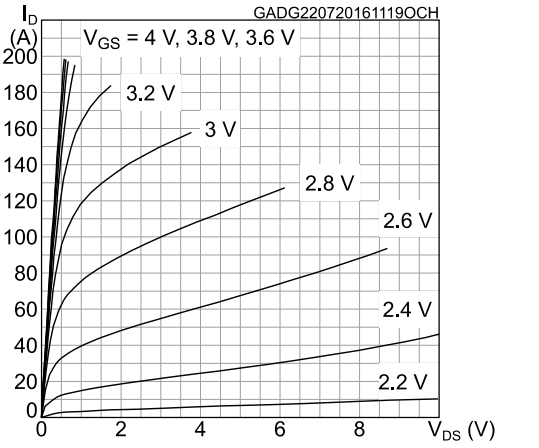


Figure 5: Transfer characteristics

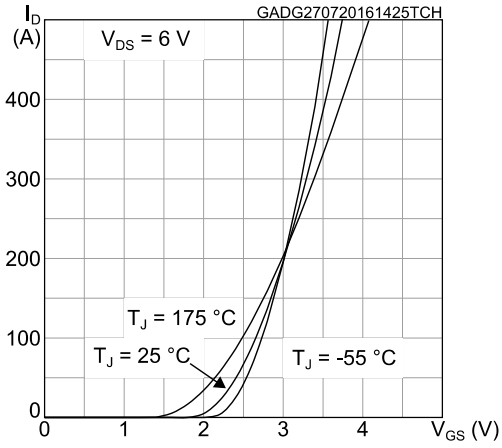


Figure 6: Gate charge vs gate-source voltage

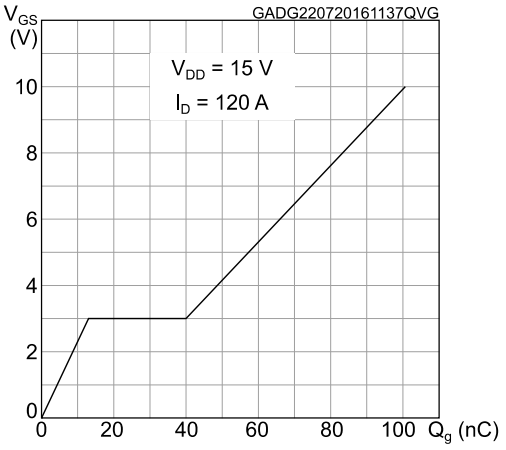


Figure 7: Static drain-source on resistance

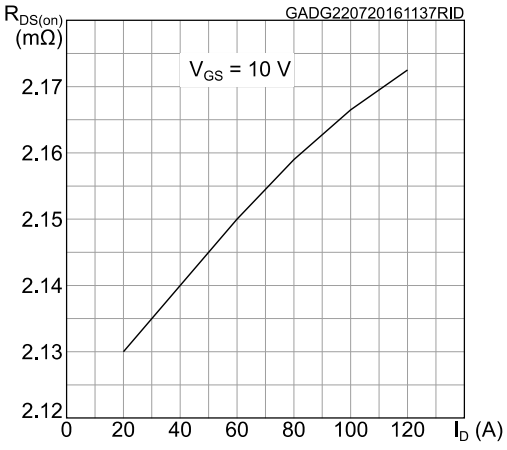


Figure 8: Capacitance variations

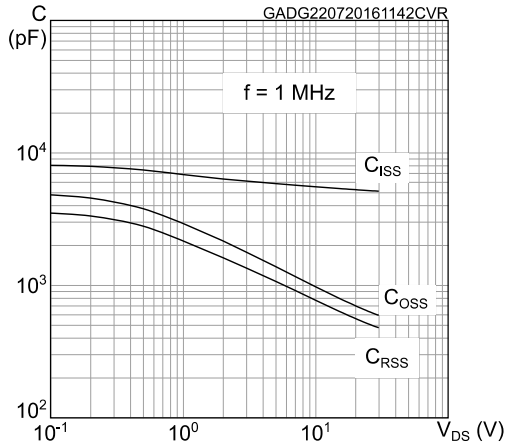


Figure 9: Normalized gate threshold voltage vs temperature

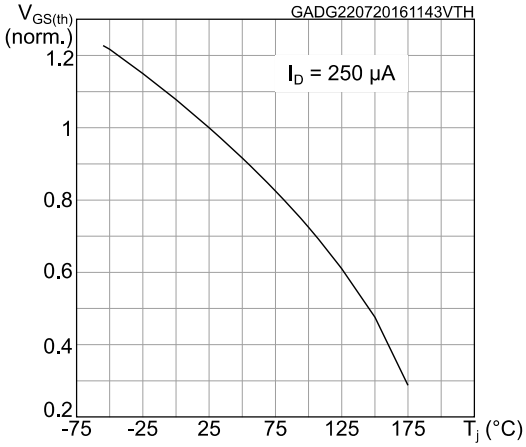


Figure 10: Normalized on-resistance vs temperature

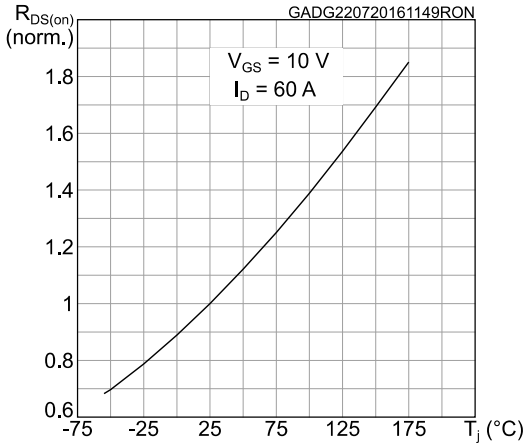


Figure 11: Normalized V(BR)DSS vs temperature

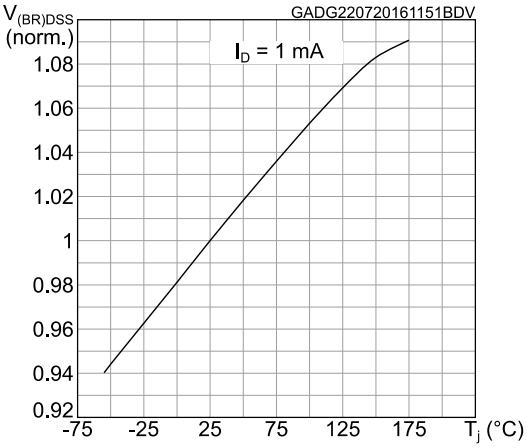
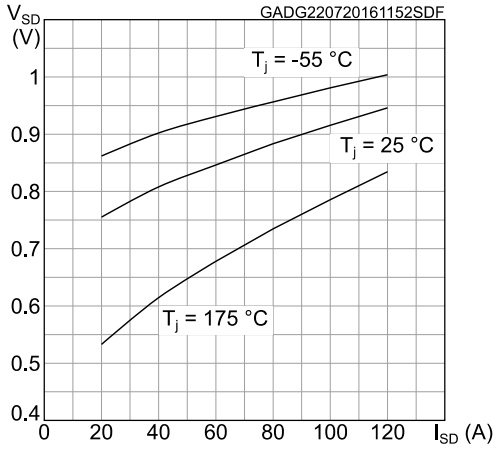


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

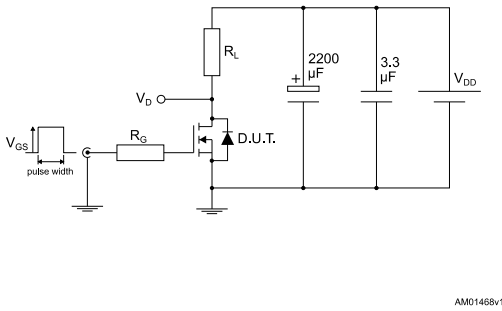


Figure 14: Test circuit for gate charge behavior

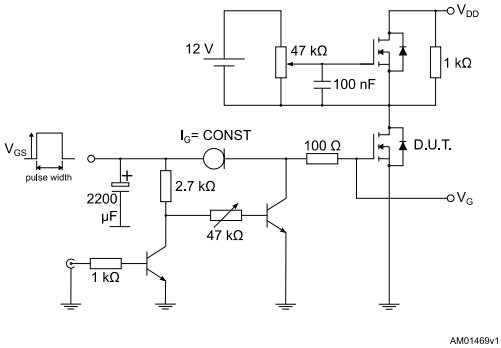


Figure 15: Test circuit for inductive load switching and diode recovery times

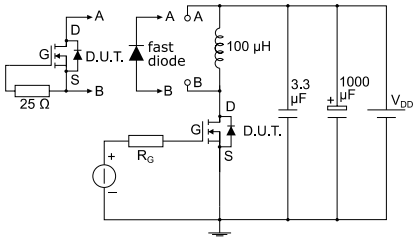


Figure 16: Unclamped inductive load test circuit

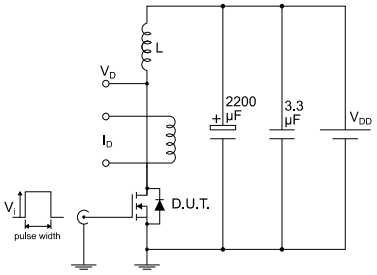


Figure 17: Unclamped inductive waveform

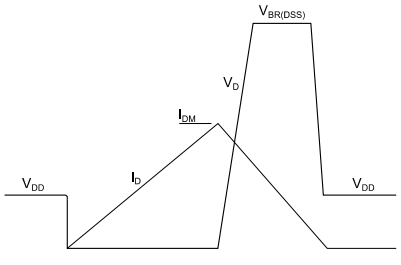
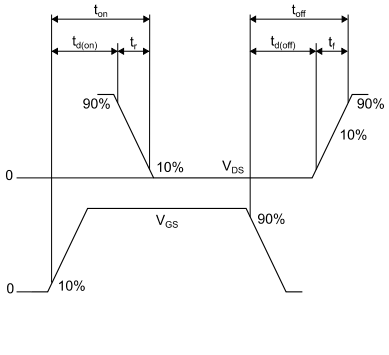


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 19: TO-220 type A package outline

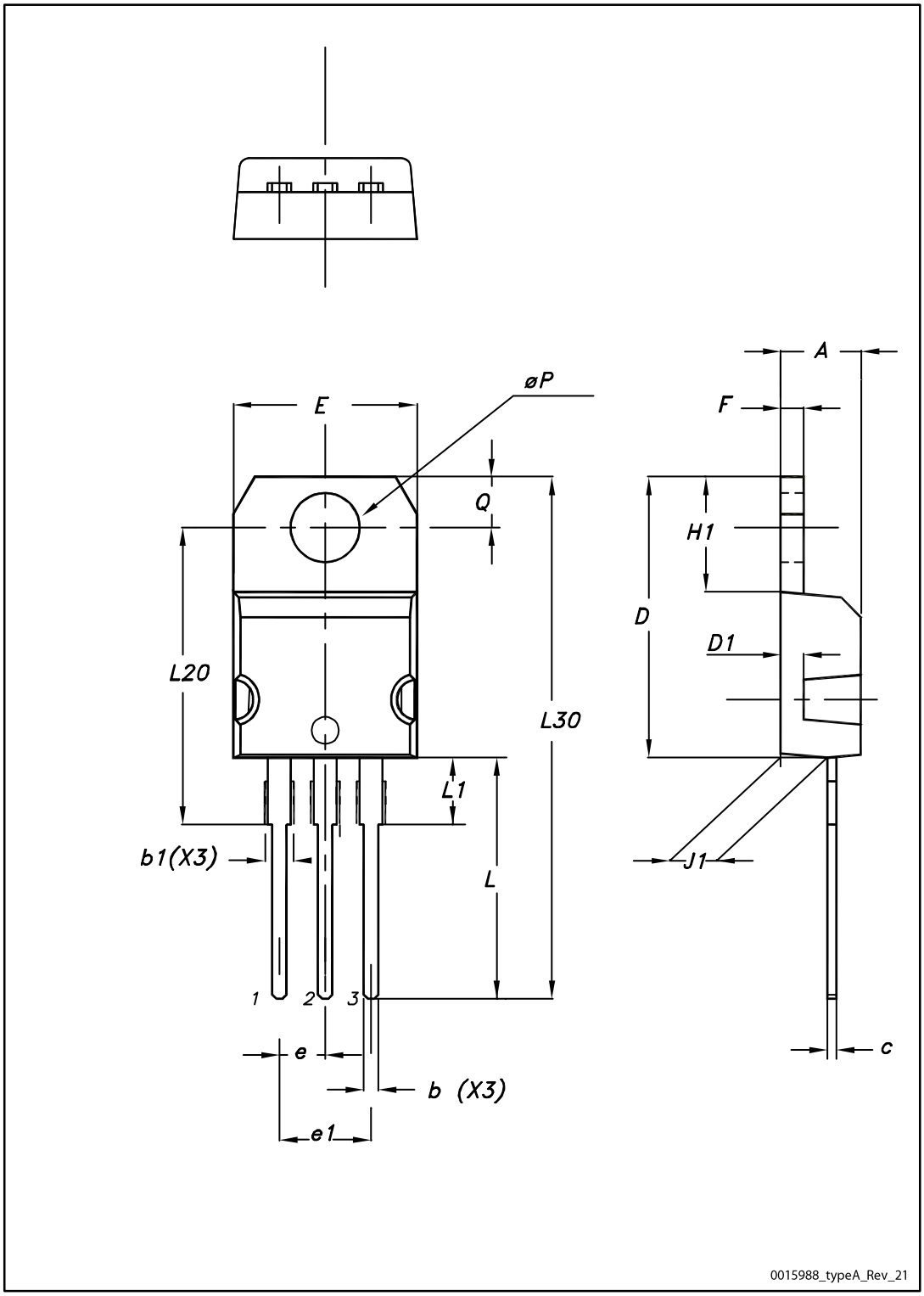


Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
14-Dec-2015	1	First release.
27-Jul-2016	2	Document status promoted from preliminary to production data. Updated *Section 2: "Electrical ratings"* and *Section 3: "Electrical characteristics"*. Added *Section 3.1: "Electrical characteristics (curves)"*. Minor text changes.

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