

# Eight Channel, High Speed, Unipolar, Ultrasound Pulser 1.5A 150V

## Features

- ▶ HVCMOS technology for high performance
- ▶ High density integrated ultrasound transmitter
- ▶ 0 to +150V output voltage
- ▶ ±1.5A source and sink current (min.)
- ▶ ±300mA current in CW mode
- ▶ Up to 18MHz operating frequency
- ▶ Matched delay times
- ▶ Built-in gate driver floating voltage regulator
- ▶ 2.5 to 3.3V CMOS logic interface

## Application

- ▶ Portable medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ NDT ultrasound transmission
- ▶ Pulse waveform generator

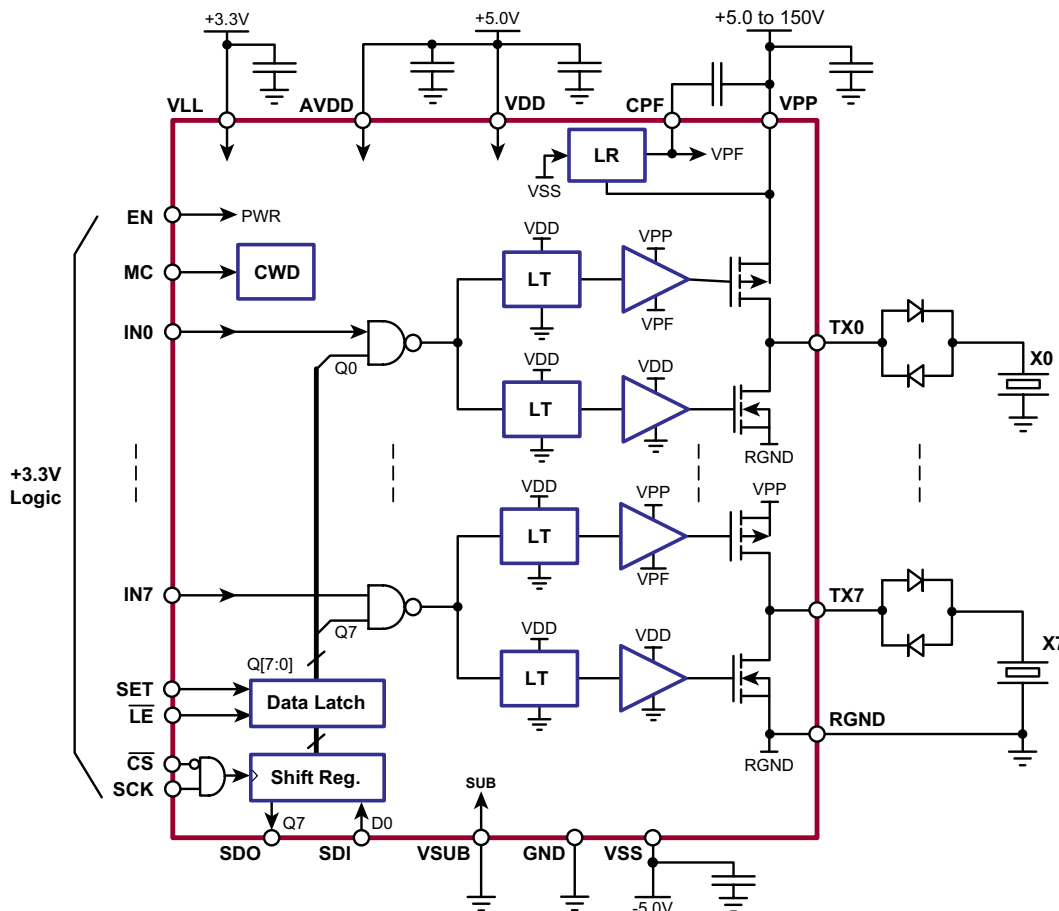
## General Description

The Supertex HV7355 is an eight-channel, unipolar, high voltage, high-speed pulse generator. It is designed for medical ultrasound applications. This high voltage and high speed integrated circuit can also be used for other piezoelectric, capacitive or MEMS sensors in ultrasonic nondestructive detection and sonar ranger applications.

The HV7355 consists of a controller logic interface circuit, level translators, MOSFET gate drivers and high current P-channel and N-channel MOSFETs as the output stage for each channel.

The output stages of each channel are designed to provide peak output currents over ±1.5A for pulsing, when MC = 1, with up to 150V swings. When MC = 0, all the output stages drop the peak current to ±500mA for low-voltage CW mode operation to save power. This direct coupling topology of the gate driver not only saves one high voltage capacitor per channel, but also makes the PCB layout easier.

## Typical Application Circuit



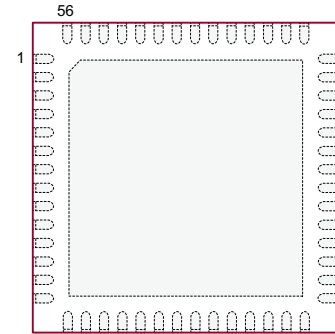
## Ordering Information

Part Number	Package Options	Packing
HV7355K6-G	56-Lead QFN (8x8)	250/Tray
HV7355K6-G M937	56-Lead QFN (8x8)	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

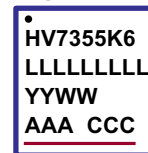


## Pin Configuration



56-Lead QFN  
(top view)

## Package Marking



L = Lot Number  
YY = Year Sealed  
WW = Week Sealed  
A = Assembler ID  
C = Country of Origin  
— = "Green" Packaging

Package may or may not include the following marks: Si or

56-Lead QFN

## Absolute Maximum Ratings

Parameter	Value
GND, RGND and $V_{SUB}$	0V
$V_{LL}$ , Positive logic supply	-0.5V to +7.0V
$V_{DD}$ , Positive logic and level translator supply	-0.5V to +7.0V
$V_{SS}$ , Negative level translator and LR supply	+0.5V to -7.0V
$V_{PP}$ , High voltage positive supply	-0.5V to +160V
( $V_{PP}$ - $V_{TXX}$ ) Voltage	-0.5V to +160V
( $V_{TXX}$ - RGND) Voltage	-0.5V to +160V
All logic input $PIN_x$ , $NIN_x$ and EN voltages	-0.5V to +7.0V
Operating temperature	-40°C to 125°C
Storage temperature	-65°C to 150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Typical Thermal Resistance

Package	$\theta_{ja}$
56-Lead QFN	21°C/W

## Power-Up Sequence

Step	Description
1	$V_{SS}$
2	$V_{LL}$ with logic signal low
3	$V_{DD}$
4	$V_{PP}$
5	EN & logic signal go to high

**Note:**

Powering up/down in any arbitrary sequence will not cause any damage to the device. The powering up/down sequence is only recommended in order to minimize possible inrush current.

## Truth Table (MC = X)

Logic Inputs			Output
EN	Q[7:0]	IN0~7	TX0~7
1	1111,1111	0	GND
1	1111,1111	1	VPP
1	0	X	GND
0	X	X	HiZ

## Power-Down Sequence

Step	Description
1	EN & logic signal low
3	$V_{PP}$
4	$V_{DD}$
5	$V_{LL}$
6	$V_{SS}$

## Drive Mode Control Table

MC	$I_{SC}$ (A)	$R_{onP}$	$R_{onN}$
0	0.50	18	13
1	1.6	8.0	3.0

**Note:**

$V_{PP} = +150V$ ,  $V_{DD} = +5.0V$ ,  $V_{LL} = +3.3V$ ,  $V_{SS} = -5.0V$ ,  $V_{SUB} = 0V$

**Operating Supply Voltages and Current (Eight Active Channels)**

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +150V$ ,  $T_A = 25^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{LL}$	Logic voltage reference	2.37	3.30	3.47	V	---
$V_{DD}$	Internal voltage supply	4.5	5.0	5.5	V	---
$V_{PP}$	Positive gate driver supply	$V_{DD}$	-	+150	V	---
$V_{SS}$	Negative low voltage supply	-5.5	-5.0	-4.5	V	---
$V_{PF}$	Gate driver floating voltage	-	5.0	-	V	---
$I_{LL}$	$V_{LL}$ Current EN = Low	-	2.0	10	$\mu A$	---
$I_{DDQ}$	$V_{DD}$ Current EN = Low	-	50	150	$\mu A$	f = 0MHz
$I_{DDEN}$	$V_{DD}$ Current EN = High	-	1.0	4.0	mA	f = 0MHz
$I_{DDEN}$	$V_{DD}$ Current MC = High	-	160	-	mA	f = 5.0MHz, continuous
$I_{DDENCW}$	$V_{DD}$ Current MC = Low	-	12	-	mA	no loads
$I_{SSQ}$	$V_{SS}$ Current EN = Low	-	5.0	20	$\mu A$	---
$I_{SSEN}$	$V_{SS}$ Current EN = High	-	1.0	4.0	mA	f = 0MHz
$I_{SSEN}$	$V_{SS}$ Current MC = High	-	95	-	mA	f = 5.0MHz, continuous
$I_{SSENCW}$	$V_{SS}$ Current MC = Low	-	50	-	mA	no loads
$I_{PPQ}$	$V_{PP}$ Current EN = Low	-	2.0	10	$\mu A$	---
$I_{PPEN}$	$V_{PP}$ Current EN = High	-	200	450	$\mu A$	f = 0MHz
$I_{PPEN}$	$V_{PP}$ Current MC = High	-	370	-	mA	f = 5.0MHz, continuous
$I_{PPENCW}$	$V_{PP}$ Current MC = Low	-	300	-	mA	no loads

**Under Voltage and Over Temperature Protection**

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{UVDD}$	$V_{DD}$ threshold	3.4	-	4.4	V	(Internal only)
$V_{UVLL}$	$V_{LL}$ threshold	-	1.7	-	V	(Internal only)
$V_{UVPF}$	$V_{PP} - V_{PF}$ threshold	2.5	-	3.8	V	(Internal only)

**Logic Inputs**

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +150V$ ,  $T_A = 25^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{IH}$	Input logic high voltage	$(V_{LL} - 0.4)$	-	$V_{LL}$	V	---
$V_{IL}$	Input logic low voltage	0	-	0.4	V	---
$I_{IH}$	Input logic high current	-	-	1.0	$\mu A$	---
$I_{IL}$	Input logic low current	-1.0	-	-	$\mu A$	---
$C_{IN}$	Input logic capacitance	-	-	5.0	pF	---

## Electrical Characteristics

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +150V$ ,  $T_A = 25^\circ C$ )

### P-Channel MOSFET Output, TX0~7

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{OUT}$	Output saturation current	1.4	1.6	-	A	MC = 1
$R_{ON}$	Channel resistance	-	8.0	-	$\Omega$	100mA
$I_{OUT}$	Output saturation current	0.5	-	-	A	MC = 0
$R_{ON}$	Channel resistance	-	18	-	$\Omega$	100mA

### N-Channel MOSFET Output, TX0~7

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{OUT}$	Output saturation current	1.5	1.7	-	A	MC = 1
$R_{ON}$	Channel resistance	-	3.0	-	$\Omega$	$I_{SD} = 100mA$
$I_{OUT}$	Output saturation current	0.5	-	-	A	MC = 0
$R_{ON}$	Channel resistance	-	22	-	$\Omega$	100mA

## AC Electrical Characteristics

(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +150V$ ,  $T_A = 25^\circ C$ )

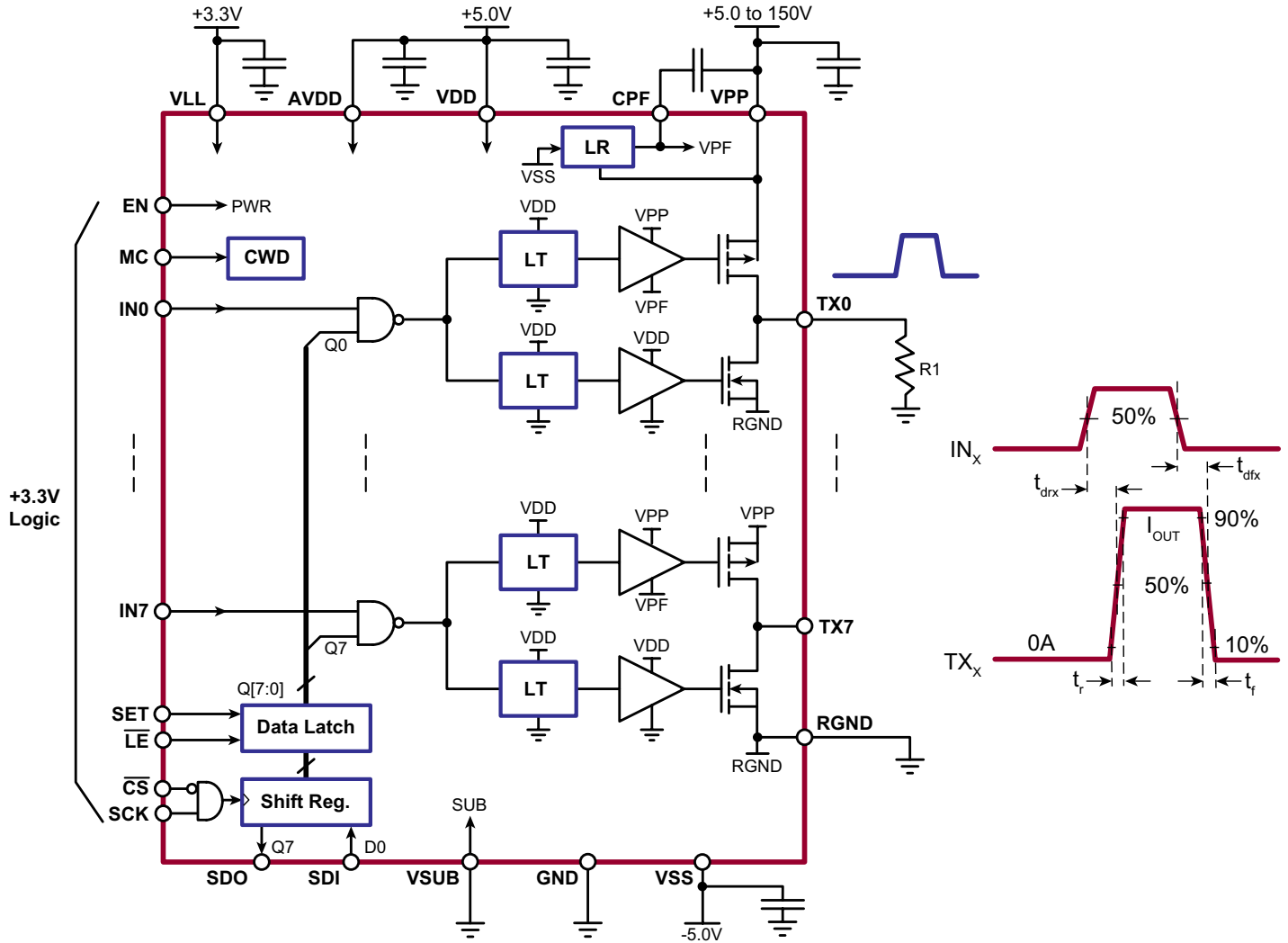
Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{inf}$	Input data rise/fall max time	-	-	10	ns	---
$t_r$	Output rise time	-	24	-	ns	330pF//2.5k $\Omega$ load
$t_f$	Output fall time	-	24	-	ns	see timing test diagram
$f_{OUT}$	Output frequency range	-	-	18	MHz	100 $\Omega$ resistor load, $V_{PP} = +90V$
$t_{EN-ON}$	Initial enable time	-	150	200	$\mu s$	2 $\mu F$ on each CPF pin to 90% of $V_{CPF}$
$t_{EN-OFF}$	Output disable time	-	2.0	5.0	$\mu s$	at 5.0MHz CW
$t_{dr}$	Delay time on inputs rise	-	5.0	-	ns	$V_{PP} = 25V$
$t_{df}$	Delay time on inputs fall	-	5.0	-	ns	1.0 $\Omega$ resistor load, 50% to 50%
$t_{dm}$	Delay on mode change	-	50	70	ns	see timing test diagram
$\Delta t_{DELAY}$	Delay time matching	-	$\pm 2.0$	-	ns	P to N, channel to channel
$t_j$	Delay jitter on rise or fall	-	15	-	ps	---

## Serial Data Interface Timing Characteristics

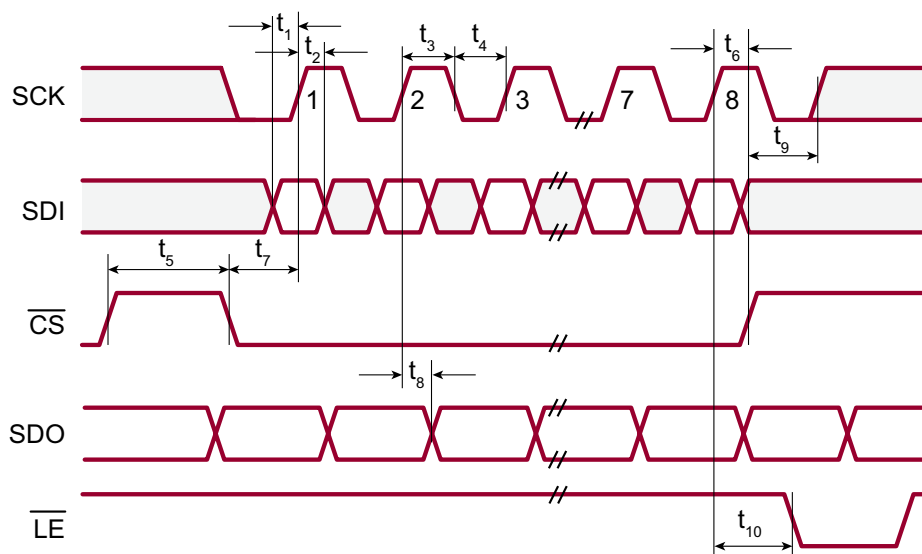
(Operating conditions, unless otherwise specified,  $V_{LL} = +3.3V$ ,  $V_{ADD} = V_{DD} = +5.0V$ ,  $V_{SS} = -5.0V$ ,  $V_{PP} = +150V$ ,  $T_A = 25^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions	
$f_{SCK}$	Serial clock max. frequency	25	-	-	MHz	All from/to 50% rise or fall edges (See timing diagram)	
$t_1$	SDI valid to SCK setup time	0	2.0	-	ns		
$t_2$	SDI valid to SCK hold time	4.0	-	-	ns		
$t_3$	SCK high time	9.0	-	-	ns		
$t_4$	SCK low time	9.0	-	-	ns		
$t_5$	$\overline{CS}$ pulse width	9.0	-	-	ns		
$t_6$	SCK high to $\overline{CS}$ high	7.0	-	-	ns		
$t_7$	$\overline{CS}$ low to SCK high	7.0	-	-	ns		
$t_8$	SDO delay from SCK rise edge	-	6.5	-	ns		SDO with 100pF to GND
$t_9$	$\overline{CS}$ high to SCK rise edge	7.0	-	-	ns		All from/to 50% rise or fall edges (See timing diagram)
$t_{10}$	SCK high to $\overline{LE}$ low	7.0	-	-	ns		

### Output Timing Test Diagram



### Serial Data Interface Timing Diagram



## Pin Description

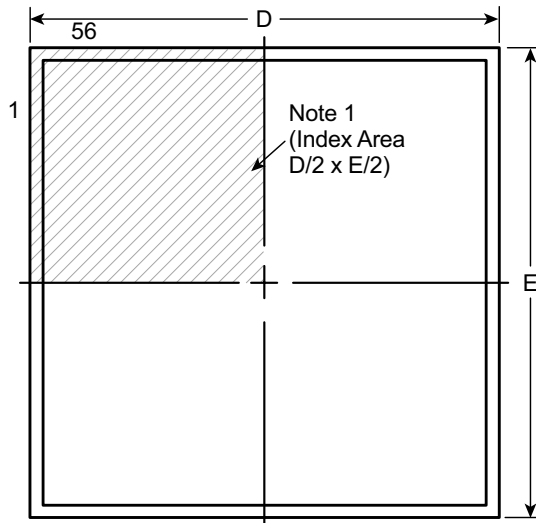
Pin	Name	Description
1	IN0	Input control for channels 0~7
2	IN1	
3	IN2	
4	IN3	
5	IN4	
6	IN5	
7	IN6	
8	$\overline{\text{IN7}}$	
9	$\underline{\text{CS}}$	Serial interface enable, active low
10	SDI	Serial shift register data input, MSB(D7) first, LSB(D0) last
11	LE	Latch enable, active low
12	SCK	Serial shift register clock
13	SDO	Serial shift register data output
14	SET	Set latch data Q[7:0] = 1, regardless the shift register inputs or LE, active high
15	MC	Output current mode control pin, see Drive Mode Control Table
16	VLL	Logic Hi voltage reference input (+3.3V)
17	VSS	Negative power supply(-5.0V)
18	CPF	Gate driver floating voltage decoupling capacitor to $V_{PP}$
19	VPP	Positive high voltage power supply (+150V)
20	VPP	
21	VPP	
22	VPP	
23	VDD	Positive voltage supply for gate drivers (+5.0V)
24	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
25	RGND	
26	RGND	
27	RGND	

## Pin Description (cont.)

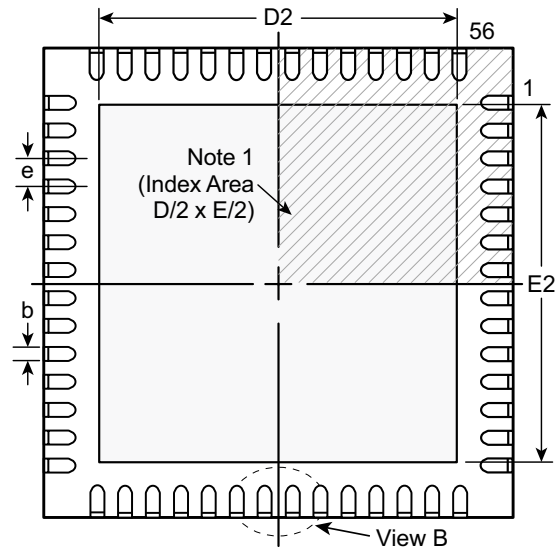
Pin	Name	Description
28	TX7	Output for channel 0~7
29	TX7	
30	TX6	
31	TX6	
32	TX5	
33	TX5	
34	TX4	
35	TX4	
36	TX3	
37	TX3	
38	TX2	
39	TX2	
40	TX1	
41	TX1	
42	TX0	
43	TX0	
44	RGND	Output return ground, 0V, RGND pins carry high current, must connect to load transducer ground
45	RGND	
46	RGND	
47	RGND	
48	VDD	Positive voltage supply for gate drivers (+5.0V)
49	VPP	Positive high voltage power supply (+150V)
50	VPP	
51	VPP	
52	VPP	
53	CPF	Gate driver floating voltage decoupling capacitor to $V_{PP}$
54	GND	Logic input reference ground, 0V
55	AVDD	Positive internal voltage supply (+5.0V)
56	EN	Chip power enable, active high
VSUB (Thermal Pad)		Substrate bottom is internally connected to the central thermal pad on the bottom of package. It must be connected to GND (0V) externally

# 56-Lead QFN Package Outline (K6)

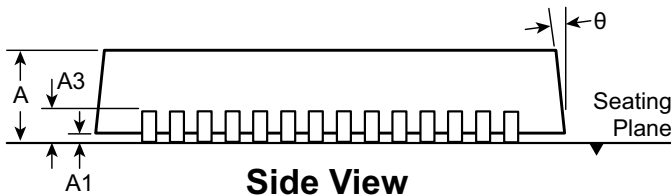
8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



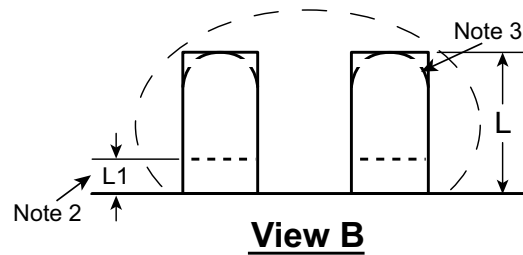
**Top View**



**Bottom View**



**Side View**



**View B**

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	7.85*	2.75	7.85*	2.75	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	8.00	5.70	8.00	5.70		0.40	-	-
	MAX	1.00	0.05		0.30	8.15*	6.70†	8.15*	6.70†		0.50	0.15	14°

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

Supertex Doc.#: DSPD-56QFNK68X8P050, Version A031010.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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