# Si53306

## 1:4 Low-Jitter Universal Buffer/Level Translator

### Features

- 4 differential or 8 LVCMOS outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: 1 to 725 MHz
- Any-format input with pin selectable output formats: LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS
- Synchronous output enable
- Independent $V_{DD}$ and $V_{DDO}$ : 1.8/2.5/3.3 V
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 16-QFN (3 mm x 3 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C

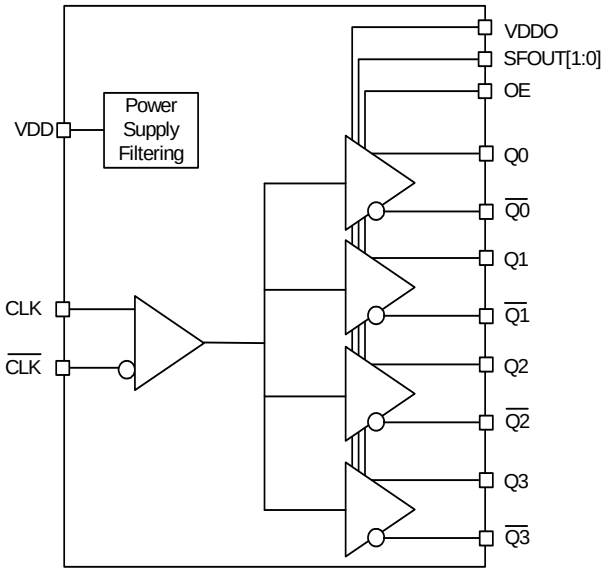
### Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

### Description

The Si53306 is an ultra low jitter four output differential buffer with pin-selectable output clock signal format. The Si53306 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53306 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

### Functional Block Diagram

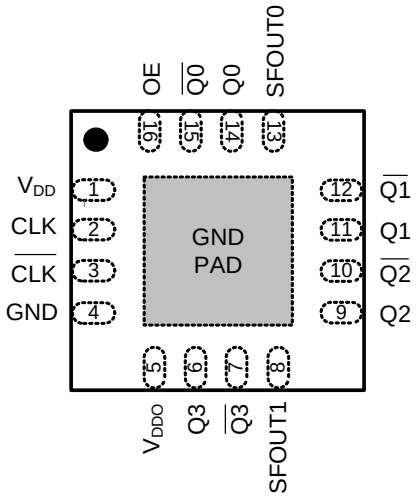




**Ordering Information:**

See page 25.

**Pin Assignments**




Patents pending

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# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | | –40 | — | 85 | °C |
| Supply Voltage Range* | $V_{DD}$ | LVDS, CML | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL, LVCMOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | HCSL | 2.97 | 3.3 | 3.63 | V |
| Output Buffer Supply Voltage* | $V_{DDOX}$ | LVDS, CML | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL, LVCMOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | HCSL | 2.97 | 3.3 | 3.63 | V |
| ***Note:** Core supply $V_{DD}$ and output buffer supplies $V_{DDO}$ are independent. | | | | | | |

### Table 2. Input Clock Specifications

($V_{DD}$=1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$=–40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential Input Common Mode Voltage | $V_{CM}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | 0.05 | — | — | V |
| Differential Input Swing (peak-to-peak) | $V_{IN}$ | | 0.2 | — | 2.2 | V |
| LVCMOS Input High Voltage | $V_{IH}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | $V_{DD}$ x 0.7 | — | — | V |
| LVCMOS Input Low Voltage | $V_{IL}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | — | — | $V_{DD}$ x 0.3 | V |
| Input Capacitance | $C_{IN}$ | CLK pins with respect to GND | — | 5 | — | pF |

**Table 3. DC Common Characteristics**
($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | | — | 55 | 100 | mA |
| Output Buffer Supply Current (Per Clock Output) @100 MHz (diff) @200 MHz (CMOS) | $I_{DDOX}$ | LVPECL (3.3 V) | — | 35 | — | mA |
| | | Low Power LVPECL (3.3 V)* | — | 35 | — | mA |
| | | LVDS (3.3 V) | — | 20 | — | mA |
| | | CML (3.3 V) | — | 40 | — | mA |
| | | HCSL, 100 MHz, 2 pF load (3.3 V) | — | 35 | — | mA |
| | | CMOS (2.5 V, SFOUT = Open/0), per output, $C_L$ = 5 pF, 200 MHz | — | 10 | — | mA |
| | | CMOS (3.3 V, SFOUT = 0/1), per output, $C_L$ = 5 pF, 200 MHz | — | 20 | — | mA |
| Voltage Reference | $V_{REF}$ | $V_{REF}$ output pin (VDD = 2.5 V, 3.3 V) | — | VDD/2 | — | V |
| Input High Voltage | $V_{IH}$ | SFOUTX, OEX | 0.8 x VDD | — | — | V |
| Input Mid Voltage | $V_{IM}$ | SFOUTX, 3-level input pins | 0.45 x VDD | 0.5 x VDD | 0.55 x VDD | V |
| Input Low Voltage | $V_{IL}$ | SFOUTX, OEX | — | — | 0.2 x VDD | V |
| Output Voltage High | $V_{OH}$ | $I_{DD}$ = –1 mA | 0.8xVDD | — | — | V |
| Output Voltage Low | $V_{OL}$ | $I_{DD}$ = 1 mA | — | — | 0.2xVDD | V |
| Internal Pull-down Resistor | $R_{DOWN}$ | SFOUTX | — | 25 | — | kΩ |
| Internal Pull-up Resistor | $R_{UP}$ | SFOUTX, OEX | — | 25 | — | kΩ |
| ***Note:** Low-power LVPECL mode supports an output termination scheme that will reduce overall system power. | | | | | | |

### Table 4. Output Characteristics (LVPECL)

($V_{DD}$ = $V_{DDOX}$ = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output DC Common Mode Voltage | $V_{COM}$ | | $V_{DDOX}$ – 1.595 | — | $V_{DDOX}$ – 1.245 | V |
| Single-Ended Output Swing* | $V_{SE}$ | | 0.55 | 0.80 | 1.050 | V |
| ***Note:** Unused outputs can be left floating. Do not short unused outputs to ground. | | | | | | |

### Table 5. Output Characteristics (Low Power LVPECL)

($V_{DD}$ = $V_{DDOX}$ = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output DC Common Mode Voltage | $V_{COM}$ | $R_L$ = 100 Ω across Qn and $\overline{Qn}$ | $V_{DDOX}$ – 1.895 | | $V_{DDOX}$ – 1.275 | V |
| Single-Ended Output Swing* | $V_{SE}$ | $R_L$ = 100 Ω across Qn and $\overline{Qn}$ | 0.25 | 0.60 | 0.85 | V |
| ***Note:** $R_L$ = 100 W across Qn and $\overline{Qn}$. | | | | | | |

### Table 6. Output Characteristics—CML

($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single-Ended Output Swing | $V_{SE}$ | Terminated as shown in Figure 7 (CML termination). | 300 | 400 | 500 | mV |

### Table 7. Output Characteristics—LVDS

($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 247 | — | 454 | mV |
| Output Common Mode Voltage ($V_{DDO}$ = 2.5 V or 3.3V) | $V_{COM1}$ | $V_{DDOX}$ = 2.38 to 2.63 V, 2.97 to 3.63 V, $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 1.10 | 1.25 | 1.35 | V |
| Output Common Mode Voltage ($V_{DDO}$ = 1.8 V) | $V_{COM2}$ | $V_{DDOX}$ = 1.71 to 1.89 V, $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 0.85 | 0.97 | 1.10 | V |

### Table 8. Output Characteristics—LVCMOS

($V_{DD}$ = $V_{DDOX}$ = 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High* | $V_{OH}$ | | 0.80 x $V_{DDOX}$ | — | — | V |
| Output Voltage Low* | $V_{OL}$ | | — | — | 0.20 x $V_{DDOX}$ | V |
| ***Note:** $I_{OH}$ and $I_{OL}$ per the Output Signal Format Table for specific $V_{DDOX}$ and SFOUTX settings. | | | | | | |

### Table 9. Output Characteristics—HCSL

($V_{DD}$ = $V_{DDOX}$ = 3.3 V ± 10%, TA = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High | $V_{OH}$ | $R_L$ = 50 Ω to GND | 550 | 700 | 850 | mV |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 50 Ω to GND | –150 | 0 | 150 | mV |
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 50 Ω to GND | 550 | 700 | 850 | mV |
| Crossing Voltage | $V_C$ | $R_L$ = 50 Ω to GND | 250 | 350 | 550 | mV |

### Table 10. AC Characteristics

($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,$T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency | F | LVPECL, low power LVPECL, LVDS, CML, HCSL | 1 | — | 725 | MHz |
| | | LVCMOS | 1 | — | 200 | MHz |
| Duty Cycle<br>**Note:** 50% input duty cycle. | $D_C$ | 200 MHz, 20/80% $T_R/T_F$<10% of period (LVCMOS) (12 mA drive) | 40 | 50 | 60 | % |
| | | 20/80% $T_R/T_F$<10% of period (Differential) | 47 | 50 | 53 | % |
| Minimum Input Clock Slew Rate | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |

**Notes:**

1. HCSL measurements were made with receiver termination. See Figure 7 on page 17.
2. Output to Output skew specified for outputs with an identical configuration.
3. Defined as skew between any output on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

**Table 10. AC Characteristics (Continued)**
($V_{DD}$ = $V_{DDOX}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise/Fall Time | $T_R/T_F$ | LVPECL, LVDS, CML, HCSL[1], Low-Power LVPECL 20/80% | — | — | 400 | ps |
| | | 200 MHz, 20/80%, 2 pF load (LVCMOS) | — | — | 750 | ps |
| Minimum Input Pulse Width | $T_W$ | | 500 | — | — | ps |
| Additive Jitter (Differential Clock Input) | J | $V_{DD}$ = $V_{DDOX}$ = 2.5/3.3 V, LVPECL/LVDS, F = 725 MHz, 0.75 V/ns input slew rate | — | 50 | 65 | fs |
| Propagation Delay | $T_{PLH}$, $T_{PHL}$ | LVPECL | 425 | 625 | 825 | ps |
| | | LVDS | — | TBD | — | ps |
| Output Enable Time | $T_{EN}$ | F = 1 MHz | — | 2500 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output Disable Time | $T_{DIS}$ | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output to Output Skew[2] | $T_{SK}$ | LVCMOS, drive 12 mA to 2 pF | — | 60 | — | ps |
| | | LVPECL | — | 30 | 75 | ps |
| | | LVDS | — | 50 | — | ps |
| Part to Part Skew[3] | $T_{PS}$ | Differential | — | — | 150 | ps |
| Power Supply Noise Rejection[4] | PSRR | 10 kHz sinusoidal noise | — | –72.5 | — | dBc |
| | | 100 kHz sinusoidal noise | — | –70 | — | dBc |
| | | 500 kHz sinusoidal noise | — | –67.5 | — | dBc |
| | | 1 MHz sinusoidal noise | — | –62.5 | — | dBc |

**Notes:**
1. HCSL measurements were made with receiver termination. See Figure 7 on page 17.
2. Output to Output skew specified for outputs with an identical configuration.
3. Defined as skew between any output on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

**Table 11. Additive Jitter, Differential Clock Input**

| $V_{DD}$ | Input[1,2] | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz)[3] | |
|---|---|---|---|---|---|---|---|
| | Freq (MHz) | Clock Format | Amplitude $V_{IN}$ (Single-Ended, Peak-to-Peak) | Differential 20%-80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 150 | 200 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 145 | 195 |

**Notes:**
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

### Table 12. Additive Jitter, Single-Ended Clock Input

| $V_{DD}$ | Input[1,2] | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz)[3] | |
|---|---|---|---|---|---|---|---|
| | Freq (MHz) | Clock Format | Amplitude $V_{IN}$ (single-ended, peak to peak) | SE 20%-80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 200 | Single-ended | 1.70 | 1 | LVCMOS[4] | 120 | 160 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 150 | 200 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVCMOS[4] | 130 | 180 |
| 2.5 | 200 | Single-ended | 1.70 | 1 | LVCMOS[5] | 120 | 160 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 145 | 195 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVCMOS[5] | 140 | 180 |

**Notes:**
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input (see Figure 1). LVCMOS jitter is measured single-ended.
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11).
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11).

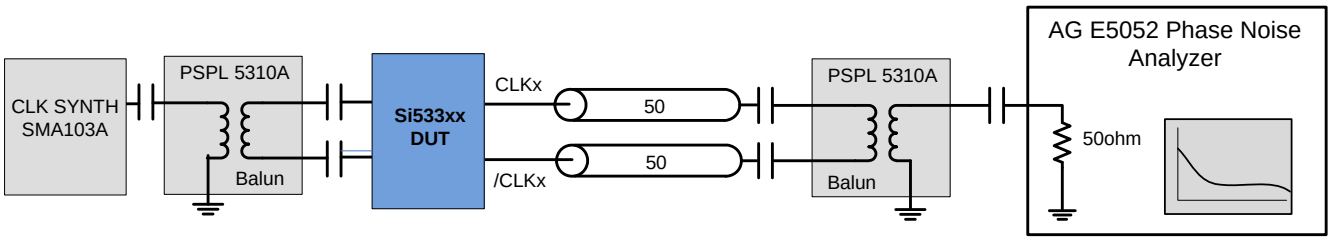



**Figure 1. Differential Measurement Method Using a Balun**

**Table 13. Thermal Conditions**

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $\theta_{JA}$ | Still air | 57.6 | °C/W |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | Still air | 41.5 | °C/W |

**Table 14. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | | –55 | — | 150 | °C |
| Supply Voltage | $V_{DD}$ | | –0.5 | — | 3.8 | V |
| Input Voltage | $V_{IN}$ | | –0.5 | — | $V_{DD}$+ 0.3 | V |
| Output Voltage | $V_{OUT}$ | | — | — | $V_{DD}$+ 0.3 | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 kΩ | — | — | 2000 | V |
| ESD Sensitivity | CDM | | — | — | 500 | V |
| Peak Soldering Reflow Temperature | $T_{PEAK}$ | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | $T_J$ | | — | — | 125 | °C |

**Note:** Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

# 2. Functional Description

The Si53306 is a low jitter, low skew 1:4 differential buffer. The device has a universal input that accepts most common differential or LVCMOS input signals. The Si53306 features control pins for output enable, output signal format selection and LVCMOS drive strength.

## 2.1. Universal, Any-Format Input

The Si53306 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 15 and 16 summarize the various ac- and dc-coupling options supported by the device. Figures 3 and 4 show the recommended input clock termination options. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended since low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. For more information, see “AN766: Understanding and Optimizing Clock Buffer Additive Jitter Performance”.

**Table 15. LVPECL, LVCMOS, and LVDS**

| | LVPECL | | LVCMOS | | LVDS | |
|---|---|---|---|---|---|---|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | N/A | N/A | No | No | Yes | No |
| 2.5/3.3 V | Yes | Yes | No | Yes | Yes | Yes |

**Table 16. HCSL and CML**

| | HCSL | | CML | |
|---|---|---|---|---|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | No | No | Yes | No |
| 2.5/3.3 V | Yes (3.3 V) | Yes (3.3 V) | Yes | No |

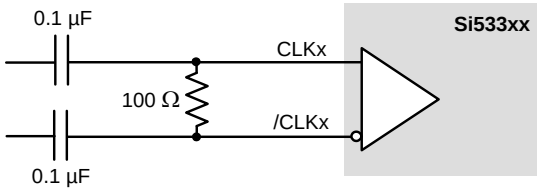



**Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination**

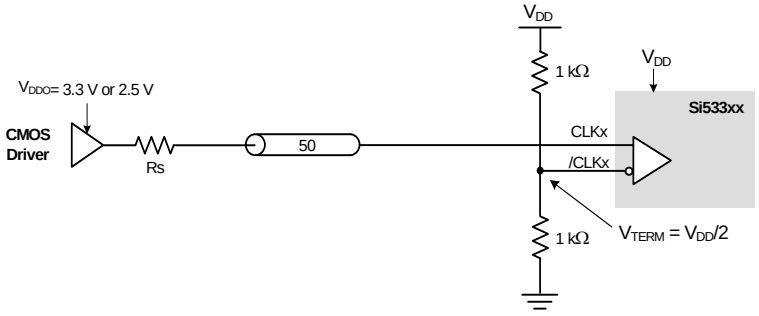
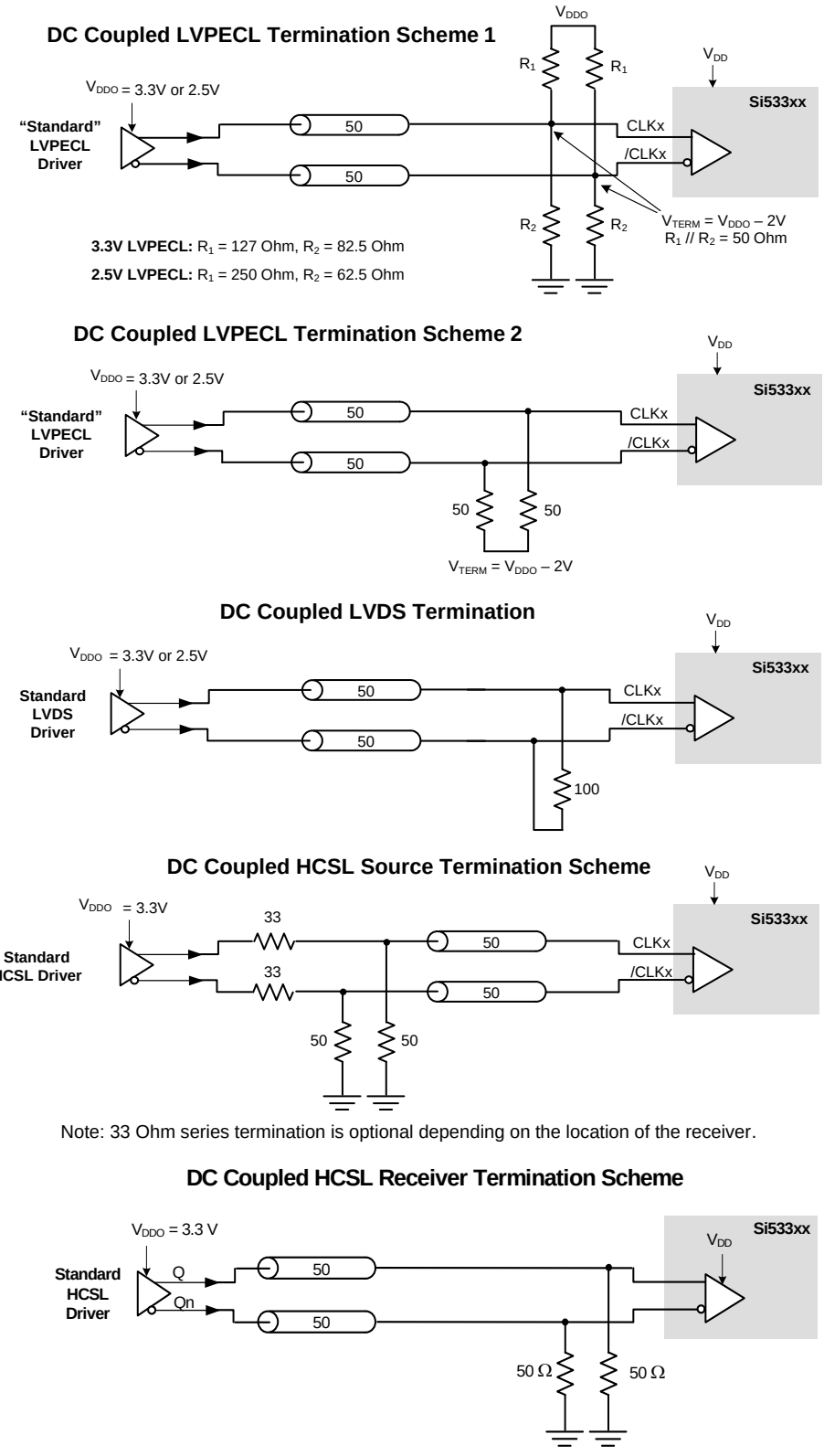



**Figure 3. LVCMOS DC-Coupled Input Termination**




Note: 33 Ohm series termination is optional depending on the location of the receiver.

**Figure 4. Differential DC-Coupled Input Terminations**

## 2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to $V_{DD}$. The inverting input is biased with a 75 kΩ pullup to $V_{DD}$.

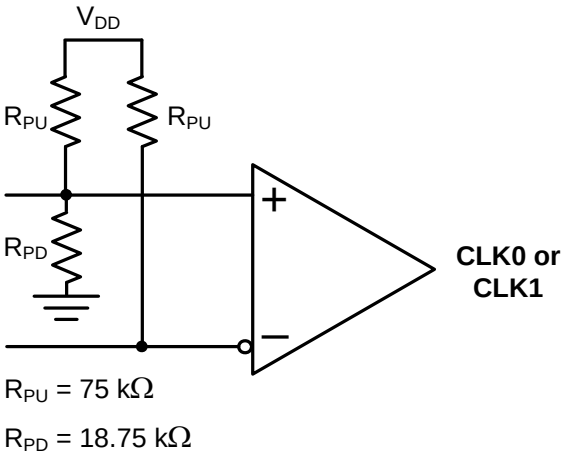



**Figure 5. Input Bias Resistors**

## 2.3. Universal, Any-Format Output Buffer

The Si53306 has highly flexible output drivers that support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUT1 and SFOUT0 are 3-level inputs that can be pin-strapped to select the output clock signal formats. This feature enables the device to be used for format translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each $V_{DDO}$ setting.

**Table 17. Output Signal Format Selection**

| SFOUT1 | SFOUT0 | $V_{DDOX}$ = 3.3 V | $V_{DDOX}$ = 2.5 V | $V_{DDOX}$ = 1.8 V |
|---|---|---|---|---|
| Open* | Open* | LVPECL | LVPECL | N/A |
| 0 | 0 | LVDS | LVDS | LVDS |
| 0 | 1 | LVCMOS, 24 mA drive | LVCMOS, 18 mA drive | N/A |
| 1 | 0 | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive | N/A |
| 1 | 1 | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive | N/A |
| Open* | 0 | LVCMOS, 6 mA drive | LVCMOS, 4 mA drive | N/A |
| Open* | 1 | LVPECL low power | LVPECL low power | N/A |
| 0 | Open* | CML | CML | CML |
| 1 | Open* | HCSL | N/A | N/A |

***Note:** SFOUTX are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin floats to $V_{DD}/2$.

## 2.4. Synchronous Output Enable

The Si53306 features a synchronous output enable (disable) feature. Output enable is sampled and synchronized on the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.

When OE is low, Q is held low and $\overline{Q}$ is held high for differential output formats. For LVCMOS output format options, both Q and $\overline{Q}$ are held low when OE is set low. The device outputs are enabled when the output enable pin is unconnected. See Table 10, “AC Characteristics,” on page 7 for output enable and output disable times.

## 2.5. Output Enable Logic

All four outputs are controlled with a single output enable (OE) pin. Table 18 summarizes the input and output clock based upon the state of the input clock and the OE pin.

**Table 18. Input Mux and Output Enable Logic**

| CLK | OE[1] | Q[2] |
|---|---|---|
| L | H | L |
| H | H | H |
| X | L | L[3] |

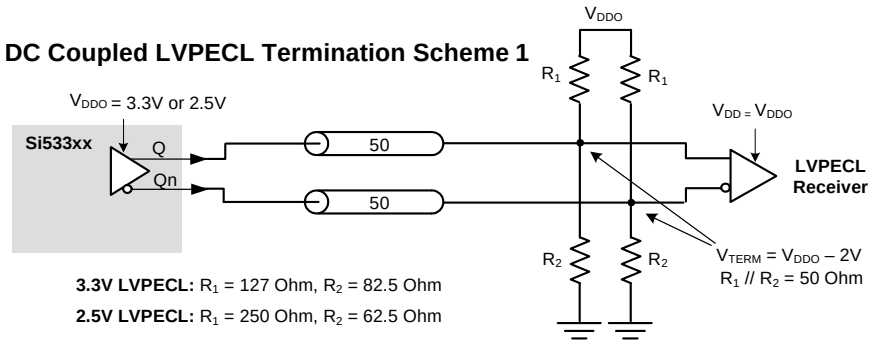
**Notes:**
1. Output enable active high
2. On the next negative transition of CLK.
3. Single-end: Q = low, $\overline{Q}$ = low
   Differential: Q = low, $\overline{Q}$ = high

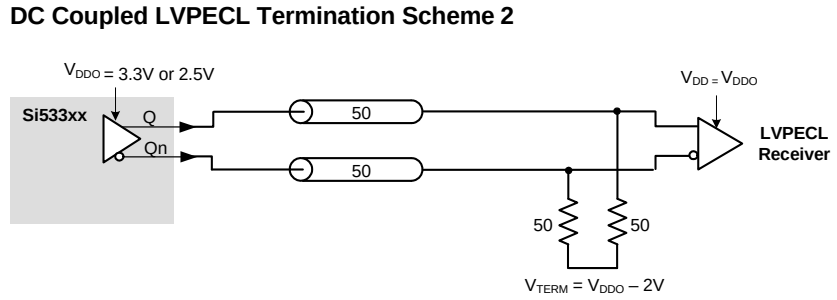
## 2.6. Power Supply ($V_{DD}$ and $V_{DDOX}$)

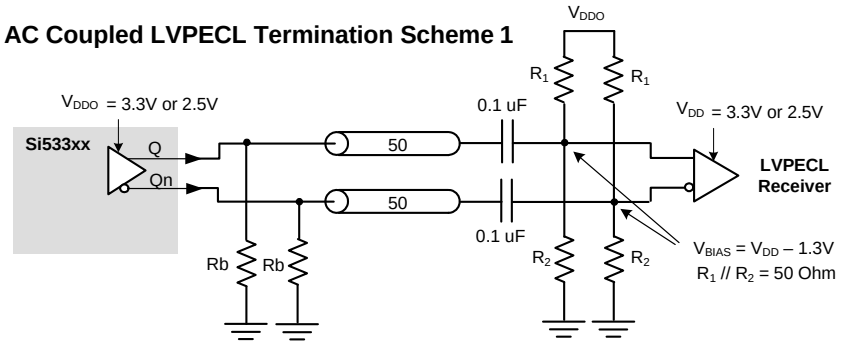
The device includes separate core ($V_{DD}$) and output driver supplies ($V_{DDOX}$). This feature allows the core to operate at a lower voltage than $V_{DDO}$, reducing current consumption in mixed supply applications. The core $V_{DD}$ supports 3.3 V, 2.5 V, or 1.8 V. The outputs have their own supply, $V_{DDO}$, supporting 3.3 V, 2.5 V, or 1.8 V.

## 2.7. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused outputs can be left floating. Do not short unused outputs to ground.



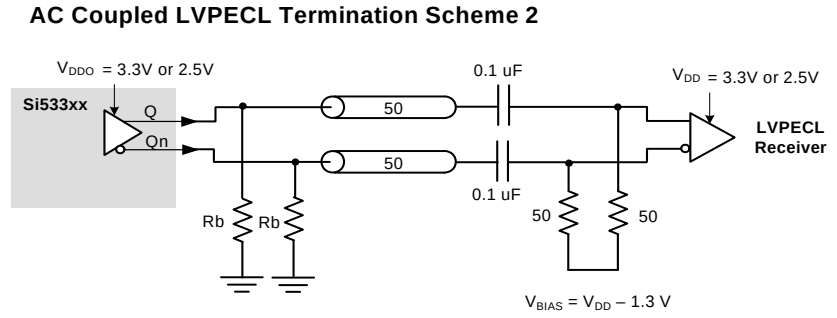
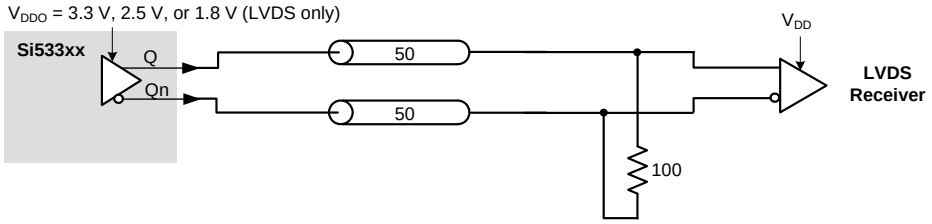
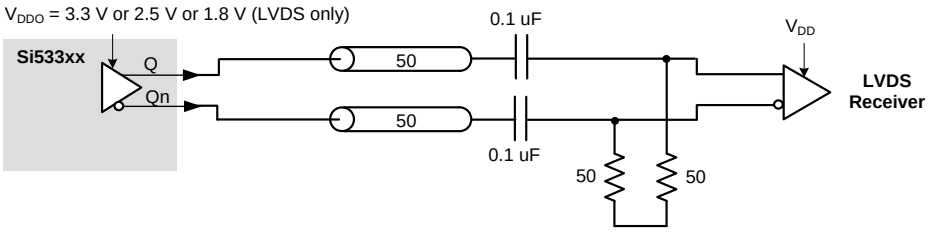




**Figure 6. LVPECL Output Termination**

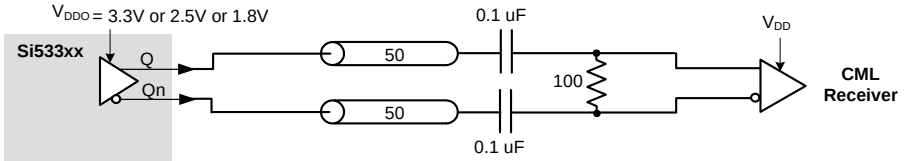
**DC Coupled LVDS and Low-Power LVPECL Termination**



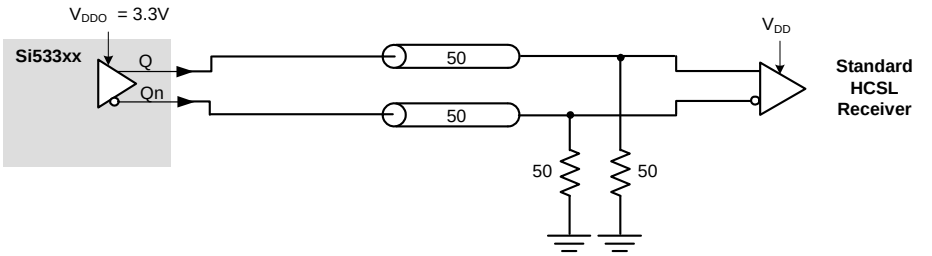

**AC Coupled LVDS and Low-Power LVPECL Termination**




**AC Coupled CML Termination**




**DC Coupled HCSL Receiver Termination**




**DC Coupled HCSL Source Termination**

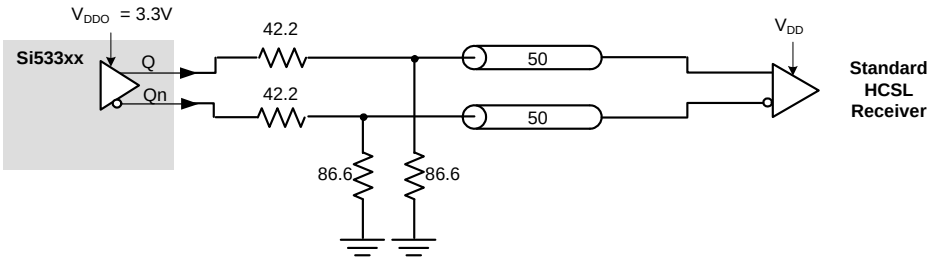



**Figure 7. LVDS, CML, HCSL, and Low-Power LVPECL Output Termination**

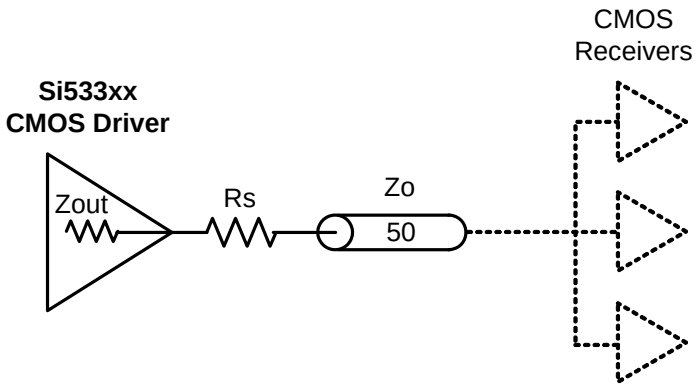



**Figure 8. LVCMOS Output Termination**

**Table 19. Recommended LVCMOS $R_S$ Series Termination**

| SFOUT1 | SFOUT0 | $R_S$ (Ω) | |
|---|---|---|---|
| | | 3.3 V | 2.5 V |
| 0 | 1 | 33 | 33 |
| 1 | 0 | 33 | 33 |
| 1 | 1 | 33 | 33 |
| Open | 0 | 0 | 0 |

## 2.8. AC Timing Waveforms

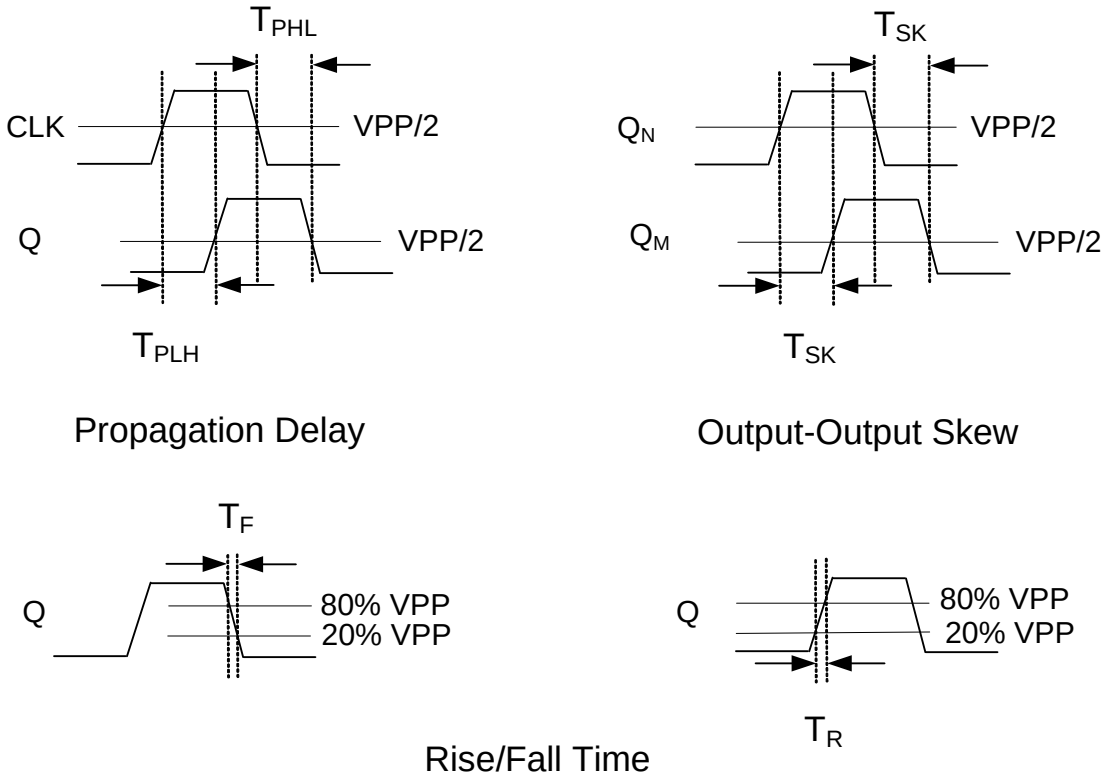



**Figure 9. AC Waveforms**

## 2.9. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

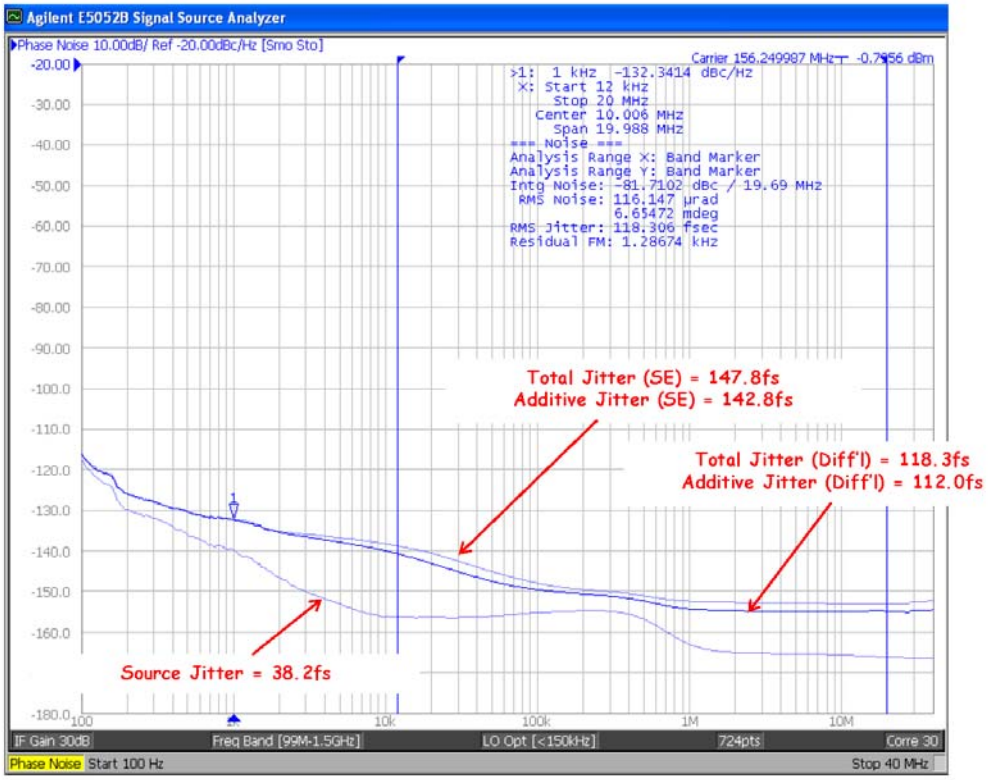
**Source Jitter**: Reference clock phase noise.

**Total Jitter (SE)**: Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

**Total Jitter (Diff'l)**: Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 10.

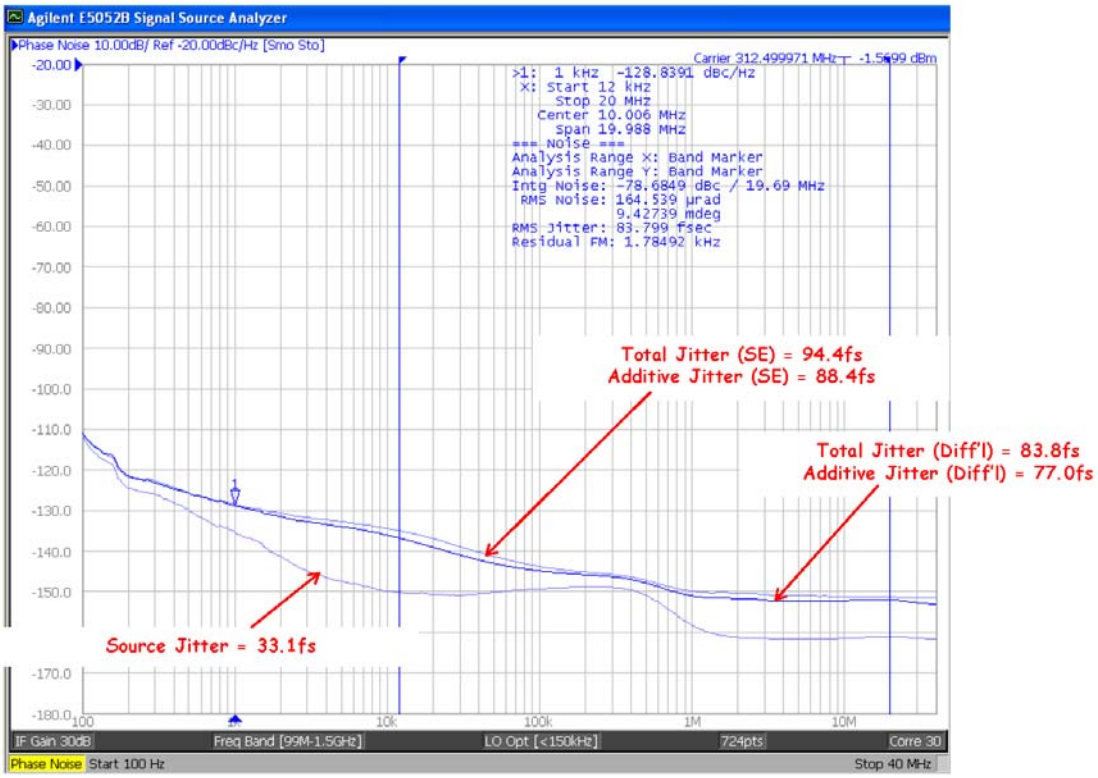
**Note:** To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



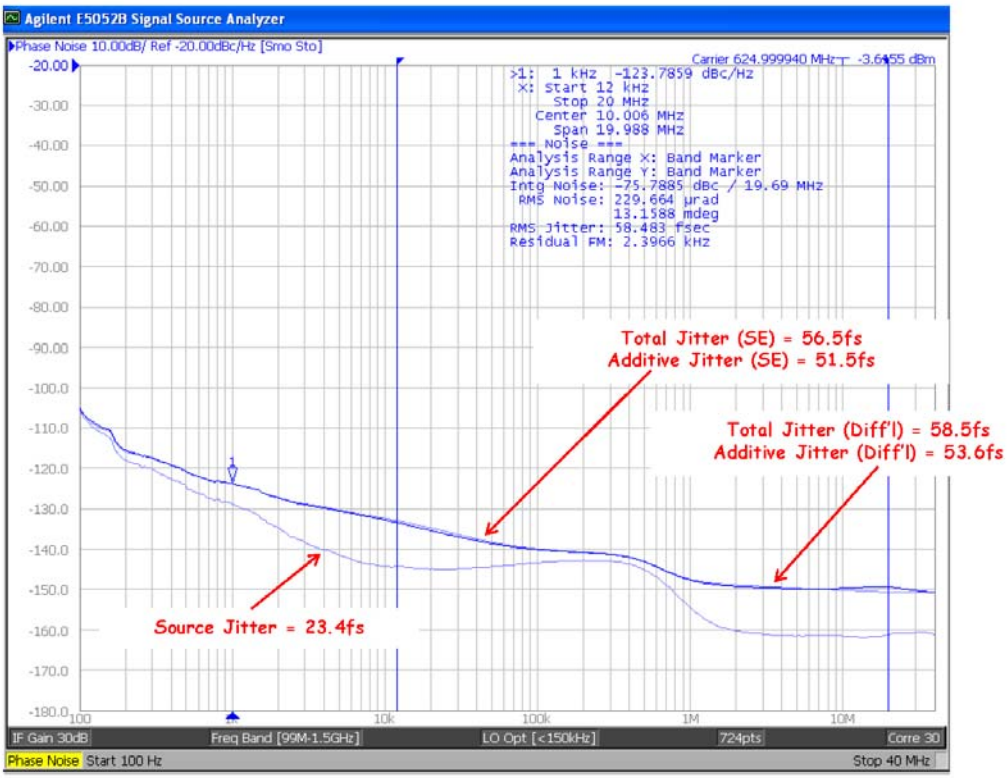

| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff'l) (fs) | Additive Jitter (Diff'l) (fs) |
|---|---|---|---|---|---|---|
| 156.25 | 1.0 | 38.2 | 147.8 | 142.8 | 118.3 | 112.0 |

**Figure 10. Source, Additive, and Total Jitter (156.25 MHz)**




| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff'l) (fs) | Additive Jitter (Diff'l) (fs) |
|---|---|---|---|---|---|---|
| 312.5 | 1.0 | 33.10 | 94.39 | 88.39 | 83.80 | 76.99 |

**Figure 11. Source, Additive, and Total Jitter (312.5 MHz)**




| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff'l) (fs) | Additive Jitter (Diff'l) (fs) |
|---|---|---|---|---|---|---|
| 625 | 1.0 | 23.4 | 56.5 | 51.5 | 58.5 | 53.6 |

**Figure 12. Source, Additive, and Total Jitter (625 MHz)**

## 2.10. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

## 3. Pin Description: 16-Pin QFN

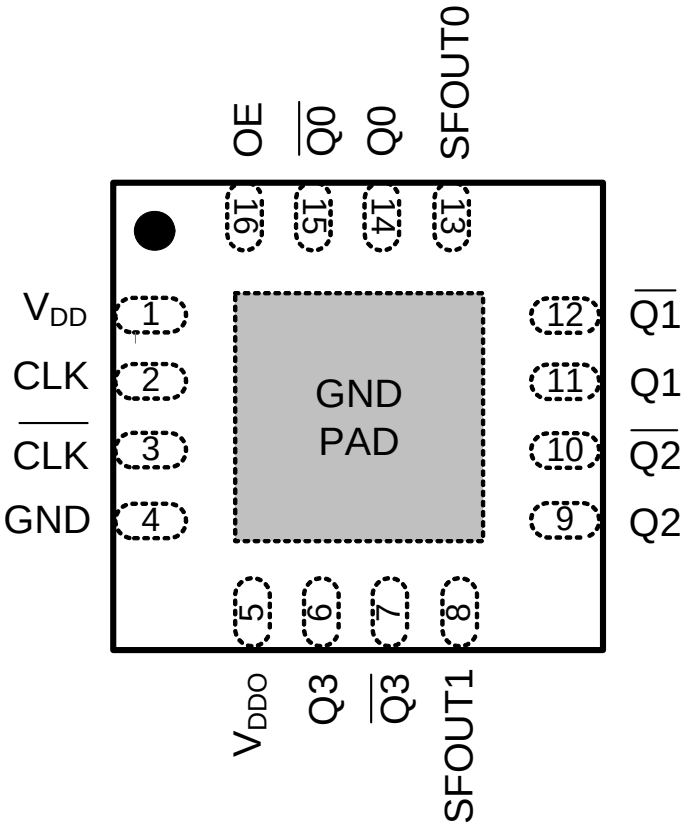



**Table 20. Pin Description**

| Pin | Name | Description |
|---|---|---|
| 1 | VDD | Core voltage supply.<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DD}$ pin as possible. |
| 2 | CLK | Input clock. |
| 3 | $\overline{CLK}$ | Input clock (complement).<br>When the CLK is driven by a single-ended input, connect /CLK to VDD/2.<br>See Figure 1, “Differential Measurement Method Using a Balun,” on page 10. |
| 4 | GND | Ground. |
| 5 | VDDO | Output voltage supply— All outputs (Q0 to Q3).<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DDO}$ pin as possible. |
| 6 | Q3 | Output clock 3. |
| 7 | $\overline{Q3}$ | Output clock 3 (complement). |
| 8 | SFOUT1 | Output signal format control pin 1.<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |

**Table 20. Pin Description (Continued)**

| Pin | Name | Description |
|---|---|---|
| 9 | Q2 | Output clock 2. |
| 10 | $\overline{Q2}$ | Output clock 2 (complement). |
| 11 | Q1 | Output clock 1. |
| 12 | $\overline{Q1}$ | Output clock 1 (complement). |
| 13 | SFOUT0 | Output signal format control pin 0.<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 14 | Q0 | Output clock 0. |
| 15 | $\overline{Q0}$ | Output clock 0 (complement). |
| 16 | OE | Output enable.<br>When OE = high, all outputs are enabled.<br>When OE = low, Q is held low, and $\overline{Q}$ is held high for differential formats.<br>For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low.<br>OE contains an internal pull-up resistor. |
| GND Pad | GND | Ground. |

## 4. Ordering Guide

| Part Number | Package | Pb-Free, ROHS-6 | Temperature |
|---|---|---|---|
| Si53306-B-GM | 16-QFN | Yes | –40 to 85 °C |
| Si53301/4-EVB | NA | Yes | –40 to 85 °C |

## 5. Package Outline

Figure 13 shows the package dimensions for the 3x3 mm 16-pin QFN package. Table 21 lists the values for the dimensions shown in the illustration.

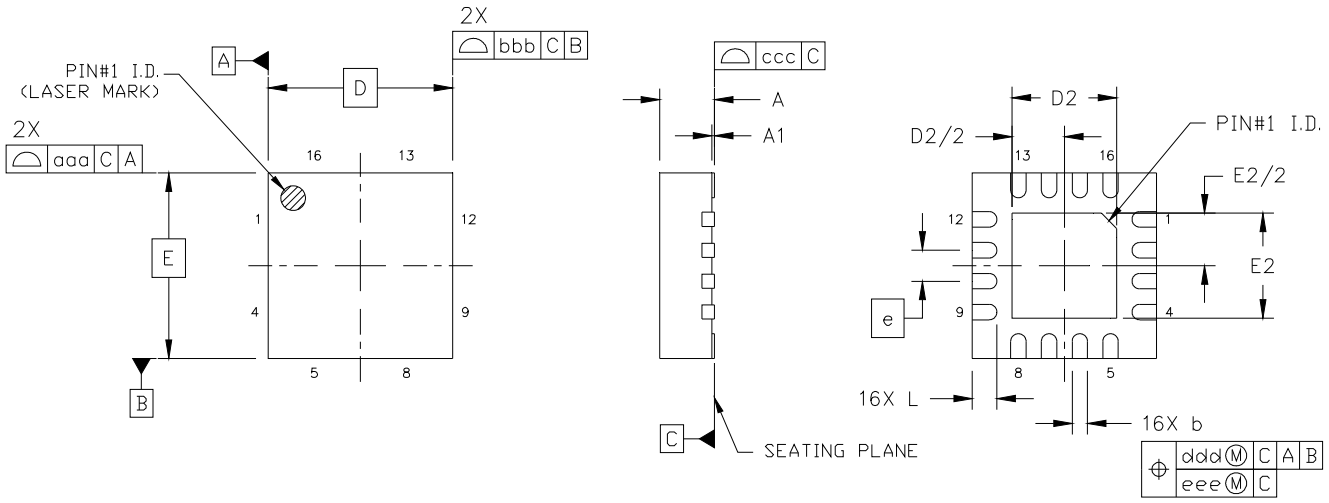



**Figure 13. Si53306 3x3 mm 16-QFN Package Diagram**

**Table 21. Package Diagram Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | | 3.00 BSC. | |
| D2 | 1.65 | 1.70 | 1.75 |
| e | | 0.50 BSC. | |
| E | | 3.00 BSC. | |
| E2 | 1.65 | 1.70 | 1.75 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.05 |

**Notes:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 6. PCB Land Pattern

Figure 14 shows the PCB land pattern dimensions for the 3x3 mm 16-pin QFN package. Table 22 lists the values for the dimensions shown in the illustration.

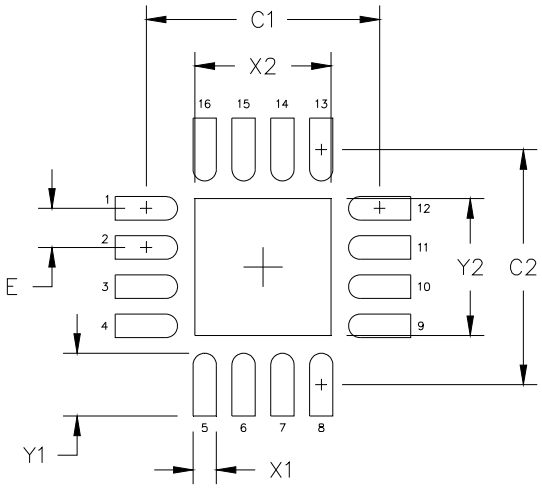



**Figure 14. Si53306 3x3 mm 16-QFN Package Land Pattern**

**Table 22. PCB Land Pattern Dimensions**

| Dimension | mm |
|---|---|
| C1 | 3.00 |
| C2 | 3.00 |
| E | 0.50 |
| X1 | 0.30 |
| Y1 | 0.80 |
| X2 | 1.75 |
| Y2 | 1.75 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

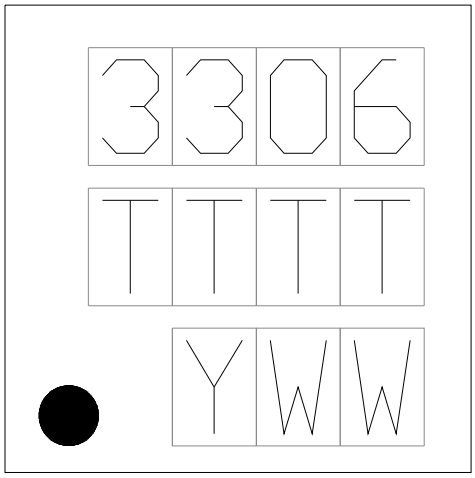
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2x2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

**Card Assembly**

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 7. Top Marking

## 7.1. Si53306 Top Marking




## 7.2. Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font Size:** | 0.635 mm (25 mils)<br>Right-Justified | |
| **Line 1 Marking:** | Product ID | **3306** |
| **Line 2 Marking:** | TTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| **Line 3 Marking** | Circle = 0.5 mm Diameter (Bottom-Left Justified) | Pin 1 Identifier |
| | YWW = Date Code | Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date. |

## NOTES:

## CONTACT INFORMATION

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