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Kind regards,

Team Nexperia

# PBLS4005Y; PBLS4005V

40 V PNP BISS loadswitch

Rev. 03 — 16 February 2009

Product data sheet

## 1. Product profile

### 1.1 General description

PNP low  $V_{CEsat}$  Breakthrough In Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in one package.

Table 1. Product overview

| Type number | Package |       |
|-------------|---------|-------|
|             | NXP     | JEITA |
| PBLS4005Y   | SOT363  | SC-88 |
| PBLS4005V   | SOT666  | -     |

### 1.2 Features

- Low  $V_{CEsat}$  (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

### 1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

### 1.4 Quick reference data

Table 2. Quick reference data

| Symbol  | Parameter                               | Conditions                         | Min                   | Typ | Max  | Unit       |
|---|---|------------------------------------|-----------------------|-----|------|------------|
| <b>TR1; PNP low <math>V_{CEsat}</math> transistor</b> |   |                                    |                       |     |      |            |
| $V_{CEO}$   | collector-emitter voltage               | open base                          | -                     | -   | -40  | V          |
| $I_C$   | collector current                       |                                    | -                     | -   | -500 | mA         |
| $R_{CEsat}$   | collector-emitter saturation resistance | $I_C = -500$ mA;<br>$I_B = -50$ mA | <a href="#">[1]</a> - | 440 | 700  | m $\Omega$ |
| <b>TR2; NPN resistor-equipped transistor</b>          |   |                                    |                       |     |      |            |
| $V_{CEO}$   | collector-emitter voltage               | open base                          | -                     | -   | 50   | V          |

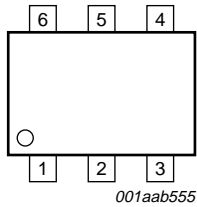
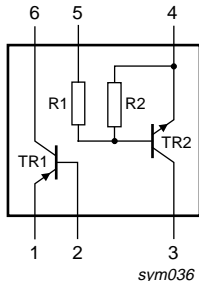
**Table 2. Quick reference data ...continued**

| Symbol | Parameter               | Conditions | Min | Typ | Max | Unit       |
|--------|-------------------------|------------|-----|-----|-----|------------|
| $I_O$  | output current          |            | -   | -   | 100 | mA         |
| R1     | bias resistor 1 (input) |            | 33  | 47  | 61  | k $\Omega$ |
| R2/R1  | bias resistor ratio     |            | 0.8 | 1   | 1.2 |            |

[1] Pulse test:  $t_p \leq 300 \mu\text{s}$ ;  $\delta \leq 0.02$ .

## 2. Pinning information

**Table 3. Pinning**

| Pin | Description            | Simplified outline   | Graphic symbol   |
|-----|------------------------|--|--|
| 1   | emitter TR1            |  |  |
| 2   | base TR1               |  |  |
| 3   | output (collector) TR2 |  |  |
| 4   | GND (emitter) TR2      |  |  |
| 5   | input (base) TR2       |  |  |
| 6   | collector TR1          |  |  |

## 3. Ordering information

**Table 4. Ordering information**

| Type number | Package |  | Version |
|-------------|---------|--|---------|
|             | Name    | Description                              |         |
| PBLS4005Y   | SC-88   | plastic surface-mounted package; 6 leads | SOT363  |
| PBLS4005V   | -       | plastic surface-mounted package; 6 leads | SOT666  |

## 4. Marking

**Table 5. Marking codes**

| Type number | Marking code <sup>[1]</sup> |
|-------------|-----------------------------|
| PBLS4005Y   | S5*                         |
| PBLS4005V   | K5                          |

[1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

## 5. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol  | Parameter                 | Conditions                    | Min | Max  | Unit |
|---|---------------------------|-------------------------------|-----|------|------|
| <b>TR1; PNP low <math>V_{CEsat}</math> transistor</b> |                           |                               |     |      |      |
| $V_{CBO}$   | collector-base voltage    | open emitter                  | -   | -40  | V    |
| $V_{CEO}$   | collector-emitter voltage | open base                     | -   | -40  | V    |
| $V_{EBO}$   | emitter-base voltage      | open collector                | -   | -6   | V    |
| $I_C$   | collector current         |                               | -   | -500 | mA   |
| $I_{CM}$  | peak collector current    | single pulse; $t_p \leq 1$ ms | -   | -1   | A    |
| $I_B$   | base current              |                               | -   | -50  | mA   |
| $I_{BM}$  | peak base current         | single pulse; $t_p \leq 1$ ms | -   | -100 | mA   |
| $P_{tot}$   | total power dissipation   | $T_{amb} \leq 25$ °C          | [1] | 200  | mW   |
| <b>TR2; NPN resistor-equipped transistor</b>          |                           |                               |     |      |      |
| $V_{CBO}$   | collector-base voltage    | open emitter                  | -   | 50   | V    |
| $V_{CEO}$   | collector-emitter voltage | open base                     | -   | 50   | V    |
| $V_{EBO}$   | emitter-base voltage      | open collector                | -   | 10   | V    |
| $V_I$   | input voltage             |                               |     |      |      |
|   | positive                  |                               | -   | +40  | V    |
|   | negative                  |                               | -   | -10  | V    |
| $I_O$   | output current            |                               | -   | 100  | mA   |
| $I_{CM}$  | peak collector current    | single pulse; $t_p \leq 1$ ms | -   | 100  | mA   |
| $P_{tot}$   | total power dissipation   | $T_{amb} \leq 25$ °C          | [1] | 200  | mW   |
| <b>Per device</b>                                     |                           |                               |     |      |      |
| $P_{tot}$   | total power dissipation   | $T_{amb} \leq 25$ °C          | -   | 300  | mW   |
| $T_j$   | junction temperature      |                               | -   | 150  | °C   |
| $T_{amb}$   | ambient temperature       |                               | -65 | +150 | °C   |
| $T_{stg}$   | storage temperature       |                               | -65 | +150 | °C   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

## 6. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol            | Parameter                                   | Conditions  | Min    | Typ | Max | Unit |
|-------------------|---|-------------|--------|-----|-----|------|
| <b>Per device</b> |   |             |        |     |     |      |
| $R_{th(j-a)}$     | thermal resistance from junction to ambient | in free air |        |     |     |      |
|                   | SOT363                                      |             | [1]    | -   | 416 | K/W  |
|                   | SOT666                                      |             | [1][2] | -   | 416 | K/W  |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

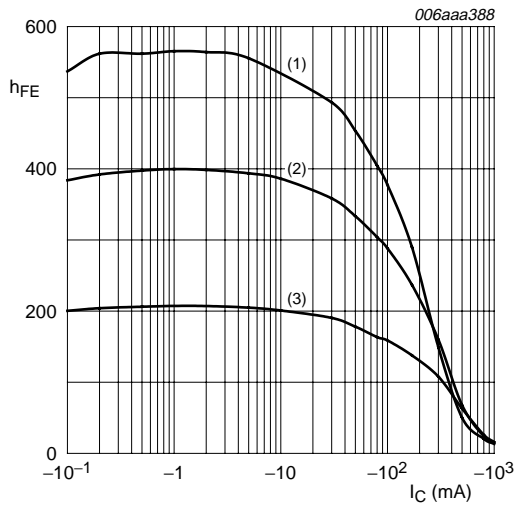
**7. Characteristics**

**Table 8. Characteristics**

*T<sub>amb</sub> = 25 °C unless otherwise specified.*

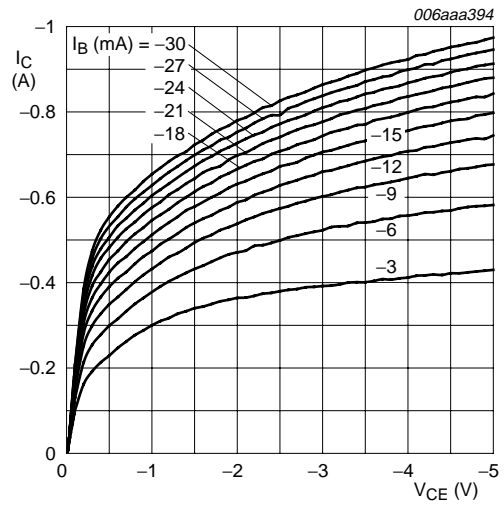
| Symbol   | Parameter                               | Conditions   | Min | Typ | Max  | Unit |    |
|--|---|--|-----|-----|------|------|----|
| <b>TR1; PNP low V<sub>CEsat</sub> transistor</b> |   |  |     |     |      |      |    |
| I <sub>CBO</sub>                                 | collector-base cut-off current          | V <sub>CB</sub> = -40 V; I <sub>E</sub> = 0 A                                | -   | -   | -100 | nA   |    |
|  |   | V <sub>CB</sub> = -40 V; I <sub>E</sub> = 0 A;<br>T <sub>j</sub> = 150 °C    | -   | -   | -50  | μA   |    |
| I <sub>EBO</sub>                                 | emitter-base cut-off current            | V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A                                 | -   | -   | -100 | nA   |    |
| h <sub>FE</sub>                                  | DC current gain                         | V <sub>CE</sub> = -2 V; I <sub>C</sub> = -10 mA                              | 200 | -   | -    |      |    |
|  |   | V <sub>CE</sub> = -2 V; I <sub>C</sub> = -100 mA                             | [1] | 150 | -    | -    |    |
|  |   | V <sub>CE</sub> = -2 V; I <sub>C</sub> = -500 mA                             | [1] | 40  | -    | -    |    |
| V <sub>CEsat</sub>                               | collector-emitter saturation voltage    | I <sub>C</sub> = -10 mA; I <sub>B</sub> = -0.5 mA                            | -   | -   | -50  | mV   |    |
|  |   | I <sub>C</sub> = -100 mA; I <sub>B</sub> = -5 mA                             | -   | -   | -130 | mV   |    |
|  |   | I <sub>C</sub> = -200 mA; I <sub>B</sub> = -10 mA                            | -   | -   | -200 | mV   |    |
|  |   | I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA                            | [1] | -   | -    | -350 | mV |
| R <sub>CEsat</sub>                               | collector-emitter saturation resistance | I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA                            | [1] | -   | 440  | 700  | mΩ |
| V <sub>BEsat</sub>                               | base-emitter saturation voltage         | I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA                            | [1] | -   | -    | -1.2 | V  |
| V <sub>BEon</sub>                                | base-emitter turn-on voltage            | V <sub>CE</sub> = -2 V; I <sub>C</sub> = -100 mA                             | [1] | -   | -    | -1.1 | V  |
| f <sub>T</sub>                                   | transition frequency                    | I <sub>C</sub> = -100 mA; V <sub>CE</sub> = -5 V;<br>f = 100 MHz             | 100 | 300 | -    | MHz  |    |
| C <sub>c</sub>                                   | collector capacitance                   | V <sub>CB</sub> = -10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A;<br>f = 1 MHz | -   | -   | 10   | pF   |    |
| <b>TR2; NPN resistor-equipped transistor</b>     |   |  |     |     |      |      |    |
| I <sub>CBO</sub>                                 | collector-base cut-off current          | V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A                                 | -   | -   | 100  | nA   |    |
| I <sub>CEO</sub>                                 | collector-emitter cut-off current       | V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A                                 | -   | -   | 1    | μA   |    |
|  |   | V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A;<br>T <sub>j</sub> = 150 °C     | -   | -   | 50   | μA   |    |
| I <sub>EBO</sub>                                 | emitter-base cut-off current            | V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A                                  | -   | -   | 90   | μA   |    |
| h <sub>FE</sub>                                  | DC current gain                         | V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA                                 | 80  | -   | -    |      |    |
| V <sub>CEsat</sub>                               | collector-emitter saturation voltage    | I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA                              | -   | -   | 150  | mV   |    |
| V <sub>I(off)</sub>                              | off-state input voltage                 | V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA                               | -   | 1.2 | 0.8  | V    |    |
| V <sub>I(on)</sub>                               | on-state input voltage                  | V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 5 mA                               | 3   | 1.6 | -    | V    |    |
| R1   | bias resistor 1 (input)                 |  | 33  | 47  | 61   | kΩ   |    |
| R2/R1  | bias resistor ratio                     |  | 0.8 | 1   | 1.2  |      |    |
| C <sub>c</sub>                                   | collector capacitance                   | V <sub>CB</sub> = 10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A;<br>f = 1 MHz  | -   | -   | 2.5  | pF   |    |

[1] Pulse test: t<sub>p</sub> ≤ 300 μs; δ ≤ 0.02.



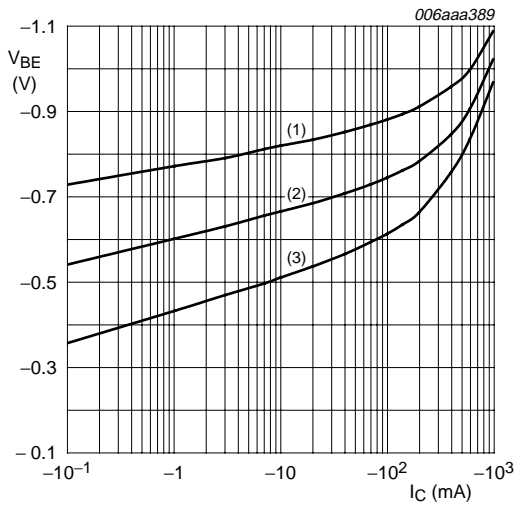
$V_{CE} = -2\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig 1. TR1 (PNP): DC current gain as a function of collector current; typical values**



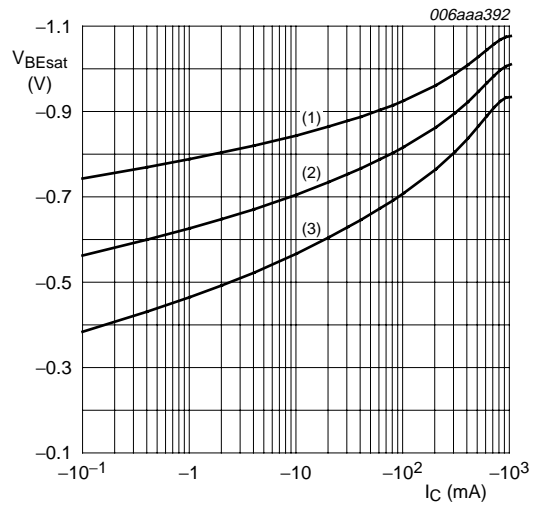
$T_{amb} = 25\text{ °C}$

**Fig 2. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values**



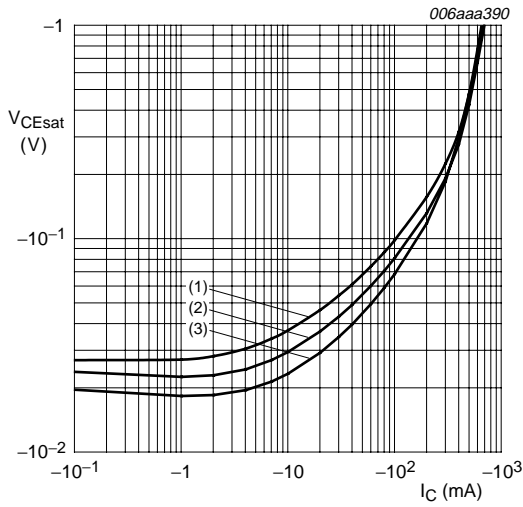
$V_{CE} = -2\text{ V}$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig 3. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values**



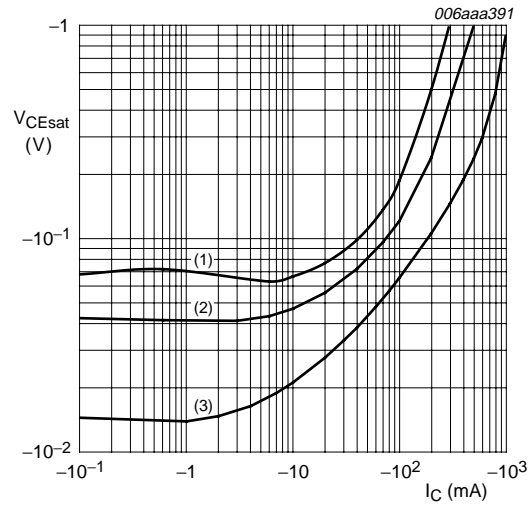
$I_C/I_B = 20$   
 (1)  $T_{amb} = -55\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig 4. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values**



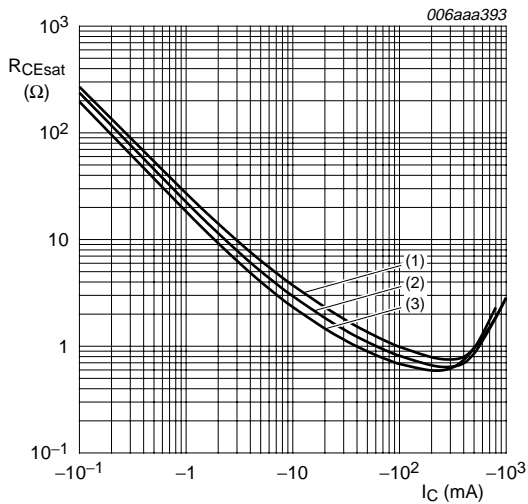
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig 5. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



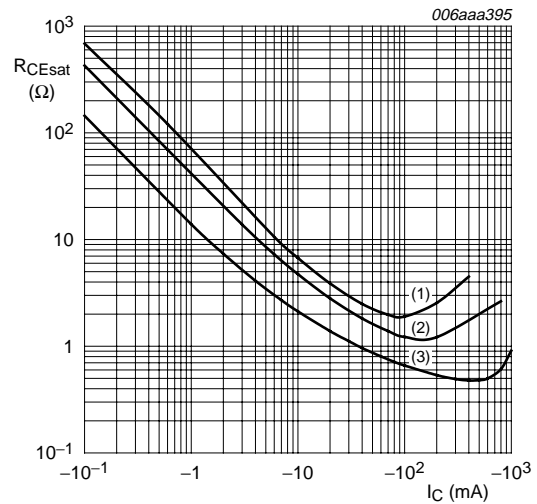
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



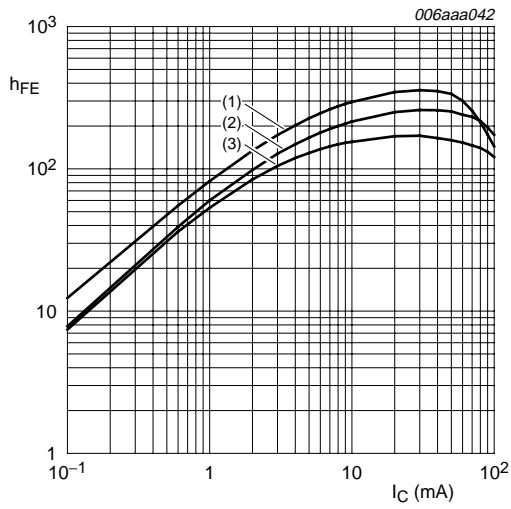
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -55\text{ °C}$

**Fig 7. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values**



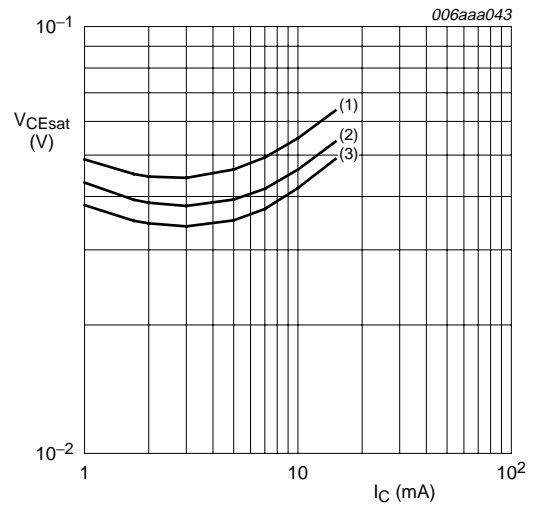
$T_{amb} = 25\text{ °C}$   
 (1)  $I_C/I_B = 100$   
 (2)  $I_C/I_B = 50$   
 (3)  $I_C/I_B = 10$

**Fig 8. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values**



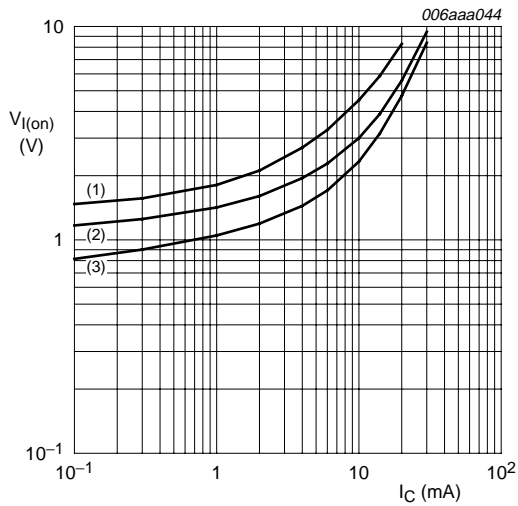
$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = 150 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

**Fig 9. TR2 (NPN): DC current gain as a function of collector current; typical values**



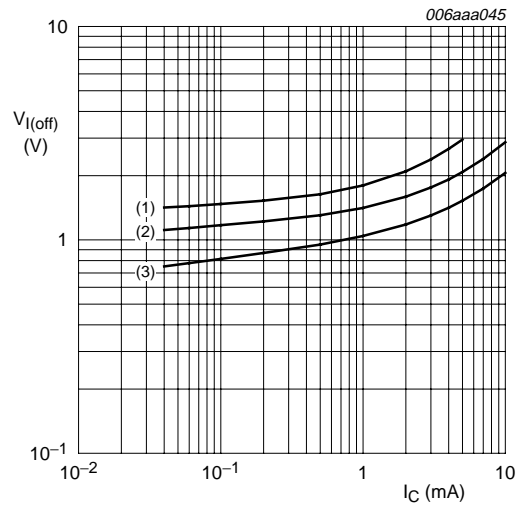
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

**Fig 10. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = 0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 11. TR2 (NPN): On-state input voltage as a function of collector current; typical values**

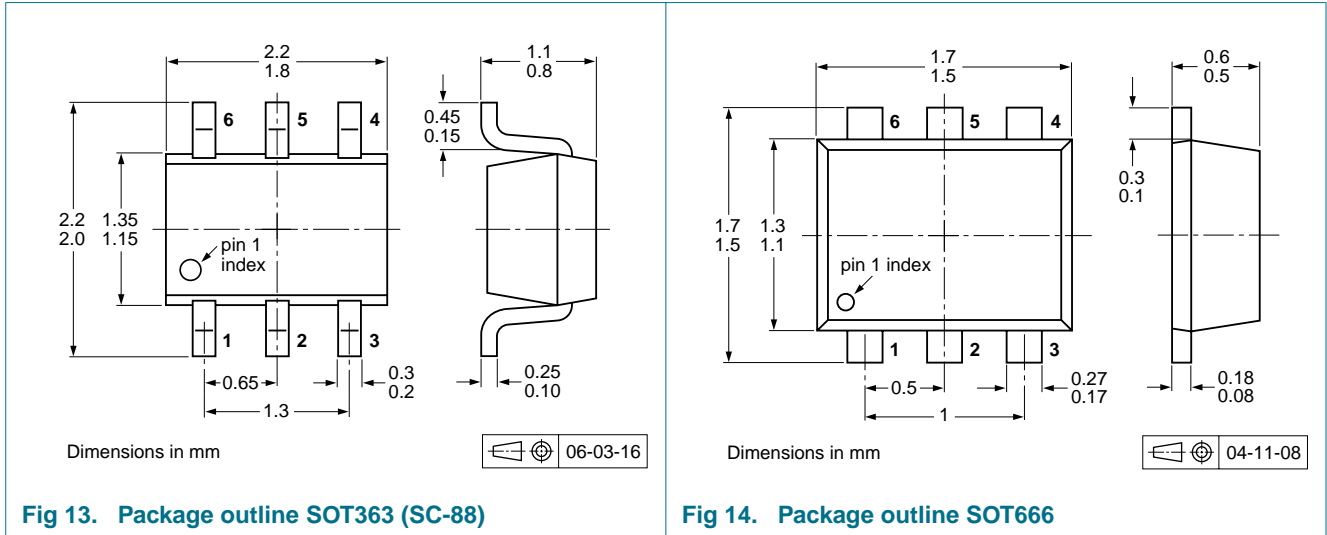


$V_{CE} = 5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 12. TR2 (NPN): Off-state input voltage as a function of collector current; typical values**



## 8. Package outline



## 9. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

| Type number | Package | Description                        | Packing quantity    |      |      |       |
|-------------|---------|------------------------------------|---------------------|------|------|-------|
|             |         |                                    | 3000                | 4000 | 8000 | 10000 |
| PBLS4005Y   | SOT363  | 4 mm pitch, 8 mm tape and reel; T1 | <sup>[2]</sup> -115 | -    | -    | -135  |
|             |         | 4 mm pitch, 8 mm tape and reel; T2 | <sup>[3]</sup> -125 | -    | -    | -165  |
| PBLS4005V   | SOT666  | 2 mm pitch, 8 mm tape and reel     | -                   | -    | -315 | -     |
|             |         | 4 mm pitch, 8 mm tape and reel     | -                   | -115 | -    | -     |

[1] For further information and the availability of packing methods, see [Section 12](#).

[2] T1: normal taping

[3] T2: reverse taping

## 10. Revision history

**Table 10. Revision history**

| Document ID           | Release date | Data sheet status  | Change notice | Supersedes            |
|-----------------------|--------------|--|---------------|-----------------------|
| PBLS4005Y_PBLS4005V_3 | 20090216     | Product data sheet   | -             | PBLS4005Y_PBLS4005V_2 |
| Modifications:        |              | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Figure 5</a>: y-axis value unit amended</li> <li><a href="#">Figure 6</a>: y-axis value unit amended</li> <li><a href="#">Section 11 "Legal information"</a>: updated</li> </ul> |               |                       |
| PBLS4005Y_PBLS4005V_2 | 20050713     | Product data sheet   | -             | PBLS4005Y_PBLS4005V_1 |
| PBLS4005Y_PBLS4005V_1 | 20041206     | Product data sheet   | -             | -                     |

## 11. Legal information

### 11.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 11.2 Definitions

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## 12. Contact information

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