Unit: mm

TOSHIBA Diodes for Protecting against ESD

## DF5A6.8LFU

# Product for Use Only as Protection against Electrostatic Discharge (ESD)

- \* This product is for protection against electrostatic discharge (ESD) only and is not intended for any other usage, including without limitation, the constant voltage diode application.
- The mounting of four devices on an ultra-compact package allows the number of parts and the mounting cost to be reduced.
- Low Terminal capacitance (between Cathode and Anode)
   : C<sub>T</sub> = 6.0 pF (typ.)

#### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics	Symbol	Rating	Unit
Power dissipation	Р	200	mW
Junction temperature	Tj	125	°C
Storage temperature range	T <sub>stg</sub>	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the

Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

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#### Weight: 0.0062 g (typ.)

#### **Electrical Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Zener voltage	VZ	$I_Z = 5 \text{ mA}$	6.5	6.8	7.1	V
Dynamic impedance	Z <sub>Z</sub>	$I_Z = 5 \text{ mA}$	_	_	50	Ω
Knee dynamic impedance	Z <sub>ZK</sub>	$I_Z = 0.5 \text{ mA}$	_	_	100	Ω
Reverse current	I <sub>R</sub>	V <sub>R</sub> = 5 V	_	_	0.5	μΑ
Terminal capacitance (between Cathode and Anode)	C <sub>T</sub>	V <sub>R</sub> = 0 V, f = 1 MHz	_	6.0	_	pF

#### **Guaranteed Level of ESD Immunity**

Test Condition	ESD Immunity Level		
IEC61000-4-2 (Contact discharge)	± 8kV		

Criterion: No damage to device elements

Start of commercial production 1999-04

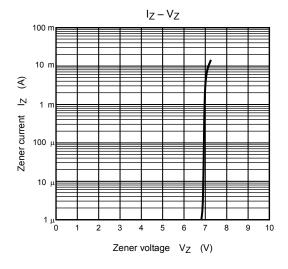
### Marking

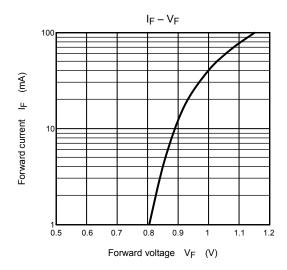
### **Equivalent Circuit (Top View)**

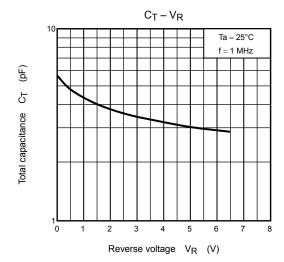




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2014-03-01