

PESD5V0S1BSF

Ultra low profile bidirectional low capacitance ESD protection diode

Rev. 2 — 18 February 2011

Product data sheet

1. Product profile

1.1 General description

Low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a SOD962 leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Bidirectional ESD protection of one line
- Low diode capacitance C_d = 35 pF
- ESD protection up to ±30 kV according IEC 61000-4-2
- Ultra small SMD package
- Symmetrical breakdown voltage

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

1.4 Quick reference data

Table 1. Quick reference data

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage		-5	-	5	V
C _d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}$	25	35	45	pF

^[1] This parameter is guaranteed by design.



2. Pinning information

Table 2. Pinning

	•		
Pin	Description	Simplified outline	Graphic symbol
1	cathode (diode 1)		
2	cathode (diode 2)	1 2	1 2 sym045
		Transparent top view	

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PESD5V0S1BSF	-	leadless ultra small package; 2 terminals; body $0.6 \times 0.3 \times 0.3$ mm	SOD962		

4. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0S1BSF	S

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{PP}	peak pulse power	$t_p = 8/20 \ \mu s$	[1][2]	100	W
I _{PP}	peak pulse current	$t_p = 8/20 \ \mu s$	[1][2]	8	Α
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	+150	°C
T_{stg}	storage temperature		-65	+150	°C

^[1] Non-repetitive current pulse 8/20 μ s exponentially decaying waveform according to IEC 61000-4-5; see Figure 1.

[2] Measured from pin 1 to pin 2.

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions		Min	Max	Unit
· LOD	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	-	30	kV
		IEC 61000-4-2 (air discharge)		-	30	kV
		MIL-STD-883 (human body model)		-	30	kV

^[1] Measured from pin 1 to pin 2.

Table 7. ESD standards compliance

Standard	Conditions
IEC 61000-4-2, level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

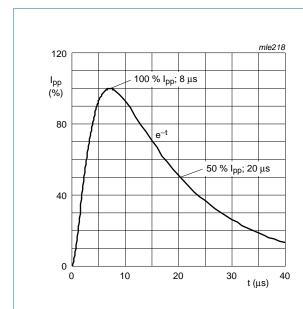


Fig 1. 8/20 μs pulse waveform according to IEC 61000-4-5

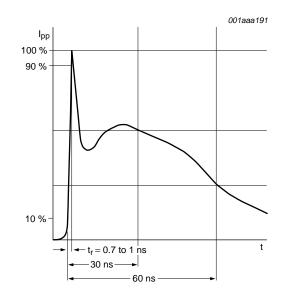


Fig 2. ESD pulse waveform according to IEC 61000-4-2

^[2] Device stressed with ten non-repetitive ESD pulses; see Figure 2.

6. Characteristics

Table 8. Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	1	Min	Тур	Max	Unit
Per diode							
V_{RWM}	reverse standoff voltage		-	- 5	-	5	V
I _{RM}	reverse leakage current	$V_{RWM} = 5 V$	•	-	1	100	nA
V_{CL}	clamping voltage	I _{PP} = 1 A	[1][2]	-	-	12	V
		I _{PP} = 8 A	[1][2]	-	-	15.5	V
V _{BR} breakdow	breakdown voltage	I _R = 1 mA	<u>[3]</u>	6	-	10	V
		$I_R = -1 \text{ mA}$	<u>[3]</u> .	-10	-	-6	V
C _d	diode capacitance	f = 1 MHz	<u>[4]</u>				
		$V_R = 0 V$		25	35	45	pF
		$V_{R} = 2.5 \text{ V}$	•	-	26.5	35	pF
		$V_R = 5 V$		-	23.7	31	pF
Ls	series inductance		<u>[5]</u> .	-	0.05	-	nΗ
R _{dyn}	dynamic resistance		<u>[6]</u> .	-	0.28	-	Ω

^[1] Non-repetitive current pulse 8/20 μ s exponentially decaying waveform according to IEC 61000-4-5; see Figure 1.

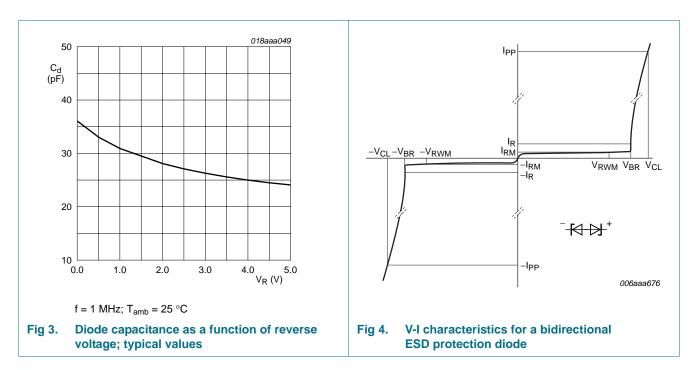
^[2] Measured from pin 1 to pin 2.

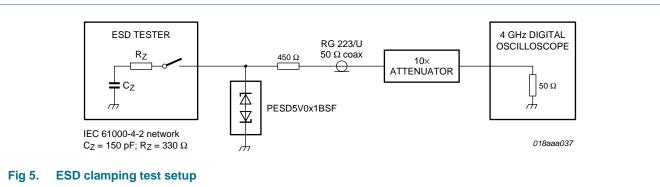
^[3] Breakdown voltage is always symmetrical within the characterized range, which means no difference in breakdown voltage from pin 1 to pin 2 and vice versa.

^[4] This parameter is guaranteed by design.

^[5] Calculated from S-parameter values.

^[6] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANS/IESD STM5.1-2008.





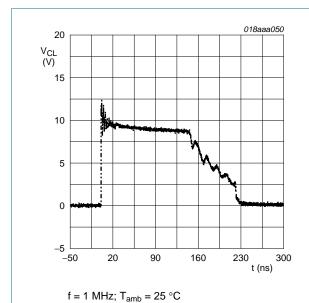


Fig 6. Clamped +1 kV ESD pulse waveform (IEC 61000-4-2 network)

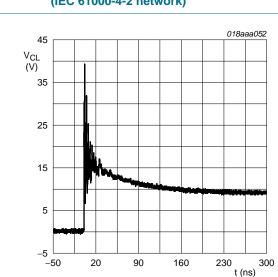


Fig 8. Clamped +8 kV ESD pulse waveform (IEC 61000-4-2 network)

 $f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^{\circ}\text{C}$

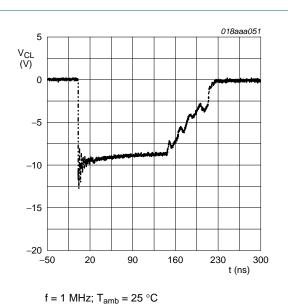


Fig 7. Clamped –1 kV ESD pulse waveform (IEC 61000-4-2 network)

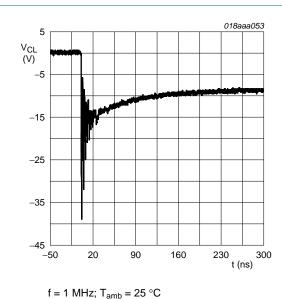
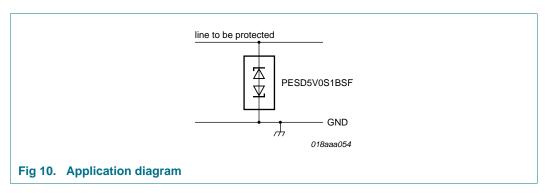


Fig 9. Clamped –8 kV ESD pulse waveform (IEC 61000-4-2 network)

7. Application information

The PESD5V0S1BSF is designed for the protection of one data or signal line from the damage caused by ESD and/or other surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground. It provides protection against surges with up to 100 W per line.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD and Electrical Fast Transient (EFT). The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible
- 2. The path length between the device and the protected line should be minimized
- 3. Avoid running protected conductors in parallel with unprotected conductors
- 4. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops
- 5. Minimize the length of the transient return path to ground
- 6. Avoid using shared transient return paths to a common ground point
- 7. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

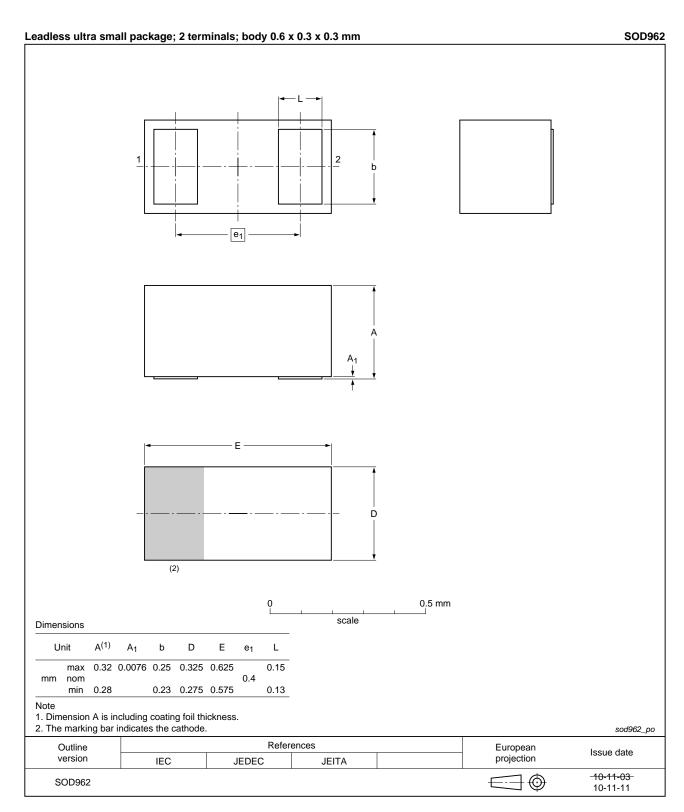


Fig 11. Package outline PESD5V0S1BSF (SOD962)

PESD5V0S1BSF

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9. Packing information

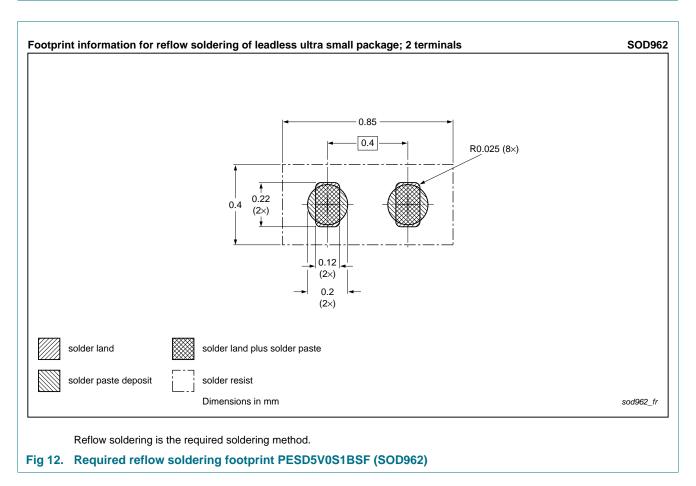
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity
			9000
PESD5V0S1BSF	SOD962	2 mm pitch, 8 mm tape and reel	-315

^[1] For further information and the availability of packing methods, see Section 13.

10. Soldering



Based on results of board mount testing, Nexperia requires the following soldering guidelines:

- 1. Soldering footprint as indicated in <u>Figure 12</u>: solder paste has to cover the whole solder land area.
- 2. Non-solder mask defined (copper-defined) solder lands.
- 3. Minimum stencil thickness of 100 μ m.
- 4. Paste type 4 or smaller sphere size.
- 5. Pick and placement accuracy of $\pm 50 \mu m$.

PESD5V0S1BSF

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0S1BSF v.2	20110218	Product data sheet	-	PESD5V0S1BSF v.1
Modifications:	odifications: Section 1.2 "Fe Table 1 and Tal Table 6 "ESD m Table 8: V _{BR} up Figure 12: title		es updated.	
PESD5V0S1BSF v.1	20101112	Preliminary data sheet	: -	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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PESD5V0S1BSF

Bidirectional low capacitance ESD protection diode

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