2.5 V/3.3 V, 2-Bit Common Control Level Translator Bus Switch

ADG3242

FEATURES

225 ps propagation delay through the switch
4.5 Ω switch connection between ports
Data rate 1.5 Gbps
2.5 V/3.3 V supply operation
Selectable level shifting/translation
Level translation
  3.3 V to 2.5 V
  3.3 V to 1.8 V
  2.5 V to 1.8 V
Small signal bandwidth 710 MHz
8-lead SOT-23 package

APPLICATIONS

3.3 V to 2.5 V voltage translation
3.3 V to 1.8 V voltage translation
2.5 V to 1.8 V voltage translation
Bus switching
Bus isolation
Hot swap
Hot plug
Analog switch applications

FUNCTIONAL BLOCK DIAGRAM

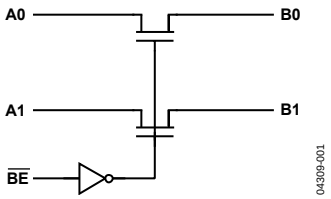

Figure 1.

GENERAL DESCRIPTION

The ADG3242 is a 2.5 V or 3.3 V, 2-bit, 2-port, common control digital switch. It is designed on a low voltage CMOS process, and provides low power dissipation, yet gives high switching speed and very low on resistance. This allows the inputs to be connected to the outputs without additional propagation delay or generating additional ground bounce noise.

These switches are enabled by means of a common bus enable ($\overline{BE}$) input signal. This digital switch allows a bidirectional signal to be switched when on. In the off condition, signal levels up to the supplies are blocked.

This device is ideal for applications requiring level translation. When operated from a 3.3 V supply, level translation from 3.3 V inputs to 2.5 V outputs is allowed. Similarly, if the device is operated from a 2.5 V supply and 2.5 V inputs are applied, the device translates the outputs to 1.8 V. In addition, a level translating select pin ($\overline{SEL}$) is included. When $\overline{SEL}$ is low, V_{CC} is reduced internally, allowing for level translation between 3.3 V inputs and 1.8 V outputs. This makes the device suitable for applications requiring level translation between different supplies, such as converter to DSP/microcontroller interfacing.

PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V supply operation.
2. Extremely low propagation delay through switch.
3. 4.5 Ω switches connect inputs to outputs.
4. Level/voltage translation.
5. Tiny SOT-23 package.

Rev. A
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TABLE OF CONTENTS

REVISION HISTORY

9/06—Rev. 0 to Rev. A

Updated Format ..... Universal
Added Table 4 5
Changes to the Ordering Guide 14

8/03—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.3 V to 3.6 V, GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	B Version[1] Min	Typ[2]	Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}	V_{CC} = 2.7 V to 3.6 V	2.0			V
		V_{CC} = 2.3 V to 2.7 V	1.7			V
Input Low Voltage	V_{INL}	V_{CC} = 2.7 V to 3.6 V			0.8	V
		V_{CC} = 2.3 V to 2.7 V			0.7	V
Input Leakage Current	I_I			±0.01	±1	µA
Off State Leakage Current	I_{OZ}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
On State Leakage Current		0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
Maximum Pass Voltage	V_P	$V_A/V_B = V_{CC} = \overline{SEL}$ = 3.3 V, I_O = −5 µA	2.0	2.5	2.9	V
		$V_A/V_B = V_{CC} = \overline{SEL}$ = 2.5 V, I_O = −5 µA	1.5	1.8	2.1	V
		$V_A/V_B = V_{CC}$ = 3.3 V, $\overline{SEL}$ = 0 V, I_O = −5 µA	1.5	1.8	2.1	V
CAPACITANCE[3]						
A Port Off Capacitance	C_A OFF	f = 1 MHz		3.5		pF
B Port Off Capacitance	C_B OFF	f = 1 MHz		3.5		pF
A, B Port On Capacitance	C_A, C_B ON	f = 1 MHz		7		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[3]						
Propagation Delay A to B or B to A, t_{PD}[4]	t_{PHL}, t_{PLH}	C_L = 50 pF, $V_{CC} = \overline{SEL}$ = 3 V			0.225	ns
Propagation Delay Matching[5]					5	ps
Bus Enable Time $\overline{BE}$ to A or B[6]	t_{PZH}, t_{PZL}	V_{CC} = 3.0 V to 3.6 V; $\overline{SEL} = V_{CC}$	1	3.2	4.6	ns
		V_{CC} = 3.0 V to 3.6 V; $\overline{SEL}$ = 0 V	1	3	4	ns
		V_{CC} = 2.3 V to 2.7 V; $\overline{SEL} = V_{CC}$	1	3	4	ns
Bus Disable Time $\overline{BE}$ to A or B[6]	t_{PHZ}, t_{PLZ}	V_{CC} = 3.0 V to 3.6 V; $\overline{SEL} = V_{CC}$	1	3	4	ns
		V_{CC} = 3.0 V to 3.6 V; $\overline{SEL}$ = 0 V	1	2.5	3.8	ns
		V_{CC} = 2.3 V to 2.7 V; $\overline{SEL} = V_{CC}$	1	2.5	3.4	ns
Maximum Data Rate		$V_{CC} = \overline{SEL}$ = 3.3 V; V_A/V_B = 2 V		1.5		Gbps
Channel Jitter		$V_{CC} = \overline{SEL}$ = 3.3 V; V_A/V_B = 2 V		45		ps p-p
DIGITAL SWITCH						
On Resistance	R_{ON}	V_{CC} = 3 V, $\overline{SEL} = V_{CC}$, V_A = 0 V, I_{BA} = 8 mA		4.5	8	Ω
		V_{CC} = 3 V, $\overline{SEL} = V_{CC}$, V_A = 1.7 V, I_{BA} = 8 mA		12	28	Ω
		V_{CC} = 2.3 V, $\overline{SEL} = V_{CC}$, V_A = 0 V, I_{BA} = 8 mA		5	9	Ω
		V_{CC} = 2.3 V, $\overline{SEL} = V_{CC}$, V_A = 1 V, I_{BA} = 8 mA		9	18	Ω
		V_{CC} = 3 V, $\overline{SEL}$ = 0 V, V_A = 0 V, I_{BA} = 8 mA		5	8	Ω
		V_{CC} = 3 V, $\overline{SEL}$ = 0 V, V_A = 1 V, I_{BA} = 8 mA		12		Ω
On Resistance Matching	ΔR_{ON}	V_{CC} = 3 V, $\overline{SEL} = V_{CC}$, V_A = 0 V, I_A = 8 mA		0.1	0.5	Ω
		V_{CC} = 3 V, $\overline{SEL}$ = 0 V, V_A = 0 V, I_A = 8 mA		0.1	0.5	Ω
POWER REQUIREMENTS						
V_{CC}			2.3		3.6	V
Quiescent Power Supply Current	I_{CC}	Digital inputs = 0 V or V_{CC}; $\overline{SEL} = V_{CC}$		0.01	1	µA
		Digital inputs = 0 V or V_{CC} ; $\overline{SEL}$ = 0 V		0.1	0.2	mA
Increase in I_{CC} per Input[7]	ΔI_{CC}	V_{CC} = 3.6 V, $\overline{BE}$ = 3.0 V; $\overline{SEL} = V_{CC}$		0.15	8	µA

[1] Temperature range is as follows: B version: −40°C to +85°C.
[2] Typical values are at 25°C, unless otherwise stated.
[3] Guaranteed by design, not subject to production test.
[4] The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Because the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
[5] Propagation delay matching between channels is calculated from the on resistance matching and load capacitance of 50 pF.
[6] See Timing Measurement Information section.
[7] This current applies to the Control Pin $\overline{BE}$ only. The A and B ports contribute no significant ac or dc currents as they transition.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC} to GND	−0.5 V to +4.6 V
Digital Inputs to GND	−0.5 V to +4.6 V
DC Input Voltage	−0.5 V to +4.6 V
DC Output Current	25 mA per channel
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

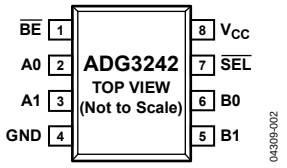


Figure 2. Pin Configuration

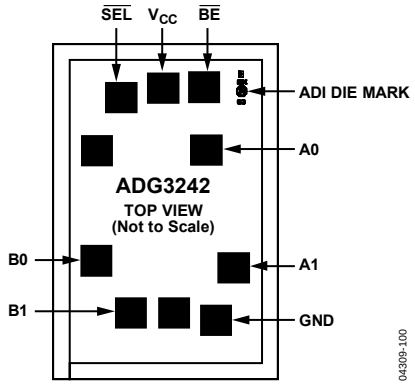


Figure 3. Die Pad Configuration (Die size: 550 µm × 820 µm)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{BE}$	Bus Enable (Active Low).
2	A0	Port A0, Input or Output.
3	A1	Port A1, Input or Output.
4	GND	Ground (0 V) Reference.
5	B1	Port B1, Input or Output.
6	B0	Port B0, Input or Output.
7	$\overline{SEL}$	Level Translation Select.
8	V_{CC}	Positive Power Supply Voltage.

Table 4. Die Pad Coordinates (Measured from the Center of the Die)

Mnemonic	X(µm)	Y(µm)
$\overline{BE}$	+93	+303
A0	+102	+150
A1	+168	−139
GND	+126	−266
B1	−88	−247
B0	−168	+121
$\overline{SEL}$	−111	+279
V_{CC}	−7	+303

Table 5. Truth Table

$\overline{BE}$	$\overline{SEL}$[1]	Function
L	L	A0 = B0, A1 = B1, 3.3 V to 1.8 V Level Shifting.
L	H	A0 = B0, A1 = B1, 3.3 V to 2.5 V/2.5 V to 1.8 V Level Shifting.
H	X	Disconnect.

[1] $\overline{SEL}$ = 0 V only when V_{DD} = 3.3 V ± 10%.

TYPICAL PERFORMANCE CHARACTERISTICS

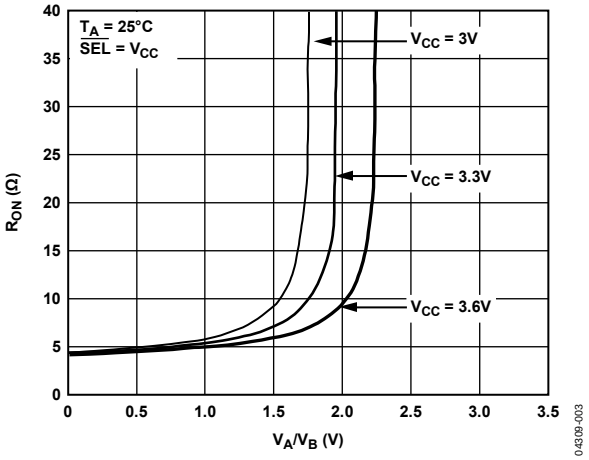


Figure 4. On Resistance vs. Input Voltage

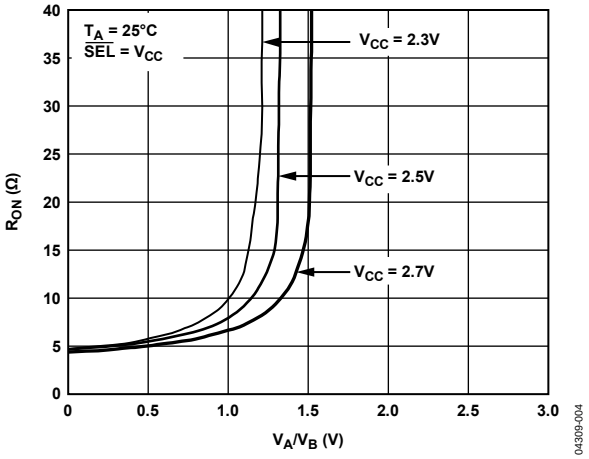


Figure 5. On Resistance vs. Input Voltage

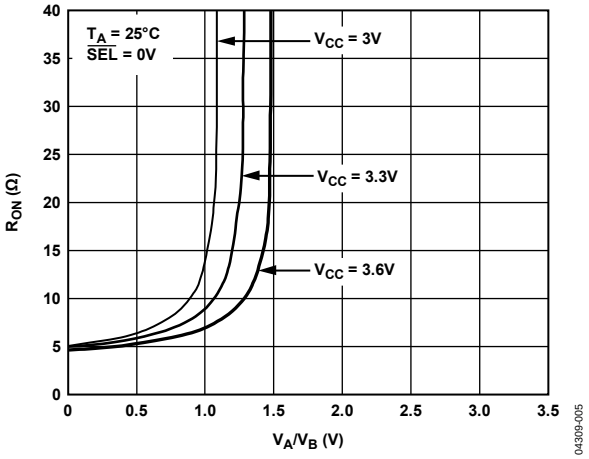


Figure 6. On Resistance vs. Input Voltage

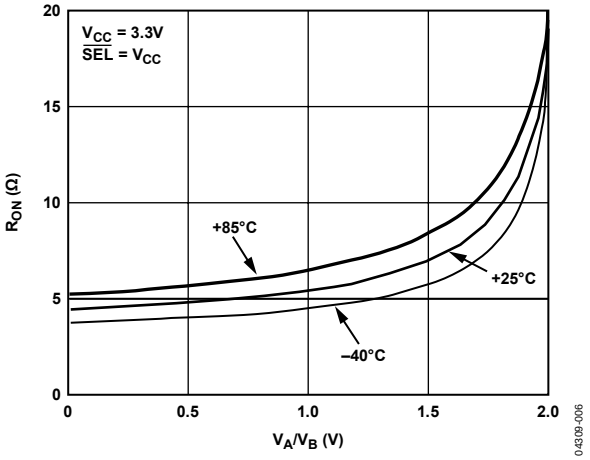


Figure 7. On Resistance vs. Input Voltage for Different Temperatures

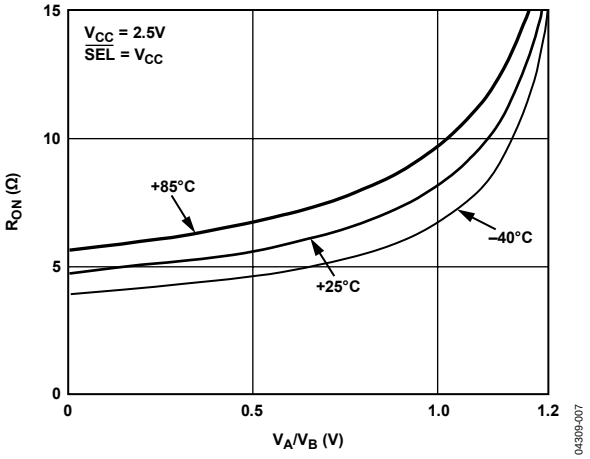


Figure 8. On Resistance vs. Input Voltage for Different Temperatures

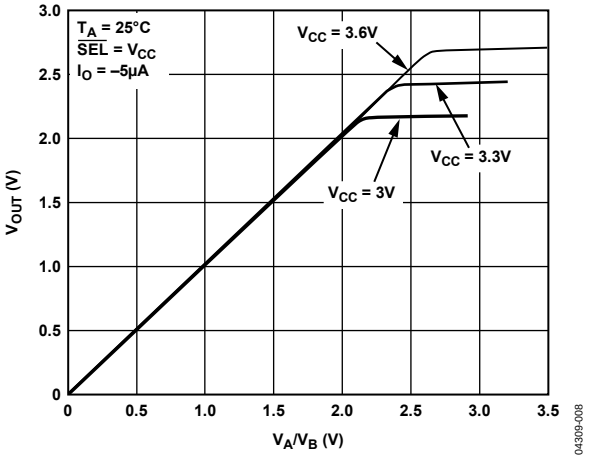


Figure 9. Pass Voltage vs. V_{CC}

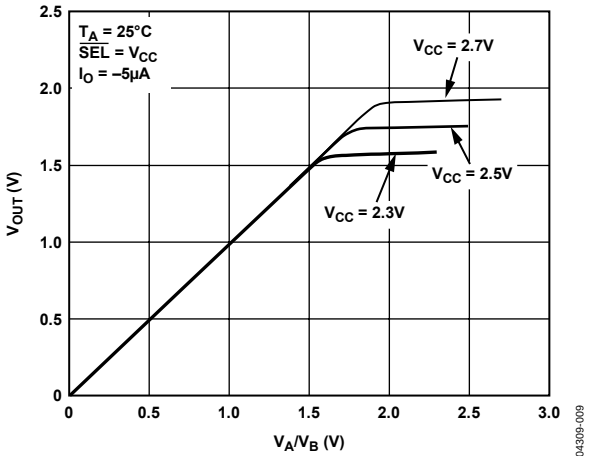


Figure 10. Pass Voltage vs. V_{CC}

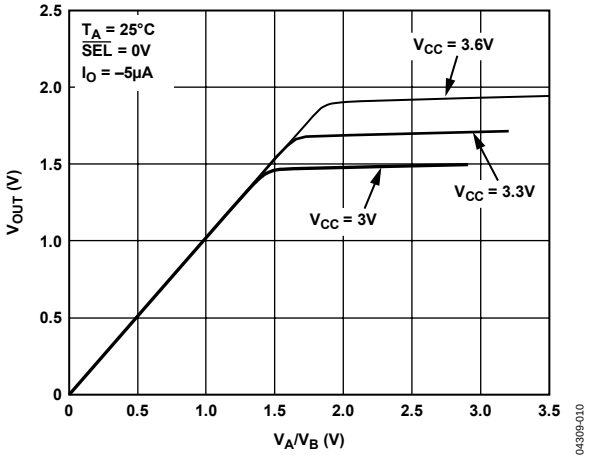


Figure 11. Pass Voltage vs. V_{CC}

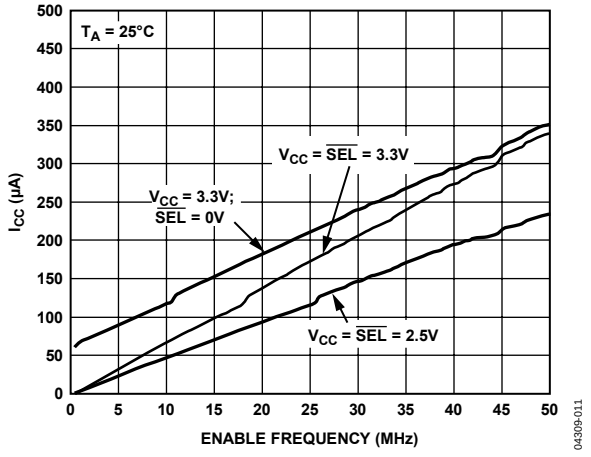


Figure 13. Output Low Characteristic

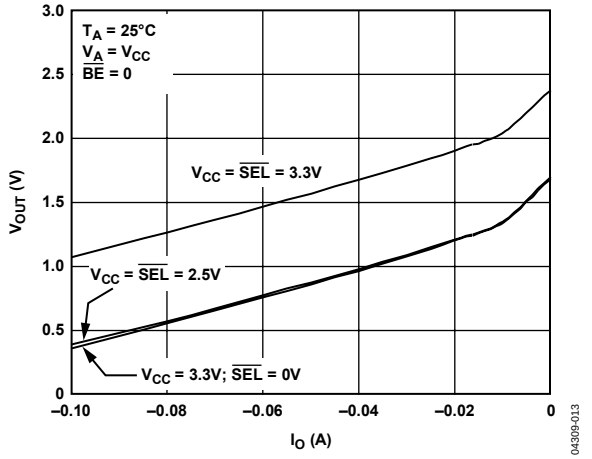


Figure 14. Output High Characteristic

Figure 12. I_{CC} vs. Enable Frequency

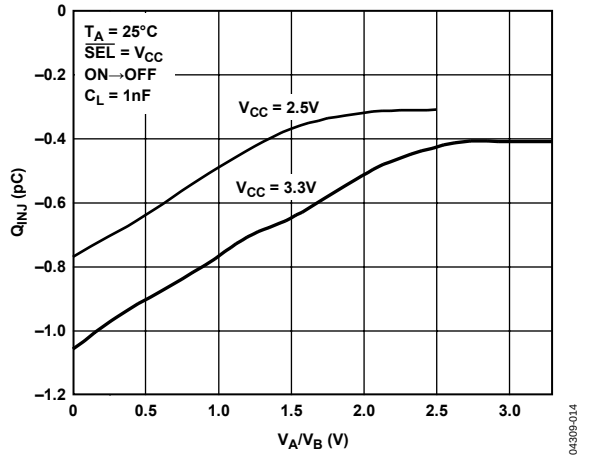


Figure 15. Charge Injection vs. Source Voltage

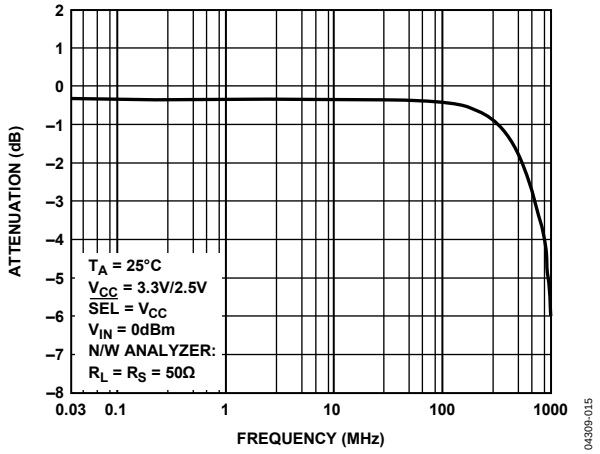


Figure 16. Bandwidth vs. Frequency

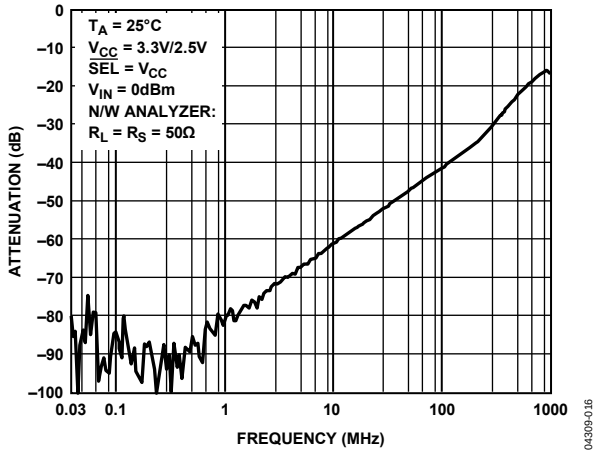


Figure 17. Crosstalk vs. Frequency

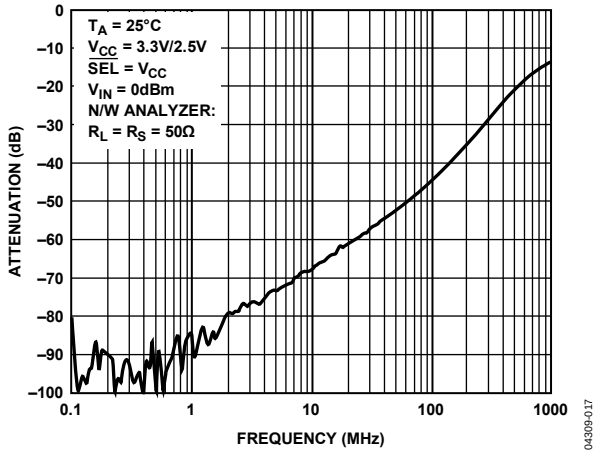


Figure 18. Off Isolation vs. Frequency

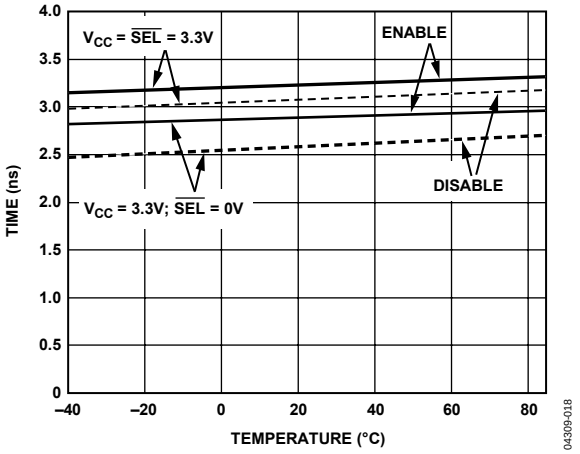


Figure 19. Enable/Disable Time vs. Temperature

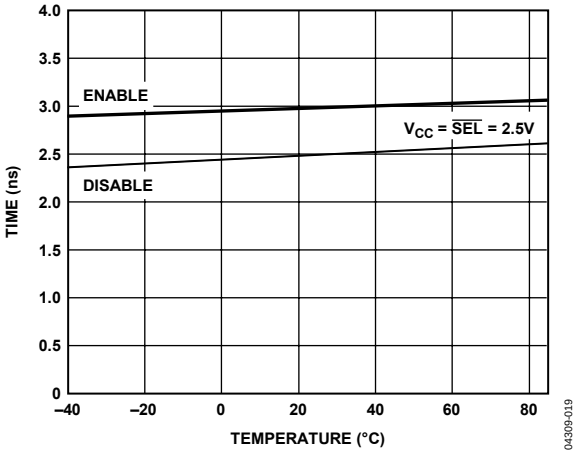


Figure 20. Enable/Disable Time vs. Temperature

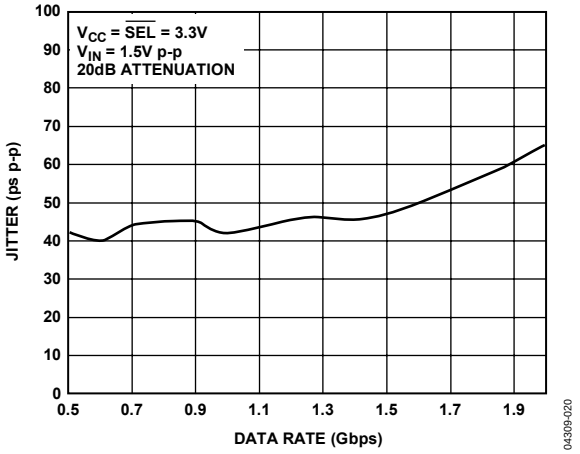


Figure 21. Jitter vs. Data Rate; PRBS 31

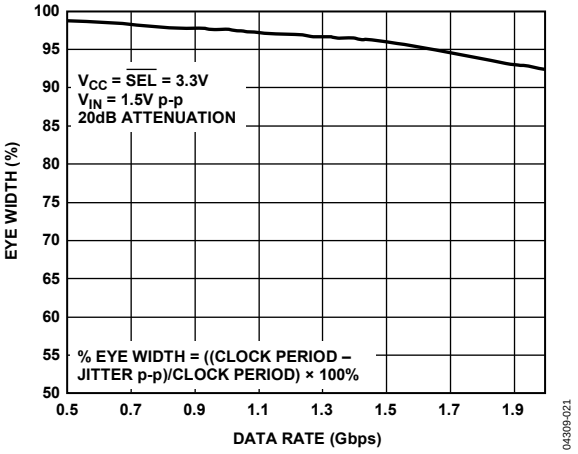


Figure 22. Eye Width vs. Data Rate; PRBS 31

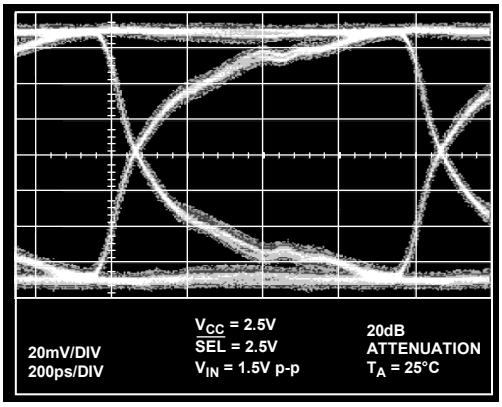


Figure 24. Eye Pattern; 1.244 Gbps, V_{CC} = 2.5 V; PRBS 31

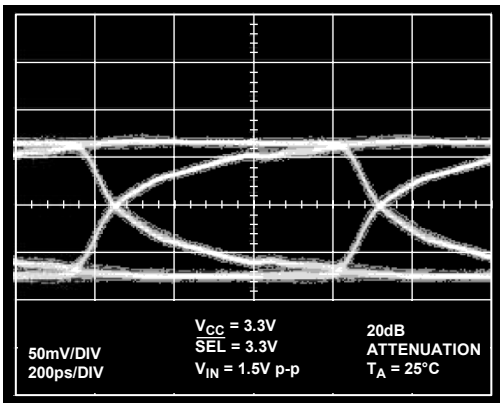


Figure 23. Eye Pattern; 1.5 Gbps, V_{CC} = 3.3 V; PRBS 31

TERMINOLOGY

V_{CC}
Positive power supply voltage.

GND
Ground (0 V) reference.

V_{INH}
Minimum input voltage for Logic 1.

V_{INL}
Maximum input voltage for Logic 0.

I_I
Input leakage current at the control inputs.

I_{OZ}
Off state leakage current. It is the maximum leakage current at the switch pin in the off state.

I_{OL}
On state leakage current. It is the maximum leakage current at the switch pin in the on state.

V_P
Maximum pass voltage. The maximum pass voltage relates to the clamped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.

R_{ON}
Ohmic resistance offered by a switch in the on state. It is measured at a given voltage by forcing a specified amount of current through the switch.

ΔR_{ON}
On resistance match between any two channels, that is, R_{ON} max to R_{ON} min.

C_X OFF
Off switch capacitance.

C_X ON
On switch capacitance.

C_{IN}
Control input capacitance. This consists of $\overline{BE}$ and $\overline{SEL}$.

I_{CC}
Quiescent power supply current. This current represents the leakage current between the V_{CC} and ground pins. It is measured when all control inputs are at logic high or low level and the switches are off.

ΔI_{CC}
Extra power supply current component for the $\overline{EN}$ control input when the input is not driven at the supplies.

t_{PLH}, t_{PHL}
Data propagation delay through the switch in the on state. Propagation delay is related to the RC time constant $R_{ON} \times C_L$, where C_L is the load capacitance.

t_{PZH}, t_{PZL}
Bus enable times. These are the times taken to cross the V_T in response to the control signal, $\overline{BE}$.

t_{PHZ}, t_{PLZ}
Bus disable times. These are the times taken to place the switch in the high impedance off state in response to the control signal. They are measured as the time taken for the output voltage to change by V_Δ from the original quiescent level, with reference to the logic level transition at the control input. (See Figure 27 for enable and disable times.)

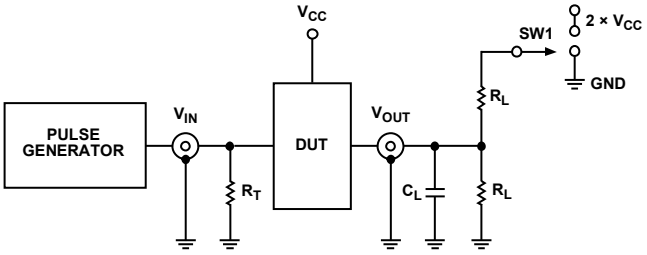
Max Data Rate
Maximum rate at which data can be passed through the switch.

Channel Jitter
Peak-to-peak value of the sum of the deterministic and random jitter of the switch channel.

TIMING MEASUREMENT INFORMATION

For the following load circuit and waveforms, the notation that is used is V_{IN} and V_{OUT} where:

$V_{IN} = V_A$ and $V_{OUT} = V_B$, or $V_{IN} = V_B$ and $V_{OUT} = V_A$



NOTES
1. PULSE GENERATOR FOR ALL PULSES: $t_R \leq 2.5$ns, $t_F \leq 2.5$ns, FREQUENCY ≤ 10MHz.
2. C_L INCLUDES BOARD, STRAY, AND LOAD CAPACITANCES.
3. R_T IS THE TERMINATION RESISTOR, SHOULD BE EQUAL TO Z_{OUT} OF THE PULSE GENERATOR.

Figure 25. Load Circuit

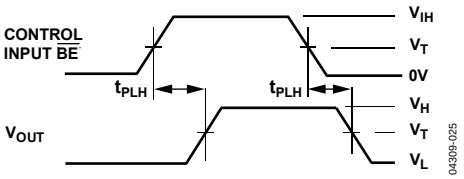


Figure 26. Propagation Delay

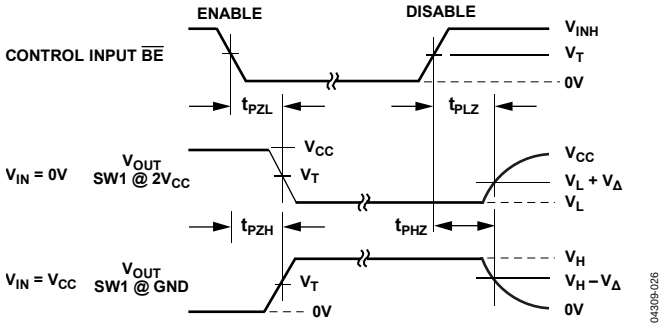


Figure 27. Enable and Disable Times

Table 6. Switch Position

Test	S1
t_{PLZ}, t_{PZL}	$2 \times V_{CC}$
t_{PHZ}, t_{PZH}	GND

Table 7. Test Conditions

Symbol	V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL}$ = V_{CC})	V_{CC} = 2.5 V ± 0.2 V ($\overline{SEL}$ = V_{CC})	V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL}$ = 0 V)	Unit
R_L	500	500	500	Ω
V_Δ	300	150	150	mV
C_L	50	30	30	pF
V_T	1.5	0.9	0.9	V

BUS SWITCH APPLICATIONS

MIXED VOLTAGE OPERATION, LEVEL TRANSLATION

Bus switches provide an ideal solution for interfacing between mixed voltage systems. The ADG3242 is suitable for applications where voltage translation from 3.3 V technology to a lower voltage technology is needed. This device translates from 3.3 V to 1.8 V, from 2.5 V to 1.8 V, or from a bidirectional 3.3 V directly to 2.5 V.

Figure 28 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor does not have 3.3 V tolerant inputs, therefore, placing the ADG3242 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, therefore introducing minimal propagation delay, timing skew, or noise.

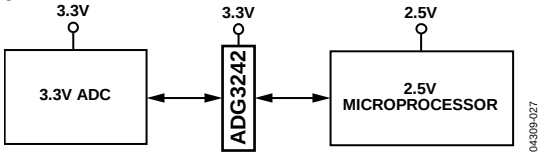


Figure 28. Level Translation Between a 3.3 V ADC and a 2.5 V Microprocessor

3.3 V TO 2.5 V TRANSLATION

When V_{CC} is 3.3 V ($\overline{SEL}$ = 3.3 V) and the input signal range is 0 V to V_{CC}, the maximum output signal is clamped to within a voltage threshold below the V_{CC} supply. In this case, the output is limited to 2.5 V, as shown in Figure 30. This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

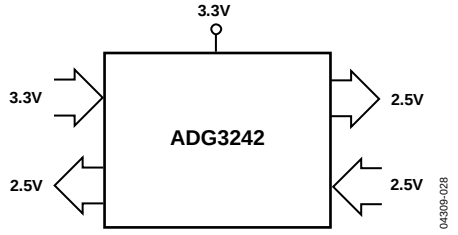


Figure 29. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

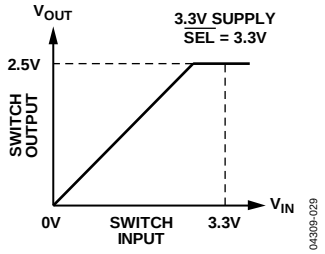


Figure 30. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

2.5 V TO 1.8 V TRANSLATION

When V_{CC} is 2.5 V ($\overline{SEL}$ = 2.5 V) and the input signal range is 0 V to V_{CC}, the maximum output signal is also clamped within a voltage threshold below the V_{CC} supply. In this case, the output is limited to approximately 1.8 V, as shown in Figure 32.

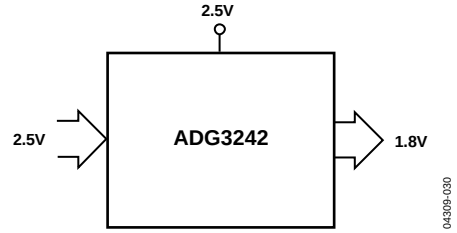


Figure 31. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 2.5 V_{CC}

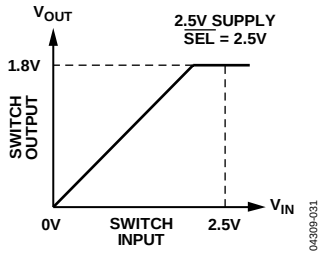


Figure 32. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

3.3 V TO 1.8 V TRANSLATION

The ADG3242 offers the option of interfacing between a 3.3 V device and a 1.8 V device. This is possible through use of the $\overline{SEL}$ pin. The $\overline{SEL}$ pin is an active low control pin. $\overline{SEL}$ activates internal circuitry in the ADG3242 that allows voltage translation between 3.3 V devices and 1.8 V devices.

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC}, the maximum output signal is clamped to 1.8 V, as shown in Figure 34. To do this, the $\overline{SEL}$ pin must be tied to Logic 0. If $\overline{SEL}$ is unused, it can be tied directly to V_{CC}.

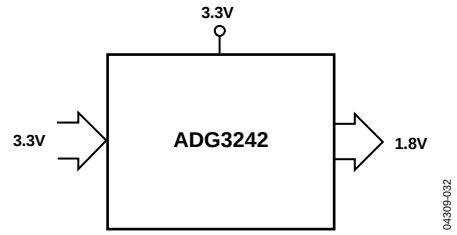


Figure 33. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0 V

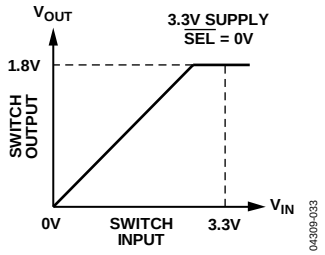


Figure 34. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0 V

BUS ISOLATION

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus bridge devices that extend the number of loads on the bus without exceeding the specifications. Because the ADG3242 is designed specifically for applications that do not need drive, yet require simple logic functions, it solves this requirement. The device isolates access to the bus, thus minimizing capacitance loading.

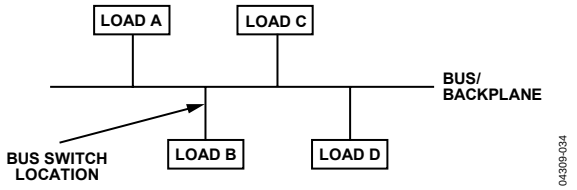


Figure 35. Location of Bus Switched in a Bus Isolation Application

HOT PLUG AND HOT SWAP ISOLATION

The ADG3242 is suitable for hot swap and hot plug applications. The output signal of the ADG3242 is limited to a voltage that is below the V_{CC} supply, as shown in Figure 30, Figure 32, and Figure 34. Thus, the switch acts like a buffer to take the impact from the hot insertion, protecting vital and expensive chipsets from damage.

In hot plug applications, the system cannot be shut down when new hardware is being added. To overcome this, a bus switch can be positioned on the backplane between the bus devices and the hot plug connectors. The bus switch is turned off during hot plug. Figure 36 shows a typical example of this type of application.

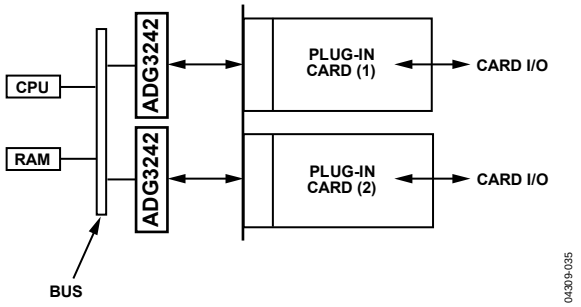


Figure 36. ADG3242 in a Hot Plug Application

There are many systems, such as docking stations, PCI boards for servers, and line cards for telecommunications switches, that require the ability to handle hot swapping. If the bus can be isolated prior to insertion or removal, there is more control over the hot swap event. This isolation can be achieved using bus switches. The bus switches are positioned on the hot swap card between the connector and the devices. During hot swap, the ground pin of the hot swap card must connect to the ground pin of the backplane before connecting to any other signal or power pins.

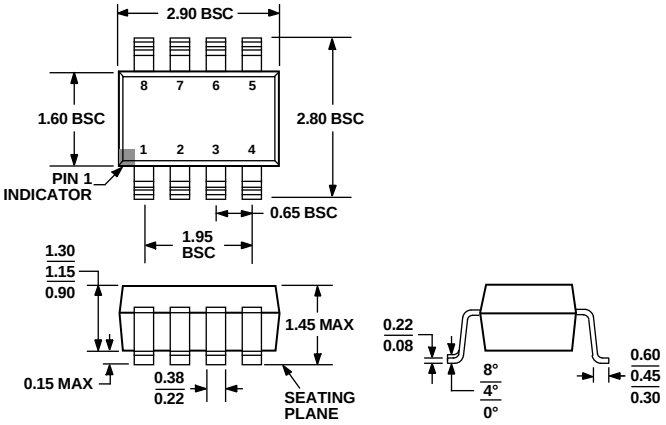
ANALOG SWITCHING

Bus switches are used in many analog switching applications, for example, video graphics. Bus switches can have lower on resistance, smaller on and off channel capacitance, and better frequency performance than their analog counterparts. The bus switch channel itself, consisting solely of an NMOS switch, limits the operating voltage (see Figure 4 for a typical plot), but in many cases, this does not present an issue.

HIGH IMPEDANCE DURING POWER-UP/POWER-DOWN

To ensure the high impedance state during power-up or power-down, $\overline{BE}$ must be tied to V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current sinking capability of the driver.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 37. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG3242BRJ-R2	−40°C to +85°C	8-Lead Small Outline Transistor [SOT-23]	RJ-8	SCA
ADG3242BRJ-REEL	−40°C to +85°C	8-Lead Small Outline Transistor [SOT-23]	RJ-8	SCA
ADG3242BRJ-REEL7	−40°C to +85°C	8-Lead Small Outline Transistor [SOT-23]	RJ-8	SCA
ADG3242BRJZ-REEL7[1]	−40°C to +85°C	8-Lead Small Outline Transistor [SOT-23]	RJ-8	SOU
ADG3242BCZ-SF3[1]	−40°C to +85°C	Die	Chip	

[1] Z = Pb-free part.

NOTES

NOTES

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C04309-0-9/06(A)

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ADG3242BRJZ-REEL7