

General Features

- Low Gate Charge
- Advanced Trench Technology
- Provide Excellent RDS(ON)
- High Power and Current Handling Capability

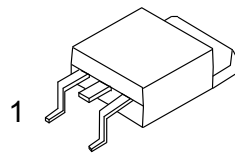
Application

- Load Switch
- PWM applications
- Power management

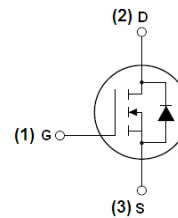
Product Summary



V _{DS}	30	V
R _{DS(on)} , Typ. @ V _{GS} =10 V	3.6	mΩ
I _D	90	A



TO-252



N-channel

Absolute Maximum Ratings (T_A =25°C unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ^B	I _D	T _C =25°C	90
		T _C =100°C	46
Pulsed Drain Current ^A	I _{DM}	255	A
Avalanche Current ^A	I _S	90	A
Single Pulse Avalanche Energy L =0.3mH ^A	E _{AS}	135	mJ
Power Dissipation ^C	P _D	T _C =25°C	65
		T _C =100°C	32
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 175	°C
Thermal Characteristics			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Case	R _{θJC}	2.3	°C/W
Maximum Junction-to-Ambient	R _{θJA}	100	

Electrical Characteristics($T_J = 25^\circ\text{C}$ unless otherwise noted)							
Symbol	Parameter	Conditions	Value			Units	
			Min	Typ	Max		
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	--	--	V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	$T_J = 25^\circ\text{C}$	--	--	1	μA
			$T_J = 125^\circ\text{C}$	--	--	25	
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	--	--	± 100	nA	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.6	2.4	V	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	--	3.6	4.5	$\text{m}\Omega$	
		$V_{GS} = 4.5\text{V}, I_D = 30\text{A}$	--	6.9	9.0	$\text{m}\Omega$	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 20\text{A}$	16	--	--	S	
V_{SD}	Diode Forward Voltage	$I_S = 30\text{A}, V_{GS} = 0\text{V}$	--	--	1	V	
I_S	Maximum Body-Diode Continuous Current ^B		--	--	90	A	
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 15\text{V}, f = 1\text{MHz}$	--	2120	--	pF	
C_{oss}	Output Capacitance		--	307	--		
C_{rss}	Reverse Transfer Capacitance		--	253	--		
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V}, I_D = 30\text{A}$	--	40	--	nC	
Q_{gs}	Gate Source Charge		--	5.4	--		
Q_{gd}	Gate Drain Charge		--	9.6	--		
$t_{D(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V}, I_D = 20\text{A}, R_G = 3\Omega$	--	15	--	ns	
t_r	Turn-On Rise Time		--	32	--		
$t_{D(off)}$	Turn-Off Delay Time		--	15	--		
t_f	Turn-Off Fall Time		--	12	--		
t_{rr}	Body Diode Reverse Recovery Time	$I_F = 30\text{A}, di/dt = 100\text{A}/\mu\text{s}$	--	23	--	ns	
Q_{rr}	Body Diode Reverse Recovery Charge		--	48	--	nC	

- A. Single pulse width limited by maximum junction temperature.
- B. The maximum current rating is package limited.
- C. The power dissipation P_D is based on $T_{J(MAX)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

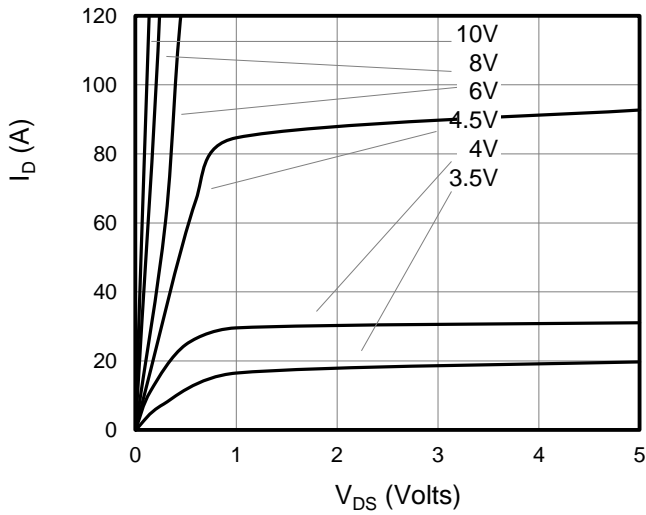


Figure 1: On-Region Characteristics

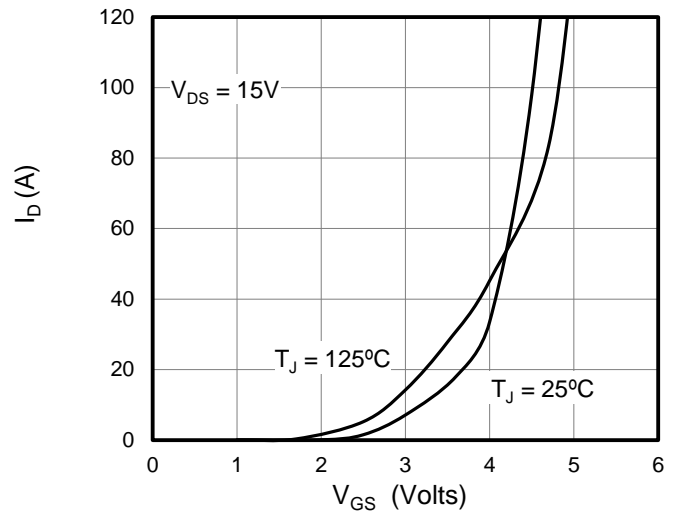


Figure 2: Transfer Characteristics

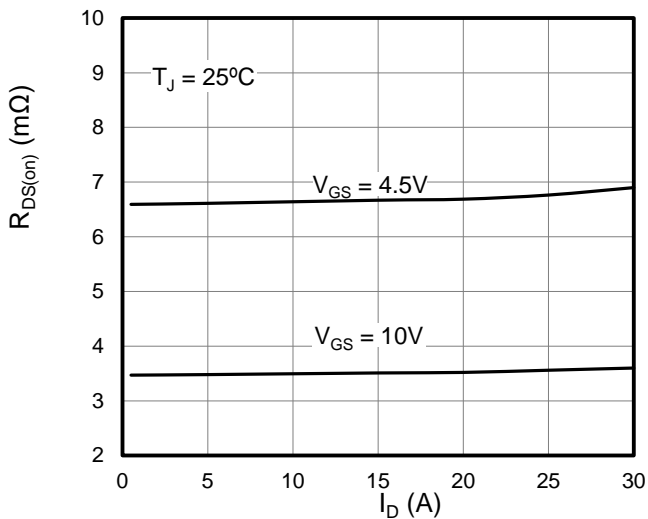


Figure 3: On-Resistance vs. Drain Current

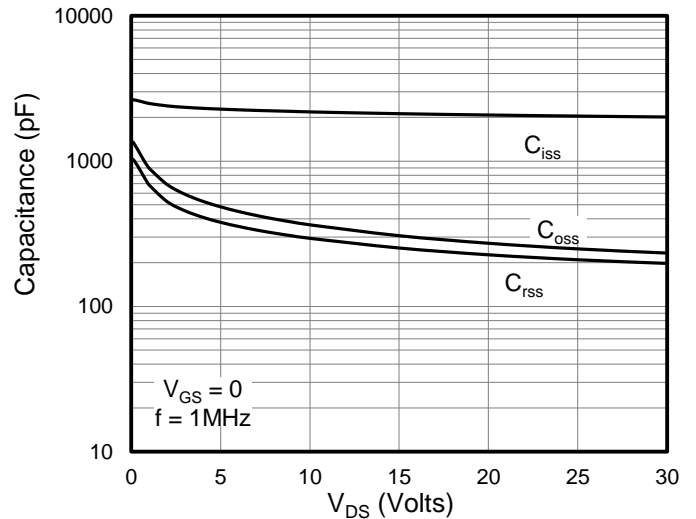


Figure 4: Capacitance Characteristics

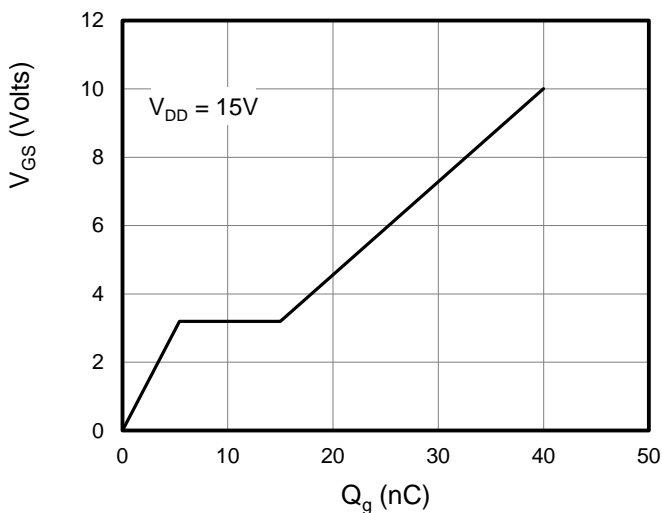


Figure 5: Gate Charge Characteristics

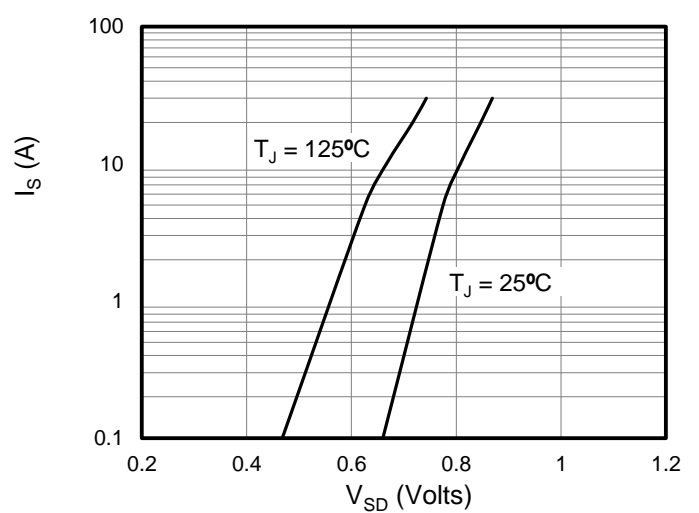


Figure 6: Body Diode Forward Voltage

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

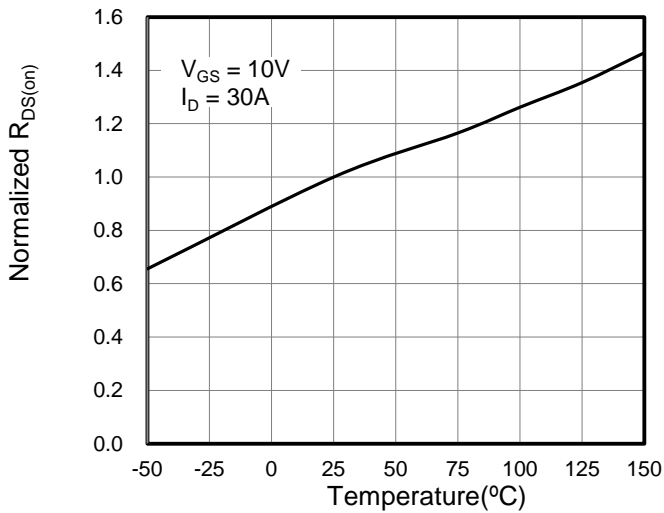


Figure 7: On-Resistance vs. Junction Temperature

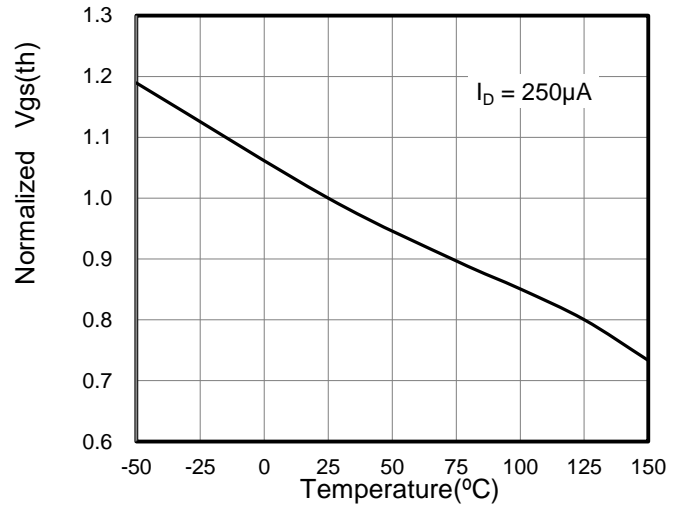


Figure 8: $V_{GS(th)}$ vs. Junction Temperature

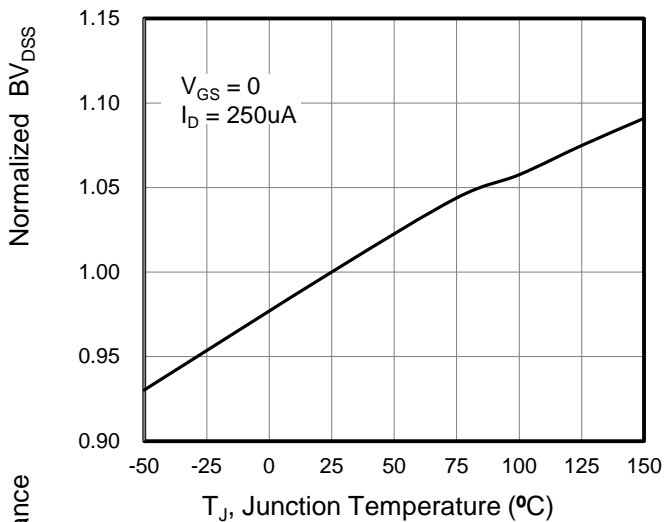


Figure 9: BV_{DSS} vs. Junction Temperature

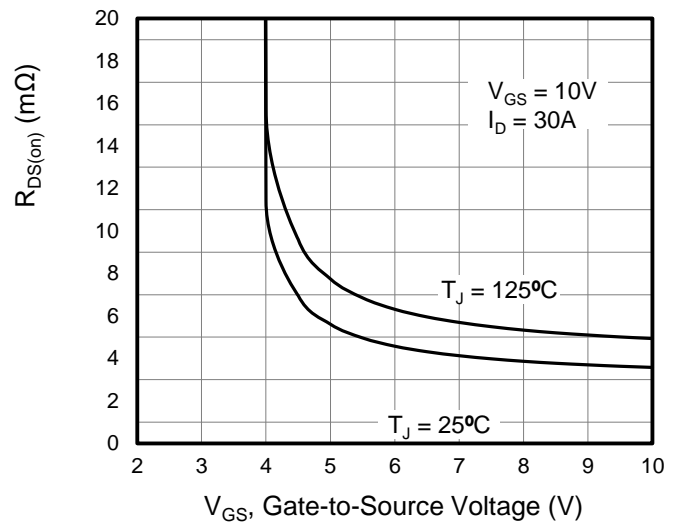


Figure 10: On-Resistance vs. Gate-Source Voltage

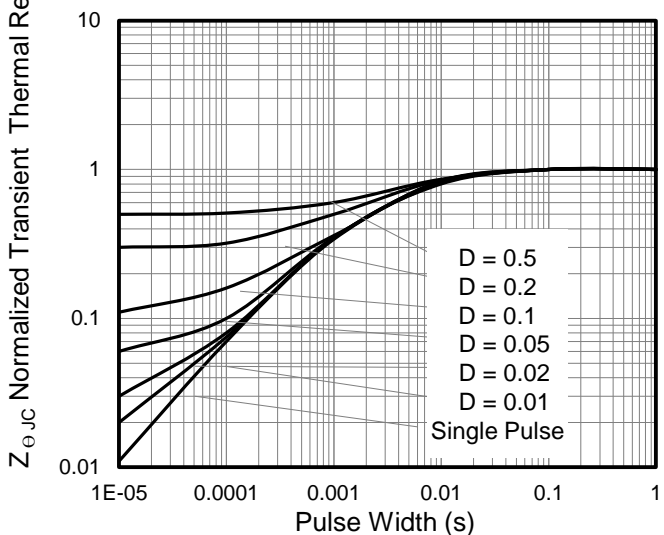


Figure 11: Normalized Transient Thermal Resistance

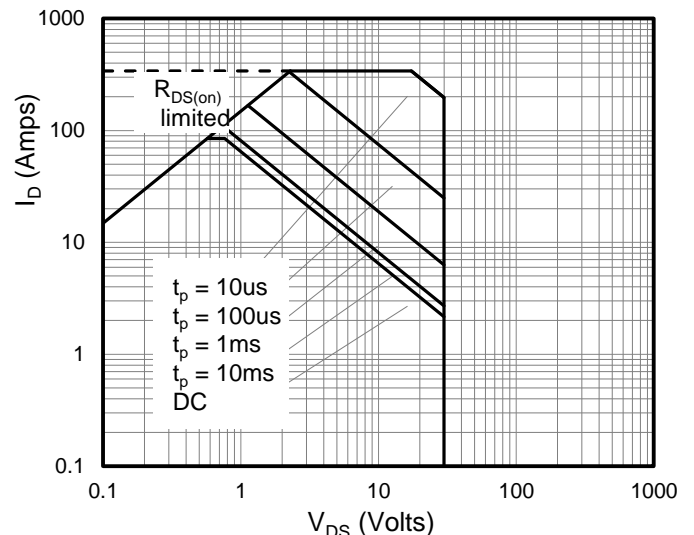


Figure 12: Safe Operating Area

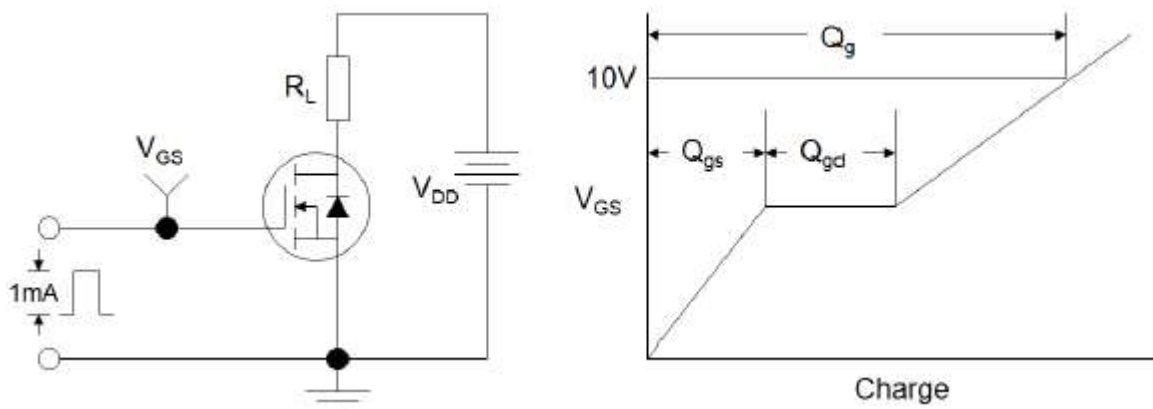


Figure 1: Gate Charge Test Circuit & Waveform

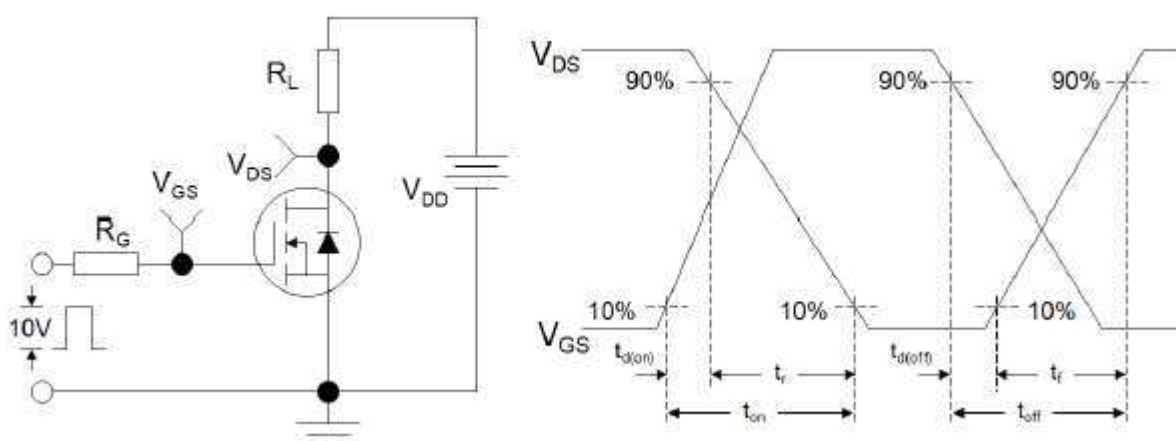


Figure 2: Resistive Switching Test Circuit & Waveforms

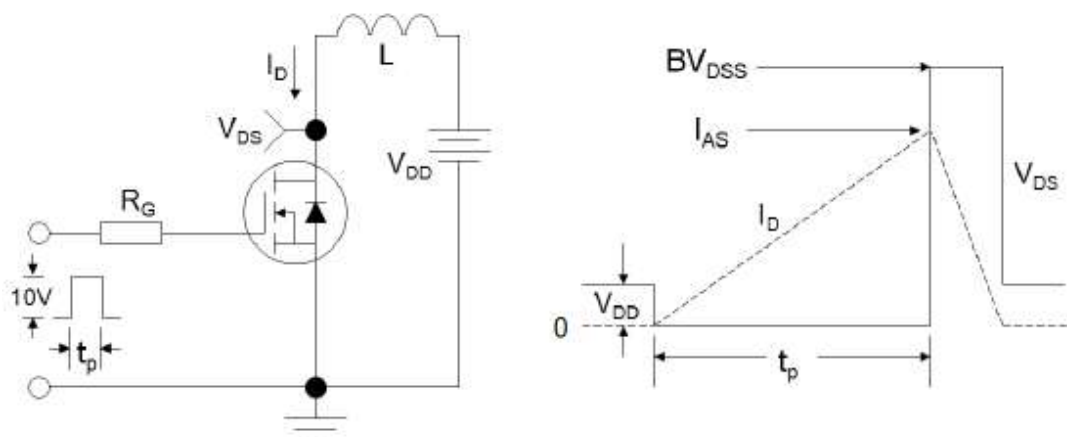


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

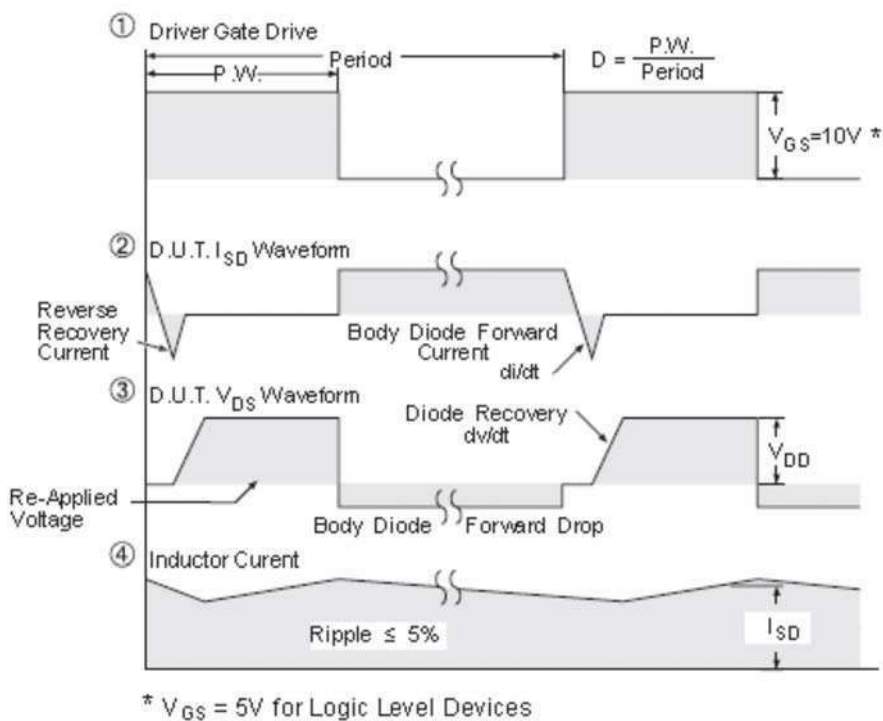
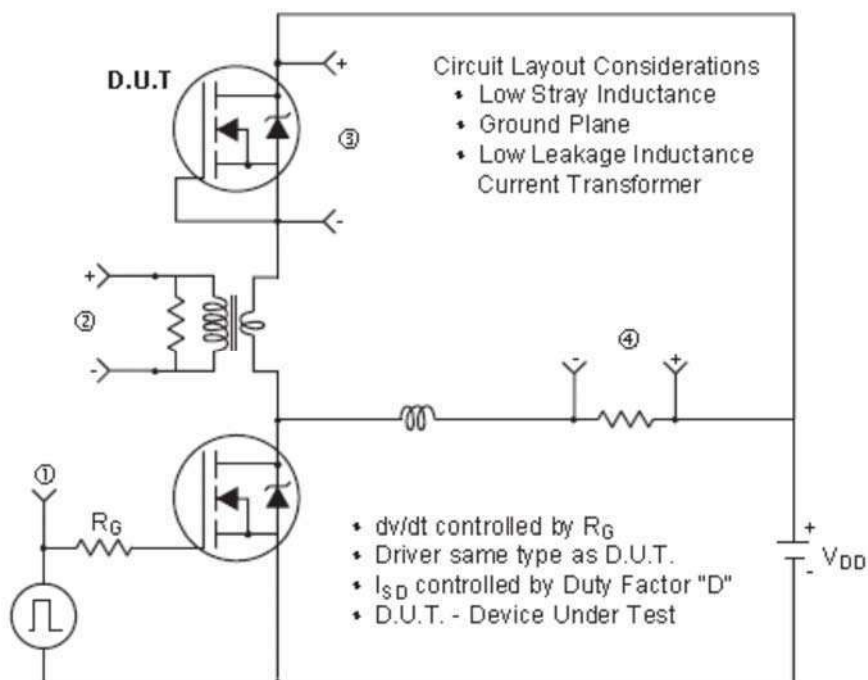
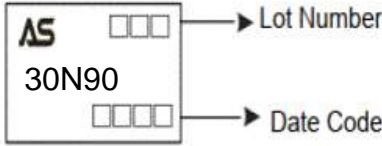


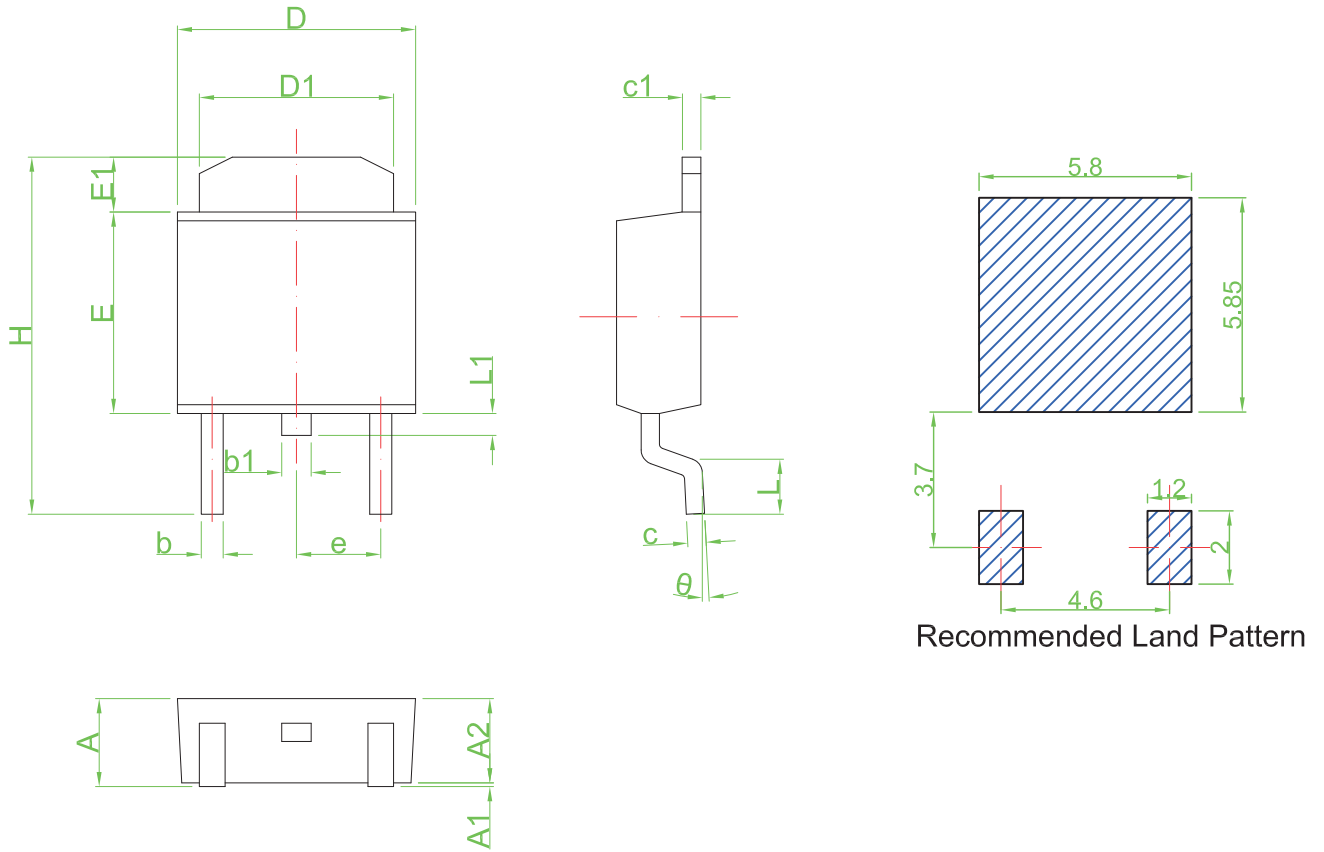
Figure 4: Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Ordering and Marking Information

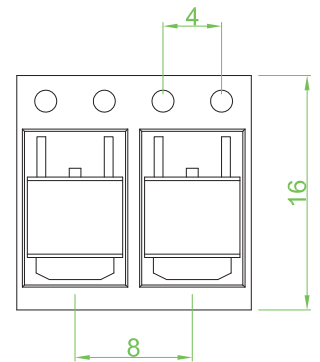
Ordering Device No.	Marking	Package	Packing	Quantity
ASDM30N90KQ-R	30N90	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 <p>The diagram shows a rectangular marking area on a TO-252 package. It contains the following information from top to bottom: the logo 'AS', the part number '30N90', two empty boxes representing the Lot Number, and four empty boxes representing the Date Code. Arrows point from the text 'Lot Number' and 'Date Code' to their respective boxes.</p>

TO-252 PACKAGE IN FORMATION



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.25	2.65	0.089	0.104
A1	0.00	0.15	0.000	0.006
A2	2.20	2.40	0.087	0.094
b	0.50	0.70	0.020	0.028
b1	0.70	0.90	0.028	0.035
c	0.46	0.66	0.018	0.026
c1	0.46	0.66	0.018	0.026
D	6.30	6.70	0.248	0.264
D1	5.20	5.40	0.205	0.213
E	5.30	5.70	0.209	0.224
E1	1.40	1.60	0.055	0.063
H	9.40	9.90	0.370	0.390
e	2.30 TYP		0.09 TYP	
L	1.40	1.77	0.055	0.070
L1	0.50	0.70	0.020	0.028
θ	0°	8°	0°	8°



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