

2N6667, 2N6668

Darlington Silicon Power Transistors

Designed for general-purpose amplifier and low speed switching applications.

- High DC Current Gain –
 $h_{FE} = 3500$ (Typ) @ $I_C = 4.0$ Adc
- Collector–Emitter Sustaining Voltage – @ 200 mAdc
 $V_{CE(sus)} = 60$ Vdc (Min) – 2N6667
 $= 80$ Vdc (Min) – 2N6668
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 5.0$ Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package
- Complementary to 2N6387, 2N6388
- These Devices are Pb–Free and are RoHS Compliant*

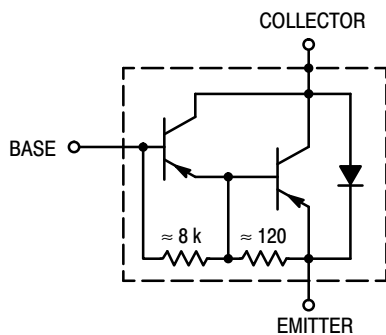


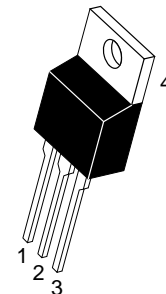
Figure 1. Darlington Schematic



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**PNP SILICON
DARLINGTON
POWER TRANSISTORS
10 A, 60–80 V, 65 W**



TO-220
CASE 221A
STYLE 1

MARKING DIAGRAM



x = 7 or 8
A = Assembly Location
Y = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping
2N6667G	TO-220 (Pb–Free)	50 Units/Rail
2N6668G	TO-220 (Pb–Free)	50 Units/Rail

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MAXIMUM RATINGS (Note 1)

Rating	Symbol	2N6667	2N6668	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous – Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	65 0.52		W W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016		W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS (Note 1) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Note 2) ($I_C = 200\text{ mAdc}, I_B = 0$)	2N6667 2N6668	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}, I_B = 0$) ($V_{CE} = 80\text{ Vdc}, I_B = 0$)	2N6667 2N6668	I_{CEO}	– –	1.0 1.0	mAdc
Collector Cutoff Current ($V_{CE} = 60\text{ Vdc}, V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 80\text{ Vdc}, V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 60\text{ Vdc}, V_{EB(off)} = 1.5\text{ Vdc}, T_C = 125^\circ\text{C}$) ($V_{CE} = 80\text{ Vdc}, V_{EB(off)} = 1.5\text{ Vdc}, T_C = 125^\circ\text{C}$)	2N6667 2N6668 2N6667 2N6668	I_{CEX}	– – – –	300 300 3.0 3.0	μAdc mAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}, I_C = 0$)		I_{EBO}	–	5.0	mAdc

ON CHARACTERISTICS (Note 1)

DC Current Gain ($I_C = 5.0\text{ Adc}, V_{CE} = 3.0\text{ Vdc}$) ($I_C = 10\text{ Adc}, V_{CE} = 3.0\text{ Vdc}$)		h_{FE}	1000 100	20000 –	–
Collector–Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}, I_B = 0.01\text{ Adc}$) ($I_C = 10\text{ Adc}, I_B = 0.1\text{ Adc}$)		$V_{CE(sat)}$	– –	2.0 3.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 5.0\text{ Adc}, I_B = 0.01\text{ Adc}$) ($I_C = 10\text{ Adc}, I_B = 0.1\text{ Adc}$)		$V_{BE(sat)}$	– –	2.8 4.5	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($I_C = 1.0\text{ Adc}, V_{CE} = 5.0\text{ Vdc}, f_{test} = 1.0\text{ MHz}$)		$ h_{fe} $	20	–	–
Output Capacitance ($V_{CB} = 10\text{ Vdc}, I_E = 0, f = 1.0\text{ MHz}$)		C_{ob}	–	200	pF
Small–Signal Current Gain ($I_C = 1.0\text{ Adc}, V_{CE} = 5.0\text{ Vdc}, f = 1.0\text{ kHz}$)		h_{fe}	1000	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Indicates JEDEC Registered Data.
2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

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R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 , MUST BE FAST RECOVERY TYPES e.g.,

1N5825 USED ABOVE $I_B \approx 100$ mA

MSD6100 USED BELOW $I_B \approx 100$ mA

FOR t_d AND t_r , D_1 IS DISCONNECTED AND $V_2 = 0$

$t_r, t_f \leq 10$ ns

DUTY CYCLE = 1.0%

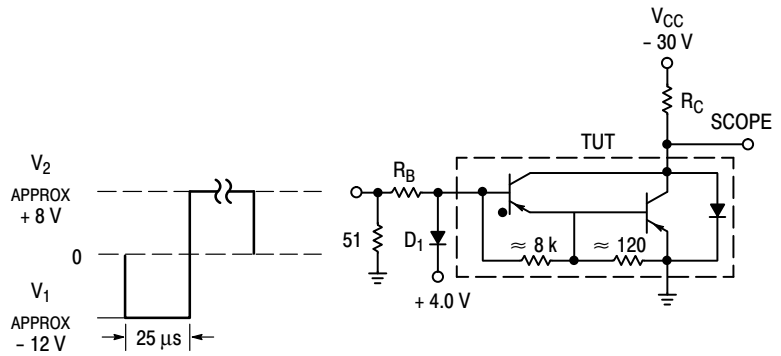


Figure 2. Switching Times Test Circuit

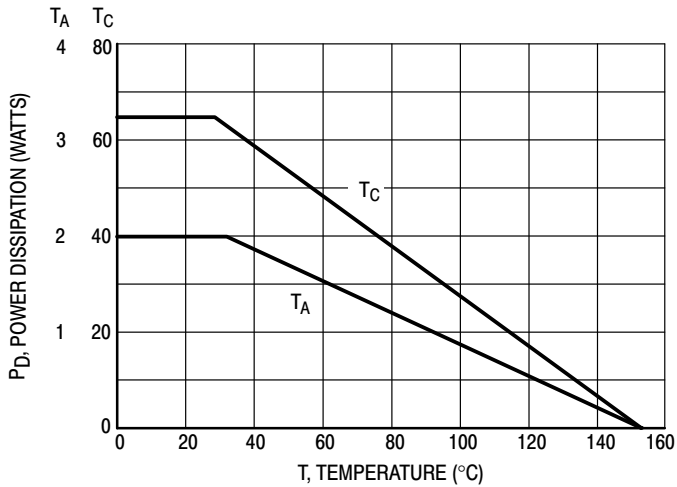


Figure 3. Power Derating

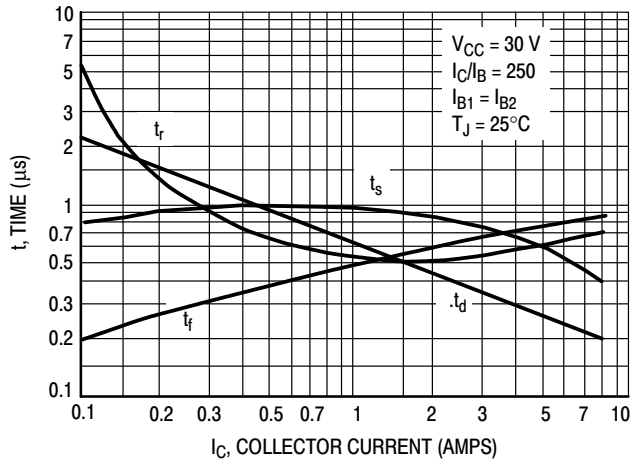


Figure 4. Typical Switching Times

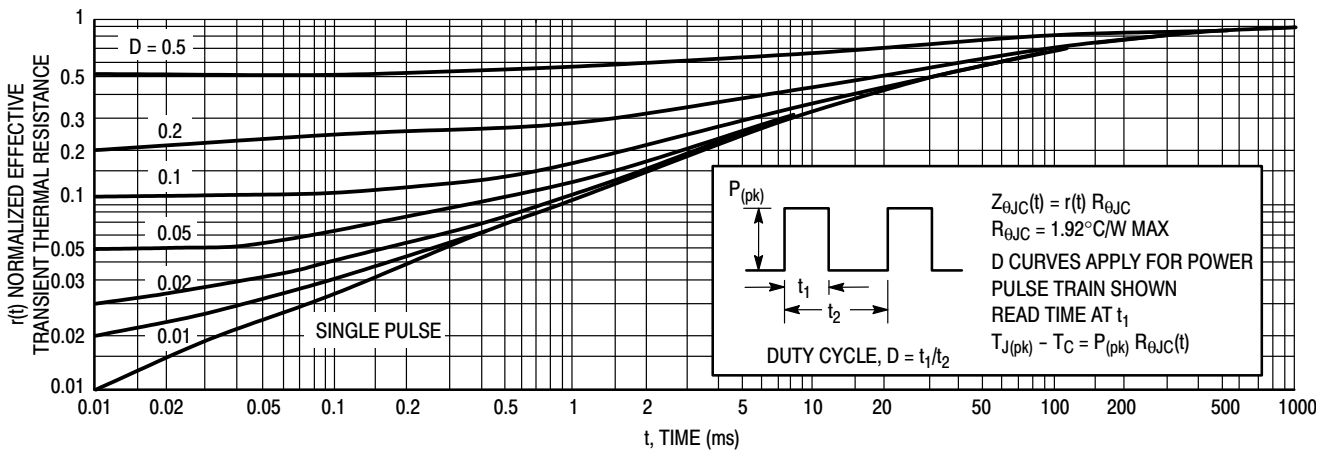


Figure 5. Thermal Response

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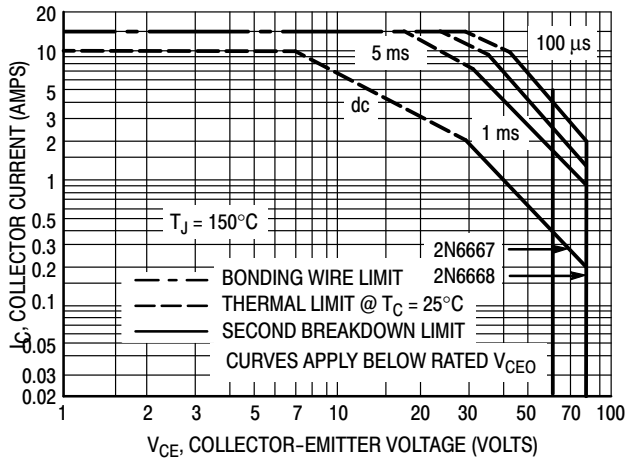


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

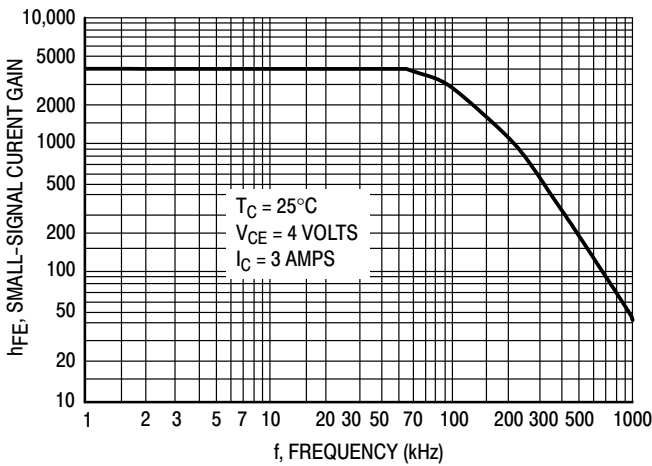


Figure 7. Typical Small-Signal Current Gain

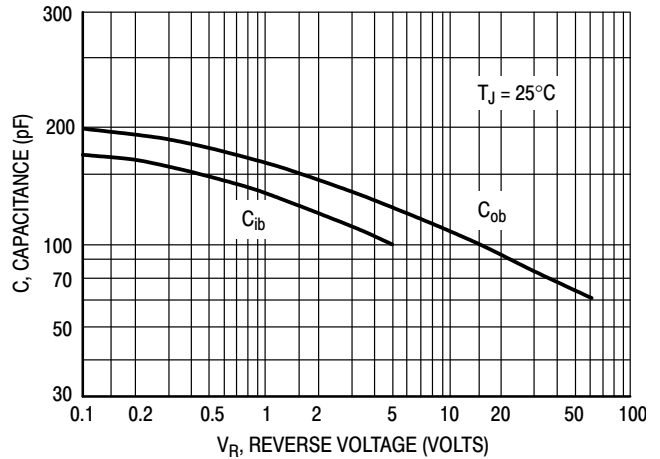


Figure 8. Typical Capacitance

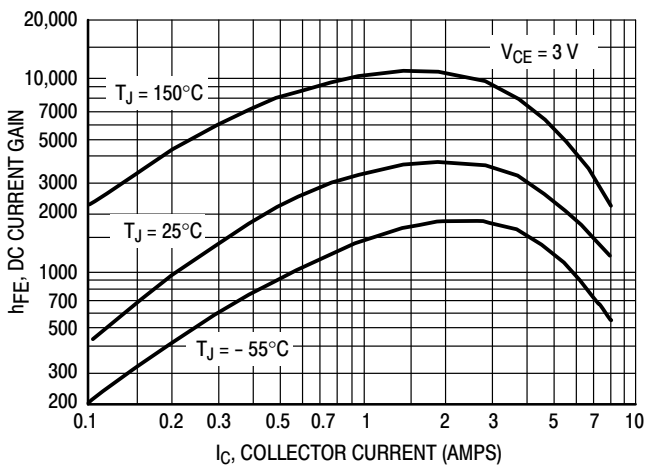


Figure 9. Typical DC Current Gain

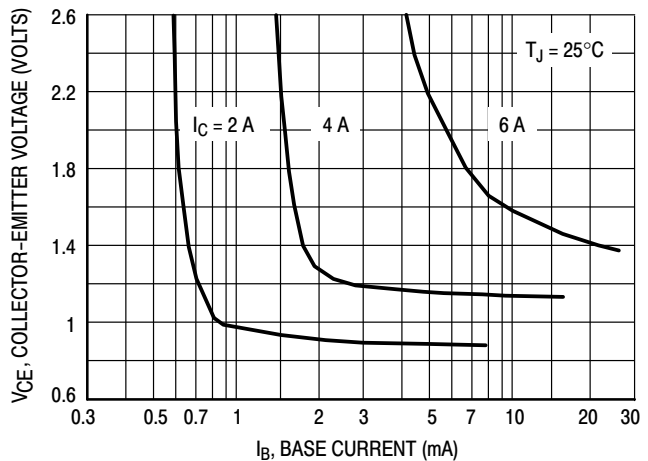


Figure 10. Typical Collector Saturation Region

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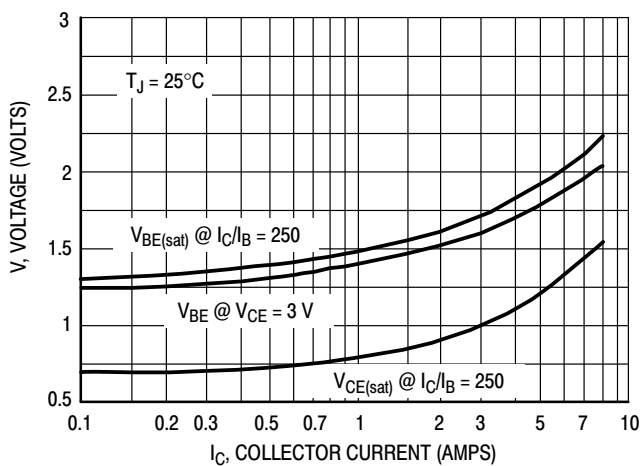


Figure 11. Typical "On" Voltages

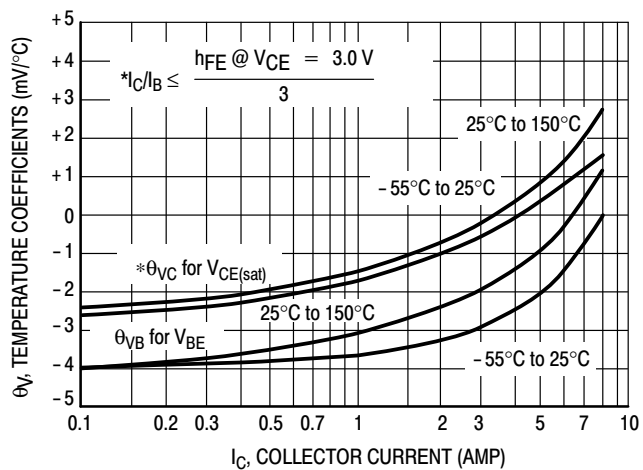


Figure 12. Typical Temperature Coefficients

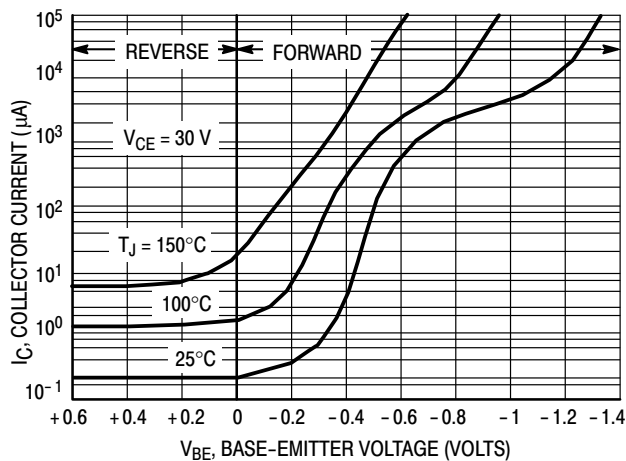
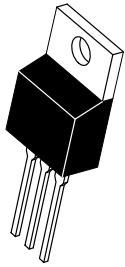


Figure 13. Typical Collector Cut-Off Region

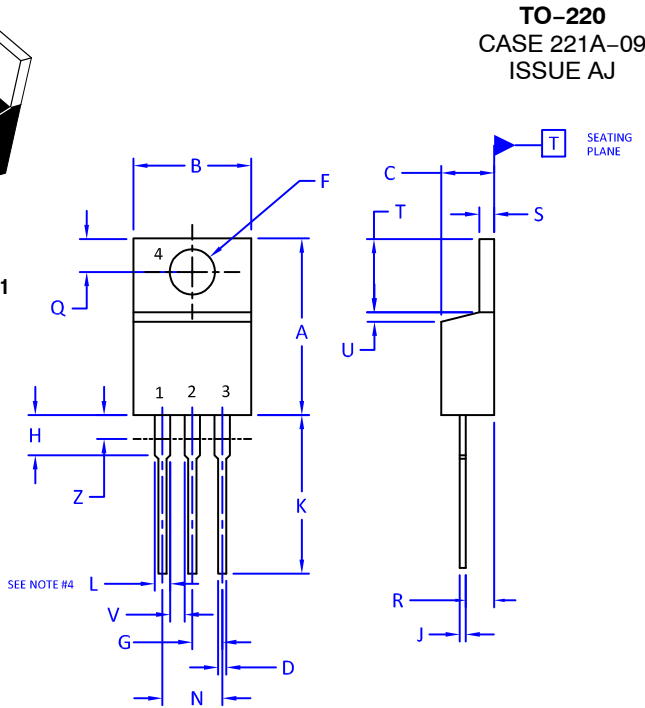
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



DATE 05 NOV 2019

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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