

# 2N6487, 2N6488 (NPN), 2N6490, 2N6491 (PNP)



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## Complementary Silicon Plastic Power Transistors

These devices are designed for use in general-purpose amplifier and switching applications.

### Features

- High DC Current Gain
- High Current Gain – Bandwidth Product
- TO–220 Compact Package
- These Devices are Pb–Free and are RoHS Compliant\*

### MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage 2N6487, 2N6490 2N6488, 2N6491	$V_{CEO}$	60 80	Vdc
Collector–Base Voltage 2N6487, 2N6490 2N6488, 2N6491	$V_{CB}$	70 90	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous	$I_C$	15	Adc
Base Current	$I_B$	5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	75 0.6	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.8 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

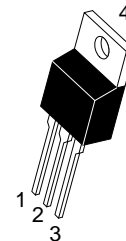
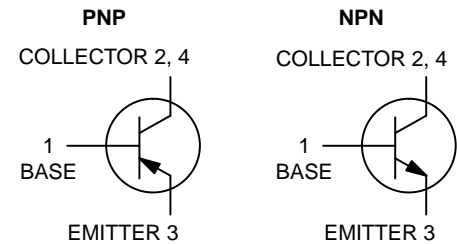
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Indicates JEDEC Registered Data.

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	70	$^\circ\text{C}/\text{W}$

## 15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80 VOLTS, 75 WATTS



TO–220  
CASE 221A  
STYLE 1

### MARKING DIAGRAM



2N64xx = Specific Device Code  
xx = See Table on Page 5  
G = Pb–Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 5 of this data sheet.

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## 2N6487, 2N6488 (NPN), 2N6490, 2N6491 (PNP)

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 3) ( $I_C = 200\text{ mA}$ , $I_B = 0$ ) 2N6487, 2N6490 2N6488, 2N6491	$V_{CE(sus)}$	60 80	– –	Vdc
Collector–Emitter Sustaining Voltage (Note 3) ( $I_C = 200\text{ mA}$ , $V_{BE} = 1.5\text{ Vdc}$ ) 2N6487, 2N6490 2N6488, 2N6491	$V_{CEX}$	70 90	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) 2N6487, 2N6490 ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) 2N6488, 2N6491	$I_{CEO}$	– –	1.0 1.0	mA
Collector Cutoff Current ( $V_{CE} = 65\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) 2N6487, 2N6490 ( $V_{CE} = 85\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) 2N6488, 2N6491 ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) 2N6487, 2N6490 ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) 2N6488, 2N6491	$I_{CEX}$	– – – –	500 500 5.0 5.0	$\mu\text{A}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	1.0	mA

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 5.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 15\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	20 5.0	150 –	–
Collector–Emitter Saturation Voltage ( $I_C = 5.0\text{ A}$ , $I_B = 0.5\text{ A}$ ) ( $I_C = 15\text{ A}$ , $I_B = 5.0\text{ A}$ )	$V_{CE(sat)}$	– –	1.3 3.5	Vdc
Base–Emitter On Voltage ( $I_C = 5.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 15\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	– –	1.3 3.5	Vdc

### DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 4) ( $I_C = 1.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	5.0	–	MHz
Small–Signal Current Gain ( $I_C = 1.0\text{ A}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	25	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data.

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

4.  $f_T = |h_{fe}| \cdot f_{test}$

# 2N6487, 2N6488 (NPN), 2N6490, 2N6491 (PNP)

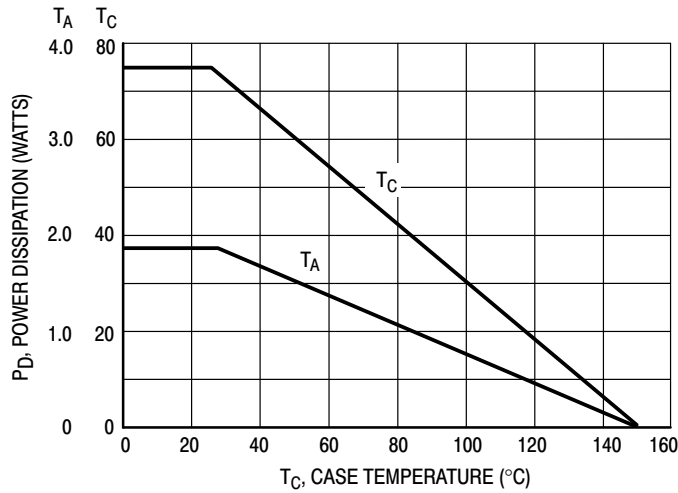
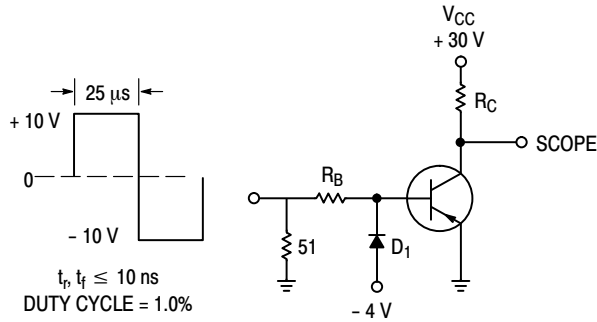


Figure 1. Power Derating



$R_B$  AND  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS. FOR PNP, REVERSE ALL POLARITIES.

$D_1$  MUST BE FAST RECOVERY TYPE, e.g.:  
 1N5825 USED ABOVE  $I_B \approx 100$  mA  
 MSD6100 USED BELOW  $I_B \approx 100$  mA

Figure 2. Switching Time Test Circuit

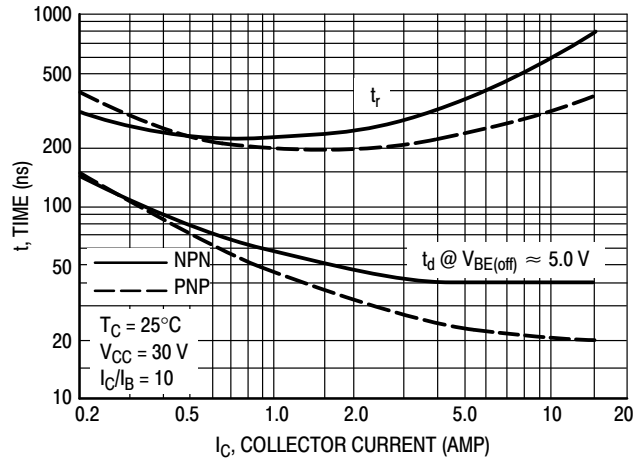


Figure 3. Turn-On Time

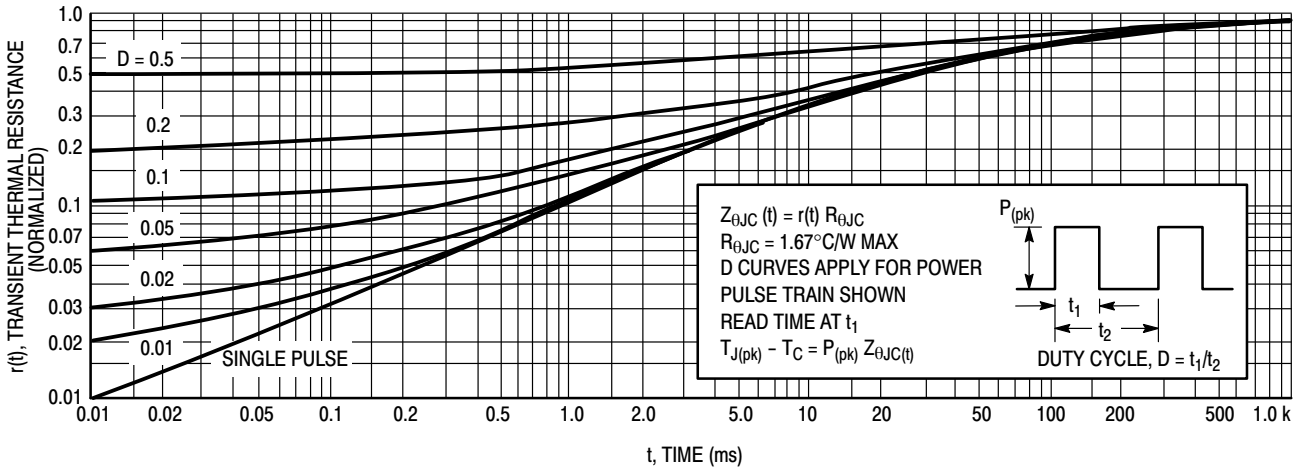
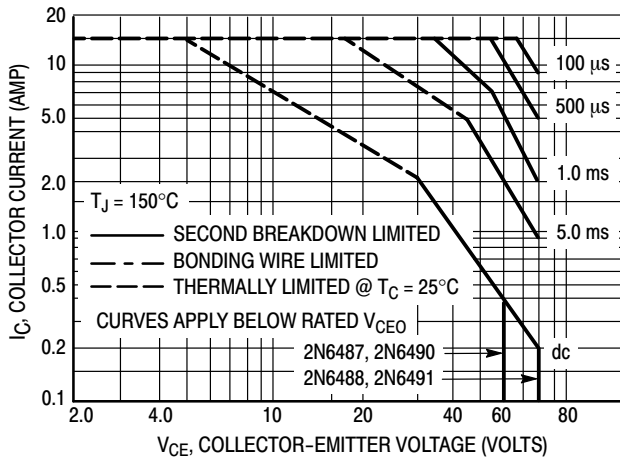


Figure 4. Thermal Response

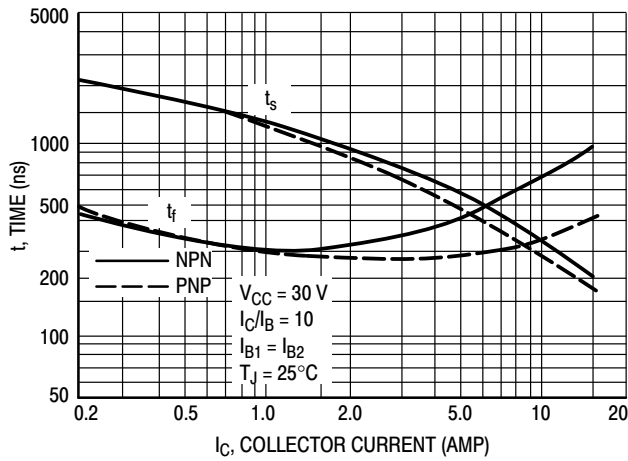
## 2N6487, 2N6488 (NPN), 2N6490, 2N6491 (PNP)



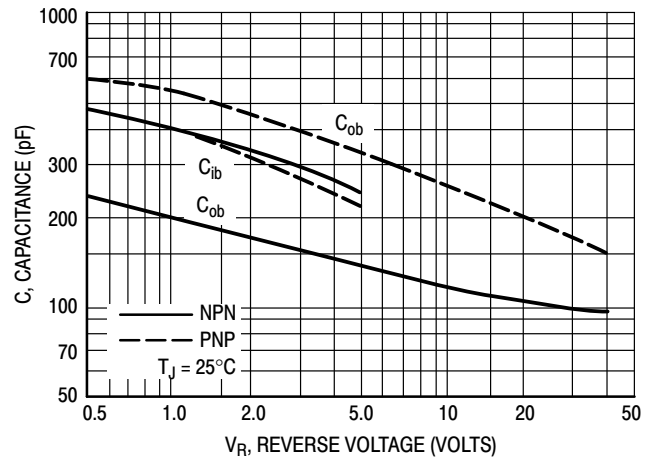
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor's average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

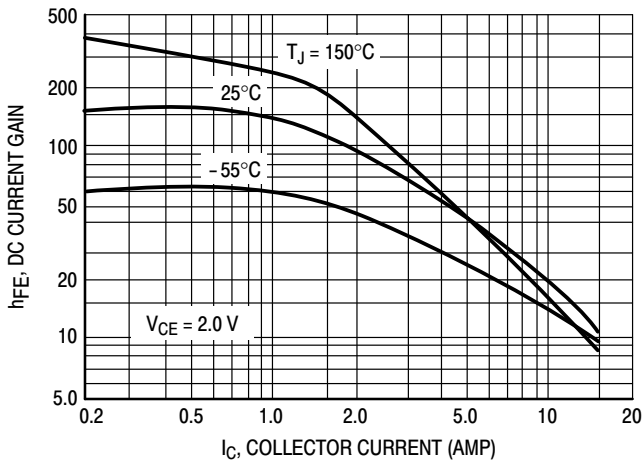


**Figure 6. Turn-Off Time**

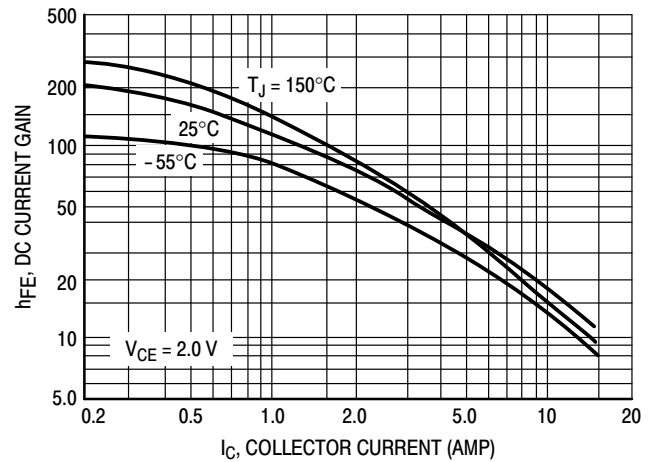


**Figure 7. Capacitances**

### NPN 2N6487, 2N6488

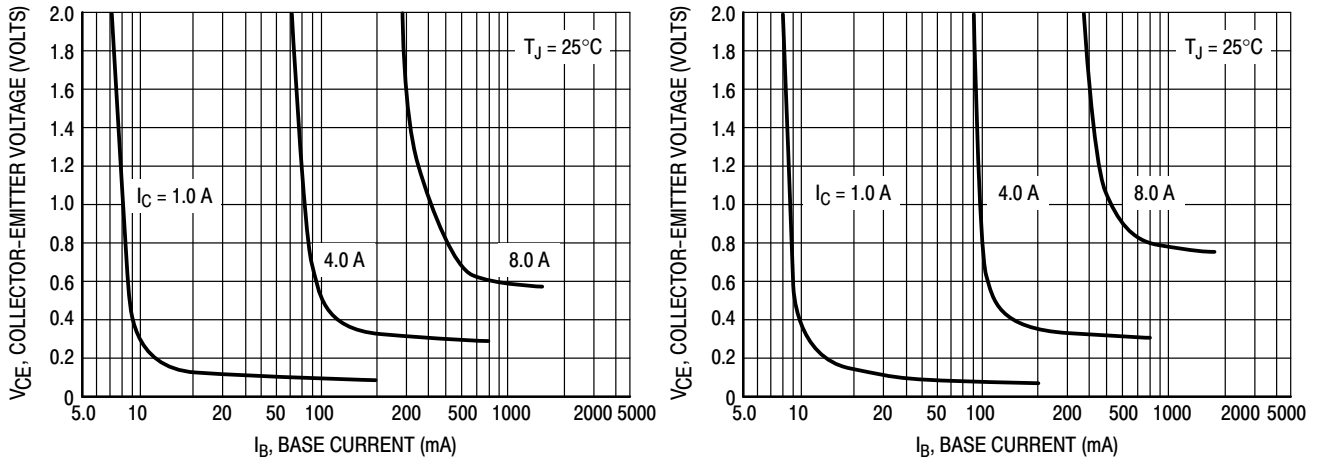


### PNP 2N6490, 2N6491

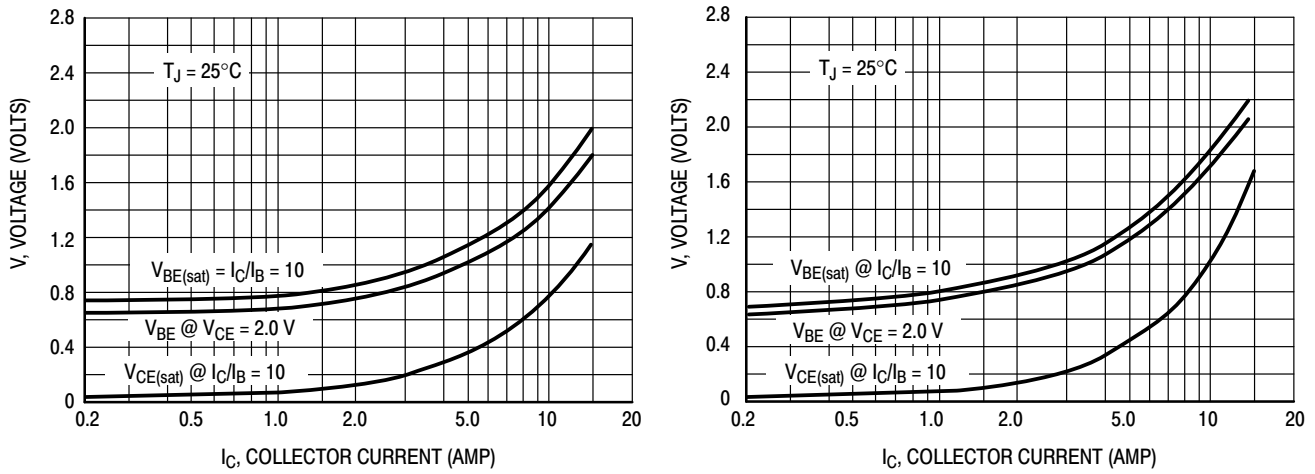


**Figure 8. DC Current Gain**

## 2N6487, 2N6488 (NPN), 2N6490, 2N6491 (PNP)



**Figure 9. Collector Saturation Region**



**Figure 10. "On" Voltages**

### ORDERING INFORMATION

Device	Device Marking	Package	Shipping
2N6487G	2N6487	TO-220 (Pb-Free)	50 Units / Rail
2N6488G	2N6488	TO-220 (Pb-Free)	50 Units / Rail
2N6490G	2N6490	TO-220 (Pb-Free)	50 Units / Rail
2N6491G	2N6491	TO-220 (Pb-Free)	50 Units / Rail

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

### TO-220 CASE 221A-09 ISSUE AJ

DATE 05 NOV 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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