

CIPOS™ Mini IM535

IM535-U6D/IM535-U6DS

Description

The CIPOS™ IM535 product family offers the chance for integrating various power and control components to increase reliability and optimize PCB size and system cost. It is designed to control three-phase motors in variable speed drives. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also less EMI and overload protection. To deliver excellent electrical performance, Infineon's leading-edge TRENCHSTOP™ IGBTs and anti-parallel diodes are combined with an optimized SOI gate driver.

Features

Package

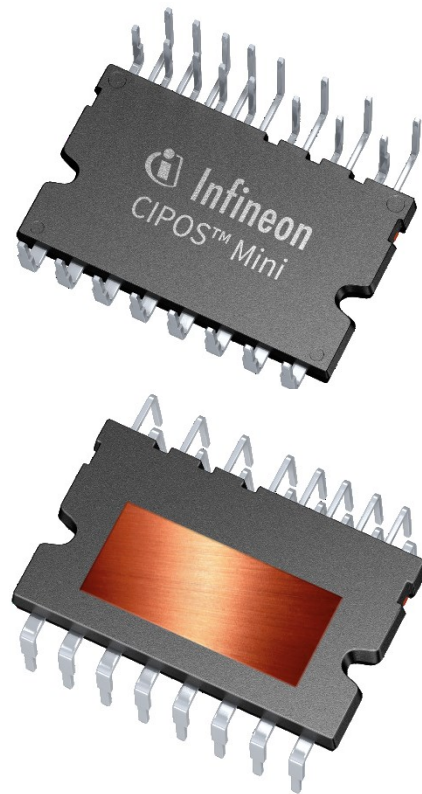
- Fully isolated dual in-line molded module
- Very low thermal resistance due to DCB substrate
- Lead-free terminal plating; RoHS compliant

Inverter

- TRENCHSTOP™ IGBTs for inverter
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative V_s potential up to -11 V for signal transmission at $V_{BS} = 15$ V
- Integrated bootstrap functionality
- Over-current shutdown
- Built-in NTC thermistor for temperature monitor
- Under-voltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Sleep function
- Cross-conduction prevention
- All of 6 switches turn off during protection

Potential applications

- Home appliances, low power motor drives



Product validation

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product Information

| Base Part Number | Package Type | Standard Pack | | Remarks |
|------------------|--------------|---------------|---------|--------------------|
| | | Form | MOQ | |
| IM535-U6D | DIP 36x21D | 14 pcs / Tube | 280 pcs | |
| IM535-U6DS | DIP 36x21D | 14 pcs / Tube | 280 pcs | Extended stand-off |

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1 Internal Electrical Schematic

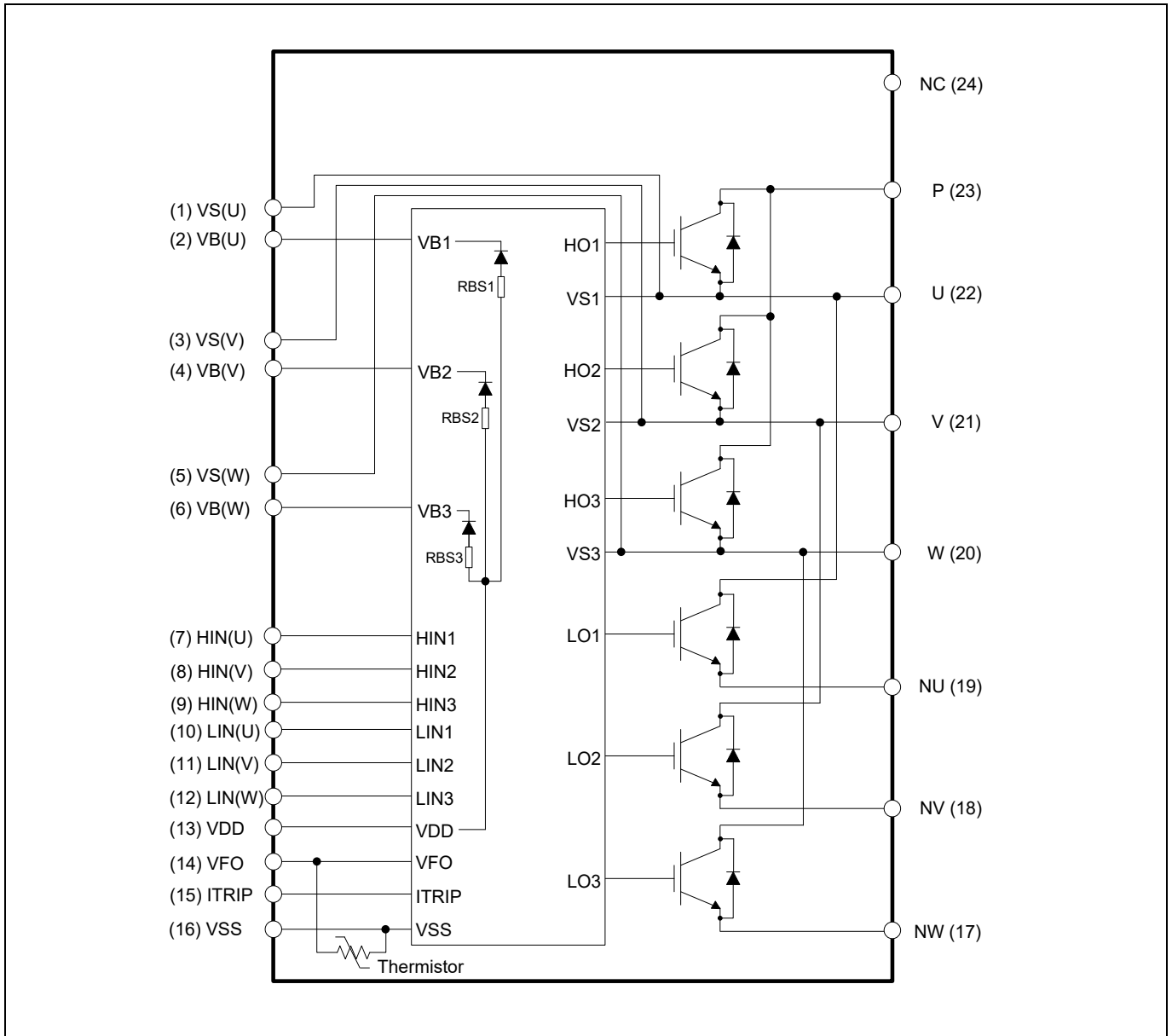


Figure 1 Internal electrical schematic

Pin Description

2 Pin Description

2.1 Pin Assignment

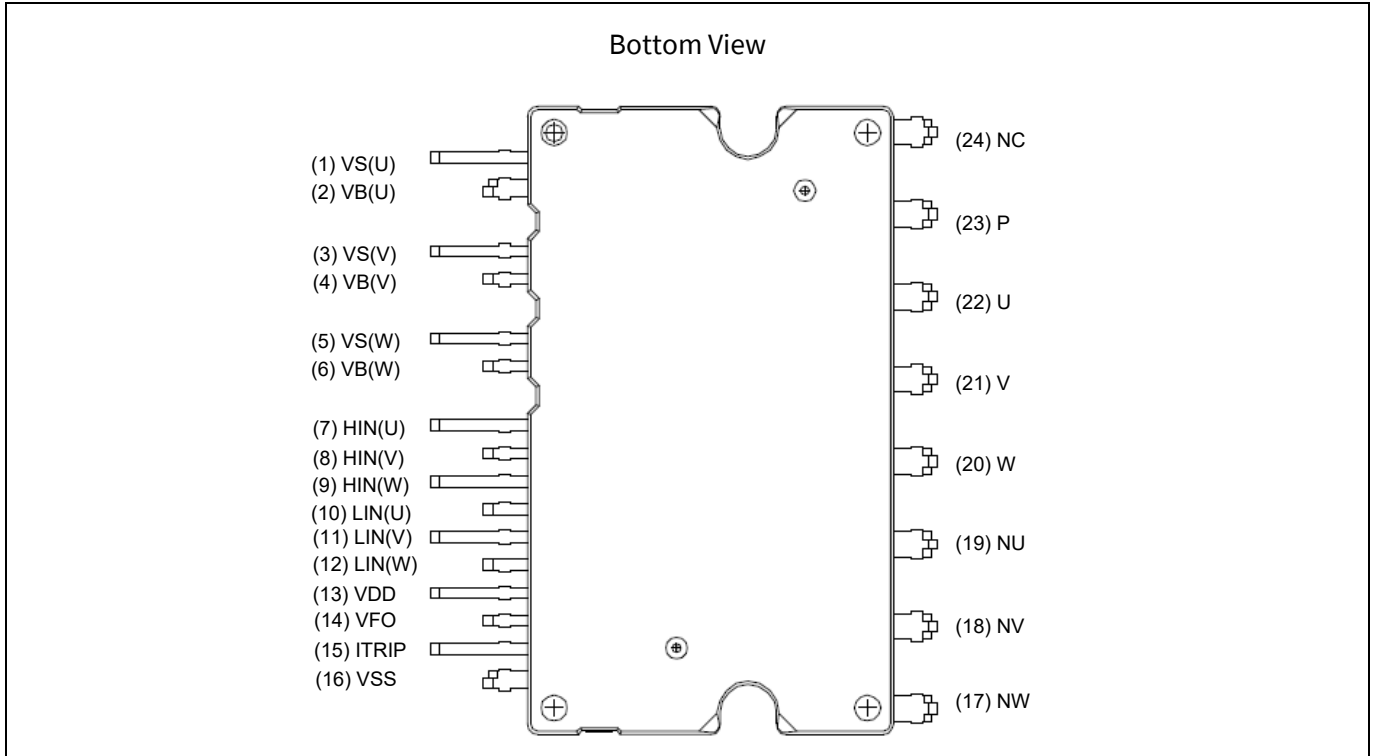


Figure 2 Pin configuration

Table 2 Pin assignment

| Pin Number | Pin name | Pin Description |
|------------|-------------------|---|
| 1 | V _{S(U)} | U-phase high-side floating IC supply offset voltage |
| 2 | V _{B(U)} | U-phase high-side floating IC supply voltage |
| 3 | V _{S(V)} | V-phase high-side floating IC supply offset voltage |
| 4 | V _{B(V)} | V-phase high-side floating IC supply voltage |
| 5 | V _{S(W)} | W-phase high-side floating IC supply offset voltage |
| 6 | V _{B(W)} | W-phase high-side floating IC supply voltage |
| 7 | HIN(U) | U-phase high-side gate driver input |
| 8 | HIN(V) | V-phase high-side gate driver input |
| 9 | HIN(W) | W-phase high-side gate driver input |
| 10 | LIN(U) | U-phase low-side gate driver input |
| 11 | LIN(V) | V-phase low-side gate driver input |
| 12 | LIN(W) | W-phase low-side gate driver input |
| 13 | V _{DD} | Low-side control supply |
| 14 | V _{FO} | Fault output / temperature monitor |
| 15 | ITRIP | Over-current shutdown input |
| 16 | V _{SS} | Low-side control negative supply |
| 17 | NW | W-phase low-side emitter |

Pin Description

| Pin Number | Pin name | Pin Description |
|------------|----------|----------------------------|
| 18 | NV | V-phase low-side emitter |
| 19 | NU | U-phase low-side emitter |
| 20 | W | Motor W-phase output |
| 21 | V | Motor V-phase output |
| 22 | U | Motor U-phase output |
| 23 | P | Positive bus input voltage |
| 24 | NC | No connection |

2.2 Pin Description

HIN(U, V, W) and LIN(U, V, W) (Low-side and high-side control pins, Pin 7 - 12)

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 5 kΩ is internally provided to pre-bias input during supply start-up, and a zener clamp is provided to protect the pin. Negative pulses down to an absolute minimum of -5.5 V are allowed that offers an outstanding robustness. Input Schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses shorter than the filter time $t_{FIL,IN}$. The Figure 4 describes how the filter works. An input pulse-width shorter than 1 μs is not recommended.

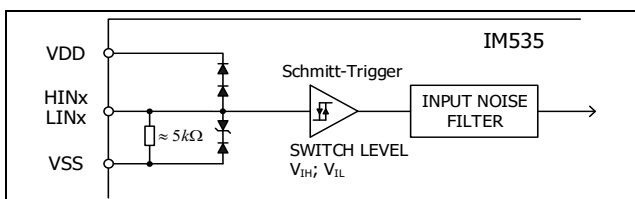


Figure 3 Input pin structure

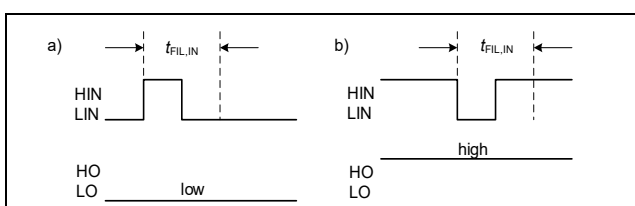


Figure 4 Input filter timing diagram

The integrated gate driver additionally provides a shoot-through prevention capability that avoids the simultaneous on-states of the same leg (i.e.

HO1 and LO1, HO2 and LO2, HO3 and LO3). When both inputs of the same leg are activated, only formerly activated one is remained activated so that the leg is kept steadily in a safe state. A minimum deadtime insertion of typically 360 ns is also provided by driver, in order to reduce cross-conduction of the IGBTs.

V_{F0} (Fault-output and NTC, Pin 14)

The V_{F0} pin indicates a module failure in case of under voltage at pin V_{DD} or in case of triggered over-current detection at ITRIP. An external pull-up resistor is required.

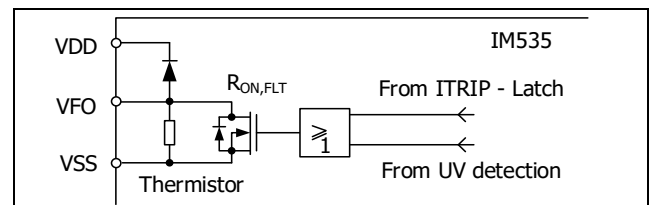


Figure 5 Internal circuit at pin V_{F0}

The sleep function is activated after each trigger of ITRIP or under-voltage lockout. A new edge input signal is mandatory to activate gate drives after fault-clear time as shown in Figure 10.

ITRIP (Over-current detection function, Pin 15)

The IM535 product family provides an over-current detection function by connecting the ITRIP input with the IGBT current feedback. The ITRIP comparator threshold (typ. 0.525 V) is referenced to V_{SS}. An input noise filter ($t_{ITRIPMIN}$ = typ. 300 ns) prevents the driver to detect false over-current events.

Over-current detection generates a shutdown of outputs of the gate driver. Fast track shutdown

Pin Description

function allows low-side outputs to be turned off faster than high side outputs about 200 ns. The fault-clear time is set to minimum 100 μ s.

V_{DD} , V_{SS} (Low-side control supply and reference, Pin 13, 16)

V_{DD} is the control supply and it provides power both to input logic and to output stage. Input logic is referenced to V_{SS} ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+} = 12.4$ V is present.

The gate driver shuts down all the outputs, when the V_{DD} supply voltage is below $V_{DDUV-} = 11.5$ V. This prevents the IGBTs from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B (U, V, W) and V_S (U, V, W) (High-side supplies, Pin 1 - 6)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to V_{SS} following the high-side IGBT emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+} = 11.5$ V and a falling threshold of $V_{BSUV-} = 10.7$ V.

V_S (U, V, W) provide a high robustness against negative voltage in respect of V_{SS} of -50 V transiently. This ensures very stable designs even under harsh conditions.

NW, NV, NU (Low-side emitter, Pin 17 - 19)

The low-side emitters are available for current measurement of each phase leg. It is recommended to keep the connection to pin V_{SS} as short as possible to avoid unnecessary inductive voltage drops.

W, V, U (High-side emitter and low-side collector, Pin 20 - 22)

These pins are connected to motor U, V, W input pins

P (Positive bus input voltage, Pin 23)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

Absolute Maximum Ratings

3 Absolute Maximum Ratings

($V_{DD} = 15\text{ V}$, $V_{GE} = 15\text{ V}$ and $T_J = 25^\circ\text{C}$, if not stated otherwise)

3.1 Module Section

| Description | Symbol | Condition | Value | Unit |
|--------------------------------|-----------|--------------------------------|-----------|------------------|
| Storage temperature range | T_{STG} | | -40 ~ 125 | $^\circ\text{C}$ |
| Operating case temperature | T_C | Refer to Figure 7 | -40 ~ 125 | $^\circ\text{C}$ |
| Operating junction temperature | T_J | | -40 ~ 150 | $^\circ\text{C}$ |
| Isolation test voltage | V_{ISO} | 1 min, RMS, $f = 60\text{ Hz}$ | 2000 | V |

3.2 Inverter Section

| Description | Symbol | Condition | Value | Unit |
|---|-----------------|--|----------|---------------|
| Max. blocking voltage | V_{CES} | $I_C = 250\ \mu\text{A}$ | 600 | V |
| DC link supply voltage of P-N | V_{PN} | Applied between P-N | 450 | V |
| DC link supply voltage (surge) of P-N | $V_{PN(surge)}$ | Applied between P-N | 500 | V |
| Continuous collector current | I_C | $T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$ | ± 30 | A |
| | | $T_C = 80^\circ\text{C}$, $T_J < 150^\circ\text{C}$ | ± 22 | |
| Maximum peak collector current | $I_{C(peak)}$ | $T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$ less than 1 ms | ± 60 | A |
| Power dissipation per IGBT | P_{tot} | | 83.3 | W |
| Short circuit withstand time ¹ | t_{SC} | $V_{DC} \leq 400\text{V}$, $T_J = 150^\circ\text{C}$ | 5 | μs |

3.3 Control Section

| Description | Symbol | Condition | Value | Unit |
|--|-----------|-----------|-------------------|------|
| High-side offset voltage | V_S | | 600 | V |
| Repetitive peak reverse voltage of bootstrap diode | V_{RRM} | | 600 | V |
| Module supply voltage | V_{DD} | | -1 ~ 20 | V |
| High-side floating supply voltage (V_B reference to V_S) | V_{BS} | | -1 ~ 20 | V |
| Input voltage(LIN, HIN, ITRIP) | V_{IN} | | -1 ~ $V_{DD}+0.3$ | V |

¹ Allowed number of short circuits: < 1000; time between short circuits: > 1 s.

4 Thermal Characteristics

| Description | Symbol | Condition | Value | | | Unit |
|---|--------------|--|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Single IGBT thermal resistance, junction to case | R_{thJC} | Low-side U-phase (See Figure 7 for T_c measurement point) | | | 1.49 | K/W |
| Single diode thermal resistance, junction to case | $R_{thJC,D}$ | Low-side U-phase | | | 2.18 | K/W |

Recommended Operation Conditions

5 Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

| Description | Symbol | Value | | | Unit |
|---|--------------------------------------|----------|--------|--------|------------|
| | | Min. | Typ. | Max. | |
| DC link supply voltage of P-N | V_{PN} | 0 | 300 | 450 | V |
| Low-side supply voltage | V_{DD} | 13 | 15 | 17.5 | V |
| High-side floating supply voltage (V_B vs. V_S) | V_{BS} | 13 | - | 17.5 | V |
| Logic input voltages LIN, HIN, ITRIP | V_{IN} V_{ITRIP} | 0 | - | 5 | V |
| Inverter PWM carrier frequency | f_{PWM} | - | - | 20 | kHz |
| External deadtime between HIN and LIN | DT | 2 | - | - | μs |
| Voltage between $V_{SS} - N$ (including surge) | V_{COMP} | -5 | - | 5 | V |
| Minimum input pulse width | $PW_{IN(ON)}$ $PW_{IN(OFF)}$ | 1 | - | - | μs |
| Control supply variation | ΔV_{BS} , ΔV_{DD} | -1 -1 | - - | 1 1 | V/ μs |

Static Parameters

6 Static Parameters

($V_{DD} = 15\text{ V}$ and $T_J = 25^\circ\text{C}$, if not stated otherwise)

6.1 Inverter Section

| Description | Symbol | Condition | Value | | | Unit |
|-----------------------------------|---------------|---|-------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Collector-emitter voltage | $V_{CE(Sat)}$ | $I_C = 30\text{ A}, T_J = 25^\circ\text{C}$ $I_C = 30\text{ A}, T_J = 150^\circ\text{C}$ | - | 1.8 | 2.1 | V |
| | | | - | 2.05 | - | |
| Collector-emitter leakage current | I_{CES} | $V_{CE} = 600\text{ V}$ | - | - | 1 | mA |
| Diode forward voltage | V_F | $I_F = 30\text{ A}, T_J = 25^\circ\text{C}$ $I_F = 30\text{ A}, T_J = 150^\circ\text{C}$ | - | 1.95 | 2.35 | V |
| | | | - | 1.9 | - | |

6.2 Control Section

| Description | Symbol | Condition | Value | | | Unit |
|---|----------------------------|---|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| Logic "1" input voltage (LIN, HIN) | V_{IH} | | 1.7 | 2.0 | 2.3 | V |
| Logic "0" input voltage (LIN, HIN) | V_{IL} | | 0.7 | 0.9 | 1.1 | V |
| ITRIP positive going threshold | $V_{IT,TH+}$ | | 475 | 525 | 570 | mV |
| ITRIP input hysteresis | $V_{IT,HYS}$ | | 45 | 70 | - | mV |
| V_{DD} and V_{BS} supply under-voltage positive going threshold | V_{DDUV+} | | 11.5 | 12.4 | 13.1 | V |
| | V_{BSUV+} | | 10.6 | 11.5 | 12.2 | |
| V_{DD} and V_{BS} supply under-voltage negative going threshold | V_{DDUV-} | | 10.6 | 11.5 | 12.3 | V |
| | V_{BSUV-} | | 9.7 | 10.7 | 11.7 | |
| V_{DD} and V_{BS} supply under-voltage lockout hysteresis | V_{DDUVH} V_{BSUVH} | | 0.5 | 0.9 | - | V |
| Quiescent V_{Bx} supply current (V_{Bx} only) | I_{QBS} | $H_{IN} = 0\text{ V}$ | - | - | 300 | μA |
| Quiescent V_{DD} supply current (V_{DD} only) | I_{QDD} | $L_{IN} = 0\text{ V}, H_{INX} = 5\text{ V}$ | - | - | 1.1 | mA |
| Input bias current for LIN, HIN | I_{IN+} | $V_{IN} = 5\text{ V}$ | - | 1.1 | 1.7 | mA |
| Input bias current for ITRIP | I_{ITRIP+} | $V_{ITRIP} = 5\text{ V}$ | - | 68 | 185 | μA |
| Input bias current for V_{FO} | I_{FO} | $V_{FO} = 5\text{ V}, V_{ITRIP} = 0\text{ V}$ | - | 60 | - | μA |
| V_{FO} output voltage | V_{FO} | $I_{FO} = 10\text{ mA}, V_{ITRIP} = 1\text{ V}$ | - | 0.35 | - | V |
| Bootstrap diode forward voltage | V_{F_BSD} | $I_F = 0.3\text{ mA}$ | - | 1.0 | - | V |
| Bootstrap diode resistance | R_{BSD} | Between $V_{F1} = 4\text{ V}$ and $V_{F2} = 5\text{ V}$ | - | 37 | - | Ω |

Dynamic Parameters

7 Dynamic Parameters

($V_{DD} = 15\text{ V}$ and $T_J = 25^\circ\text{C}$, if not stated otherwise)

7.1 Inverter Section

| Description | Symbol | Condition | Value | | | Unit |
|--|--------------|---|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| Turn-on propagation delay time | t_{on} | $V_{LIN, HIN} = 5\text{ V}$, $I_C = 30\text{ A}$, $V_{DC} = 300\text{ V}$ | - | 725 | - | ns |
| Turn-on rise time | t_r | | - | 85 | - | ns |
| Turn-on switching time | $t_{c(on)}$ | | - | 295 | - | ns |
| Reverse recovery time | t_{rr} | | - | 320 | - | ns |
| Turn-off propagation delay time | t_{off} | $V_{LIN, HIN} = 0\text{ V}$, $I_C = 30\text{ A}$, $V_{DC} = 300\text{ V}$ | - | 900 | - | ns |
| Turn-off fall time | t_f | | - | 25 | - | ns |
| Turn-off switching time | $t_{c(off)}$ | | - | 90 | - | ns |
| Short circuit propagation delay time | t_{SCP} | From $V_{IT, TH+}$ to 10% I_{SC} | - | 1550 | - | ns |
| IGBT turn-on energy (includes reverse recovery of diode) | E_{on} | $V_{DC} = 300\text{ V}$, $I_C = 30\text{ A}$ | - | 1430 | - | μJ |
| | | $T_J = 25^\circ\text{C}$ | - | 1820 | - | |
| IGBT turn-off energy | E_{off} | $V_{DC} = 300\text{ V}$, $I_C = 30\text{ A}$ | - | 495 | - | μJ |
| | | $T_J = 150^\circ\text{C}$ | - | 730 | - | |
| Diode recovery energy | E_{rec} | $V_{DC} = 300\text{ V}$, $I_C = 30\text{ A}$ | - | 105 | - | μJ |
| | | $T_J = 150^\circ\text{C}$ | - | 245 | - | |

7.2 Control Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---------------|---|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| Input filter time ITRIP | t_{ITRIP} | $V_{ITRIP} = 1\text{ V}$ | - | 530 | - | ns |
| Input filter time at LIN, HIN for turn on and off | $t_{FIL, IN}$ | $V_{LIN, HIN} = 0\text{ V}$ or 5 V | - | 290 | - | ns |
| Fault clear time after ITRIP-fault | t_{FLTCLR} | | 100 | 280 | - | μs |
| ITRIP to fault propagation delay | t_{FLT} | $V_{LIN, HIN} = 0$ or $V_{LIN, HIN} = 5\text{ V}$, $V_{ITRIP} = 1\text{ V}$ | - | 680 | 1000 | ns |
| Internal deadtime | DT_{IC} | | - | 360 | - | ns |
| Matching propagation delay time (on and off) all channels | M_T | External dead time > 500 ns | - | 20 | - | ns |

Thermistor

8 Thermistor

| Description | Condition | Symbol | Value | | | Unit |
|---|--------------------------------|-----------|-------|------|------|------------------|
| | | | Min. | Typ. | Max. | |
| Resistance | $T_{NTC} = 25^{\circ}\text{C}$ | R_{NTC} | - | 85 | - | $\text{k}\Omega$ |
| B-constant of NTC (negative temperature coefficient) thermistor | | B(25/100) | - | 4092 | - | K |

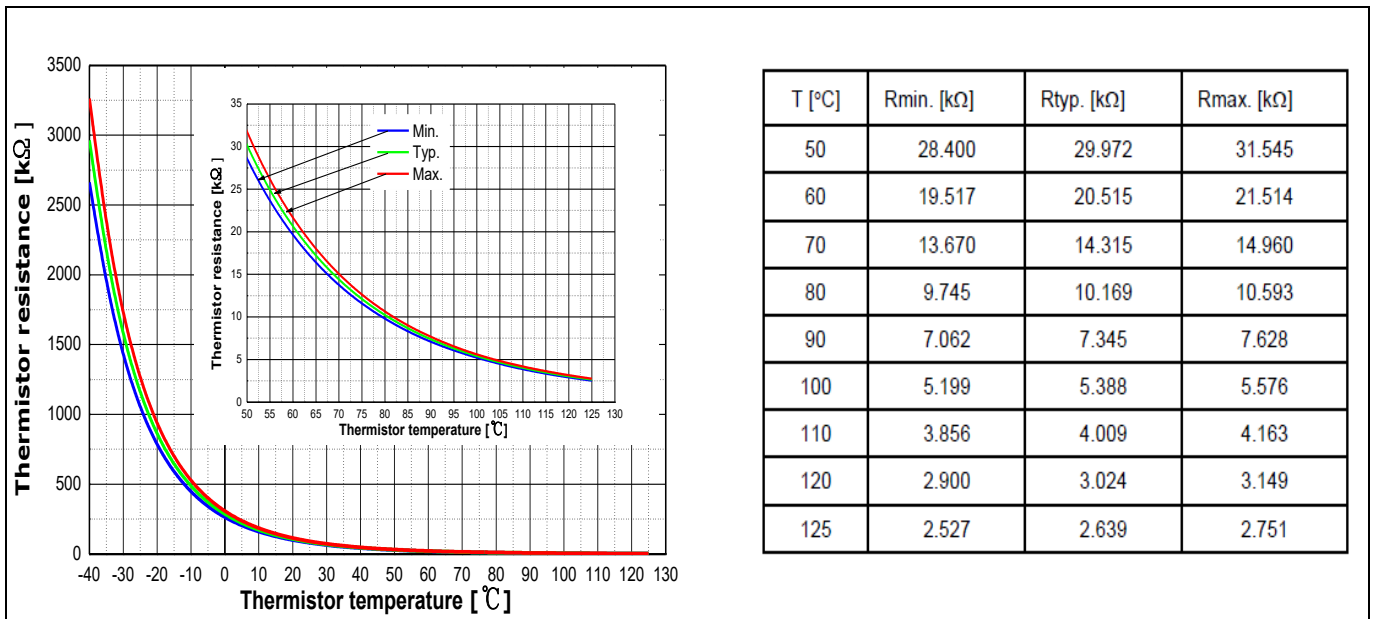


Figure 6 Thermistor resistance – temperature curve and table

(For more information, please refer to the application note)

9 Mechanical Characteristics and Ratings

| Description | Condition | Value | | | Unit |
|----------------------------------|---------------------|-------|------|------|------|
| | | Min. | Typ. | Max. | |
| Comparative tracking index (CTI) | | 600 | - | - | V |
| Mounting torque | M3 screw and washer | 0.49 | | 0.78 | Nm |
| Backside curvature | Refer to Figure 8 | -50 | - | 100 | μm |
| Weight | | - | 6.58 | - | g |

10 Qualification Information

| | | |
|--|--|--------------------------|
| UL certification | File number: E314539 | |
| Moisture sensitivity level (SOP23 only) | - | |
| RoHS compliant | Yes (Lead-free terminal plating) | |
| ESD | HBM(human body model) class as per JESD22-A114 | 2 (> 2000 V to < 4000 V) |
| | CDM(charged device model) class as per JESD22-C101 | C3 (>= 1000 V) |

11 Diagrams and Tables

11.1 T_c Measurement Point

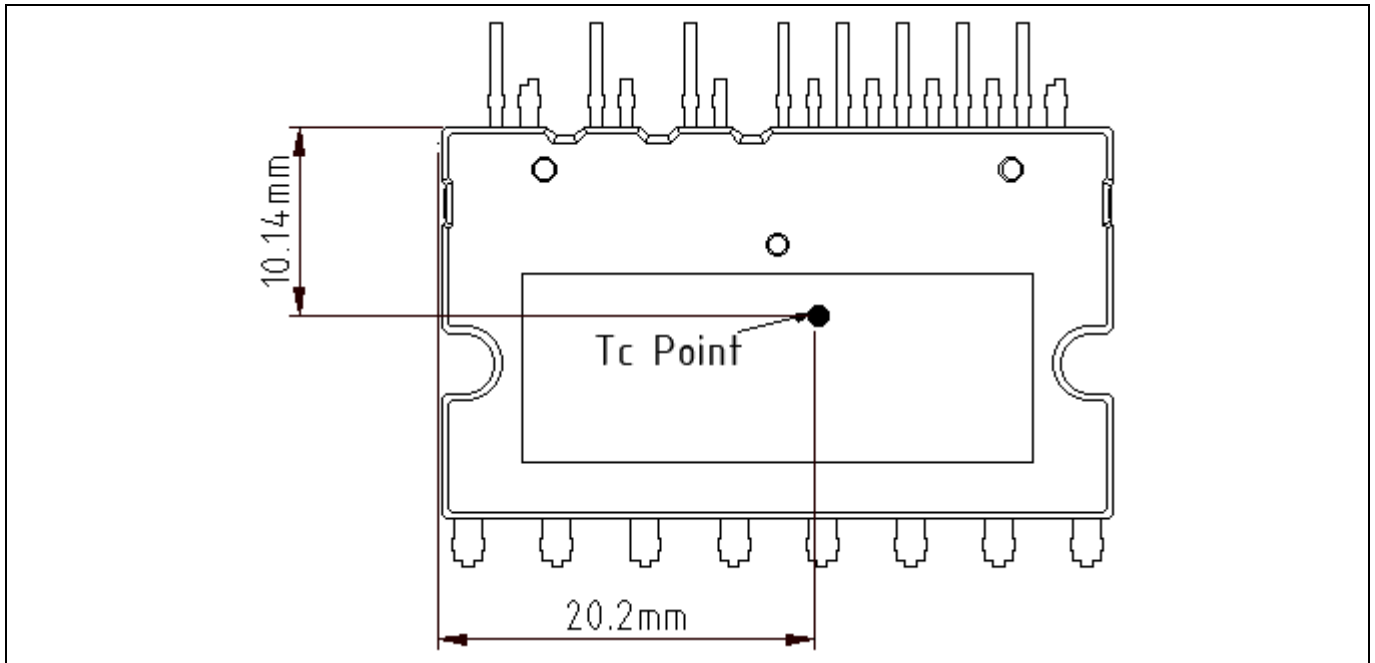


Figure 7 T_c measurement point¹

11.2 Backside Curvature Measurement Point

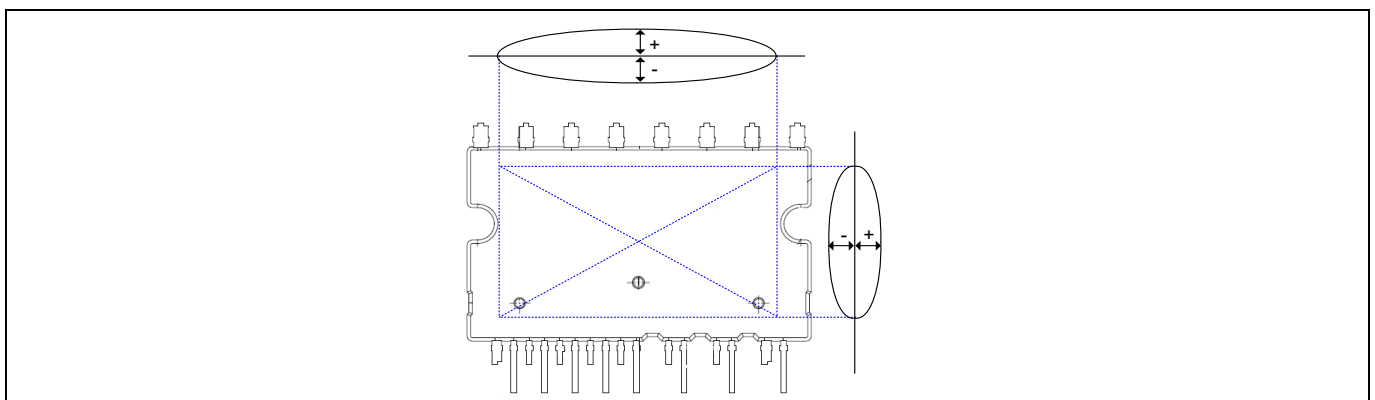


Figure 8 Backside curvature measurement position

¹Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching Time Definition

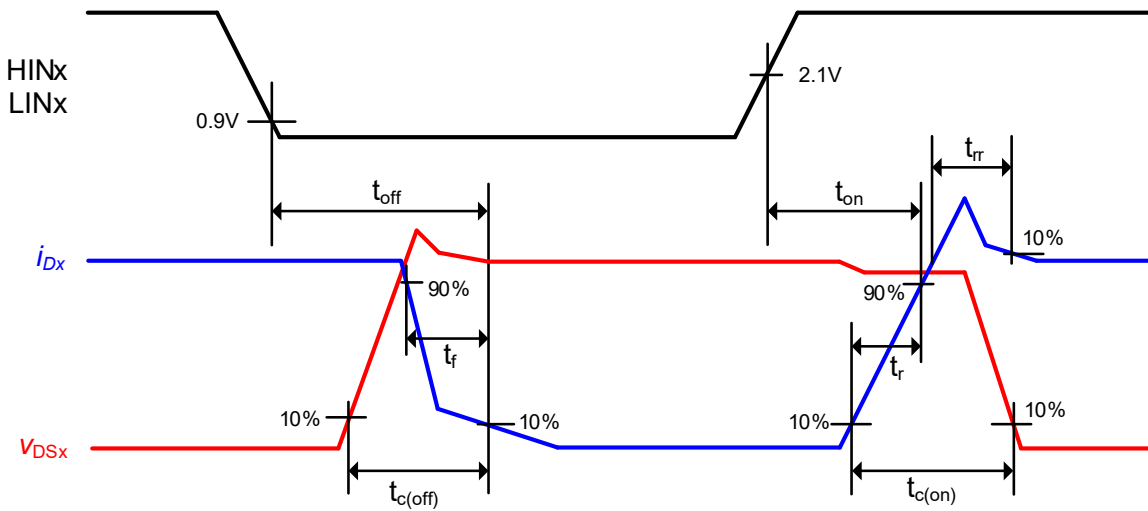


Figure 9 Switching time definition

11.4 Sleep function timing diagram

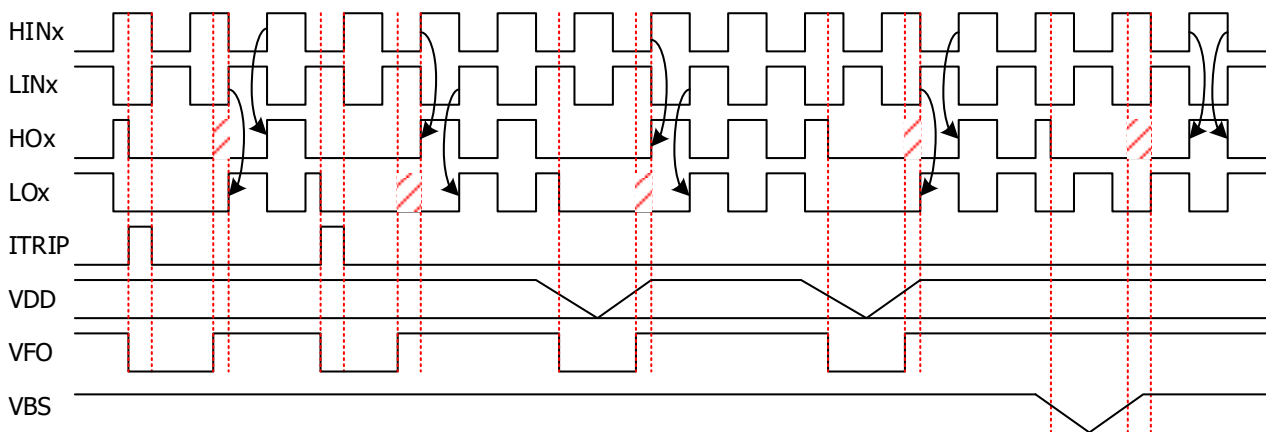


Figure 10 Sleep function timing diagram

12 Application Guide

12.1 Typical Application Schematic

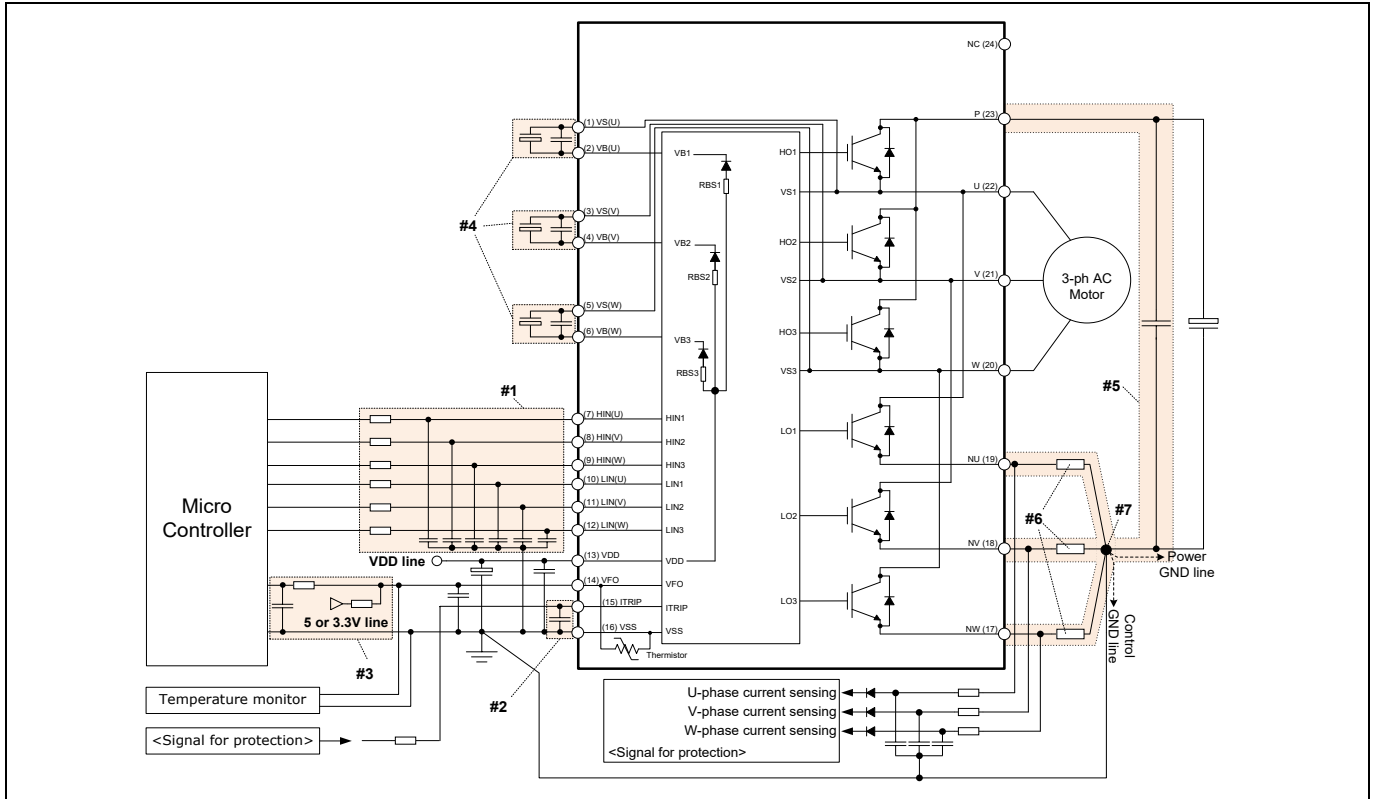


Figure 11 Typical application circuit

- #1 Input circuit
 - RC filter can be used to reduce input signal noise. (100 Ω, 1 nF)
 - The capacitors should be located close to the IPM (to V_{SS} terminal especially).
- #2 ITRIP circuit
 - To prevent a mis operation of protection function, RC filter is recommended.
 - The capacitor should be located close to ITRIP and V_{SS} terminals.
- #3 V_{F0} circuit
 - V_{F0} pin is open drain configuration. This terminal should be pulled up to the bias voltage of the 5 V/3.3 V through a proper resistor.
 - It is recommended that RC filter is placed close to the controller.
- #4 V_B-V_S circuit
 - Capacitors for high-side floating supply voltage should be placed close to V_B and V_S terminals.
- #5 Snubber capacitor
 - The wiring among the IPM, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor
 - SMD type shunt resistors are strongly recommended to minimize its internal stray inductance.
- #7 Ground pattern
 - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at one end of shunt resistor only for the same potential.

12.2 Performance Chart

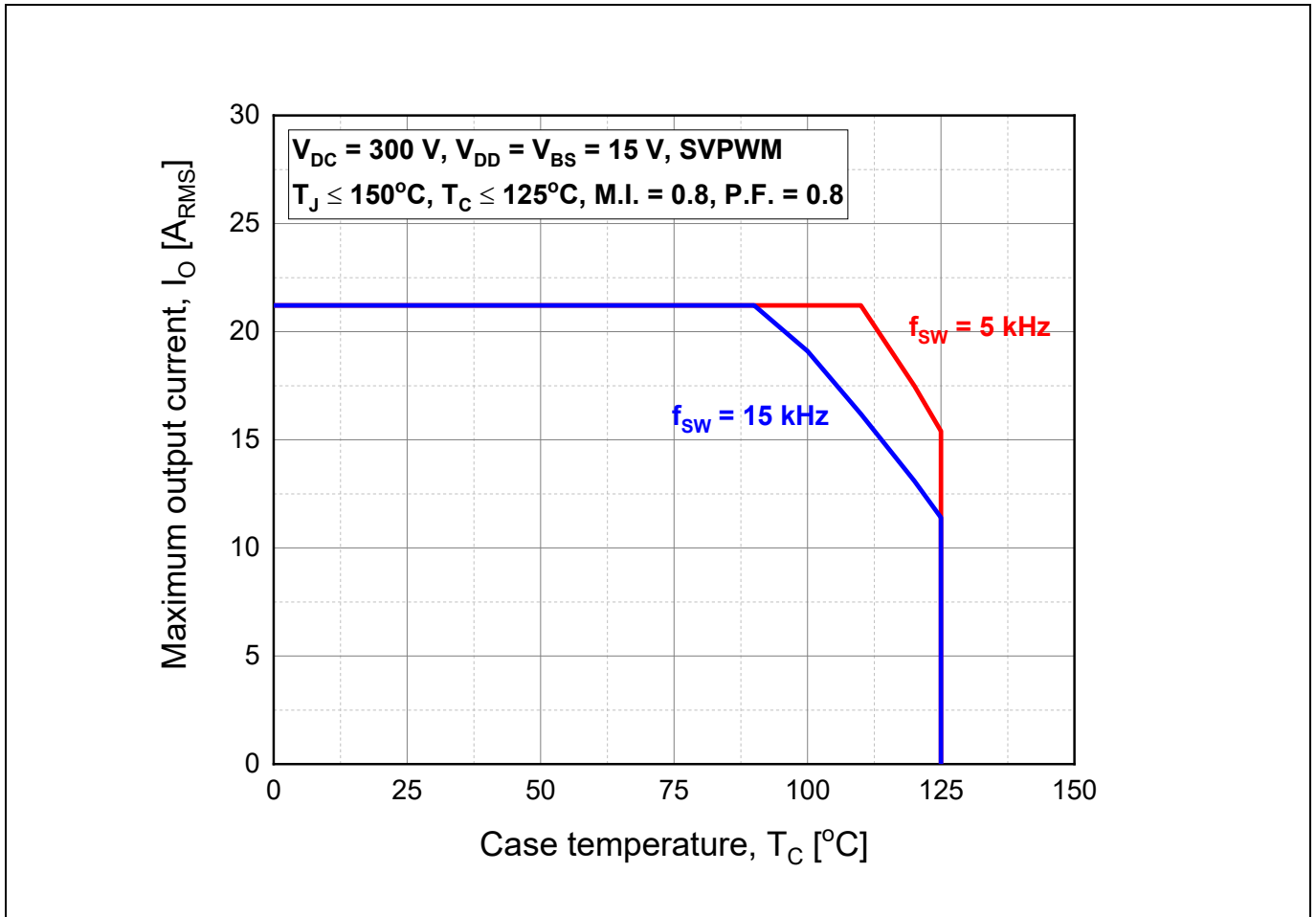


Figure 12 Maximum operating current SOA¹

¹This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

Package Outline

13 Package Outline

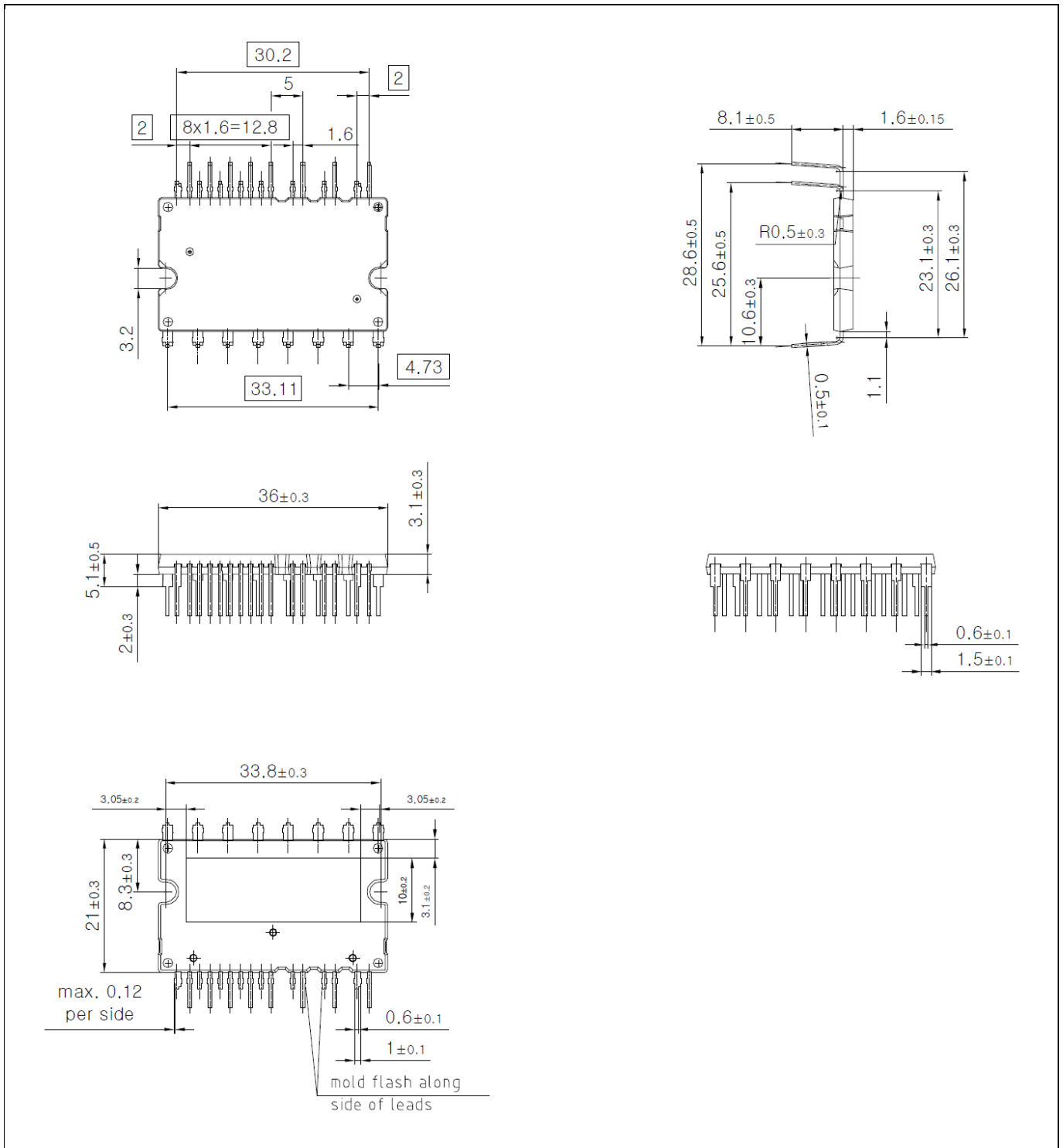


Figure 13 IM535-U6D

Package Outline

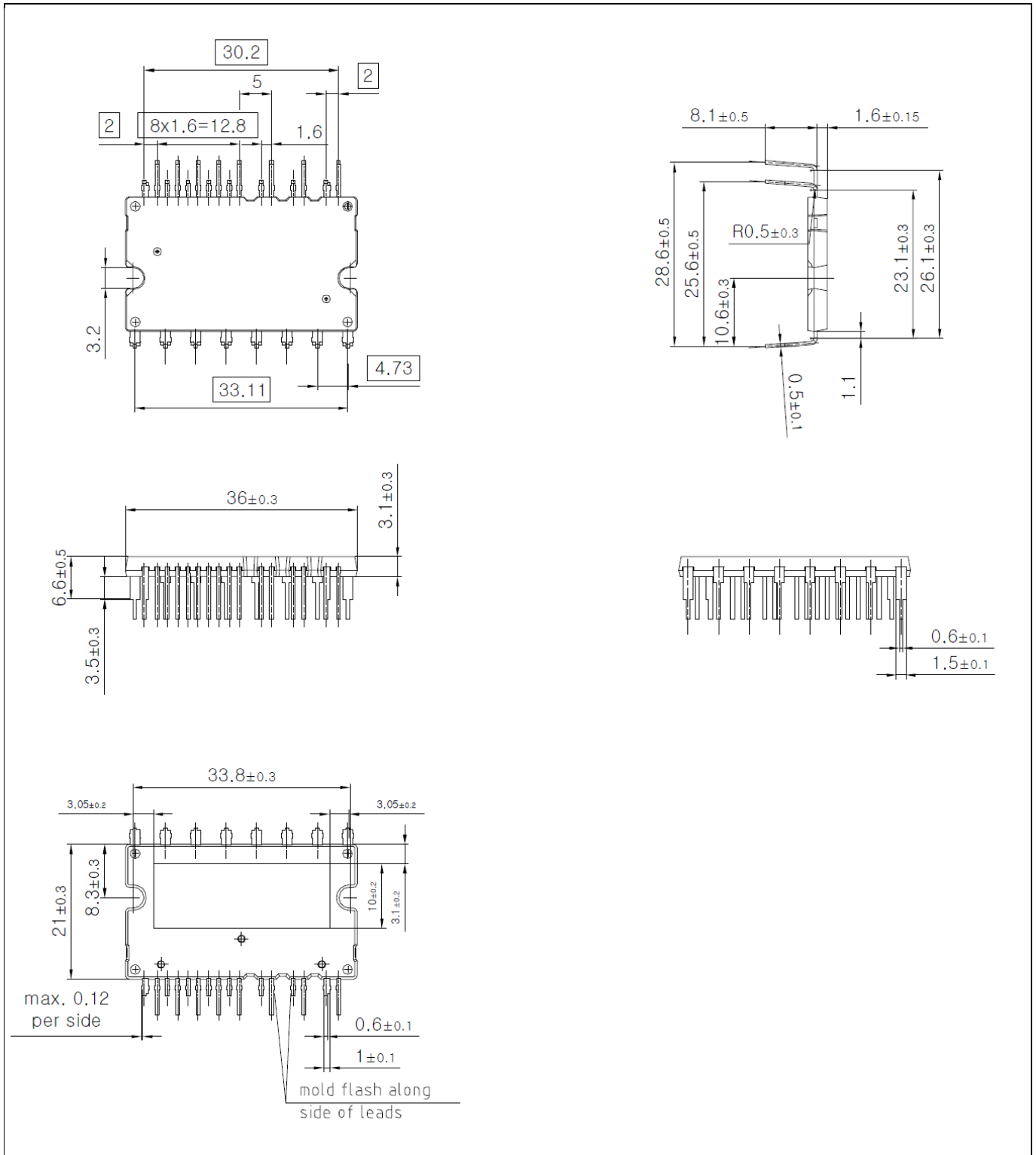


Figure 14 IM535-U6DS

Revision history

Revision history

| Document version | Date of release | Description of changes |
|-------------------------|------------------------|-------------------------------|
| Version 2.0 | 2020-05-07 | Initial release |
| | | |
| | | |

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