

System Lens Drivers

μ-step System Lens Driver for Digital Still Cameras

BU24020GU

General Description

BU24020GU is a system Lens Driver which is capable of μ -step driving and possible to configure a high precision and low noise lens driver system. This device performs μ -step driving control internally and can reduce a load of CPU.

Features

- Built-in 4 Channel Drivers
 - 1ch to 4ch: Voltage Control Type H-Bridge (for 2 STM Systems)

DVDD

(M)

DVDD

DVSS

OUT3A

OUT3B

OUT4A

OUT4B

- Built-in 2 Channel PI Driver Circuits
- Built-in PLL Circuit

Applications

Digital Still Camera

Key Specifications

- Digital Power Supply Voltage: 2.7 V to 3.6 V
 Driver Power Supply Voltage: 2.7 V to 5.5 V
- Input/Output Current (1ch to 4ch):
 - 500 mA (Max)
 - Clock Operating Frequency: 1 MHz to 28 MHz
 - ON-Resistance (1ch to 4ch): 1.5Ω (Typ)
- Operating Temperature Range: -20 °C to +85 °C

Package

VCSP85H2 (24 pin)

W (Typ) x D (Typ) x H (Max)





Typical Application Circuit

OProduct structure : Silicon integrated circuit OThis product has no designed protection against radioactive rays

 STATE1 STATE2

SDAT#

Main Host

SCLK

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Pin Configuration



Pin Description

Pin No.	Pin Name	Power Supply	Function	Pin No.	Pin Name	Power Supply	Function
A1	OUT1A	MVCC12	1ch driver A output	C4	SDATA	DVDD	SDATA logic input
A2	MVCC12	-	1ch,2ch driver power supply	C5	DVDD	-	Digital power supply
A3	OUT2A	MVCC12	2ch driver A output	D1	MGND12	-	1ch, 2ch driver ground
A4	OUT2B	MVCC12	2ch driver B output	D2	DVSS	-	Ground
A5	FCLK	DVDD	FCLK logic input	D3	SCLK	DVDD	SCLK logic input
B1	PIOUT1	DVDD	PI driver output 1	D4	PIOUT2	DVDD	PI driver output 2
B3	STATE2	DVDD	STATE2 logic input/output	D5	OUT3B	MVCC34	3ch driver B output
B4	CSB	DVDD	CSB logic input	E1	MGND34	-	3ch, 4ch driver ground
B5	SOUT	DVDD	SOUT logic output	E2	OUT4B	MVCC34	4ch driver B output
C1	OUT1B	MVCC12	1ch driver B output	E3	OUT4A	MVCC34	4ch driver A output
C2	STATE1	DVDD	STATE1 logic input/output	E4	MVCC34	-	3ch, 4ch driver power supply
C3	TEST	DVDD	TEST logic input	E5	OUT3A	MVCC34	3ch driver A output

Block Diagram



Description of Blocks

Stepping Motor Driver (1ch to 4ch Driver) Built-in PWM type stepping motor drivers.

Maximum 2 stepping motors can be driven independently.

Built-in D-class type voltage feedback circuit.

3ch/4ch drivers can also drive DC motor or voice coil motor individually.

(1) Control

Both Clock IN and Autonomous control are possible.

(a)Clock IN Control

Set the registers for the stepping motor control.

Stepping motor rotates in synchronization with clock input to the STATE1 pin and/or the STATE2 pin.

Mode of stepping motor control is selectable from µ-step, 1-2 phase excitation and 2 phase excitation. And the number of edge for electrical angle cycle is selectable from 4, 8, 32, 64, 128, 256, 512 or 1024.



(b)Autonomous Control

Stepping motor rotates by setting the registers to drive the stepping motor.

It is possible to output from serial output (the SOUT pin) the status information which are operation command status (excecution:1, stop: 0), cache register status and motor position, and to output signal (MO output) from the STATE1 pin and the STATE2 pin in synchronization with motor operation.

Mode of stepping motor control is selectable from µ-step (1024 portion), 1-2 phase excitation and 2 phase excitation. Built-in Cache register enables to set next operation commands during motor operation, and continuous operation is possible.



Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	DVDD	-0.3 to +4.5	V	
Supply voltage	MVCC	-0.3 to +7.0	V	MVCC12, MVCC34,
Input Voltage	V _{IN}	-0.3 to supply voltage+0.3	V	
Input / Output Current (Note 1)	L.	500	mA	MVCC12, MVCC34
	١N	50	mA	PIOUT1, PIOUT2
Maximum Junction Temperature	Tjmax	125	°C	
Storage Temperature Range	Tstg	-55 to +125	°C	
Power Dissipation ^(Note 2)	Pd	0.80	W	

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuity. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum ratings. Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating. (Note 1) Must not exceed Pd.

(Note 1) must not exceed 1 d. (Note 2) When use at Ta=25 °C or more, derate 8 mW per 1 °C (At mounting 50 mm x 58 mm x 1.75 mm glass epoxy board.)

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit	Remark
Digital Power Supply Voltage	DVDD	2.7	3.0	3.6	V	DVDD≤MVCC
Driver Power Supply Voltage	MVCC	2.7	5.0	5.5	V	MVCC12, MVCC34
Clock Operating Frequency	f _{FCLK}	1	-	28	MHz	Reference clock
Operating Temperature	Topr	-20	+25	+85	°C	

Electrical Characteristics

(Unless otherwise specified Ta=25 °C, DVDD=3.0 V, MVCC12=MVCC34=5.0 V)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions		
<current consumption=""></current>								
	I _{SSD}	-	50	95	μA	DVDD power supply CMD_RS = 0		
	I _{SSM}	-	0	10	μA	MVCC power supply CMD_RS = 0		
Operational Current	I _{DDD}	-	5	10	mA	DVDD power supply $CMD_RS = 1$ $f_{FCLK} = 24 MHz$ CLK_DIV setting: 0h No load		
<logic block=""></logic>								
Low-Level Input Voltage	VIL	DVSS	-	0.3 x DVDD	V			
High-Level Input Voltage	VIH	0.7 x DVDD	-	DVDD	V			
Low-Level Input Current	I⊫	0	-	10	μA	V _{IL} = DVSS		
High-Level Input Current	I _{IH}	0	-	10	μA	V _{IH} = DVDD		
Low-Level Output Voltage	V _{OL}	DVSS	-	0.2 x DVDD	V	I _{OL} = 1.0 mA		
High-Level Output Voltage	V _{OH}	0.8 x DVDD	-	DVDD	V	I _{OH} = 1.0 mA		
<pi circuit="" driver=""></pi>								
Output Voltage	V _{PIO}	-	0.15	0.5	V	I _{IH} = 30 mA		
<voltage 1ch="" 4ch="" block="" driver="" to=""></voltage>								
ON-Resistance	R _{ON}	-	1.5	2.0	Ω	$I_0 = \pm 100 \text{ mA}$ (sum of high and low sides)		
OFF-Leak Current	I _{oz}	-10	0	+10	μA	Output Hiz setting		
Accuracy of Average Voltage between Output Pins	VDIFF	-5	-	+5	%	different_output_voltage setting: 2Bh		

Typical Performance Curves

(Unless otherwise specified Ta=25 °C, DVDD=3.0 V, MVCC12=MVCC34=5.0 V)



Figure 1. Quiescent Current (DVDD) vs DVDD





Figure 3. Quiescent Current (MVCC) vs MVCC



Figure 4. Quiescent Current (MVCC) vs Temperature

Typical Performance Curves – continued

(Unless otherwise specified Ta=25 °C, DVDD=3.0 V, MVCC12=MVCC34=5.0 V)



Figure 8. Output Voltage vs DVDD (PI Driver Circuit)

Setting (Voltage Driver Block)

Timing Chart

(Unless otherwise specified Ta=25 °C, DVDD=3.0 V)

Parameter	Symbol	Design Value
SCLK Input Cycle	t _{SCLK}	100 ns or more
SCLK Low-Level Input Time	t _{SCLKL}	50 ns or more
SCLK High-Level Input Time	t _{SCLKH}	50 ns or more
SDATA Setup Time	t ssdata	50 ns or more
SDATA Hold Time	t _{HSDATA}	50 ns or more
CSB High-Level Input Time	t _{CSBH}	380 ns or more
CSB Setup Time	t _{SCSB}	50 ns or more
CSB Hold Time	t _{HCSB}	50 ns or more
FCLK Input Cycle	t _{FCLK}	36 ns or more
FCLK Low-Level Input Time	t _{FCLKL}	18 ns or more
FCLK High-Level Input Time	t _{FCLKH}	18 ns or more



(Note 3) FCLK is asynchronous with SCLK. (Note 4) The duty of FCLK and SCLK is arbitrary after observing the above table.

Serial Interface

Control command is 16-bit serial input (MSB first) and is sent via the CSB, the SCLK, and the SDATA pins. Higher 4 bits specify addresses and lower 12 bits specify data. Data of each bit is sent via the SDATA pin and taken at a rising edge of SCLK. The Data taken during CSB 'L' period is valid and is written in register at a rising edge of CSB. SOUT output is 12bit data and synchronous with a falling edge of SCLK.



Register Map^(Note 5,6,7,8)

<u> </u>															
	Addre	ss[3:0]			Data[11:0]										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	A_Mo	de[1:0]		A_SEL[2:0]	A_different_output_voltage[6:0]						
				0	0	0	0		A_Cycle[5:0] 0				0		
				0	0	1	0		A_Cycle[13:6]				•		
0	0	0	1	0	1	1	0	A_BEXC	0	0	A_BSL	A_AEXC	0	0	A_ASL
				1	1	1	0	0	0	A_PC	S[1:0]	0	0	A_PS	A_Stop
0	0	1	0	A_EN	A_RT		•	•		A_Pul	se[9:0]	•	•		•
0	0	1	1	A_ACT	A_BUSY	B_ACT	B_BUSY	L	L	L	L	L	L	L	L
0	1	0	0	B_Mo	de[1:0]		B_SEL[2:0] B_different_output_voltage[6:0]						•		
				0	0	0	0	B_Cycle[5:0] 0 (0			
				0	0	1	0	B_Cycle[13:6]				•			
				0	1	1	0	B_BEXC	0	0	B_BSL	B_AEXC	0	0	B_ASL
0	1	0	1	1	0	0	0	0	0	3_CH	DP[1:0]	0	0	4_CH	DP[1:0]
				1	0	1	3_State	_CTL[1:0]			3_F	WM_Duty	[6:0]		
				1	1	0	4_State	_CTL[1:0]			4_F	WM_Duty	[6:0]		
				1	1	1	0	0	0	B_PC	S[1:0]	0	0	B_PS	B_Stop
0	1	1	0	B_EN	B_RT					B_Pul	se[9:0]				
0	1	1	1		A_POSI	FION[9:6]			B_POSI	TION[9:6]		L	L	L	L
1	0	1	1	0	0	0	0	0	0	Edge	0	0	0	B_CTL	A_CTL
1	1	0	0	0	0	Chopp	ing[1:0]	CacheM 0 0 CLK_EN CLK_DIV[3:0]				•			
1	1	0	1	0	0	0	0	0	0	0	0	0	0	PI_CTL2	PI_CTL1
1	1	1	0	1	1	0	0	0	0	0	STB	0	0	STM_RS	CMD_RS
Othe	er than	those a	bove	Setting prohibited											

(Note 5) The notations A and B in the register map correspond to Ach and Bch respectively. Ach is defined as 1ch and 2ch driver output, Bch as 3ch and 4ch driver output.

(Note 6) After power on reset, the initial settings are stored in all registers.

(Note 7) The data at register address 4'b0011 and 4'b0111 (ACT, BUSY, A_POSITION[9:6], B_POSITION[9:6]) is internal register value and is output from the SOUT pin. 'L' in the above table indicates Low output.

(Note 8) Regarding Mode, different_output_voltage, Cycle, EN, and RT registers, the data written right before the access to the Pulse register is valid and determined at a rising edge of CSB after the access to the Pulse register.

(The Mode, different_output_voltage, Cycle, EN, RT, and Pulse registers have Cache registers. Any registers other than them do not have Cache registers.)

Application Example



I/O Equivalence Circuit

Pin	Equivalent Circuit Diagram	Pin	Equivalent Circuit Diagram
FCLK CSB SCLK SDATA		TEST ^(Note 9)	
SOUT		STATE1 STATE2	
PIOUT1 PIOUT2		OUT1A OUT1B OUT2A OUT2B	
OUT3A OUT3B OUT4A OUT4B			

(Note 9) Short the TEST pin to DVSS.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Reel

Revision History

Date	Revision	Changes
15.Mar.2010	001	New Release
18.Apr.2013	002	Update some English words, sentences, descriptions, grammar and format.
12.Mar.2019	003	In the "Typical Application Circuit" names of connected power supply are added. In the "Absolute Maximum Ratings" the "Maximum Junction Temperature" is added. In the "Absolute Maximum Ratings" notes are added. e.g. About when operating the IC over the "Absolute Maximum Ratings", "Operating Temperature" is moved to "Recommended Operating Conditions" from "Absolute Maximum Ratings". In the "Typical Performance Curves" package power dissipation graph is removed, because it's same information as Note 2 in "Absolute Maximum Ratings". "Operational Notes" are updated. Other formats are updated.

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