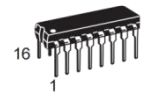
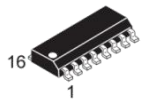
Dual Retriggerable Monostable Multivibrator with Reset

Features

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Specified from -40℃ to +105℃
- Packaging information: DIP16/SOP16/TSSOP16



DIP-16



SOP-16

TSSOP-16

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC123N	DIP-16	74HC123	TUBE	1000pcs/box
74HC123M/TR	SOP-16	74HC123	REEL	2500pcs/reel
74HC123MT/TR	TSSOP-16	HC123	REEL	2500pcs/reel

General Description

The 74HC123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($\overline{nA}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ=HIGH, $\overline{nQ}$=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input n$\overline{RD}$, which also inhibits the triggering.
3. An internal connection from n $\overline{RD}$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input n$\overline{RD}$.

Block Diagram And Pin Description

Block Diagram

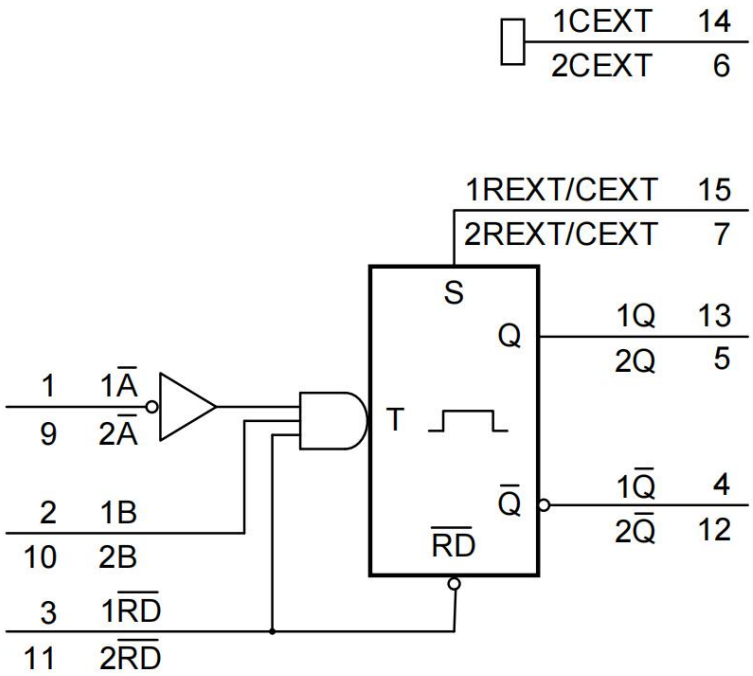


Figure 1. Logic symbol

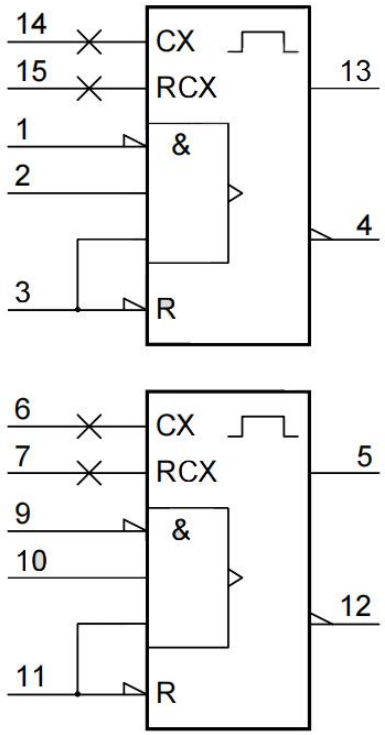


Figure 2. IEC logic symbol

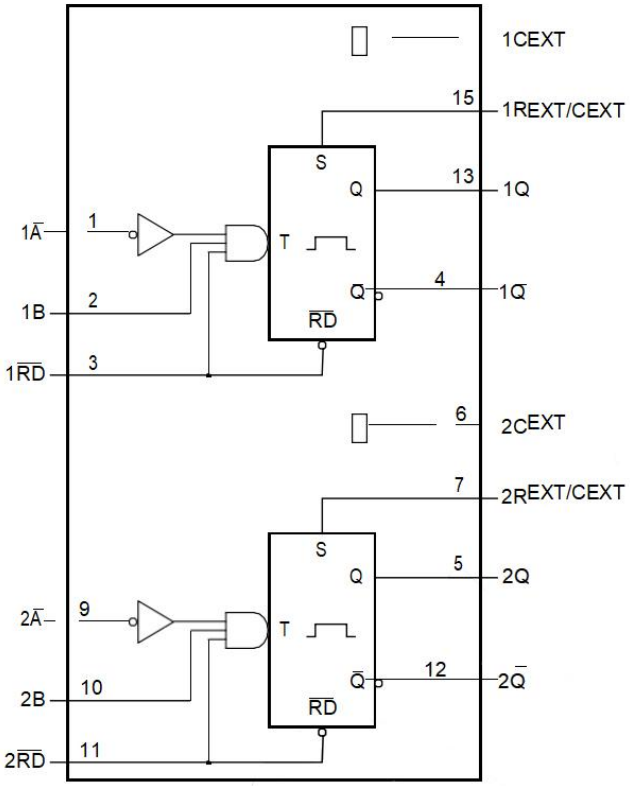


Figure 3. Functional diagram

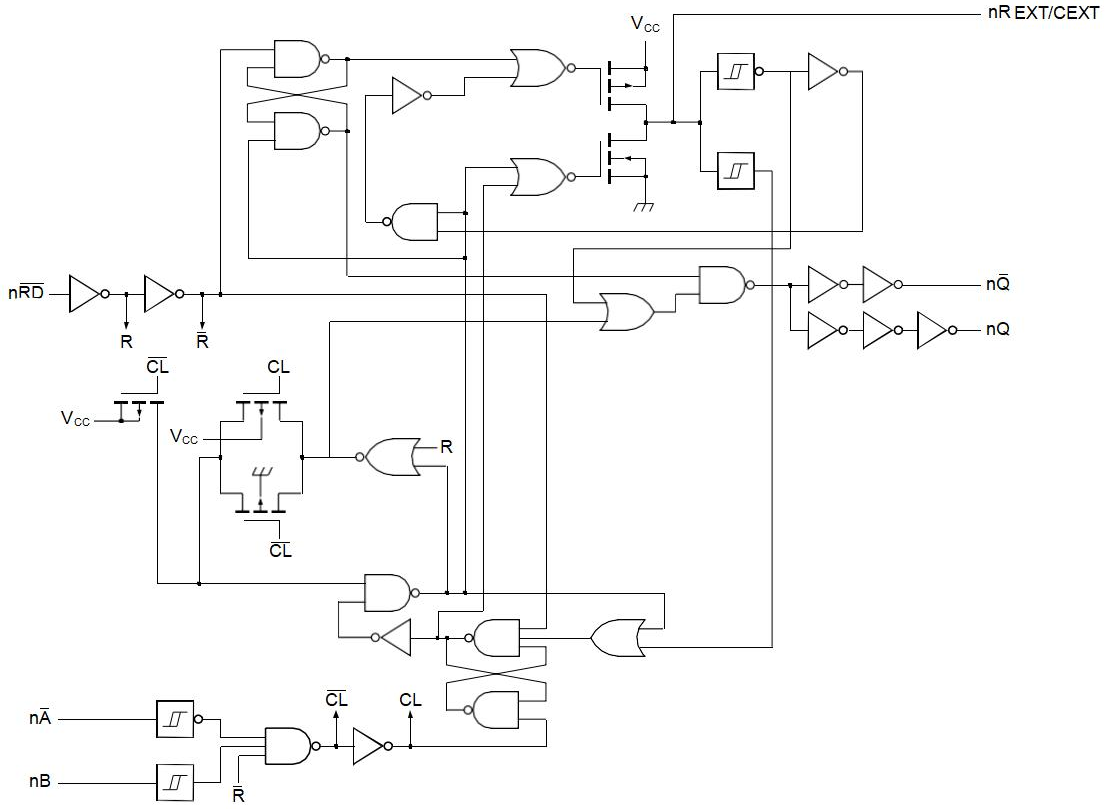
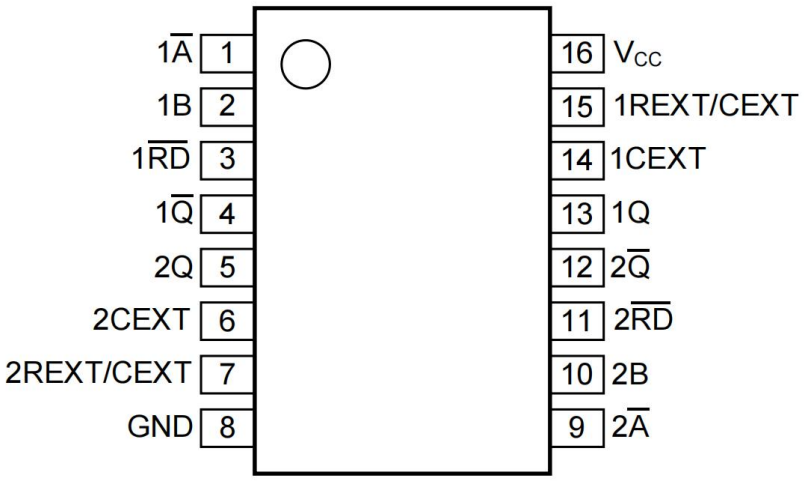


Figure 4. Logic diagram

Pin Configurations



DIP-16/SOP-16/TSSOP-16

Pin Description

Pin No.	Pin Name	Description
1	1$\overline{A}$	negative-edge triggered input 1
2	1B	positive-edge triggered input 1
3	1$\overline{RD}$	direct reset LOW and positive-edge triggered input 1
4	1$\overline{Q}$	active LOW output 1
5	2Q	active HIGH output 2
6	2CEXT	external capacitor connection 2
7	2REXT/CEXT	external resistor and capacitor connection 2
8	GND	ground (0V)
9	2$\overline{A}$	negative-edge triggered input 2
10	2B	positive-edge triggered input 2
11	2$\overline{RD}$	direct reset LOW and positive-edge triggered input 2
12	2$\overline{Q}$	active LOW output 2
13	1Q	active HIGH output 1
14	1CEXT	external capacitor connection 1
15	1REXT/CEXT	external resistor and capacitor connection 1
16	V_{CC}	supply voltage

Function Table

Input			Output	
$n\overline{RD}$	$n\overline{A}$	nB	nQ	$n\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

Note:

1. H=HIGH voltage level; L=LOW voltage level; X=don't care.
2. ↑=LOW-to-HIGH transition; ↓=HIGH-to-LOW transition.
3. ⎍=one HIGH level output pulse; ⎍=one LOW level output pulse.
4. If the mono stable was triggered before this condition was established, the pulse will continue as programmed.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	except for pins nREXT/CEXT; V_O= -0.5V to (V_{CC}+0.5V)		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-	-50	mA
storage temperature	Tstg	-		-65	+150	℃
total power dissipation	Ptot	-		-	500	mW
soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:

5. For DIP16 packages: above 70℃ the value of Ptot derates linearly with 12mW/K.
6. For SOP16 packages: above 70℃ the value of Ptot derates linearly with 8mW/K.
7. For (T)SSOP16 packages: above 60℃ the value of Ptot derates linearly with 5.5mW/K

Recommended Operating Conditions

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-		2.0	5.0	6.0	V
input voltage	V_I	-		0	-	VCC	V
output voltage	V_O	-		0	-	VCC	V
input transition rise and fall rate	Δt/ΔV	$n\overline{RD}$ input	V_{CC}=2.0V	-	-	625	ns/V
			V_{CC}=4.5V	-	1.67	139	ns/V
			V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	Tamb	-		-40	-	+105	℃

Electrical Characteristics

DC Characteristics 1 (T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(Tamb=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	VCC=2.0V		1.5	-	-	V
		VCC=4.5V		3.15	-	-	V
		VCC=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	VCC=2.0V		-	-	0.5	V
		VCC=4.5V		-	-	1.35	V
		VCC=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	VI = VIH or VIL	IO=-20uA; VCC=2.0V	1.9	-	-	V
			IO=-20uA; VCC=4.5V	4.4	-	-	V
			IO=-20uA; VCC=6.0V	5.9	-	-	V
			IO=-4mA; VCC=4.5V	3.84	-	-	V
			IO=-5.2mA; VCC=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	VI = VIH or VIL	IO=20uA; VCC=2.0V	-	-	0.1	V
			IO=20uA; VCC=4.5V	-	-	0.1	V
			IO=20uA; VCC=6.0V	-	-	0.1	V
			IO=4mA; VCC=4.5V	-	-	0.33	V
			IO=5.2mA; VCC=6.0V	-	-	0.33	V
input leakage current	I_I	VI=VCC or GND; VCC=6.0V		-	-	±1.0	uA
supply current	I_{CC}	VI=VCC or GND; IO=0A; VCC=6.0V		-	-	80	uA

DC Characteristics 3

(Tamb=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	VIH	VCC=2.0V		1.5	-	-	V
		VCC=4.5V		3.15	-	-	V
		VCC=6.0V		4.2	-	-	V
LOW-level input voltage	VIL	VCC=2.0V		-	-	0.5	V
		VCC=4.5V		-	-	1.35	V
		VCC=6.0V		-	-	1.8	V
HIGH-level output voltage	VOH	VI = VIH or VIL	IO=-20uA; VCC=2.0V	1.9	-	-	V
			IO=-20uA; VCC=4.5V	4.4	-	-	V
			IO=-20uA; VCC=6.0V	5.9	-	-	V
			IO=-4mA; VCC=4.5V	3.7	-	-	V
			IO=-5.2mA; VCC=6.0V	5.2	-	-	V
LOW-level output voltage	VOL	VI = VIH or VIL	IO=20uA; VCC=2.0V	-	-	0.1	V
			IO=20uA; VCC=4.5V	-	-	0.1	V
			IO=20uA; VCC=6.0V	-	-	0.1	V
			IO=4mA; VCC=4.5V	-	-	0.4	V
			IO=5.2mA; VCC=6.0V	-	-	0.4	V
input leakage current	II	VI=VCC or GND;VCC=6.0V		-	-	±1.0	uA
supply current	ICC	VI=VCC or GND; IO=0A; VCC=6.0V		-	-	160	uA

AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V); C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	tpd	$n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; CEXT=0pF; REXT=5kΩ; see Figure 6[1]	VCC=2.0V	-	83	255	ns
			VCC=4.5V	-	30	51	ns
			VCC=5.0V; CL=15pF	-	26	-	ns
			VCC=6.0V	-	24	43	ns
		$n\overline{RD}$(reset) to nQ or $n\overline{Q}$; CEXT=0pF; REXT=5kΩ; see Figure 6	VCC=2.0V	-	66	215	ns
			VCC=4.5V	-	25	43	ns
			VCC=5.0V; CL=15pF	-	20	-	ns
			VCC=6.0V	-	19	37	ns
transition time	tt	see Figure 6[1]	VCC=2.0V	-	19	75	ns
			VCC=4.5V	-	7	15	ns
			VCC=6.0V	-	6	13	ns
pulse width	t_W	$n\overline{A}$ LOW; see Figure 7	VCC=2.0V	100	8	-	ns
			VCC=4.5V	20	3	-	ns
			VCC=6.0V	17	2	-	ns
		nB HIGH; see Figure 7	VCC=2.0V	100	17	-	ns
			VCC=4.5V	20	6	-	ns
			VCC=6.0V	17	5	-	ns
		$n\overline{RD}$ LOW; see Figure 8	VCC=2.0V	100	14	-	ns
			VCC=4.5V	20	5	-	ns
			VCC=6.0V	17	4	-	ns
		nQ HIGH and $n\overline{Q}$ LOW; VCC=5.0V; see Figure 7, 8[2]	CEXT=100nF; REXT=10kΩ	-	450	-	us
			CEXT=0pF; REXT=5kΩ	-	75	-	ns
retrigger time	trtrig	$n\overline{A}$, nB; CEXT=0pF; REXT=5kΩ; VCC=5.0V; see Figure 7[3][4]		-	110	-	ns
external timing resistor	R_{EXT}	see Figure 7	VCC=2.0V	10	-	1000	kΩ
			VCC=5.0V	2	-	1000	kΩ
external timing capacitor	C_{EXT}	VCC=5.0V; see Figure 9[4]		-	-	-	pF
power dissipation capacitance	C_{PD}	per monostable; VI=GND to VCC[5]		-	54	-	pF

Note:

1. tpd is the same as t_{PLH} and t_{PHL}; tt is the same as t_{TH}L and t_{TLH}
2. For other REXT and CEXT combinations see Figure 9. If CEXT>10nF, the next formula is valid.
   t_W=K×R EXT×C EXT, where;
   t_W=typical output pulse width in ns;
   REXT=external resistor in kΩ; CEXT=external capacitor in pF;
   K=constant = 0.45 for VCC=5.0V and 0.55 for VCC=2.0V;
   The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7pF.

3. The time to retrigger the monostable multivibrator depends on the values of REXT and CEXT. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If CEXT>10pF,the next formula (at VCC=5.0V) for the setup time of a retrigger pulse is valid:
   trtrig=30+0.19×R_{EXT}×$C_{EXT}^{0.9}$+13×$R_{EXT}^{1.05}$, where:
   trtrig=retrigger time in ns;
   C_{EXT}=external capacitor in pF; R_{EXT}=external resistor in kΩ.
   The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7pF.
4. When the device is powered-up, initiate the device via a reset pulse, when CEXT<50pF
5. CPD is used to determine the dynamic power dissipation (PD in uW).
   $P_D=C_{PD}\times V_{CC}^2\times f\ i+\sum(C_L\times V_{CC}^2\times fo)+0.75\times C_{EXT}\times V_{CC}^2\times fo+D\times 16\times V_{CC}$ where:
   fi=input frequency in MHz; fo=output frequency in MHz;
   D=duty factor in %; CL=output load capacitance in pF;
   VCC=supply voltage in V;
   CEXT=timing capacitance in pF;
   $\sum(CL\times V_{CC}^2\times fo)$=sum of outputs.

AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	tpd	$n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6[1]	V_{CC}=2.0V	-	-	320	ns
			V_{CC}=4.5V	-	-	64	ns
			V_{CC}=6.0V	-	-	54	ns
		$n\overline{RD}$(reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=2.0V	-	-	270	ns
			V_{CC}=4.5V	-	-	54	ns
			V_{CC}=6.0V	-	-	46	ns
transition time	tt	see Figure 6[1]	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	$n\overline{A}$ LOW; see Figure 7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		nB HIGH; see Figure 7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		$n\overline{RD}$ LOW; see Figure 8	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

AC Characteristics 3

(T_{amb}=-40℃to +105℃, GND=0V; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	$n\overline{RD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6[1]	V_{CC}=2.0V	-	-	385	ns
			V_{CC}=4.5V	-	-	77	ns
			V_{CC}=6.0V	-	-	65	ns
		$n\overline{RD}$(reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=2.0V	-	-	325	ns
			V_{CC}=4.5V	-	-	65	ns
			V_{CC}=6.0V	-	-	55	ns
transition time	t_t	see Figure 6[1]	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	$n\overline{A}$ LOW; see Figure 7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		nB HIGH;	V_{CC}=2.0V	150	-	-	ns
		see Figure 7	V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		$n\overline{RD}$ LOW; see Figure 8	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

Testing Circuit

AC Testing Circuit

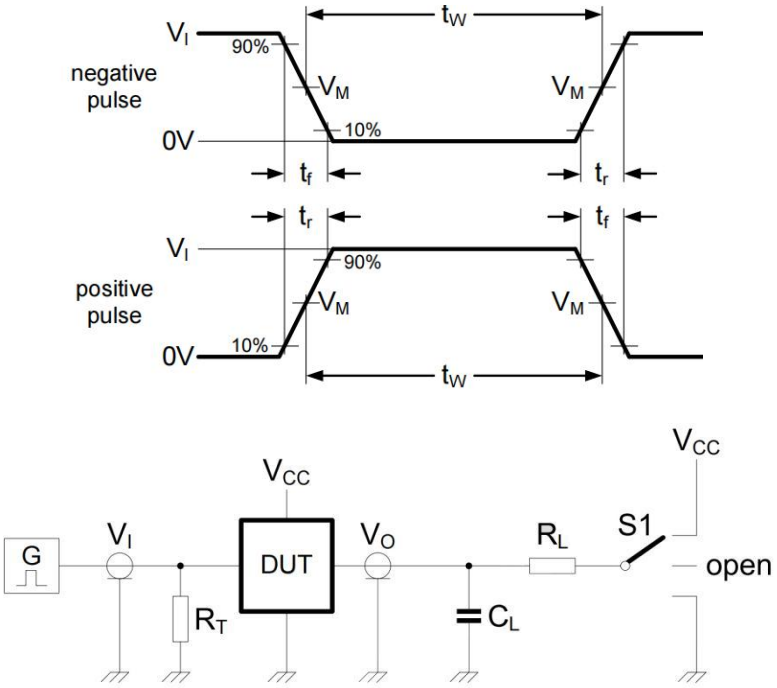


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulsegenerator.

S1=Test selection switch.

AC Testing Waveforms

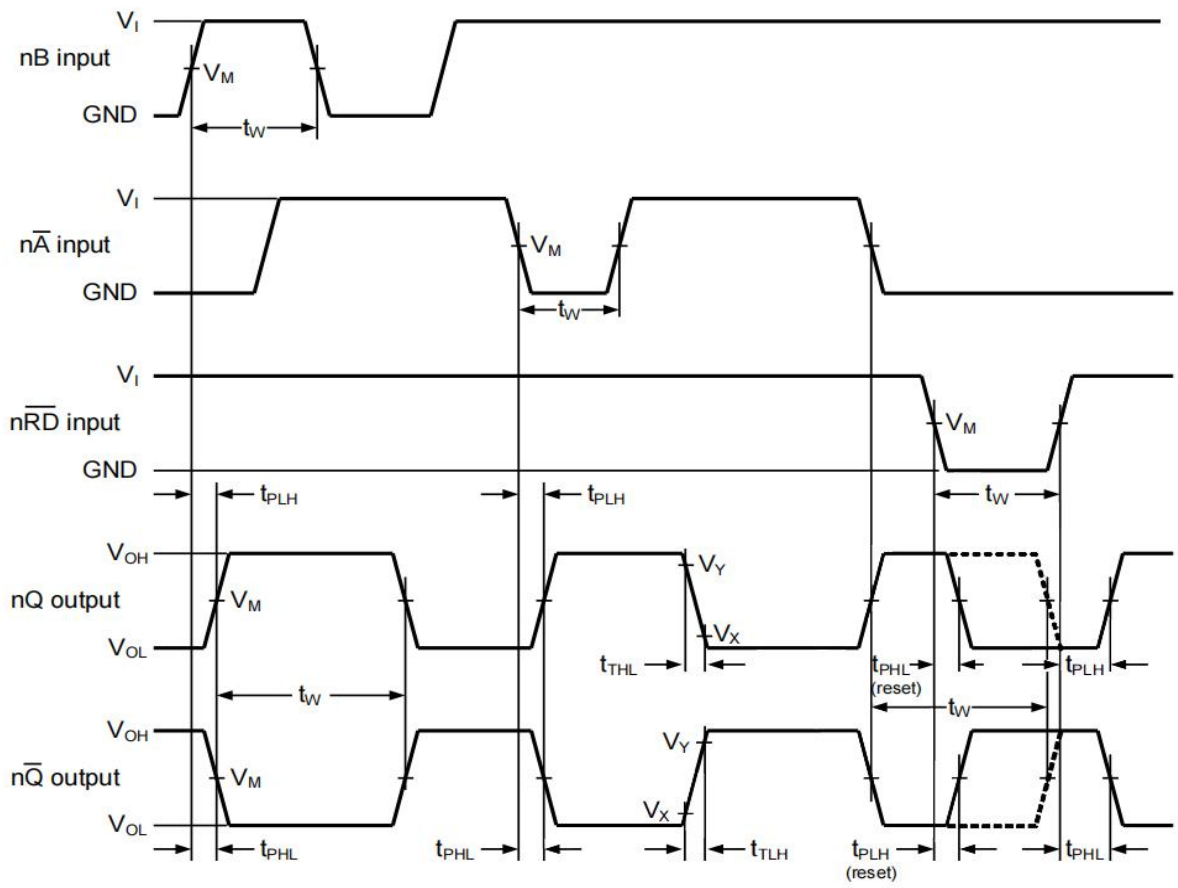


Figure 6. Propagation delays from inputs (n$\overline{A}$, nB, n$\overline{RD}$) to outputs (nQ, n$\overline{Q}$) and output transition times

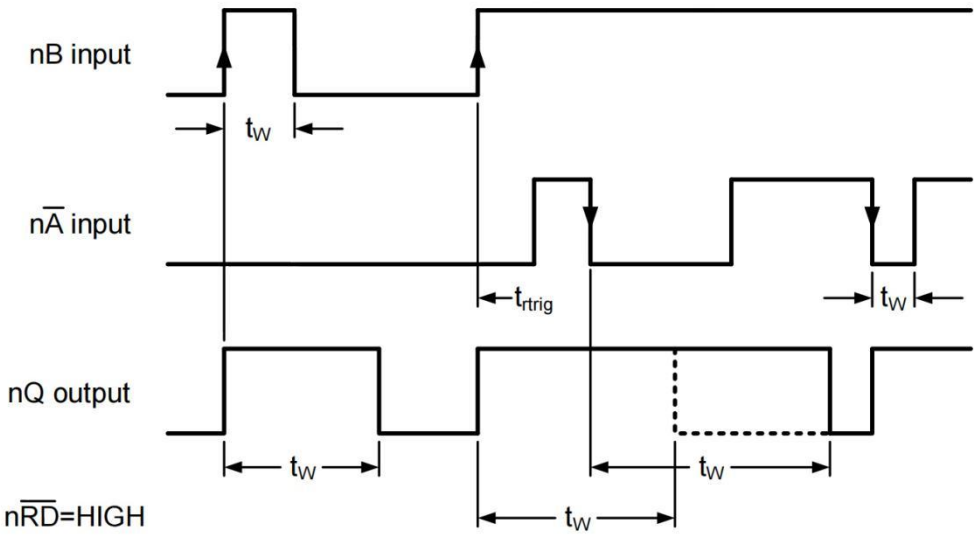


Figure 7. Output pulse control using retrigger pulse

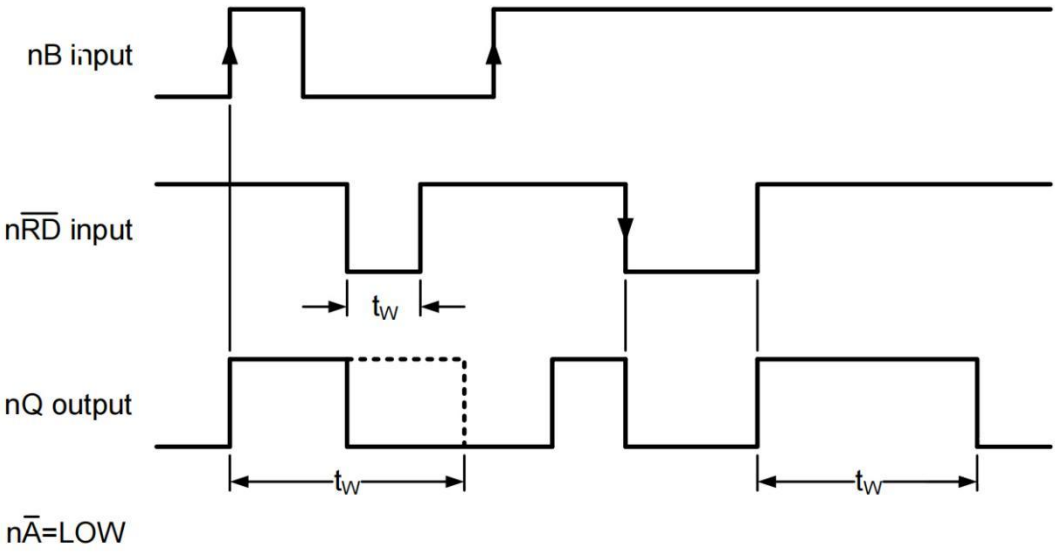
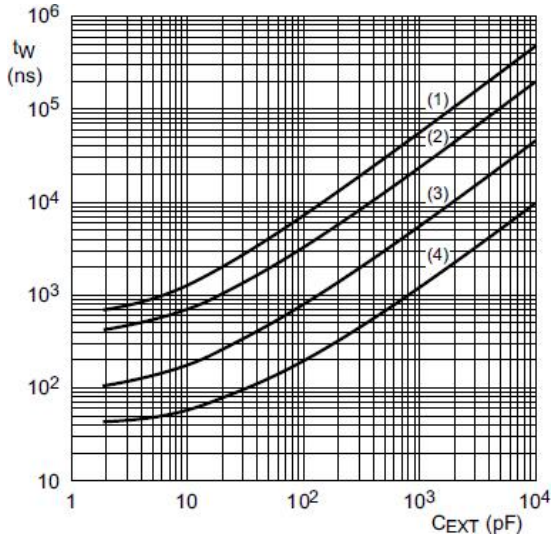


Figure 8. Output pulse control using reset input nRD



V_{CC}=5.0V; Tamb=25℃.

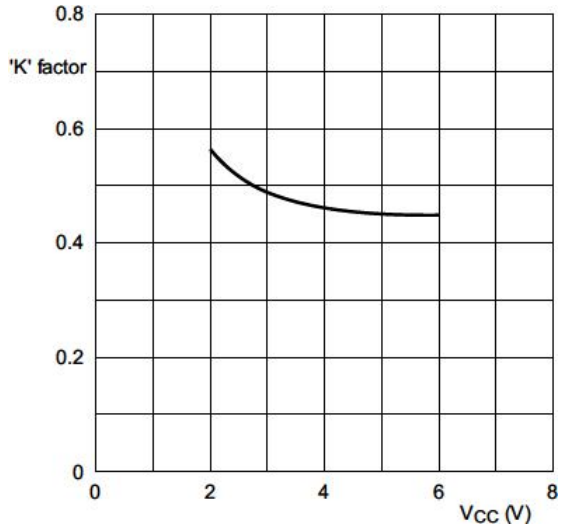
R_{EXT}=100kΩ

R_{EXT}=50kΩ

R_{EXT}=10kΩ

R_{EXT}=2kΩ

Figure 9. Typical output pulse width as a function of the external capacitor value



C_{EXT}=10nF; R_{EXT}=10kΩ to 100kΩ.Tamb=25℃.

Figure 10. 74HC123 typical 'K' factor as function of VCC

Measurement Points

Type	Input	Output
	VM	VM
74HC123	0.5×V_{CC}	0.5×V_{CC}

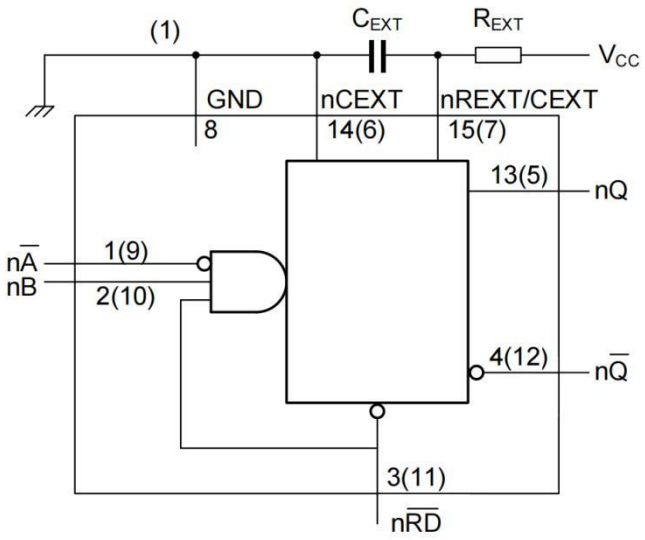
Test data

Type	Input		Load		S1 position
	V_I	t_R,t_F	C_L	R_L	t_{PHL},t_{PLH}
74HC123	V_{CC}	6ns	15pF,50pF	1kΩ	Open

Typical Application Circuit And Application Note

Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.



For minimum noise generation it is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Figure 11. Timing component connections

Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT}. This output pulse can be eliminated using the circuit shown in Figure 12.

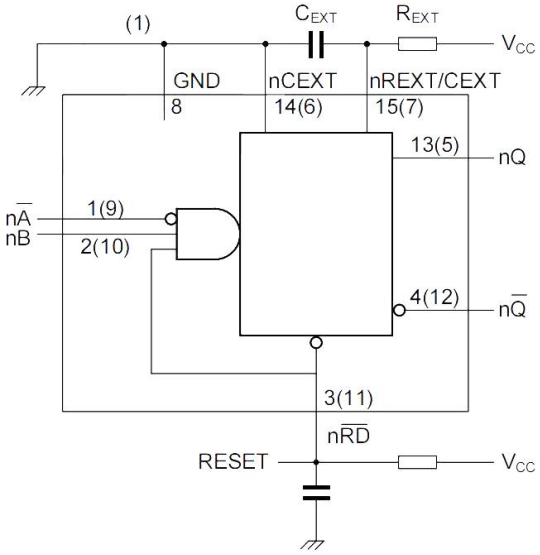


Figure 12. Power-up output pulse elimination circuit

Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 13.

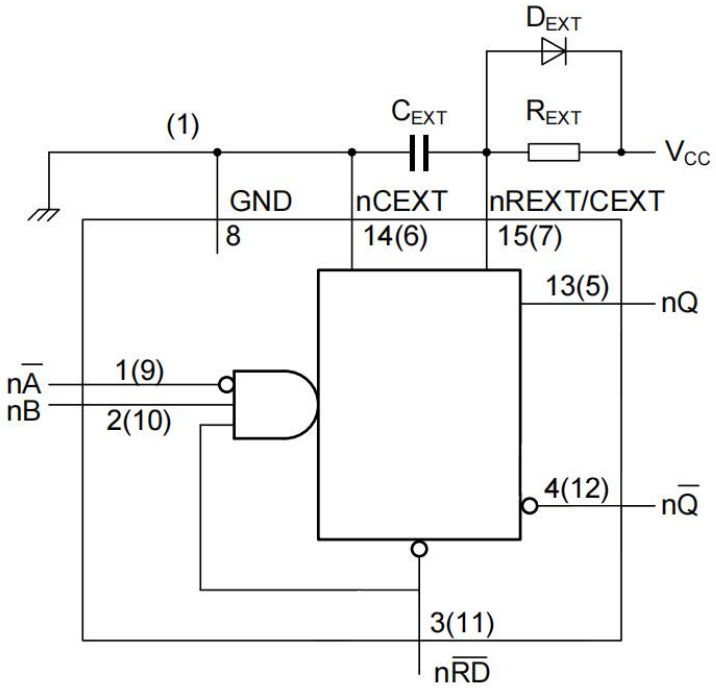
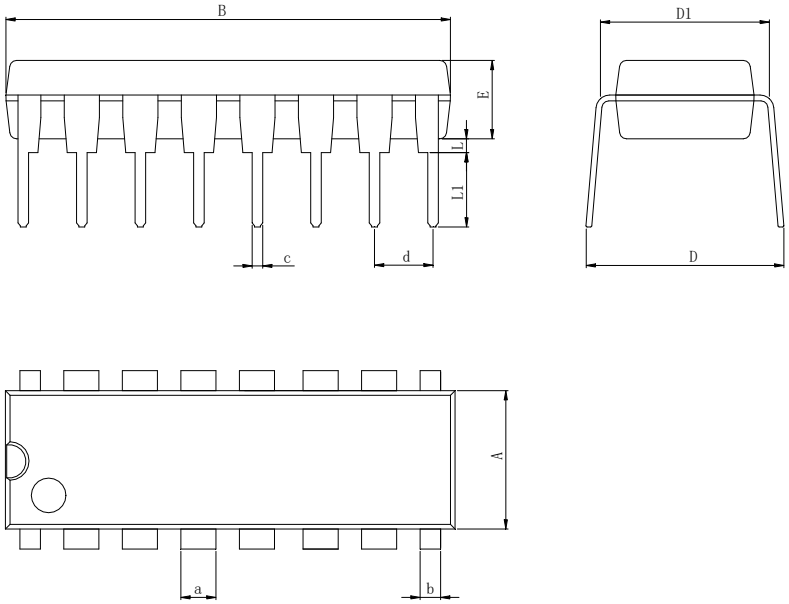


Figure 13. Power-down protection circuit

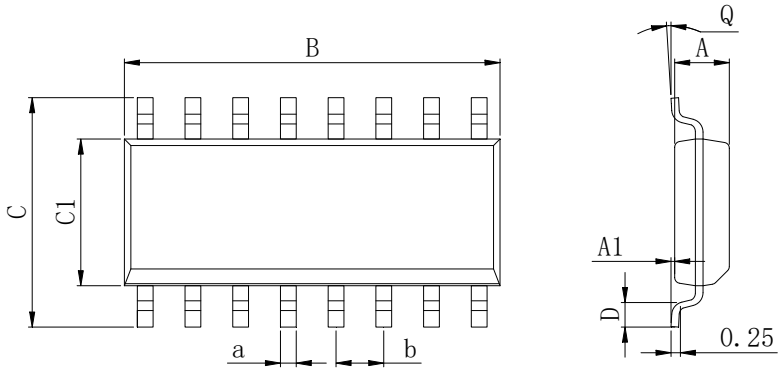
Physical Dimensions

DIP16



Dimensions In Millimeters(DIP16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

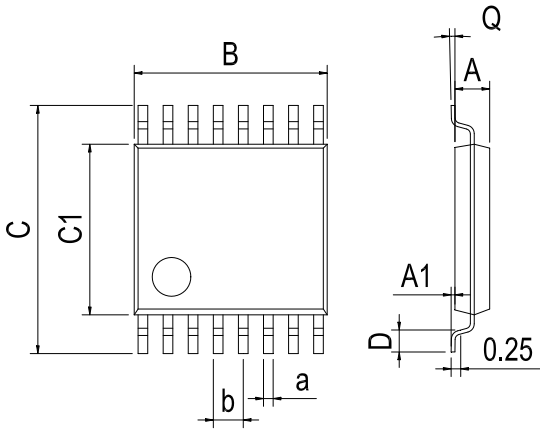
SOP16



Dimensions In Millimeters(SOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP16



Dimensions In Millimeters(TSSOP16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety,security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.