

# 74LV04AT

## Hex inverter

Rev. 1 — 18 May 2017

Product data sheet

## 1 General description

The 74LV04AT is a hex inverter with TTL inputs.

Designed to operate over a  $V_{CC}$  range from 4.5 V to 5.5 V, the inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2 Features and benefits

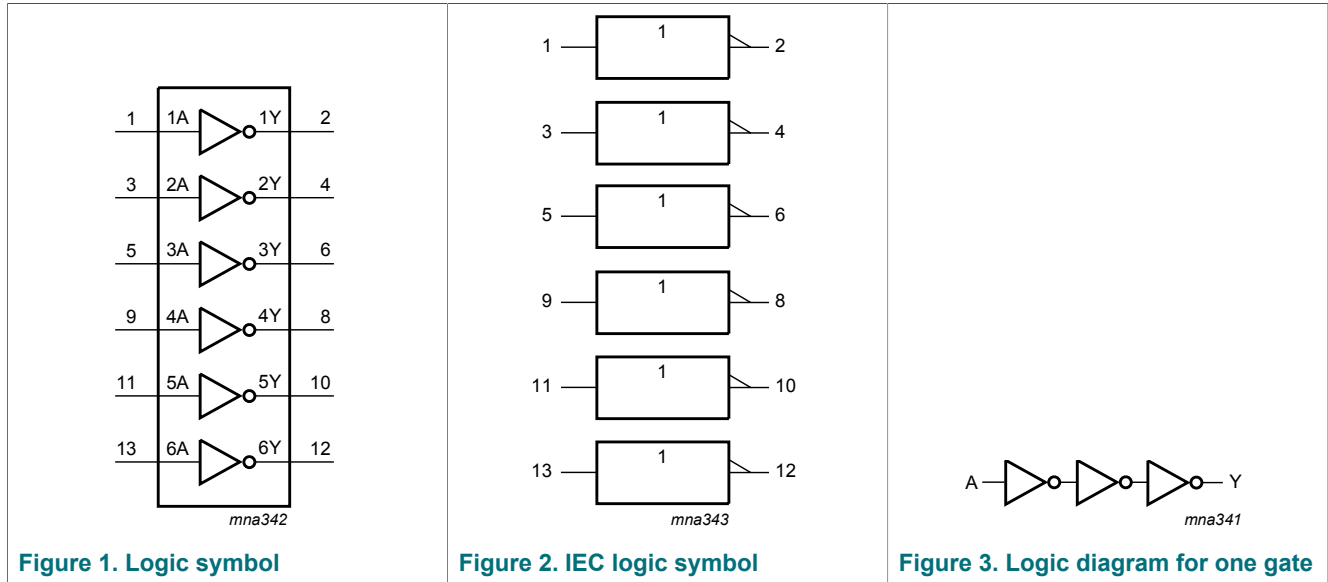
- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical  $t_{pd}$  of 3.3 ns at 5 V
- Typical  $V_{OL(p)} < 0.8$  V at  $V_{CC} = 5$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OH(v)} > 2.3$  V at  $V_{CC} = 5$  V,  $T_{amb} = 25$  °C
- Supports mixed-mode voltage operation on all ports
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 3 kV
  - MM JESD22-A115-A exceeds 150 V
  - CDM JESD22-C101E exceeds 2 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3 Ordering information

Table 1. Ordering information

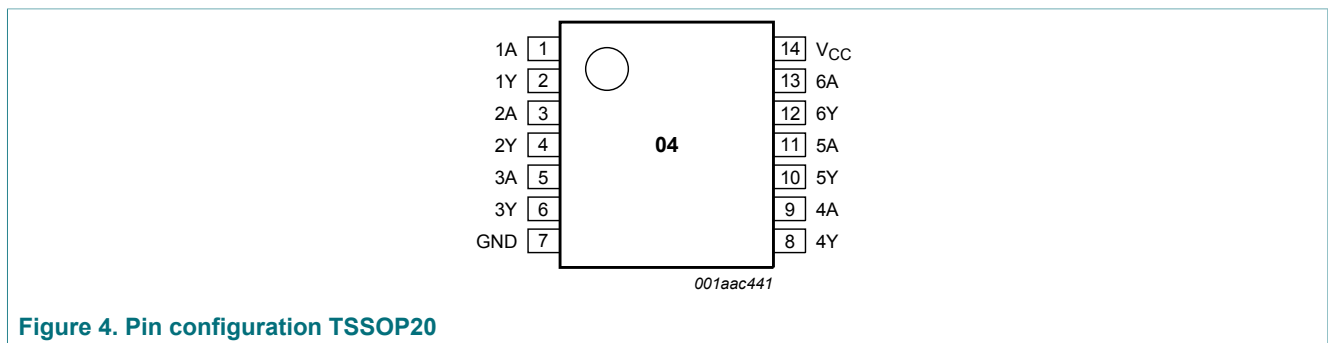
Type number	Package			
	Temperature range	Name	Description	Version
74LV04ATPW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

## 4 Functional diagram



## 5 Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6 Functional description

Table 3. Function table <sup>[1]</sup>

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level

## 7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$V_O$	output voltage	active mode	-0.5	$V_{CC} + 0.5$	V
		power-down or 3-state mode	-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±35	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] This value is limited to 7.0 V maximum.

[4] For TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

## 8 Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		4.5	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	active mode	0	$V_{CC}$	V
		power-down or 3-state mode	0	5.5	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 5.0$ V ± 0.5 V	-	20	ns/V

## 9 Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2	-	-	2	-	2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	-	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -12 mA	3.8	-	-	3.8	-	3.8	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	-	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 12mA	-	-	0.55	-	0.55	-	0.55	V
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = GND to 5.5 V; V <sub>CC</sub> = 0 V	-	-	0.5	-	5	-	5	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2	-	20	-	20	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other pins at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ . For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Figure 5</a> <sup>[2]</sup>								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
		$C_L = 15\text{ pF}$	-	3.3	6.3	1	7.3	1	8.1	ns
		$C_L = 50\text{ pF}$	-	5.1	7.7	1	8.8	1	10.4	ns
$C_I$	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 5\text{ V}$	-	2	6	-	6	-	6	pF
$C_O$	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 5\text{ V}$	-	5	-	-	-	-	-	pF
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}$ ; $f = 10\text{ MHz}$ ; $V_I = GND$ to $V_{CC}$ <sup>[3]</sup>	-	9	-	-	-	-	-	pF

[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 5\text{ V}$ .

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$

where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

**Table 8. Noise characteristics**

$GND = 0\text{ V}$ . For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			Unit
			Min	Typ	Max	
$V_{CC} = 5\text{ V}; C_L = 50\text{ pF}$						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.2	0.8	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-0.8	-0.3	-	V
$V_{OH(v)}$	HIGH-level output voltage (valley)		-	4.5	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage (dynamic)		2	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage (dynamic)		-	-	0.8	V

10.1 Waveforms and test circuit

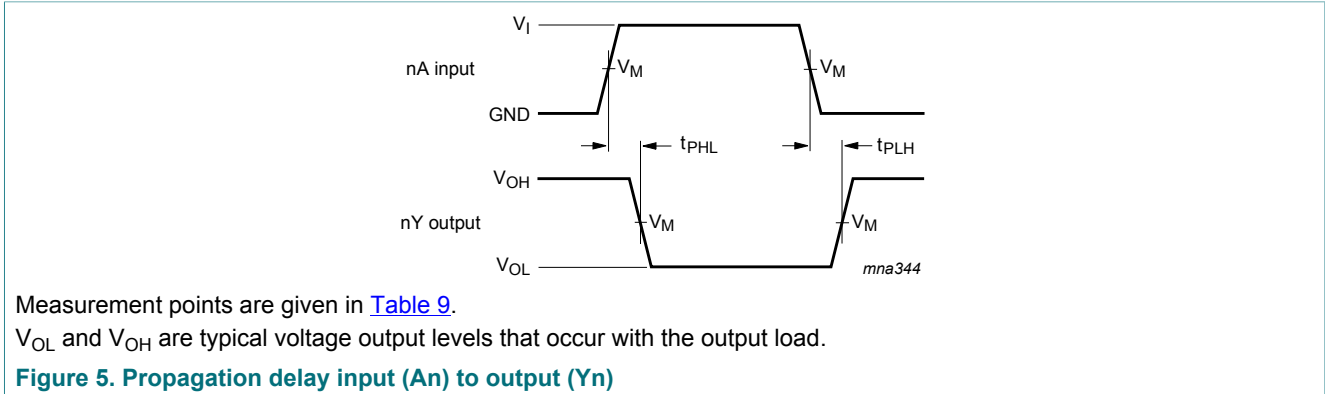


Table 9. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

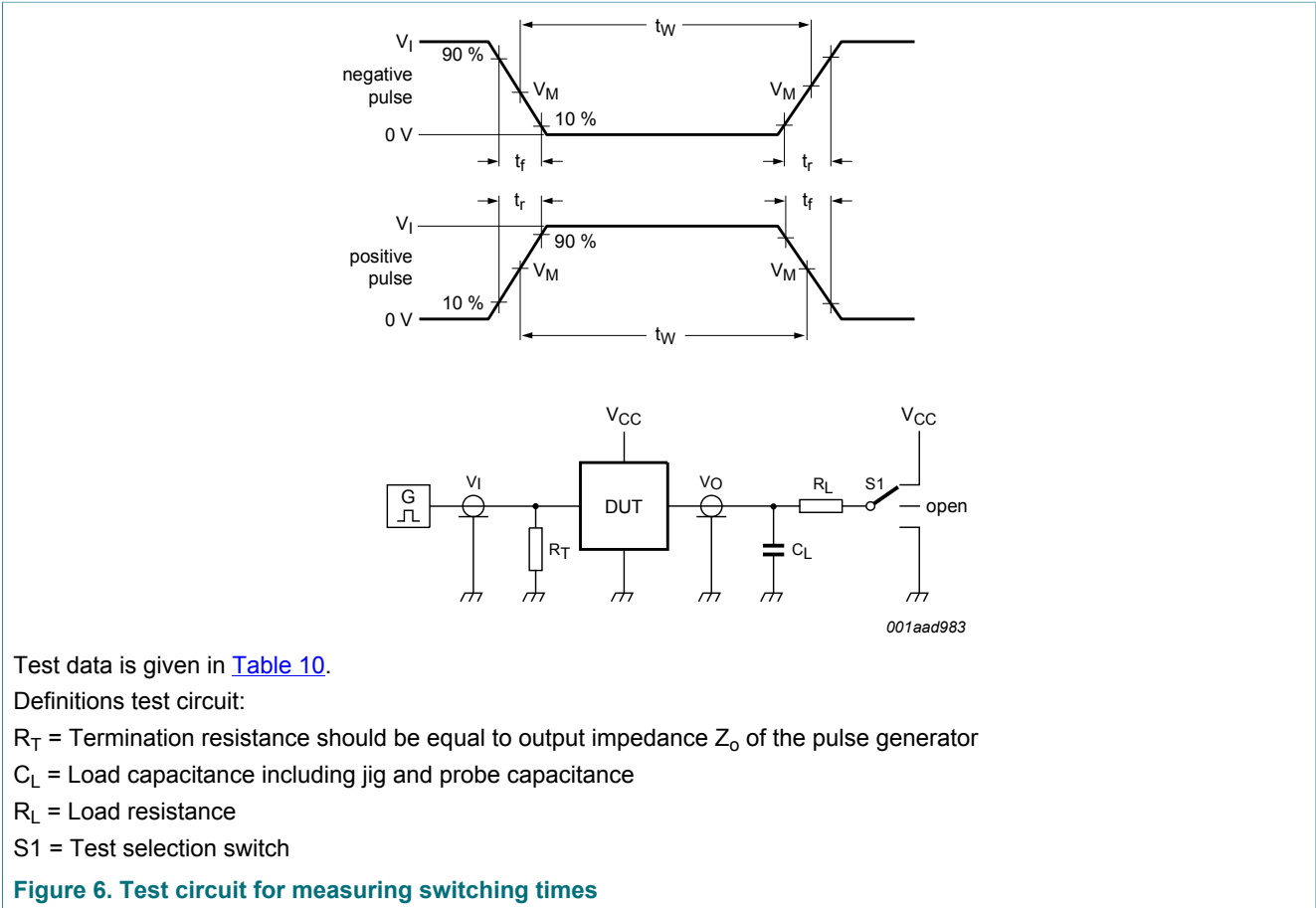


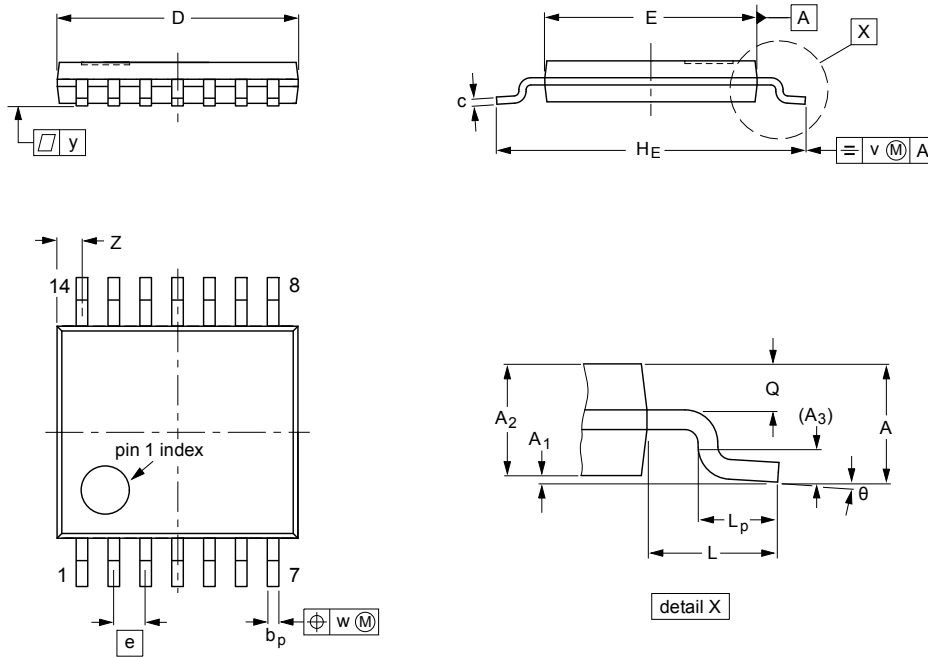
Table 10. Test data

Input		Load		S1 position		
$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
GND to 3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	$V_{CC}$

11 Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Figure 7. Package outline SOT402-1 (TSSOP14)



## 12 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV04AT v.1	20170518	Product data sheet	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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