



# Wideband 2.5 GHz, 37 dB Isolation at 1 GHz, CMOS, 1.65 V to 2.75 V, 4:1 Mux/SP4T

Enhanced Product

**ADG904-EP**

## FEATURES

- Wideband switch: -3 dB frequency at 2.5 GHz
- Absorptive 4:1 mux/single-pole, four-throw (SP4T)
- High off isolation (37 dB at 1 GHz)
- Low insertion loss (1.1 dB dc to 1 GHz)
- Single 1.65 V to 2.75 V power supply ( $V_{DD}$ )
- CMOS/LVTTL control logic
- 20-lead, 4 mm × 4 mm LFCSP package
- Low power consumption (2.5  $\mu$ A maximum)

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: -55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

## APPLICATIONS

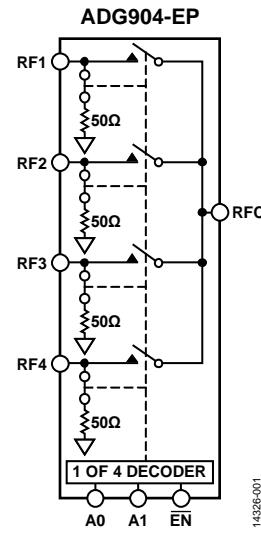
- Wireless communications
- General-purpose radio frequency (RF) switching
- Dual-band applications
- High speed filter selection
- Digital transceiver front-end switches
- IF switching
- Tuner modules
- Antenna diversity switching

## GENERAL DESCRIPTION

The ADG904-EP is a wideband analog 4:1 multiplexer that uses a CMOS process to provide high isolation and low insertion loss to 1 GHz. The ADG904-EP is an absorptive/matched mux with 50 Ω terminated shunt legs. This device is designed such that the isolation is high over the dc to 1 GHz frequency range.

The ADG904-EP switches one of four inputs to a common output, RFC, as determined by the 3-bit binary address lines A0, A1, and EN. A Logic 1 on the EN pin disables the device.

## FUNCTIONAL BLOCK DIAGRAM



14326-001

Figure 1.

The device has on-board CMOS control logic, which eliminates the need for external control circuitry. The control inputs are both CMOS and LVTTL compatible. The low power consumption of this device makes it ideally suited for wireless applications and general-purpose high frequency switching.

Additional application and technical information can be found in the [ADG904](#) data sheet.

## PRODUCT HIGHLIGHTS

1. 37 dB off isolation at 1 GHz.
2. 1.1 dB insertion loss at 1 GHz.
3. 20-lead LFCSP package.

Rev. C

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## REVISION HISTORY

### 5/2017—Rev. B to Rev. C

Change to Endnote 1, Table 3 .....	3
Updated Outline Dimensions .....	11

### 3/2017—Rev. A to Rev. B

Changes to Endnote 4, Table 1.....	3
Added Endnote 1, Table 2.....	4

### 11/2016—Rev. 0 to Rev. A

Changes to Figure 15.....	9
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### 6/2016—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD}$  = 1.65 V to 2.75 V, GND = 0 V, input power = 0 dBm, temperature range =  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ <sup>1</sup>	Max	Unit
AC ELECTRICAL CHARACTERISTICS						
–3 dB Frequency <sup>2</sup>				2.5		GHz
Insertion Loss	S12, S21	DC to 100 MHz; $V_{DD} = 2.5\text{ V} \pm 10\%$ ; see Figure 18 500 MHz; $V_{DD} = 2.5\text{ V} \pm 10\%$ 1000 MHz; $V_{DD} = 2.5\text{ V} \pm 10\%$		0.5	1	dB
Isolation—RFC to RF1x	S12, S21	100 MHz; see Figure 17 500 MHz; see Figure 17 1000 MHz; see Figure 17	51	60		dB
Crosstalk	S12, S21	100 MHz; see Figure 19 500 MHz; see Figure 19 1000 MHz; see Figure 19	30	37		dB
Return Loss <sup>2</sup>	S11, S22	DC to 100 MHz 500 MHz 1000 MHz	19	27		dB
On Channel		DC to 100 MHz 500 MHz 1000 MHz		26		dB
Off Channel		DC to 100 MHz 500 MHz 1000 MHz	14	22		dB
Timing				18		dB
On Switching Time <sup>2</sup>	$t_{ON(\bar{EN})}$	50% $\bar{EN}$ to 90% RF; see Figure 15		8.5	10	ns
Off Switching Time <sup>2</sup>	$t_{OFF(\bar{EN})}$	50% $\bar{EN}$ to 10% RF; see Figure 15		13	16	ns
Transition Time	$t_{TRANS}$	50% A0/A1 to 10% RF		12	15	ns
Rise Time <sup>2</sup>	$t_{RISE}$	10% to 90% RF; see Figure 16		3	5	ns
Fall Time <sup>2</sup>	$t_{FALL}$	90% to 10% RF; see Figure 16		7.5	11	ns
Third-Order Intermodulation Intercept	IP3	900 MHz/901 MHz, 4 dBm; see Figure 21	25	31		dBm
Video Feedthrough <sup>3</sup>		See Figure 20		3		mV p-p
INPUT POWER						
1 dB Input Compression	P1dB	1000 MHz <sup>4</sup> ; see Figure 22		16		dBm
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	$V_{INH}$	$V_{DD} = 2.25\text{ V}$ to $2.75\text{ V}$ $V_{DD} = 1.65\text{ V}$ to $1.95\text{ V}$	1.7			V
Input Low Voltage	$V_{INL}$	$V_{DD} = 2.25\text{ V}$ to $2.75\text{ V}$ $V_{DD} = 1.65\text{ V}$ to $1.95\text{ V}$	0.65 $V_{DD}$			V
Input Leakage Current	$I_I$	$0\text{ V} \leq V_{IN} \leq 2.75\text{ V}$		0.7		V
				0.35 $V_{DD}$		V
CAPACITANCE <sup>2</sup>		$f = 1\text{ MHz}$		$\pm 0.1$	$\pm 1$	$\mu\text{A}$
RF Port On Capacitance	$C_{RF\text{ ON}}$			3		pF
Digital Input Capacitance	$C$			2		pF
POWER REQUIREMENTS						
$V_{DD}$			1.65		2.75	V
Quiescent Power Supply Current	$I_{DD}$	Digital inputs = 0 V or $V_{DD}$		0.1	2.5	$\mu\text{A}$

<sup>1</sup> Typical values are at  $V_{DD} = 2.5\text{ V}$  and  $25^{\circ}\text{C}$ , unless otherwise stated.

<sup>2</sup> Guaranteed by design, not subject to production test.

<sup>3</sup> Video feedthrough is the dc transience at the output of any port of the switch when the control voltage is switched from high to low or low to high in a  $50\ \Omega$  test setup, measured with 1 ns rise time pulses and 500 MHz bandwidth.

<sup>4</sup> Less than 100 MHz, refer to the [AN-952 Application Note](#) for more information about power handling.

**CONTINUOUS CURRENT PER CHANNEL**

Table 2.

Parameter	25°C	85°C	105°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL <sup>1</sup>						20-lead LFCSP, $\theta_{JA} = 30.4^\circ\text{C}/\text{W}$ , dc bias = 0.5 V
$V_{DD} = 2.75 \text{ V}, V_{SS} = 0 \text{ V}$	93.1	10.8	5.9	3.3	mA maximum	
$V_{DD} = 1.65 \text{ V}, V_{SS} = 0 \text{ V}$	82.6	10.8	5.9	3.3	mA maximum	

<sup>1</sup> Guaranteed by design, not production tested.

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

**Table 3.**

Parameter	Rating
V <sub>DD</sub> to GND <sup>1</sup>	-0.5 V to +4 V
Inputs to GND <sup>1</sup>	-0.5 V to V <sub>DD</sub> + 0.3 V <sup>2</sup>
Continuous Current	Data <sup>3</sup> + 15%
Input Power <sup>4</sup>	18 dBm
Operating Temperature Range (Industrial)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C
Electrostatic Discharge (ESD)	1 kV

<sup>1</sup> Tested at +125°C.

<sup>2</sup> RFx off port inputs to ground = -0.5 V to V<sub>DD</sub> - 0.5 V.

<sup>3</sup> See Table 2.

<sup>4</sup> Input power is tested with switch in both open and close position. Power is applied on RFx, while RFC is terminated to a 50 Ω resistor to GND.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

**Table 4. Thermal Resistance**

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
CP-20-6 <sup>1</sup>	30.4	2.83	°C/W

<sup>1</sup> Test condition: thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

**Table 5. Truth Table**

A1	A0	EN	On Switch <sup>1</sup>
X <sup>2</sup>	X <sup>2</sup>	1	None
0	0	0	RF1
0	1	0	RF2
1	0	0	RF3
1	1	0	RF4

<sup>1</sup> Off switches have 50 Ω termination to GND.

<sup>2</sup> X means don't care.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

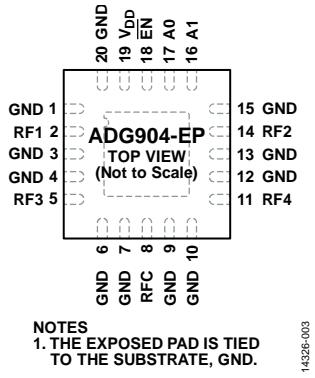


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function
0	EPAD	Exposed Pad. The exposed pad is tied to the substrate, GND.
1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 20	GND	Ground Reference Points for All Circuitry on the Device.
2	RF1	RF 1 Port.
5	RF3	RF 3 Port.
8	RFC	Common RF Port for Switch.
11	RF4	RF 4 Port.
14	RF2	RF 2 Port.
16	A1	Logic Control Input 1.
17	A0	Logic Control Input 0.
18	EN	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, Ax logic inputs determine on switches.
19	V <sub>DD</sub>	Power Supply Input. This device operates from 1.65 V to 2.75 V. V <sub>DD</sub> must be decoupled to GND.

## TYPICAL PERFORMANCE CHARACTERISTICS

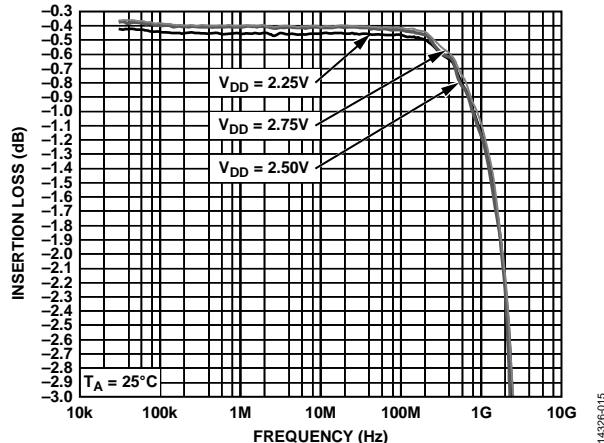


Figure 3. Insertion Loss vs. Frequency for  $V_{DD} > 2.2$  V (RFx to RFC)

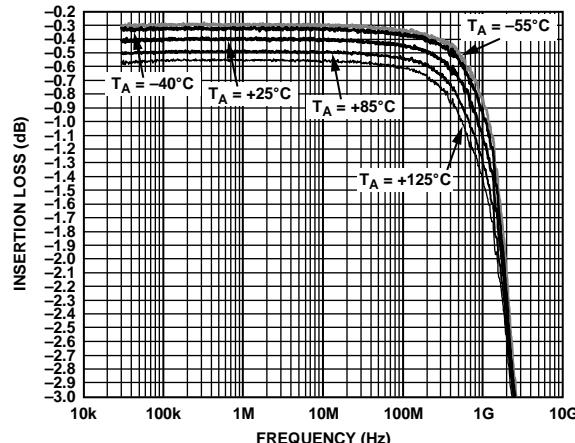


Figure 6. Insertion Loss vs. Frequency over Various Temperature (RFx to RFC)

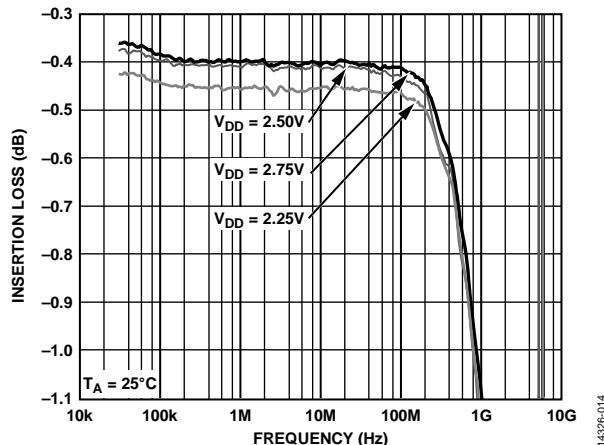


Figure 4. Insertion Loss vs. Frequency for  $V_{DD} > 2.2$  V (RFx to RFC)  
Zoomed View of Figure 3

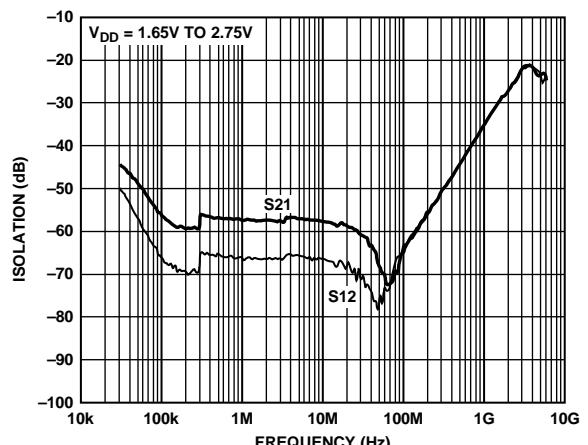


Figure 7. Isolation vs. Frequency over Supplies (RFx to RFC)

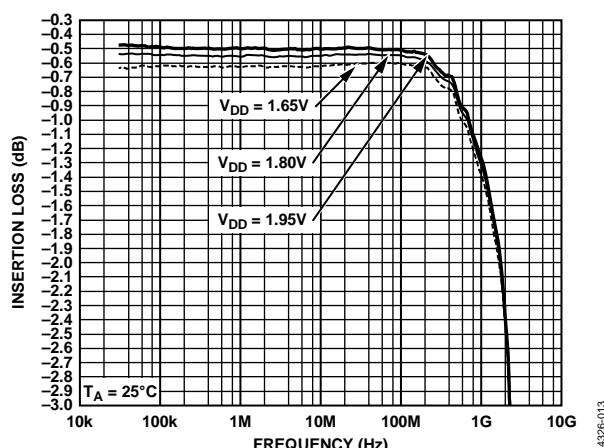


Figure 5. Insertion Loss vs. Frequency for  $V_{DD} < 2$  V (RFx to RFC)

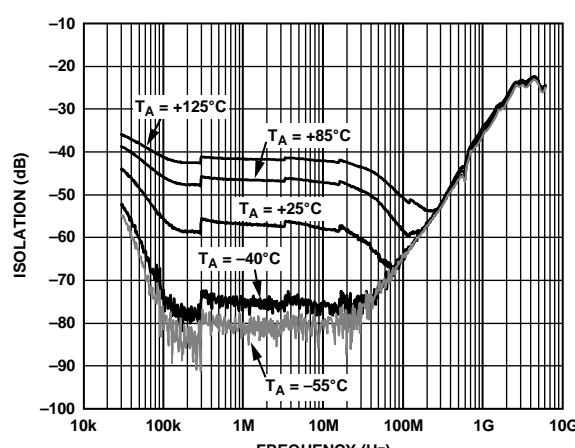


Figure 8. Isolation vs. Frequency over Various Temperature (RFx to RFC)

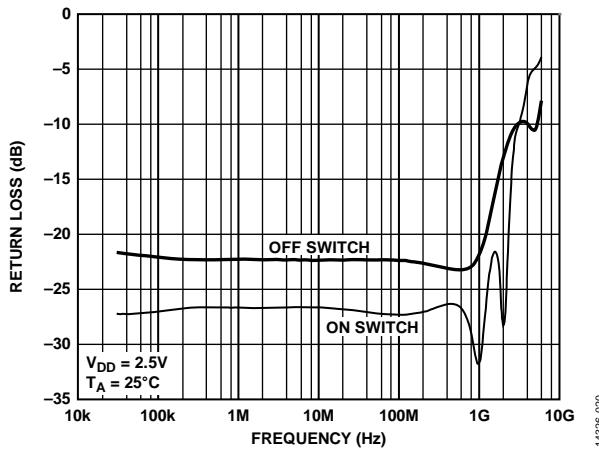


Figure 9. Return Loss vs. Frequency (RFx to RFC)

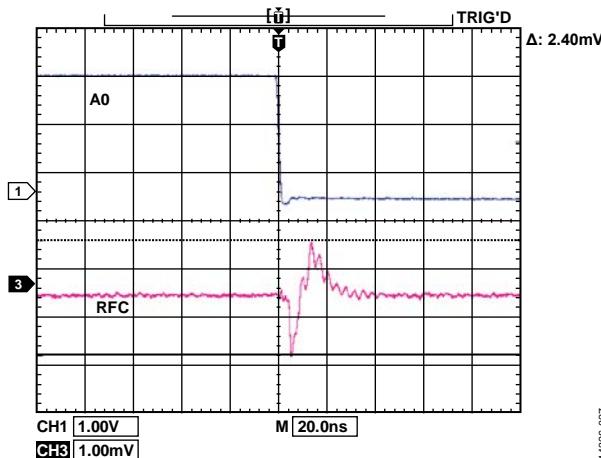


Figure 12. Video Feedthrough

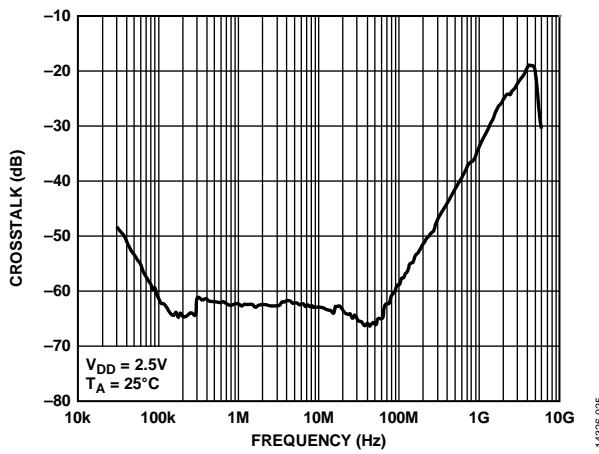


Figure 10. Crosstalk vs. Frequency

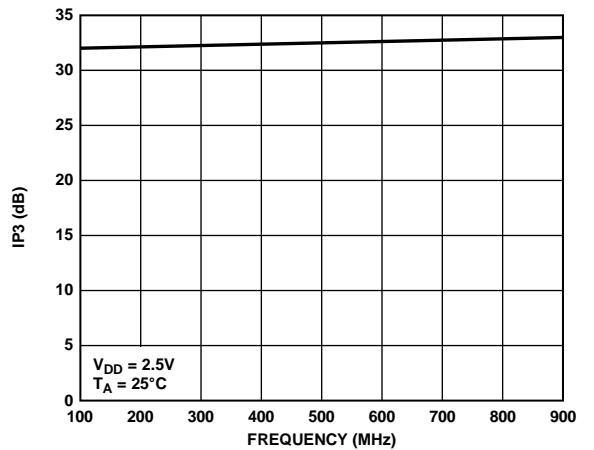


Figure 13. Third-Order Intermodulation Intercept (IP3) vs. Frequency

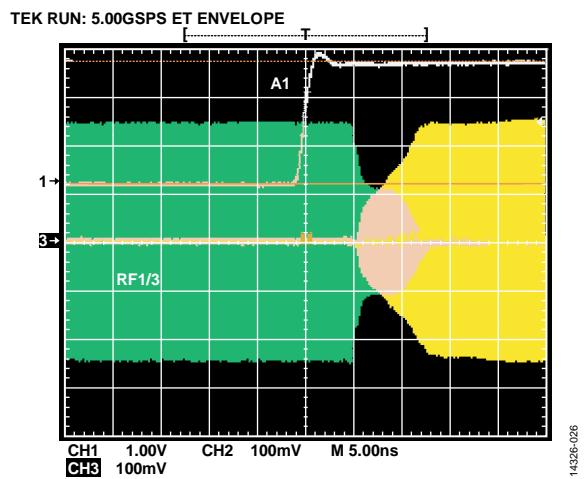


Figure 11. Switch Timing

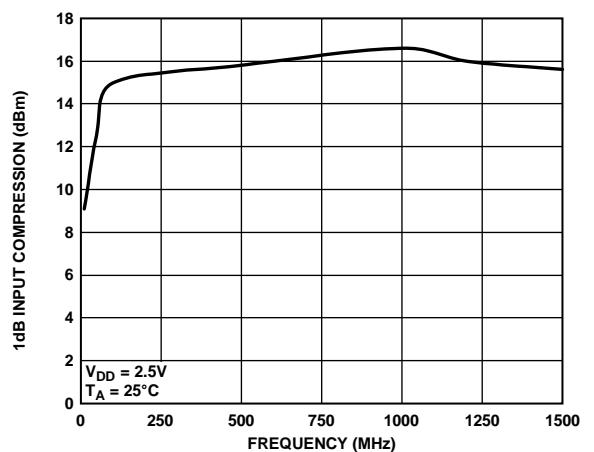
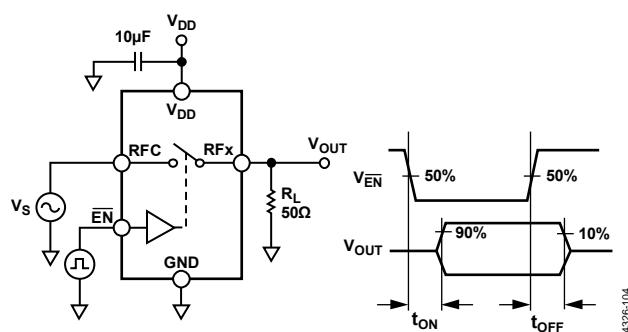
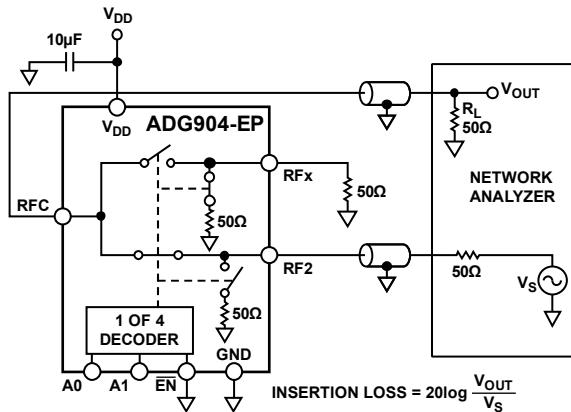


Figure 14. 1 dB Input Compression vs. Frequency (DC Bias Not Used)

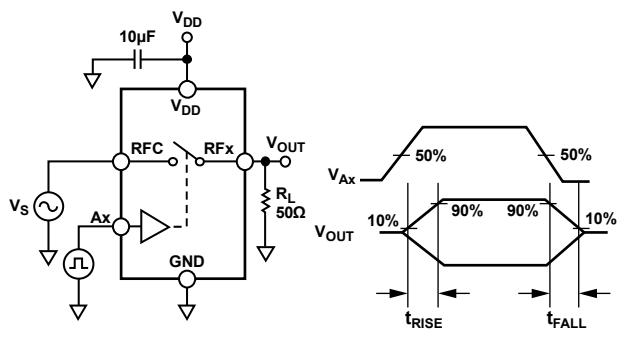
## TEST CIRCUITS



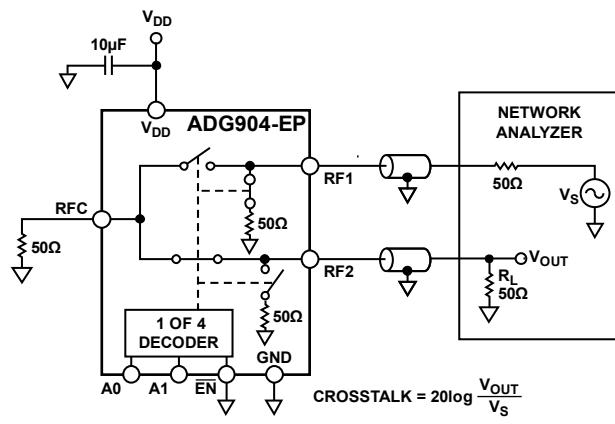
14326-104



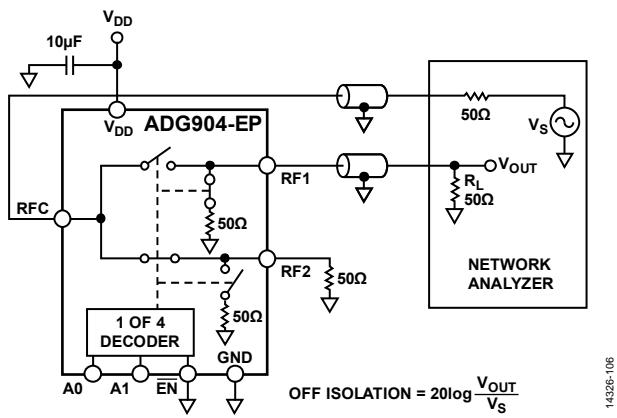
14326-107



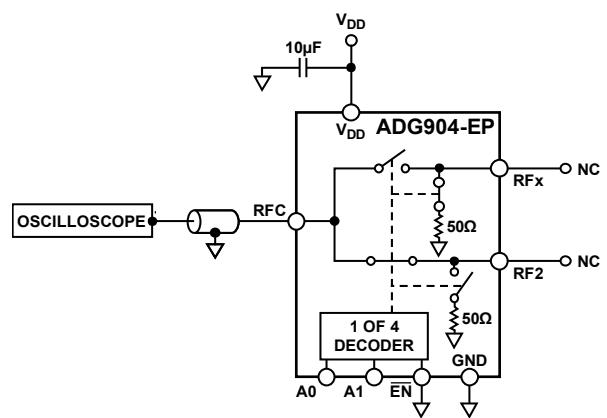
14326-105



14326-108



14326-106



14326-109

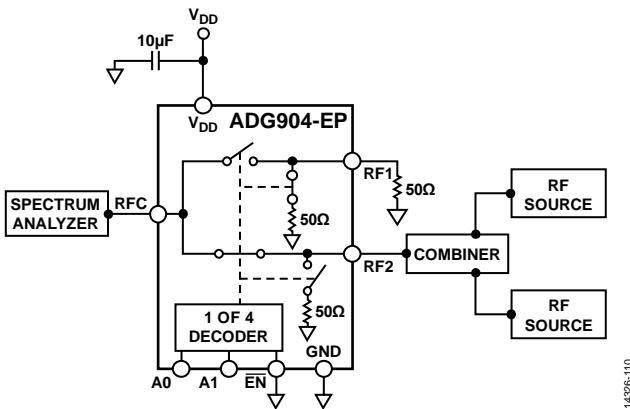


Figure 21. Third-Order Intermodulation Intercept (IP3)

1426-10

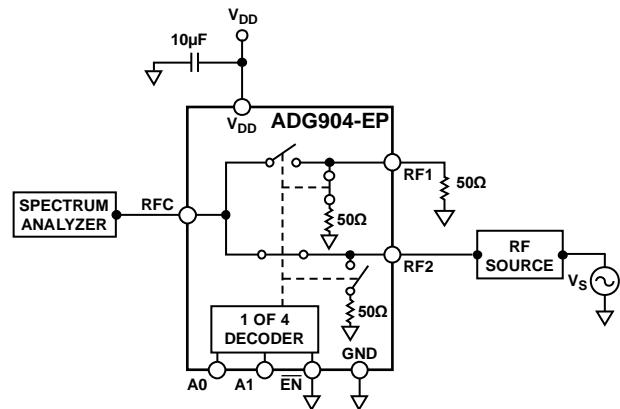


Figure 22. 1 dB Input Compression (P1dB)

1426-11

## OUTLINE DIMENSIONS

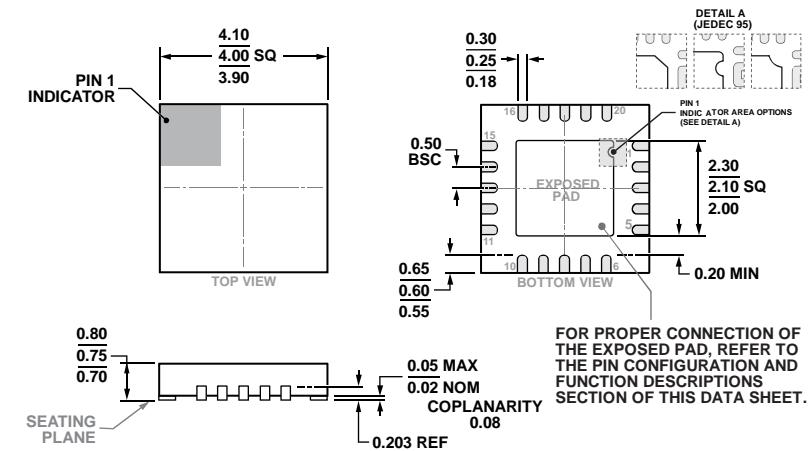


Figure 23. 20-Lead Lead Frame Chip Scale Package [LFCSP]  
 4 mm × 4 mm Body and 0.75 mm Package Height  
 (CP-20-6)

Dimensions shown in millimeters

02-13-2017-B

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG904SCPZ-EP	−55°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
ADG904SCPZ-EP-RL7	−55°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6

<sup>1</sup> Z = RoHS Compliant Part.