

# NCP4371

## Qualcomm Quick Charge™ 3.0 HVDCP Controller

NCP4371 is a USB secondary side fast-charging controller, supporting Qualcomm Quick Charge 3.0 (QC 3.0) High Voltage Dedicated Charging Port (HVDCP) Class A and Class B specification. NCP4371 allows for selection of the output voltage of an AC-DC USB adapter based on commands from the Portable Device (PD) being powered. Selecting a higher charging voltage will reduce the charging current for a given power level resulting in reduced IR drops and increased system efficiency. Another advantage of QC3.0 is a decreased battery charging time and a reduced PD system cost thanks to the ability to select an optimum charging voltage. This eliminates the need for costly DC-DC converters within the PD. The USB-bus voltage can be controlled in discreet steps from 3.6 V up to 20 V. The output current is limited not to exceed maximum allowable power level.

The NCP4371 resides at the secondary (isolated) side of the adapter. It includes voltage and current feedback regulation eliminating the need for a shunt regulator such as TL431.

The NCP4371 provides charging current limits down to  $V_{BUS} = 2.2$  V protecting the portable device from excessive currents in case of a soft short-circuit condition.

The NCP4371 integrates a safe-discharge circuitry to quickly and reliably discharge output capacitors in case the USB cable is unplugged or connected to a 5 V only USB port.

### Features

- Supports Qualcomm Quick Charge 3.0 HVDCP Class A/B
- Output Voltage Can be Configured in Discreet Steps from
  - ◆ Class A: 3.6 V up to 12 V
  - ◆ Class B: 3.6 V up to 20 V
- Compatible with USB Battery Charging Specification Revision 1.2 (USB BC1.2)
- Constant Voltage and Constant Current Regulation
- Soft Short-Circuit Current Limitation Down to  $V_{BUS} = 2.2$  V
- Removes a Need for the Secondary Side Shunt Regulator such as TL431
- Output Capacitor Safe-Discharge Circuitry at Cable Unplug
- Fast Dynamic Response
- Built-in Power Limiting Function
- Low Supply Current
- Wide Operating Input Voltage Range: 2.2 V to 28 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

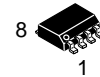
### Typical Applications

- Fast Charging AC/DC Adapters for Smart Phones, Tablets and Other Portable Devices



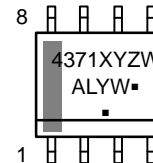
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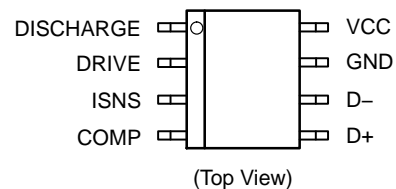
### MARKING DIAGRAM



4371XYZW = Specific Device Code  
(See Device Options Table)

A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 13 of this data sheet.

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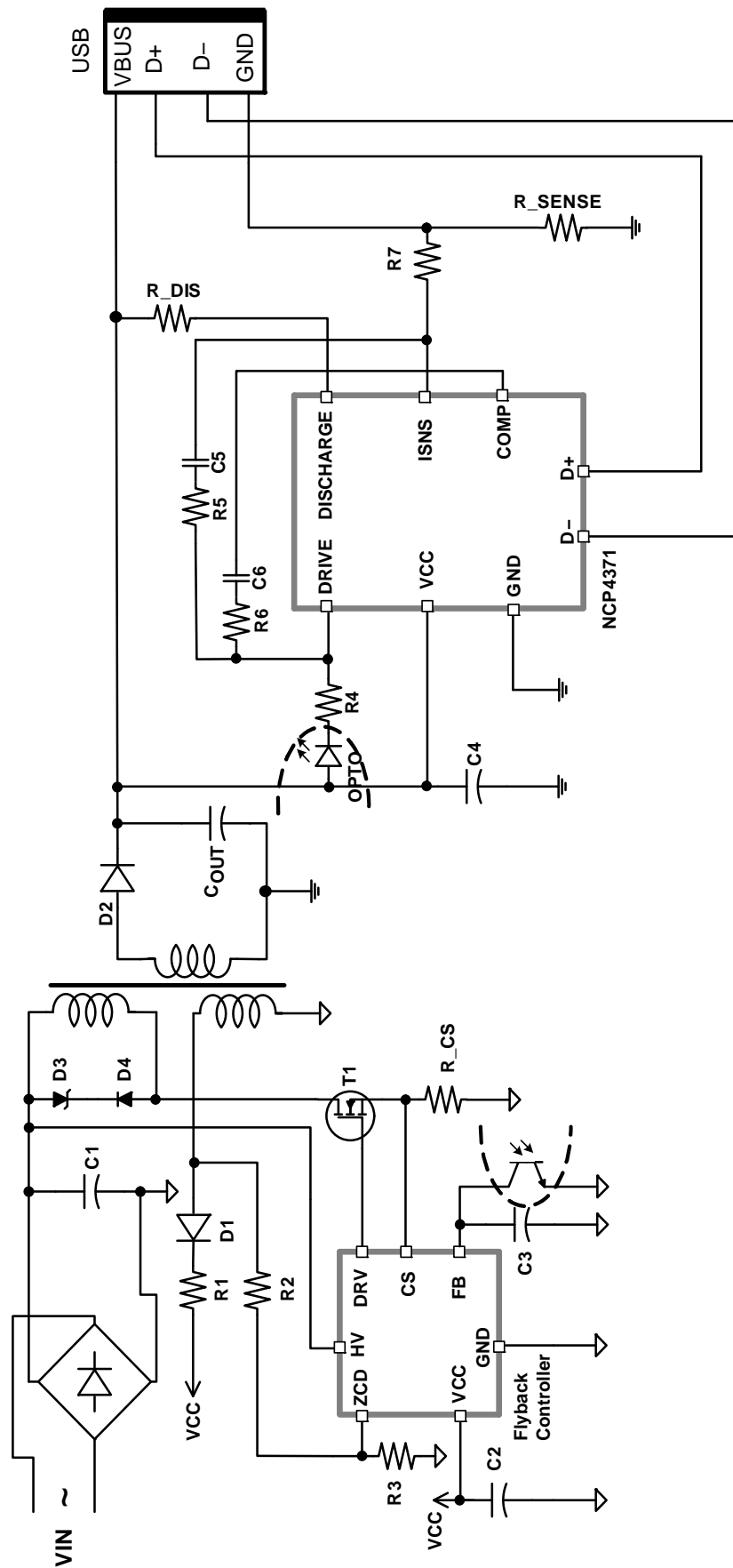
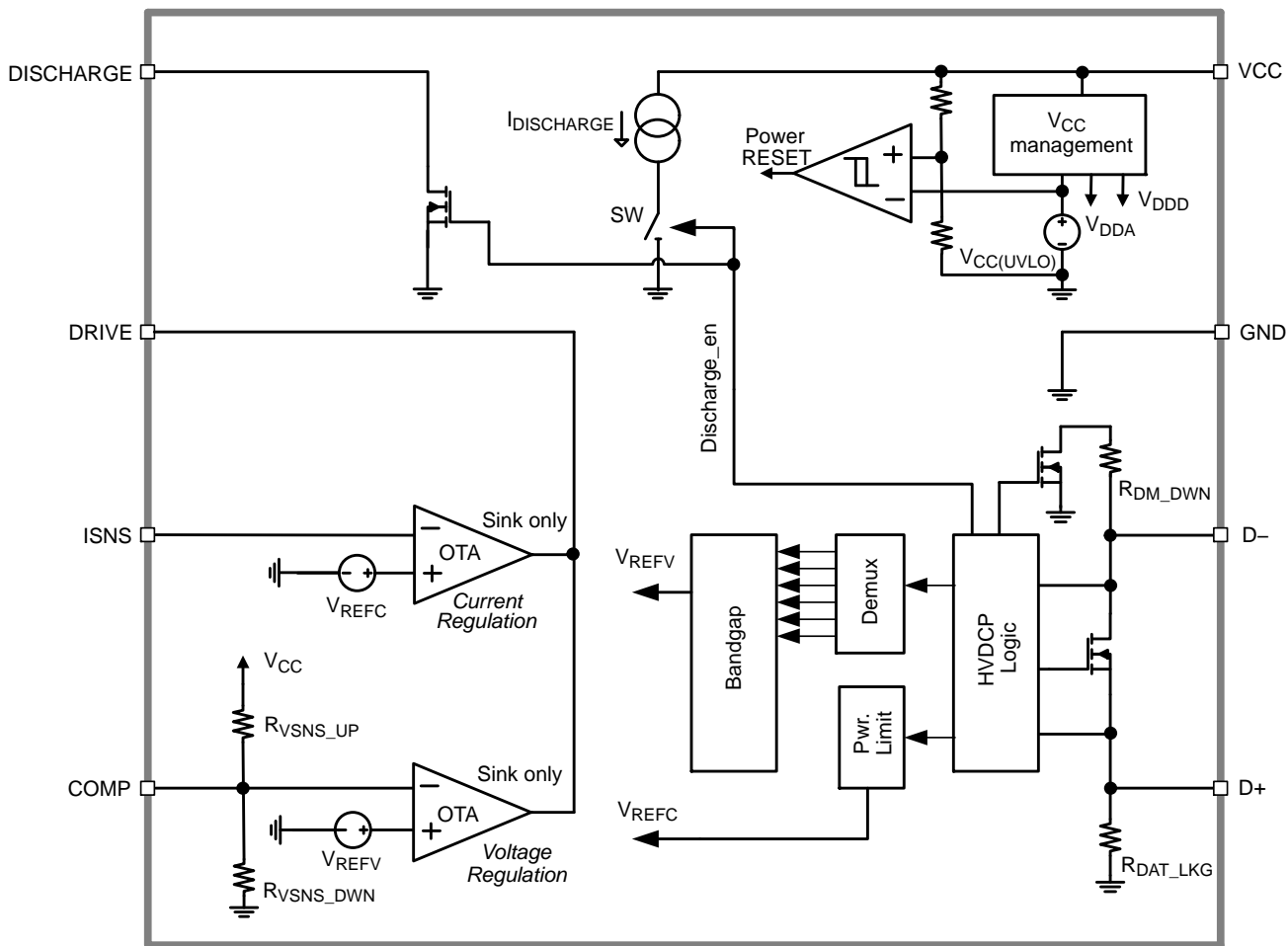


Figure 1. Typical Application Schematic

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**Figure 2. Simplified Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin No. | Pin Name  | Description   |
|---------|-----------|---|
| 1       | DISCHARGE | This output is used to safely discharge $V_{BUS}$ output capacitors when an unplug event is detected  |
| 2       | DRIVE     | Output of current sinking OTA amplifier or amplifiers driving feedback optocoupler's LED. Connect here compensation network (networks) as well. |
| 3       | ISNS      | Current sensing input for output current regulation, connect it to shunt resistor in ground branch.   |
| 4       | COMP      | Compensation pin of output voltage regulation, connected to a feedback compensation network.  |
| 5       | D+        | USB D+ Data Line Input  |
| 6       | D-        | USB D- Data Line Input  |
| 7       | GND       | Ground  |
| 8       | VCC       | Supply voltage pin  |

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**Table 2. MAXIMUM RATINGS**

| Rating  | Symbol                               | Value                        | Unit          |
|---|--------------------------------------|------------------------------|---------------|
| Supply Voltage                                | $V_{CC}$                             | -0.3 to 28.0<br>$\pm 100$    | V<br>mA       |
| DISCHARGE pin                                 | $V_{DISCHARGE}$                      | -0.3 to $V_{CC}$<br>+500/-40 | V<br>mA       |
| DRIVE pin                                     | $V_{DRIVE}$                          | -0.3 to $V_{CC}$<br>+100/-90 | V<br>mA       |
| D+, D-, VSNS, ISNS Input Voltage              | $V_{D+}, V_{D-}, V_{VSNS}, V_{ISNS}$ | -0.3 to 5.5<br>$\pm 100$     | V<br>mA       |
| Junction to Air Thermal Resistance, SOIC8     | $R_{\theta J-A, SOIC8}$              | 160                          | $^{\circ}C/W$ |
| Maximum Junction Temperature                  | $T_{JMAX}$                           | 125                          | $^{\circ}C$   |
| Storage Temperature                           | $T_{STG}$                            | -60 to 150                   | $^{\circ}C$   |
| ESD Capability, Human Body Model (Notes 1, 4) | ESD <sub>HBM</sub>                   | 6000                         | V             |
| ESD Capability, Machine Model (Note 1)        | ESD <sub>MM</sub>                    | 200                          | V             |
| ESD Capability, Charged Device Model (Note 1) | ESD <sub>CDM</sub>                   | 750                          | V             |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)  
 ESD Charged Device Model per JEDEC Standard JESD22-C101D  
 Latchup Current Maximum Rating <100 mA per JEDEC standard: JESD78 with respect to max. ratings table values
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
4. D+ vs. D- pin capability HBM 2500 V

**Table 3. ELECTRICAL CHARACTERISTICS**

-40 $^{\circ}C \leq T_J \leq 125^{\circ}C$ ;  $V_{CC} = 5 V$ ; unless otherwise noted. Typical values are at  $T_J = +25^{\circ}C$ .

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

**SUPPLY**

|                                 |  |               |     |     |     |         |
|---------------------------------|--|---------------|-----|-----|-----|---------|
| Minimum Operating Input Voltage | $V_{CC}$ voltage at which current limiting OTA is enabled                        | $V_{CC(min)}$ | -   | -   | 2.2 | V       |
| $V_{CC}$ HVDCP Logic Enable     | $V_{CC}$ increasing level at which the HVDCP commands are accepted               | $V_{CC(ON)}$  | 2.9 | 3.2 | 3.4 | V       |
| $V_{CC}$ HVDCP Logic Disable    | $V_{CC}$ decreasing level at which the HVDCP commands are stopped to be accepted | $V_{CC(OFF)}$ | 2.7 | 3.0 | 3.2 | V       |
| Quiescent Current               |  | $I_{CC}$      |     |     | 300 | $\mu A$ |

**VOLTAGE CONTROL LOOP OTA**

|  |                       |                 |      |      |      |            |
|--|-----------------------|-----------------|------|------|------|------------|
| Transconductance                                 | Sink current only     | $g_{mv}$        | -    | 1    | -    | S          |
| Voltage Control Reference Voltage                | Nominal $V_{BUS}=5 V$ | $V_{REFV}$      | 1.21 | 1.25 | 1.29 | V          |
| Sink Current Capability                          |                       | $I_{SINKV}$     | 2.0  |      |      | mA         |
| Output Voltage Sense Divider Resistor, Pull-Up   |                       | $R_{VSNS\_UP}$  |      | 66   |      | k $\Omega$ |
| Output Voltage Sense Divider Resistor, Pull-Down |                       | $R_{VSNS\_DWN}$ |      | 24   |      | k $\Omega$ |

**CURRENT CONTROL LOOP OTA**

|                                   |                                     |               |    |    |    |    |
|-----------------------------------|-------------------------------------|---------------|----|----|----|----|
| Transconductance                  | Sink current only                   | $g_{mc}$      | -  | 3  | -  | S  |
| Current Control Reference Voltage | Current limit A reference set-point | $V_{REFC(A)}$ | 10 | 14 | 18 | mV |
|                                   | Current limit B reference set-point | $V_{REFC(B)}$ | 12 | 17 | 21 |    |
|                                   | Current limit C reference set-point | $V_{REFC(C)}$ | 18 | 22 | 26 |    |
|                                   | Current limit D reference set-point | $V_{REFC(D)}$ | 24 | 28 | 32 |    |
|                                   | Current limit E reference set-point | $V_{REFC(E)}$ | 29 | 33 | 37 |    |
|                                   | Current limit F reference set-point | $V_{REFC(F)}$ | 34 | 38 | 42 |    |
|                                   | Current limit G reference set-point | $V_{REFC(G)}$ | 40 | 44 | 48 |    |
|                                   | Current limit H reference set-point | $V_{REFC(H)}$ | 53 | 57 | 61 |    |

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**Table 3. ELECTRICAL CHARACTERISTICS**

-40°C ≤ T<sub>J</sub> ≤ 125°C; V<sub>CC</sub> = 5 V; unless otherwise noted. Typical values are at T<sub>J</sub> = +25°C.

| Parameter                           | Test Conditions  | Symbol                | Min   | Typ   | Max  | Unit |
|-------------------------------------|--|-----------------------|-------|-------|------|------|
| <b>CURRENT CONTROL LOOP OTA</b>     |  |                       |       |       |      |      |
| Sink Current Capability             |  | I <sub>SINKC</sub>    | 2.0   |       |      | mA   |
| <b>HVDCP</b>                        |  |                       |       |       |      |      |
| Output Voltage Selection Reference  |  | V <sub>SEL_REF</sub>  | 1.8   | 2     | 2.2  | V    |
| Data Detect Voltage                 |  | V <sub>DAT_REF</sub>  | 0.25  | 0.325 | 0.4  | V    |
| Data Line Leakage Resistance        |  | R <sub>DAT_LKG</sub>  | 300   | -     | 1500 | kΩ   |
| D- Pull-Down Resistance             |  | R <sub>DM_DWN</sub>   | 14.25 | 19.53 | 24.8 | kΩ   |
| D+ to D- Resistance During DCP Mode |  | R <sub>DCP_DAT</sub>  |       |       | 45   | Ω    |
| <b>OUTPUT CAPACITOR DISCHARGER</b>  |  |                       |       |       |      |      |
| Discharge Comparator OFF Voltage    | V <sub>BUS_REF</sub> = 5 V, V <sub>DIS(OFF)</sub> sensed at VCC pin  | V <sub>DIS(OFF)</sub> |       | 5.2   |      | mV   |
| VCC Discharge Current               | Discharge current of the internal current sink at the VCC pin  | I <sub>DIS(VCC)</sub> |       |       | 90   | mA   |
| DISCHARGE Pin Maximum Sink Current  | Maximum sink current of the DISCHARGE pin<br>Minimum recommended external discharge resistor value connected from V <sub>BUS</sub> to DISCHARGE pin is R <sub>DIS</sub> ≥ 70 Ω (Class A)<br>R <sub>DIS</sub> ≥ 120 Ω (Class B) | I <sub>DIS(EXT)</sub> |       | 150   |      | mA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

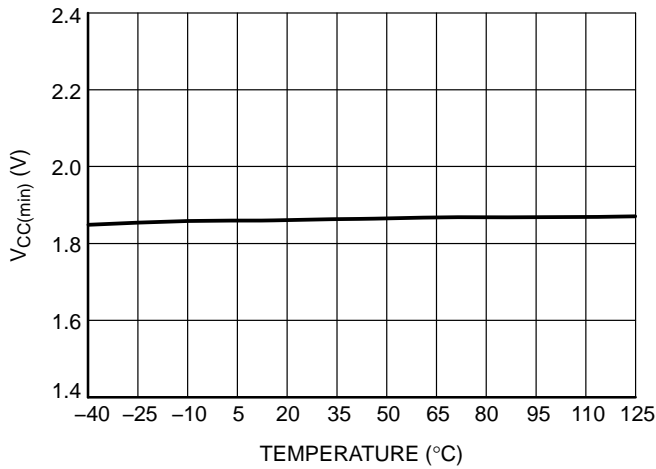


Figure 3. V<sub>CC</sub> Minimum Operating Input Voltage, V<sub>CC(min)</sub>

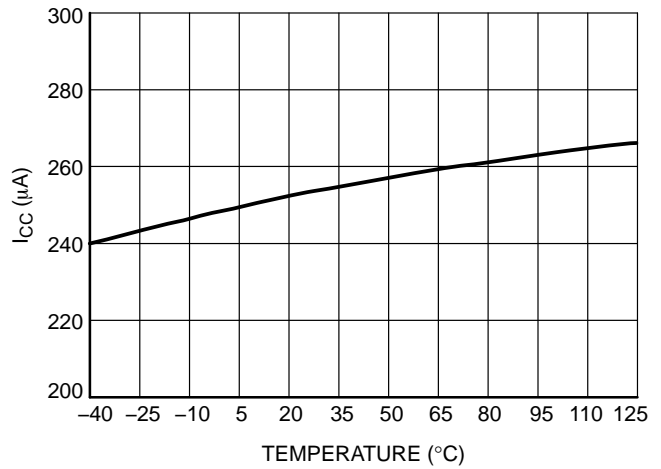


Figure 4. Quiescent Current, I<sub>CC</sub>

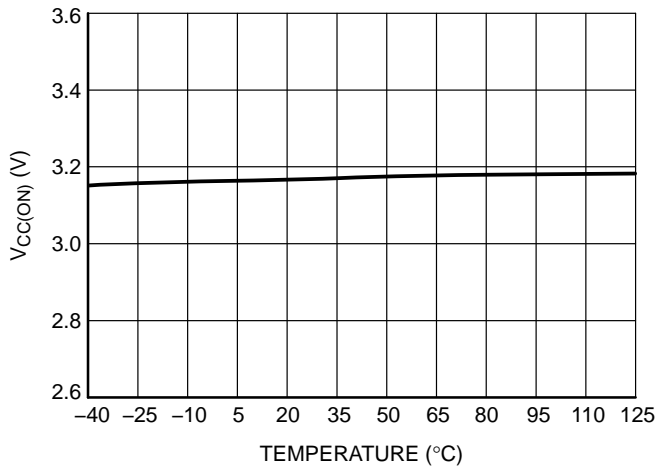


Figure 5. V<sub>CC</sub> HVDCP Logic Enable, V<sub>CC(ON)</sub>

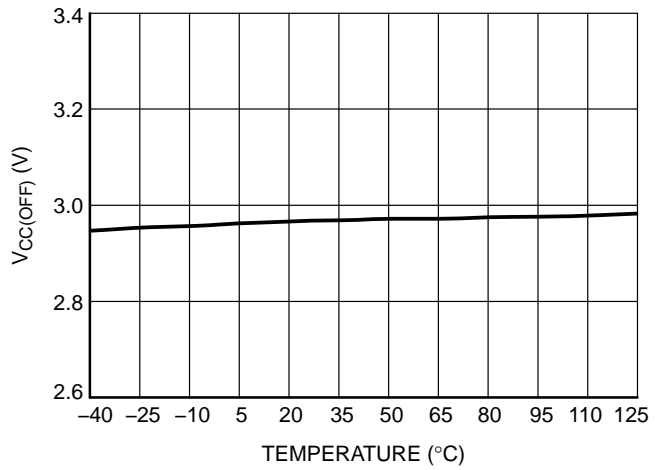


Figure 6. V<sub>CC</sub> HVDCP Logic Disable, V<sub>CC(OFF)</sub>

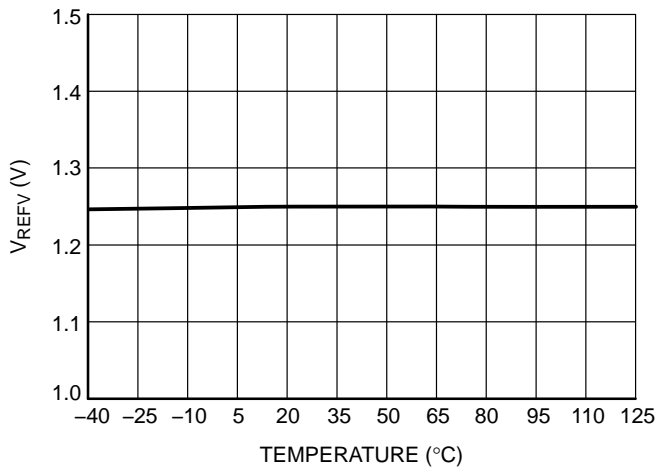


Figure 7. Voltage Control Reference Voltage, V<sub>REFV</sub>

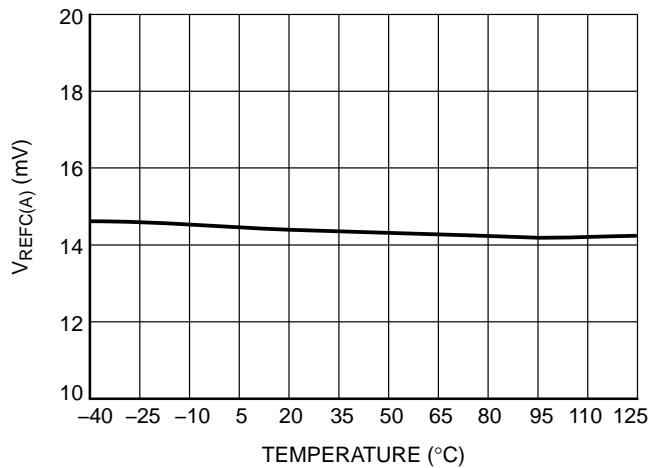


Figure 8. Current Control Reference Voltage, V<sub>REFC(A)</sub>

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## TYPICAL CHARACTERISTICS

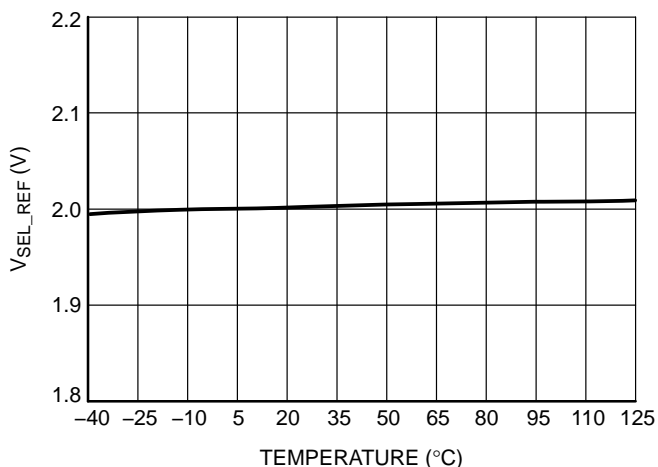


Figure 9. Output Voltage Selection Reference, V<sub>SEL\_REF</sub>

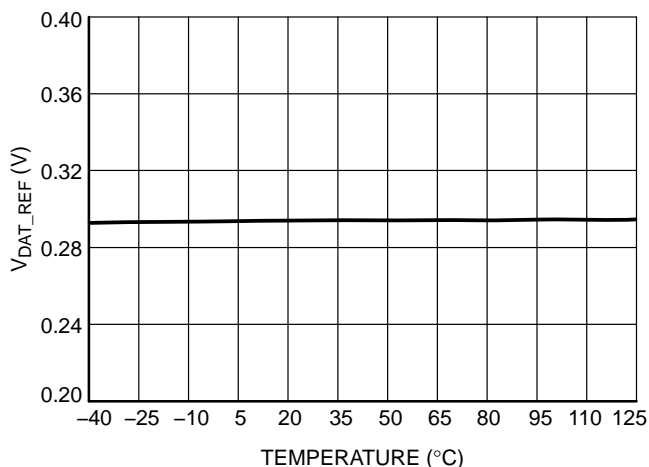


Figure 10. Data Detect Voltage, V<sub>DAT\_REF</sub>

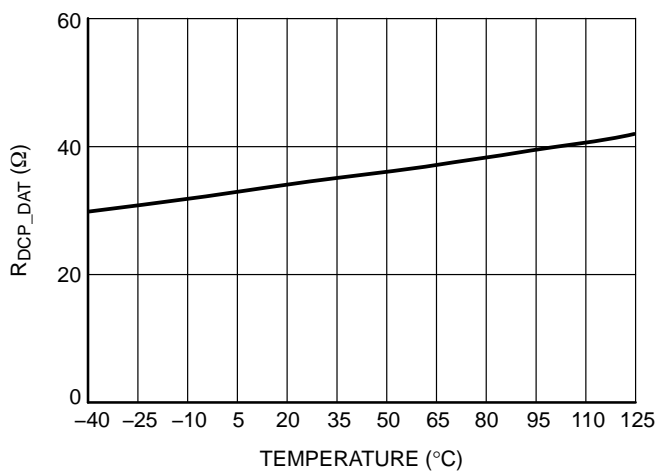


Figure 11. D+ to D- Resistance During DCP Mode, R<sub>DCP\_DAT</sub>

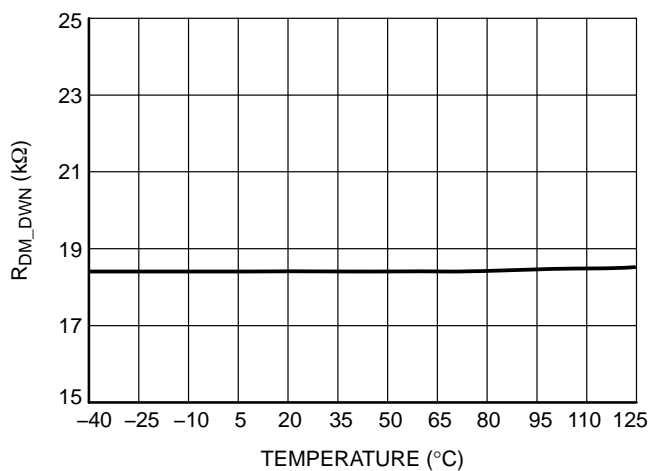


Figure 12. D- Pull-Down Resistance, R<sub>DM\_DWN</sub>

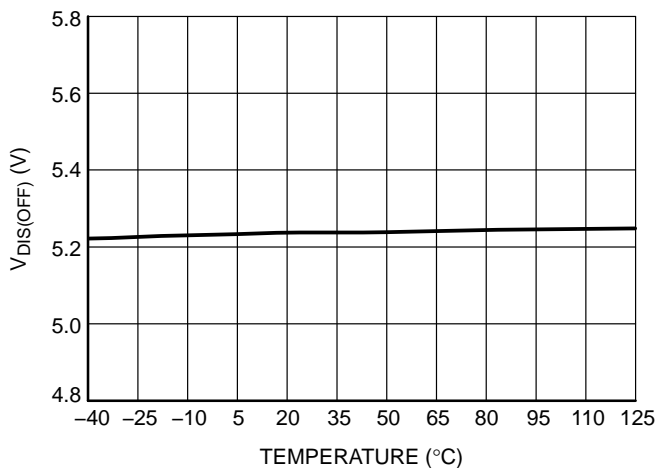


Figure 13. Discharge Comparator OFF Voltage, V<sub>DIS(OFF)</sub>

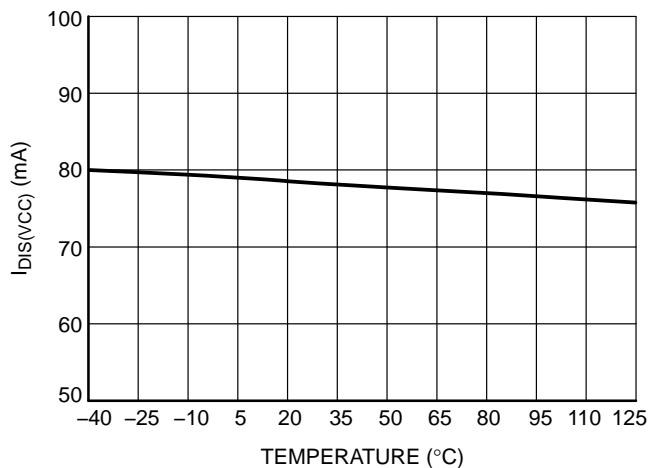


Figure 14. VCC Discharge Current, I<sub>DIS(VCC)</sub>

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## TYPICAL CHARACTERISTICS

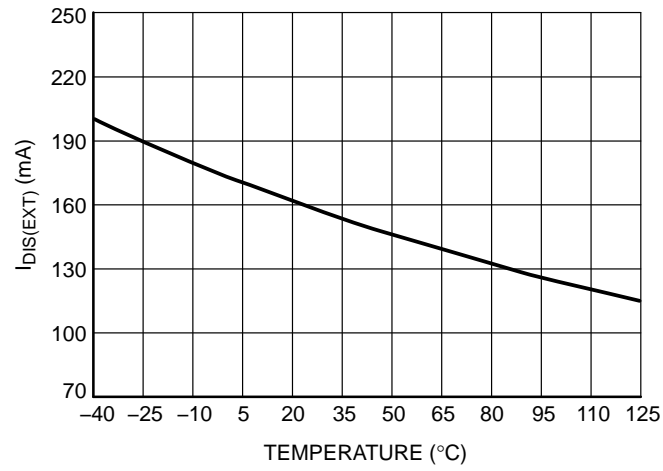


Figure 15. VCC Discharge Current,  $I_{DIS(EXT)}$



APPLICATION INFORMATION

The NCP4371 is designed to operate as an output voltage and current controller for USB chargers, which resides on the secondary side of the off-line adapter. It enables to accommodate the output voltage based on the request from the portable device in order to optimize the battery charge time. The NCP4371 is compatible with Qualcomm Quick Charge 3.0 HVDCP specification. The output voltage can be increased or decreased in discrete steps. The output current is limited not to exceed the maximum power limit for given output voltage level. The internal discharge switch discharges the output capacitors to a safe voltage level in a case of the cable unplug.

Voltage Regulation

The Voltage Regulation Path eliminates a need for a voltage shunt regulator at the secondary side of the off-line supply. The voltage on VCC pin is divided by internal resistor divider ( $R_{VSNS\_UP}$ ,  $R_{VSNS\_DWN}$ ) and compared with the internal precise voltage reference  $V_{REFV}$ . The voltage difference is amplified by  $g_{mV}$  of the transconductance amplifier. The amplifier output current is connected to the DRIVE pin. This DRIVE pin drives regulation optocoupler that provides regulation of primary side. The internal voltage reference  $V_{REFV}$  is adjustable based on the command from the Portable Device compatible with Qualcomm Quick Charge specification. The voltage control loop compensation network shall be connected between DRIVE and COMP pins.

Current Regulation

The output current is sensed by the shunt resistor  $R_{SENSE}$  in series with the load. Voltage drop on  $R_{SENSE}$  is compared with internal precise voltage reference  $V_{REFC}$  at ISNS transconductance amplifier input. Voltage difference is amplified by  $g_{mC}$  to output current of amplifier, connected to the DRIVE pin.

HVDCP Mode

After power-up pins D+ and D- of NCP4371 are shorted with impedance  $R_{DCP\_DAT}$  and internal reference voltage  $V_{REFV}$  is set to  $V_{BUS}$  voltage 5 V. The device is in a BC1.2 compatible mode. If a portable device compatible with the Qualcomm Quick Charge specification is connected a negotiation between HVDCP and PD is executed. Once the negotiation is successful the NCP4371 opens D+ and D- short connection and D- is pulled down with a  $R_{DM\_DWN}$ . The NCP4371 enters HVDCP mode. It monitors D+ and D- inputs. Based on the specified control patterns the internal voltage reference value  $V_{REFV}$  is adjusted in order to increase or decrease output voltage to the required value. The NCP4371 is available in Class A and Class B version. Class A allows to change the output voltage up to  $V_{BUS} = 12$  V. Class B allows output voltage up to 20 V. If the unplug event is detected the decoder circuitry turns-on an internal current sink, which discharges the output capacitors to a safe voltage level. If the NCP4371 is set to a

Continuous mode it responds to the PD requests in a Single request mode. It does not support Group request mode.

Table 4. D+ AND D- OUTPUT VOLTAGE CODING

| Portable Device |       | HVDCP Class A    | HVDCP Class B   |
|-----------------|-------|------------------|-----------------|
| D+              | D-    | Adapter Voltage  | Adapter Voltage |
| 0.6 V           | 0.6 V | 12 V             | 12 V            |
| 3.3 V           | 0.6 V | 9 V              | 9 V             |
| 0.6 V           | 3.3 V | Continuous mode  | Continuous mode |
| 3.3 V           | 3.3 V | Previous voltage | 20 V            |
| 0.6 V           | GND   | 5 V              | 5V              |

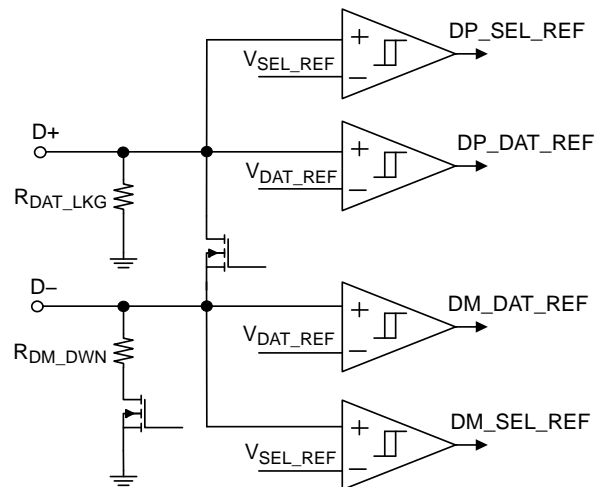


Figure 16. HVDCP D+ and D- Comparators

HVDCP Mode – Continuous Mode

The continuous mode of operation leverages the previously unused state in QC2.0. If the portable devices try and utilize this mode, it applies voltages on D+ and D- per Table 4. Assuming the HVDCP supports this mode of operation, it will glitch filter the request as it currently does, using  $T_{GLITCH\_V\_CHANGE}$ . Before the portable device can begin to increment or decrement the voltage, it must wait  $T_{V\_NEW\_REQUEST\_CONT}$  before pulling D+ and D- high or low. Once this time has finished, the portable device now attempts to increment or decrement the voltage. To increment, the portable device sends a pulse of width  $T_{ACTIVE}$  by pulling D+ to  $V_{DP\_UP}$  and then must return D+ to  $V_{DP\_SRC}$  for  $T_{INACTIVE}$ .

The NCP4371 responds to the increment/decrement request in a single request mode, i.e. the output voltage is changed immediately with each request. For the single request, and HVDCP recognizes a rising edge on D+ for an increment, and falling edge on D- for a decrement, and glitch filters this with  $T_{GLITCH\_CONT\_CHANGE}$ . After this period, it begins changing its output voltage by incrementing or decrementing in a 200 mV step. The output voltage is at its final value within  $T_{V\_CONT\_CHANGE\_SINGLE}$ .

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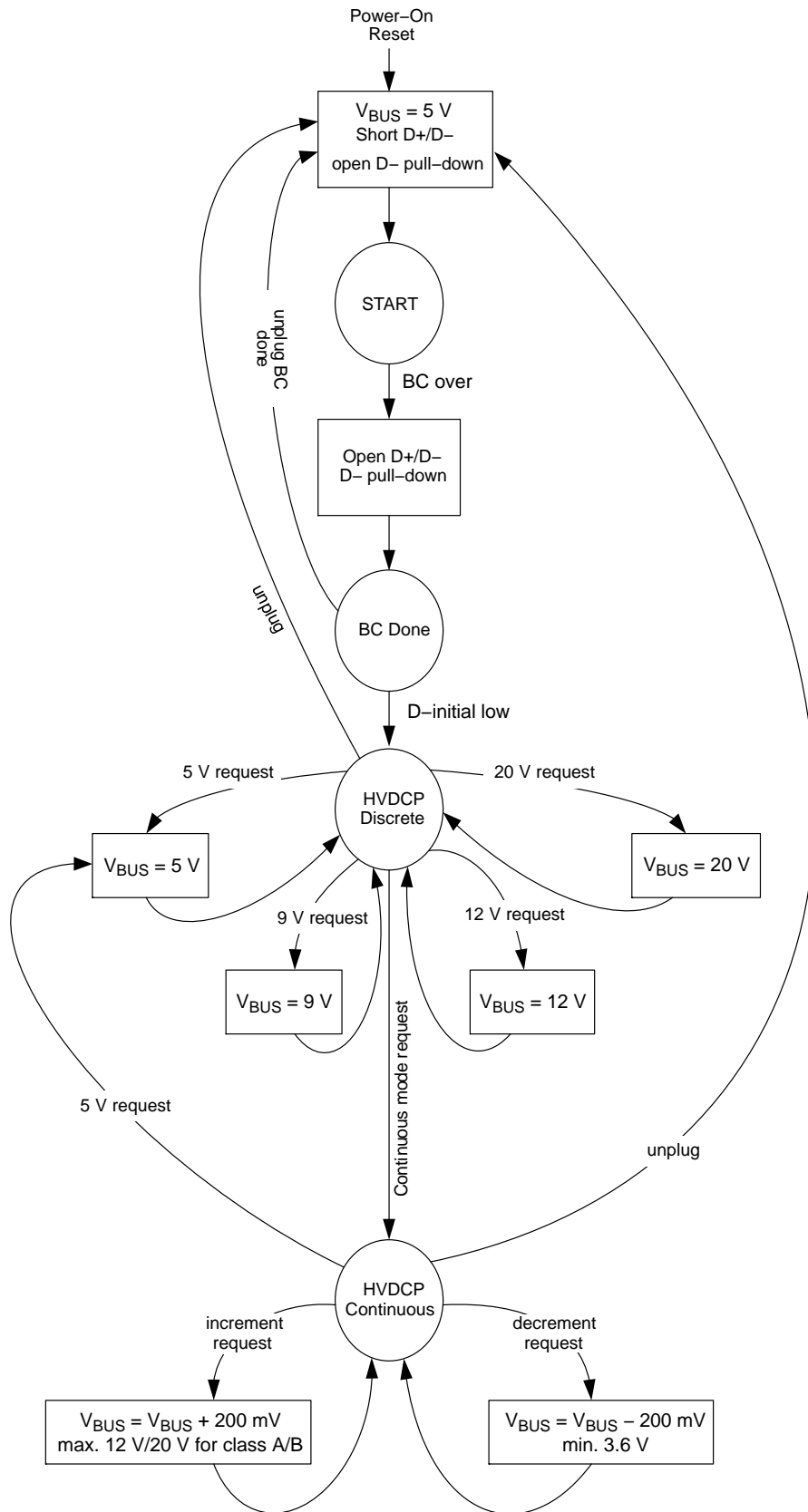


Figure 17. NCP4371 State Diagram

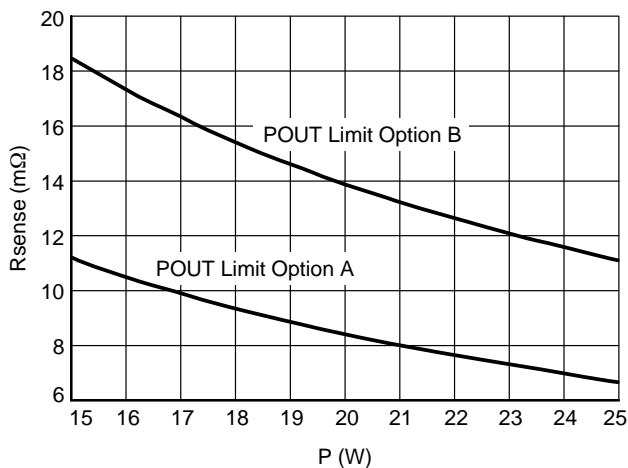
**Power Limit**

The protocol decoder and the power limit logic will limit maximum output current to keep regulation within recommended  $V_{out}/I_{out}$  operating range. The Power Limit block adjusts  $V_{REFC}$  voltage reference at the current regulation loop in order to limit the maximum output current.

The NCP4371 is designed to give a user a high degree of freedom to optimize maximum power and current limit profile of the target application. The user can scale both – maximum output power and maximum current limit independently.

The NCP4371 has two constant power curves defined – “Option A” for Class A only and “Option B” for either Class A or Class B. Power Option C shall be used for applications where constant power regulation is not required. If Power Option C is selected then power limiting curve is ignored. The applications based on Power Option C operate in “constant current regulation mode”.

In order to scale the power limit curve for the given power a selection of the current sense resistor has to be done. The relation between current sense resistor and output power limit is given by the curves in Figure 18.



**Figure 18. R<sub>SENSE</sub> vs. P<sub>OUT</sub> Limit Curve**

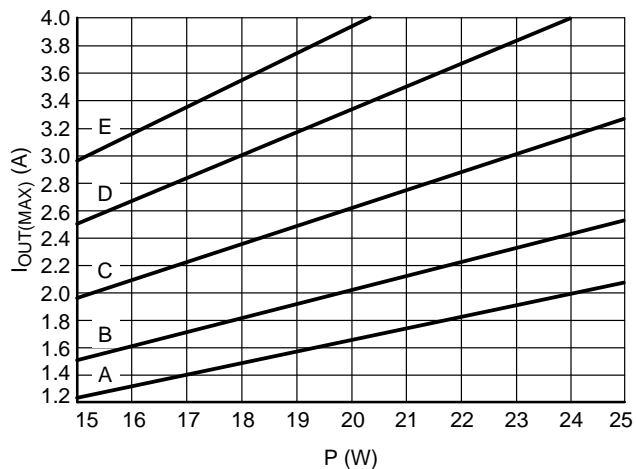
The characteristics in the Figure 23 cover a range P<sub>OUT</sub> = 15 – 25 W. For powers outside this interval following formula can be used for R<sub>SENSE</sub> selection:

Option A (Class A only) :  $R_{SENSE} = \frac{168}{P_{max}}$  [mΩ] (eq. 1)

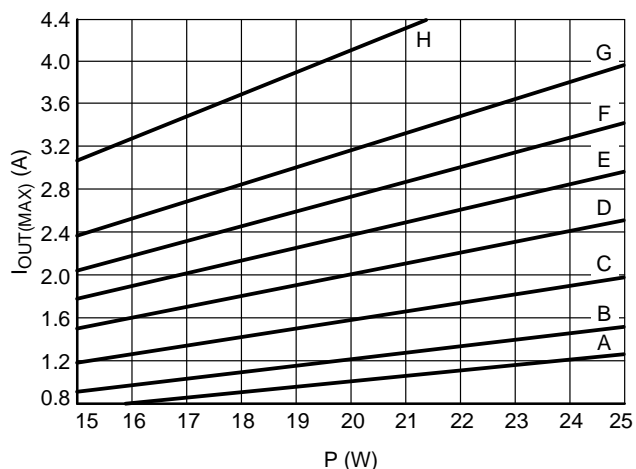
Option B (Class A & B) :  $R_{SENSE} = \frac{277}{P_{max}}$  [mΩ] (eq. 2)

Once the Power limit is defined by an R<sub>SENSE</sub> selection the user needs to define a maximum output current limit. This current limit can be given by a connector or cable maximum current rating.

There are 5 current limit options available for Power Option A and 8 current limit options for Power Option B and C. Each power limit option corresponds to a particular Current Control Reference Voltage ( $V_{REFC}$ ), which limits the maximum output current for the selected R<sub>SENSE</sub> resistor. The user has to make a selection from current limit characteristics shown in Figure 19. Each power limit curve represents a unique device option (see Table Device Options).



**Power Option A Current Limit Selection**



**Power Option B Current Limit Selection**

**Figure 19. Current Limit Characteristics**

Table 5. CURRENT LIMIT OPTION REFERENCE VOLTAGE

| Current Limit Option | A  | B  | C  | D  | E  | F  | G  | H  |
|----------------------|----|----|----|----|----|----|----|----|
| $V_{REFC}[mV]$       | 14 | 17 | 22 | 28 | 33 | 38 | 44 | 57 |

**Soft Short–Circuit Protection**

In case of a short–circuit at the USB cable end or the portable device USB receptacle it is desired to limit the short circuit current to prevent a portable device or cable from a damage. The NCP4371 offers an extended region of output current limiting down to  $V_{BUS} = 2.2 V$ . If the  $V_{BUS}$  falls below  $V_{CC(OFF)}$  then the HVDCP logic is disabled and D+/- pins are shorted. No further commands from the portable device are accepted. The only feature enabled is the output current limiting at the moment. The device stays in the current limiting mode until  $V_{CC}$  rises back above  $V_{CC(ON)}$  threshold. The device logic will resume its operation and goes to a default BC1.2 compatible mode. A new negotiation between the charger and portable device has to be carried out in order to enable HVDCP compatibility mode.

**Discharge**

If voltage level lower than actual  $V_{BUS}$  is requested by PD the discharge circuitry discharges the output capacitors to reach the new voltage level in a short time. As well, the discharge circuitry is activated if cable unplug event is detected. The NCP4371 features two discharge paths. By default, the discharge is done via built–in regulated current source at VCC pin. If the VCC pin discharge capability is not sufficient an external discharge resistor  $R_{DIS}$  has to be used.

The discharge resistor is wired from a positive pole of the output capacitor to the DISCHARGE pin. The minimum recommended value of the discharge resistor  $R_{DIS}$  is  $70 \Omega$  for Class A and  $120 \Omega$  for Class B. The DISCHARGE pin has an internal protection for a case the user wires the pin directly to  $V_{BUS}$ . If this condition is detected the discharge MOSFET at the pin is turned off. It is highly recommended to use an external discharge resistor always if Class B device is used. In case of Class A device and  $C_{OUT} < 1500 \mu F$  the DISCHARGE pin can be left disconnected.

**Dual Discharge Path**

The NCP4371 allows to select between a single discharge path and the dual discharge. By default, if an external discharge resistor  $R_{DIS}$  is connected between a positive pole of the output capacitor and the DISCHARGE pin, the NCP4371 recognize it and the internal discharge path via VCC pin is disabled. Some applications may require even stronger discharge capability or may need to discharge two capacitors connected at two different nodes (USB–Type C output capacitors before and after VBUS switch). The NCP4371 allows to enable a simultaneous function of internal discharge via VCC pin and external DISCHARGE pin. Figure 20 shows an application idea of the dual discharge paths in the USB–Type C adapter design.

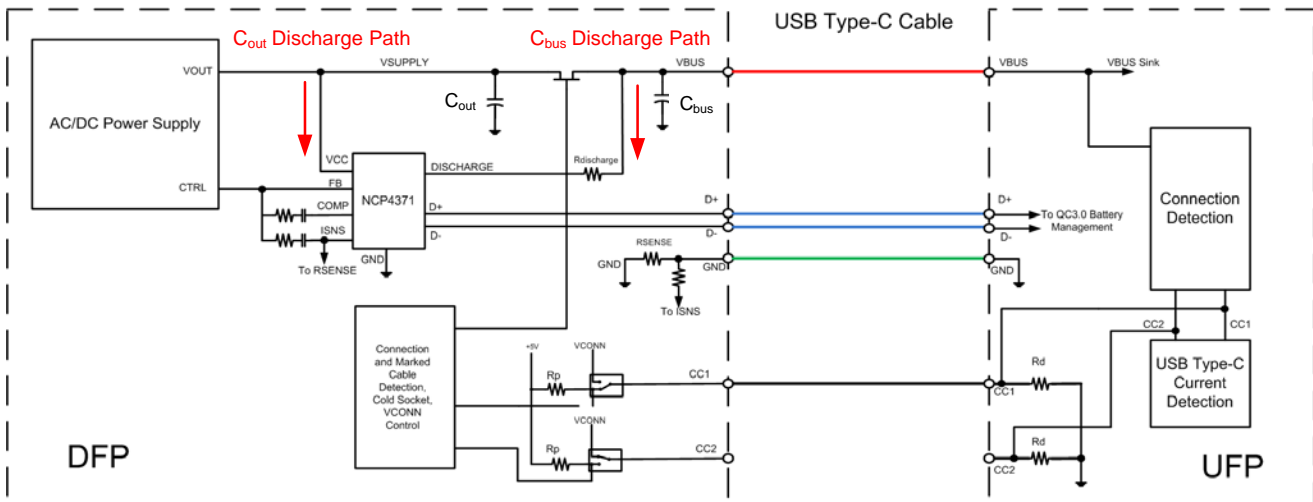


Figure 20. Dual Discharge Path – Application Idea (USB–Type C Adapter)

# NCP4371

**Table 6. DEVICE OPTIONS**

| OPN #<br>NCP4371xyzwDR2G | QuickCharge<br>Class A/B<br>X |         | Power Limit<br>Y |           |                | Current Limit (mV)<br>Z |    |    |    |    |    |    |    | Discharge<br>W |      |
|--------------------------|-------------------------------|---------|------------------|-----------|----------------|-------------------------|----|----|----|----|----|----|----|----------------|------|
|                          | A                             | B       | A                | B         | C              | A                       | B  | C  | D  | E  | F  | G  | H  | S              | D    |
|                          | Class A                       | Class B | Class A          | Class A&B | No Power Limit | 14                      | 17 | 22 | 28 | 33 | 38 | 44 | 57 | Single         | Dual |
| NCP4371AACDR2G           | X                             |         | X                |           |                |                         |    | X  |    |    |    |    |    | X              |      |
| NCP4371AAEDR2G           | X                             |         | X                |           |                |                         |    |    |    | X  |    |    |    | X              |      |
| NCP4371AADDR2G           | X                             |         | X                |           |                |                         |    |    | X  |    |    |    |    | X              |      |
| NCP4371ACCDR2G           | X                             |         |                  |           | X              |                         |    | X  |    |    |    |    |    | X              |      |
| NCP4371BBEDR2G           |                               | X       |                  | X         |                |                         |    |    |    | X  |    |    |    | X              |      |
| NCP4371BBCDDR2G          |                               | X       |                  | X         |                |                         |    | X  |    |    |    |    |    |                | X    |

NOTE: Device option with 4371XYZ marking are single discharge path version exclusively.

## ORDERING INFORMATION

| Device          | Marking  | Package             | Shipping†          |
|-----------------|----------|---------------------|--------------------|
| NCP4371AACDR2G  | 4371AAC  | SOIC-8<br>(Pb-Free) | 2500 / Tape & Reel |
| NCP4371AAEDR2G  | 4371AAE  |                     |                    |
| NCP4371AADDR2G  | 4371AAD  |                     |                    |
| NCP4371ACCDR2G  | 4371ACC  |                     |                    |
| NCP4371BBEDR2G  | 4371BBE  |                     |                    |
| NCP4371BBCDDR2G | 4371BBCD |                     |                    |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

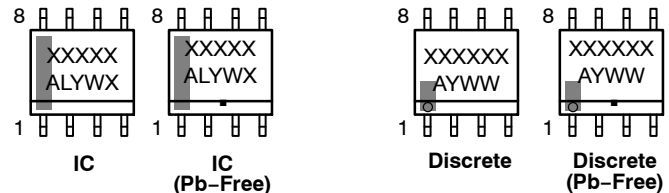
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### STYLES ON PAGE 2

|                  |             |  |
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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC_OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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