TEXAS INSTRUMENTS

SN74LVC1G125-Q1

SGES002D – APRIL 2003 – REVISED AUGUST 2019

SN74LVC1G125-Q1 Single-BUS buffer gate with 3-state output

1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device Human-Body Model (HBM) ESD Classification Level 2
  - Device Charged-Device Model (CDM) ESD Classification Level C5
- Available in the small 1.45-mm^2 package (DRY) With 0.5-mm Pitch
- Supports 5-V V_{CC} Operation
- Over-voltage tolerant inputs accept voltages to 5.5 V
- Provides down translation to V_{CC}
- Max t_{pd} of 3.7 ns at 3.3 V
- Low power consumption, 10-μA Max I_{CC}
- ±24-mA Output drive at 3.3 V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA Per JESD 78, Class II

2 Applications

- Qualified for Automotive Applications
- Increase digital signal drive strength
- Redrive up to 100 MHz square wave signals
- Enable or disable a digital signal with high-impedance off state

3 Description

This bus buffer gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G125-Q1 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G125-Q1 device is available in a variety of packages including the small DRY package with a body size of 1.45 mm × 1.00 mm.

Device Information[1]

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
1P1G125QDCKRQ1	SOT-23 (5)	2.90 mm × 1.60 mm
CLVC1G125QDBVRQ1	SC70 (5)	2.00 mm × 1.25 mm
1P1G125QDRYRQ1	SON (6)	1.45 mm × 1.00 mm

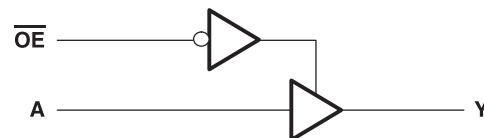(1) For all available packages, see the orderable addendum at the end of the data sheet.
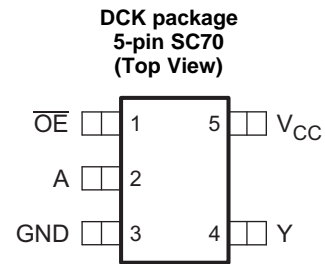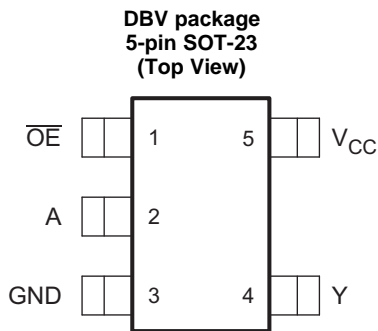
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2008) to Revision D — **Page**

5 Pin Configuration and Functions

**DBV package
5-pin SOT-23
(Top View)**

$\overline{OE}$ — 1 5 — V_{CC}
A — 2
GND — 3 4 — Y

**DCK package
5-pin SC70
(Top View)**

$\overline{OE}$ — 1 5 — V_{CC}
A — 2
GND — 3 4 — Y

**DRY package
6-pin SON
(Transparent Top View)**

$\overline{OE}$ — 1 6 — V_{CC}
A — 2 5 — N.C.
GND — 3 4 — Y

N.C. – No internal connection

See mechanical drawings for dimensions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV, DCK	DRY		
$\overline{OE}$	1	1	Input	Active low Output Enable Input
A	2	2	Input	Input A
GND	3	3	—	Ground
Y	4	4	Output	Output Y
V_{CC}	5	6	—	Positive supply
NC	–	5	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Product Folder Links: *SN74LVC1G125-Q1*

6.3 Recommended Operating Conditions[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

	THERMAL METRIC[(1)]	SN74LVC1G125-Q1			UNIT
		DBV	DCK	DRY	
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	278	439	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164	93	277	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	65	271	°C/W
ψ_{JT}	Junction-to-top characterization parameter	44	2	84	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62	64	271	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	−40 °C to 125 °C			UNIT
				MIN	TYP[1]	MAX	
V_{OH}		I_{OH} = −100 µA	1.65 V to 5.5 V	V_{CC} − 0.1			V
		I_{OH} = −4 mA	1.65 V	1.2			
		I_{OH} = −8 mA	2.3 V	1.9			
		I_{OH} = −16 mA	3 V	2.4			
		I_{OH} = −24 mA	3 V	2.3			
			4.5 V	3.8			
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 8 mA	2.3 V			0.3	
		I_{OL} = 16 mA	3 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
			4.5 V			0.55	
I_I	A or $\overline{OE}$ inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10	µA
I_{OZ}		V_O = 0 to 5.5 V	3.6 V			10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	µA
C_I		V_I = V_{CC} or GND	3.3 V		4		pF

(1)   All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

over recommended operating free-air temperature range of −40°C to 125°C, C_L = 50 pF (unless otherwise noted)
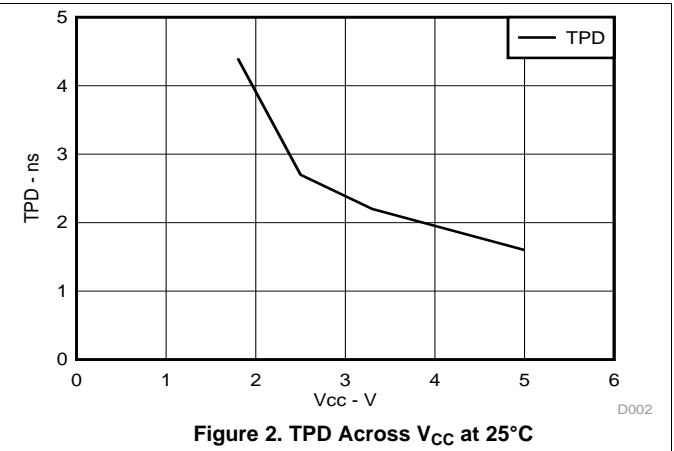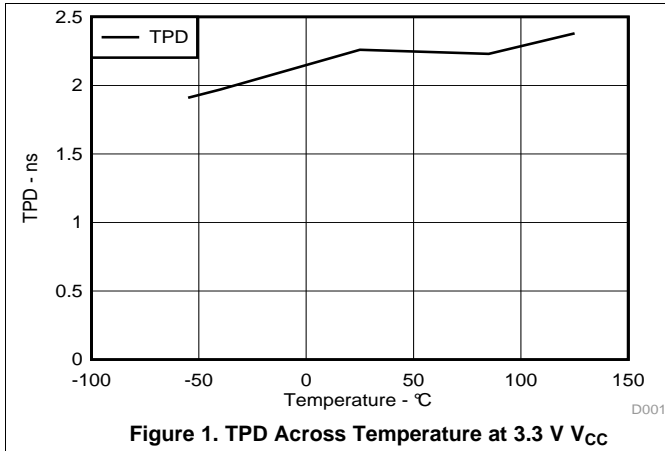(see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1	5.1	1	4.1	ns
t_{en}	$\overline{OE}$	Y	1	6	1	5	ns
t_{dis}	$\overline{OE}$	Y	1	5	1	4.2	ns

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	19	21	pF
		Outputs disabled		2	4	

Product Folder Links: *SN74LVC1G125-Q1*

6.8 Typical Characteristics

Figure 1. TPD Across Temperature at 3.3 V V$_{CC}$
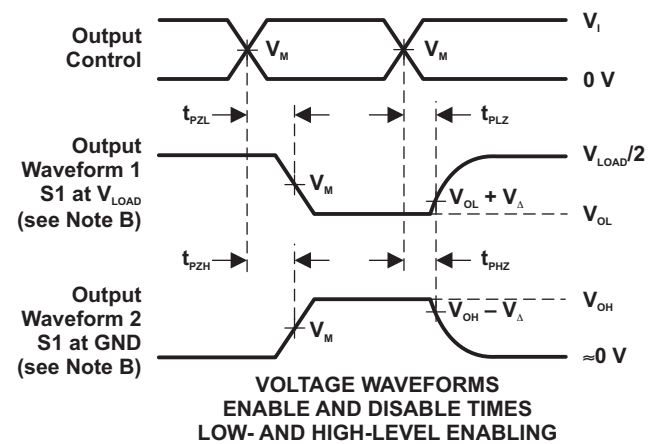
Figure 2. TPD Across V$_{CC}$ at 25°C

7 Parameter Measurement Information

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
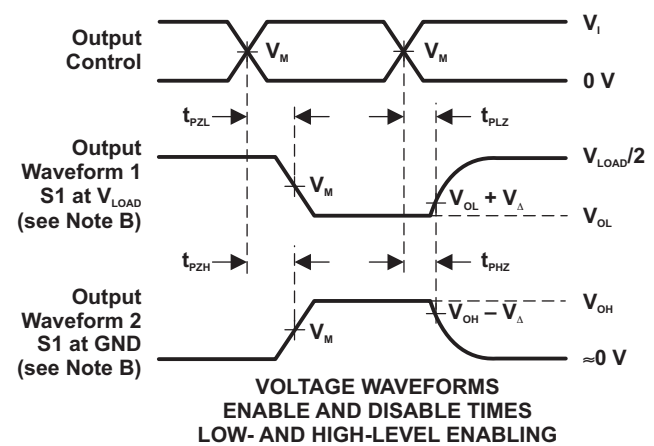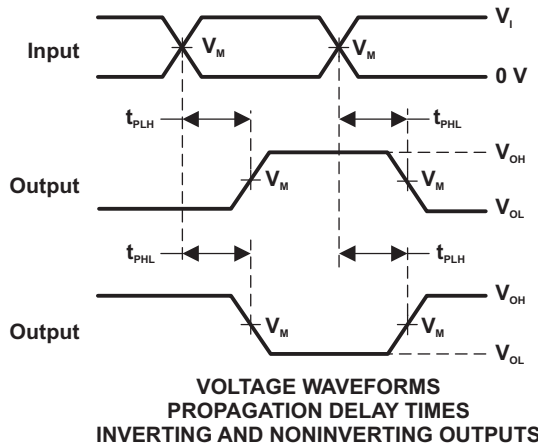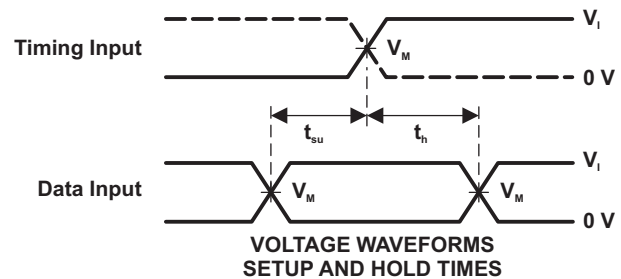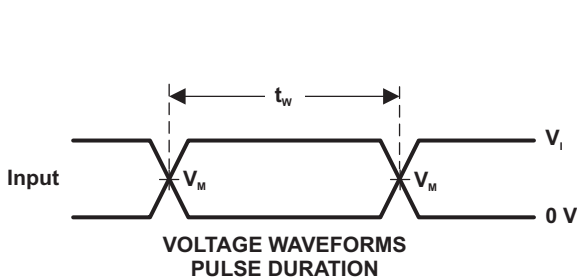H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

Product Folder Links: *SN74LVC1G125-Q1*

Parameter Measurement Information (continued)

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

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NOTES: A. C_L includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
     D. The outputs are measured one at a time, with one transition per measurement.
     E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
     F. t_{PZL} and t_{PZH} are the same as t_{en}.
     G. t_{PLH} and t_{PHL} are the same as t_{pd}.
     H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1G125-Q1 device contains one buffer gate device with output enable control and performs the Boolean function Y = A. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram
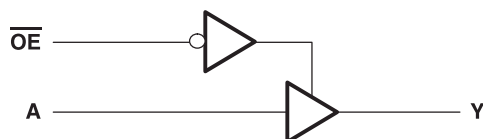
8.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 5.5 V
- Allows down voltage translation
- Inputs accept voltages to 5.5 V
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Product Folder Links: *SN74LVC1G125-Q1*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G125-Q1 device is a high drive CMOS device that can be used as a output enabled buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC}.
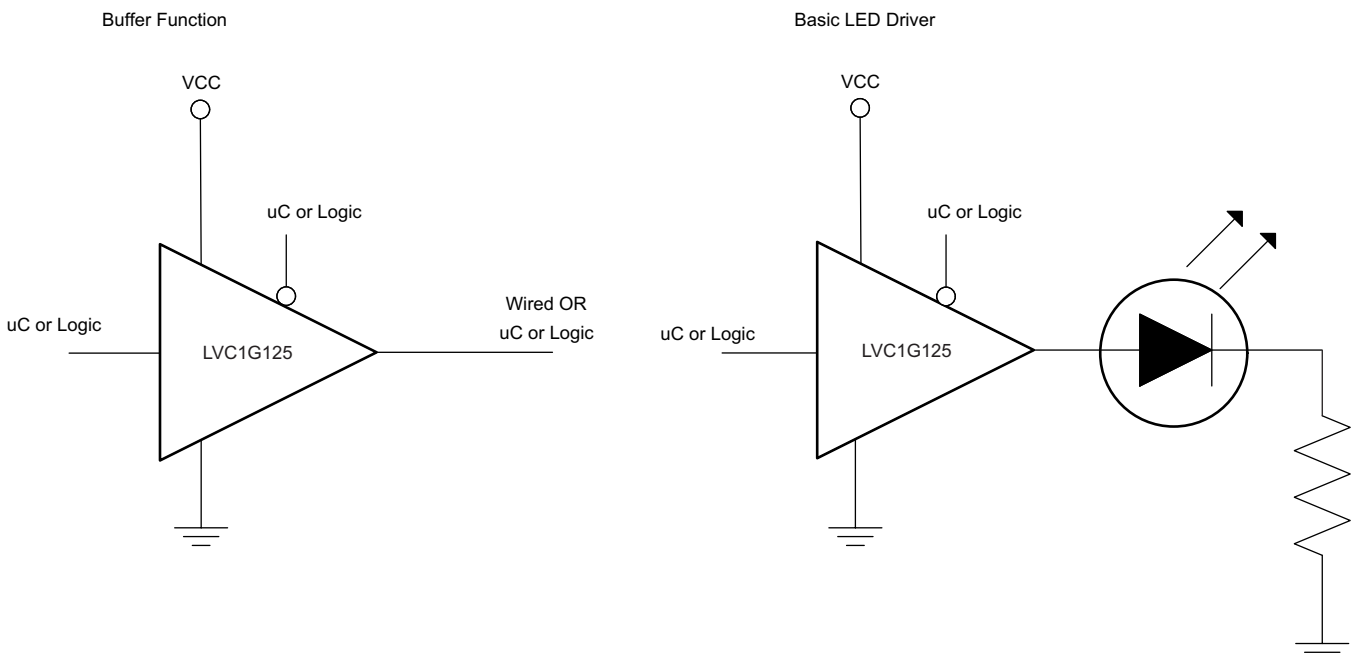
9.2 Typical Application

Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   – Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions
   – Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Typical Application (continued)

  – Outputs should not be pulled above V_{CC}.
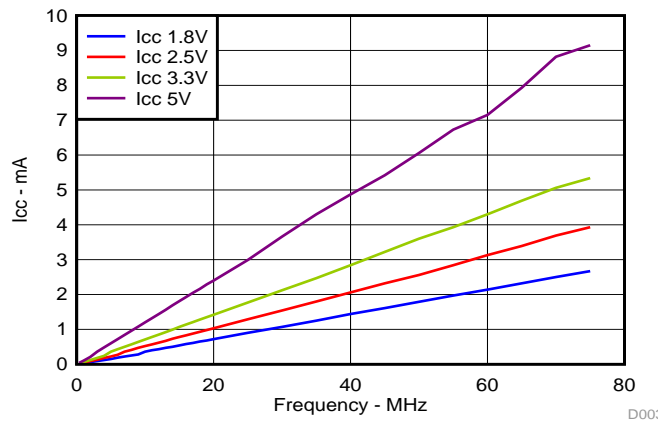
9.2.3 Application Curves

Figure 6. I_{CC} vs Frequency, Square wave input signal

10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1-μF capacitor is recommended and if there are multiple VCC pins then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 7 shows the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient.
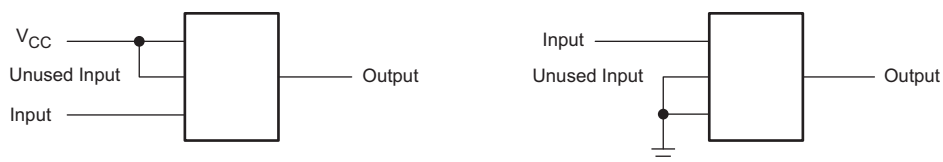
11.2 Layout Example

Figure 7. Package Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.
    This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
1P1G125QDCKRG4Q1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CMR	Samples
1P1G125QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CMR	Samples
1P1G125QDRYRQ1	PREVIEW	SON	DRY	6	5000	TBD	Call TI	Call TI	-40 to 125		
CLVC1G125QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C25O	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G125-Q1 :

- Catalog: SN74LVC1G125

- Enhanced Product: SN74LVC1G125-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1P1G125QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
CLVC1G125QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1P1G125QDCKRQ1	SC70	DCK	5	3000	202.0	201.0	28.0
CLVC1G125QDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0

PIN 1
INDEX AREA

3.0
2.6

1.75
1.45

B

A

C

0.1 C

1.45 MAX

1

5

2X 0.95

1.9

2

3.05
2.75

1.9

5X 0.5
0.3

⊕ 0.2Ⓜ C A B

3

4

(1.1)

0.15 TYP
0.00

0.25

GAGE PLANE

0.22 TYP
0.08

8° TYP
0°

0.6 TYP
0.3

SEATING PLANE
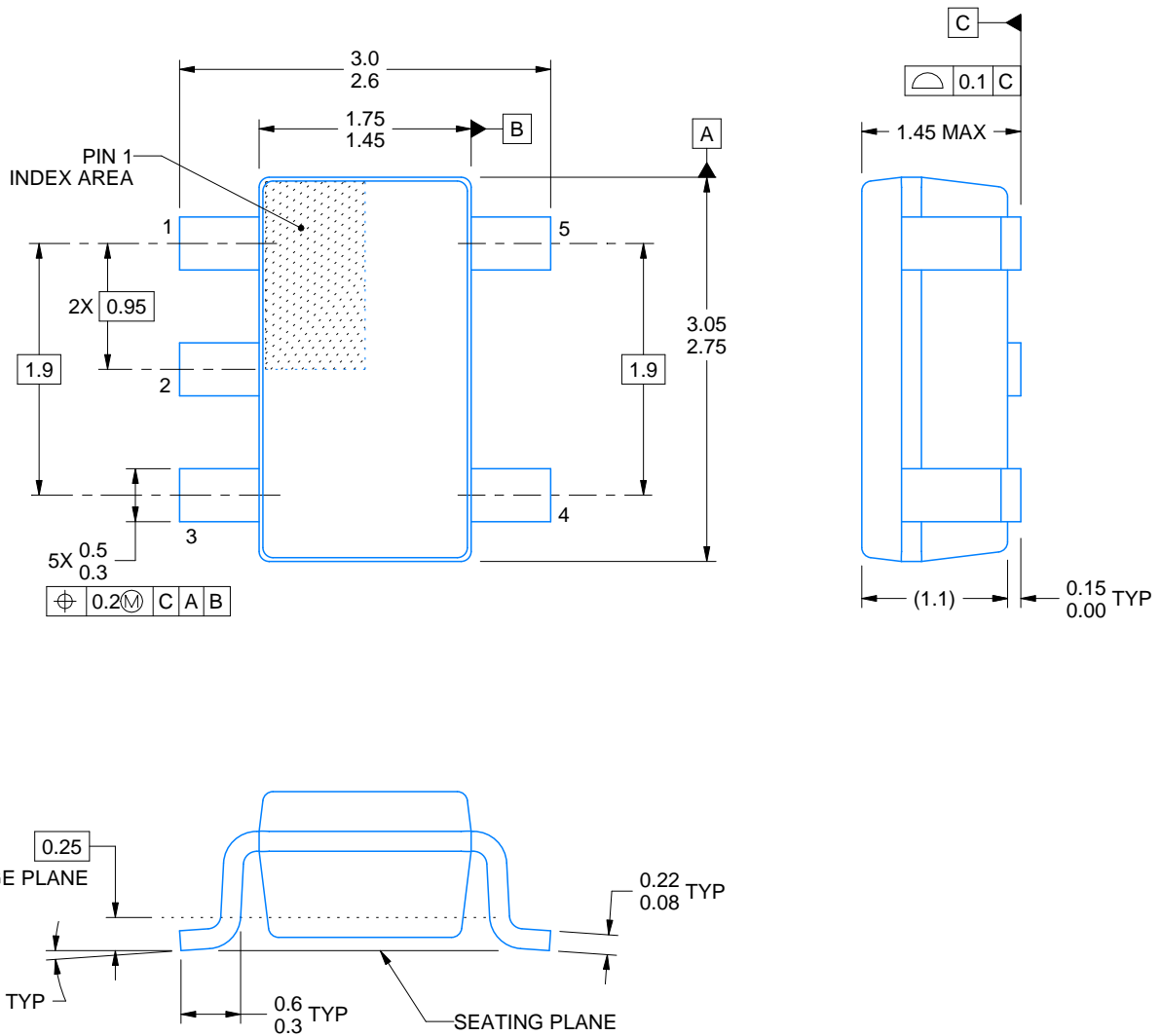
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

TEXAS INSTRUMENTS

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PKG

5X (1.1)

1

5X (0.6)

5

SYMM

(1.9)

2

2X (0.95)

3

4

(R0.05) TYP

(2.6)
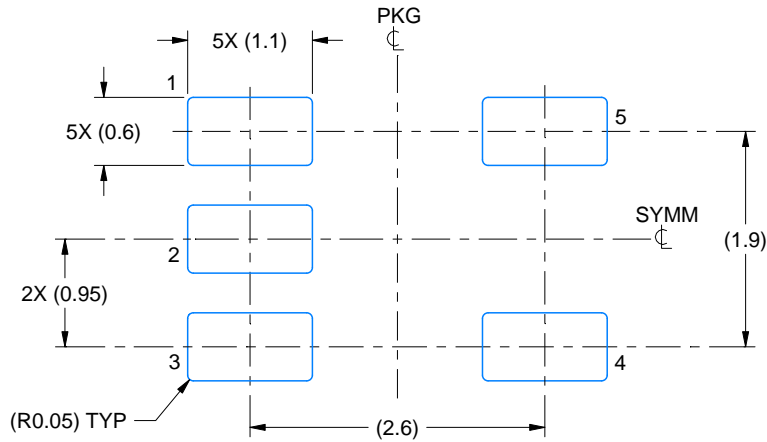
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED
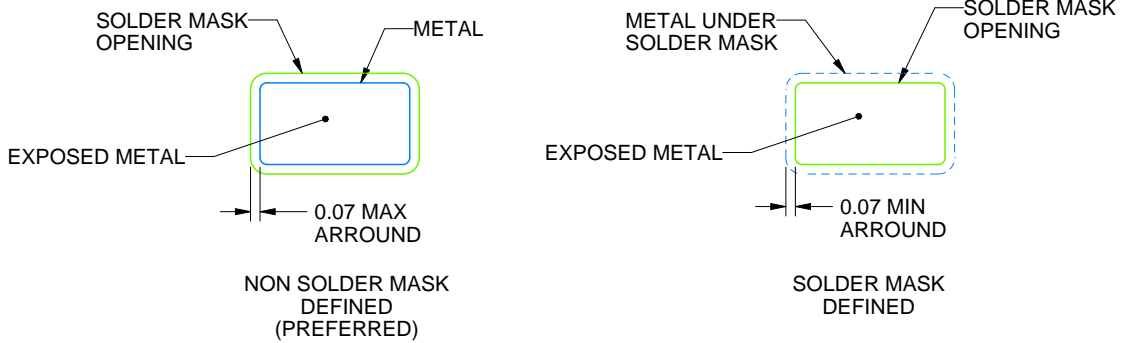
SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A
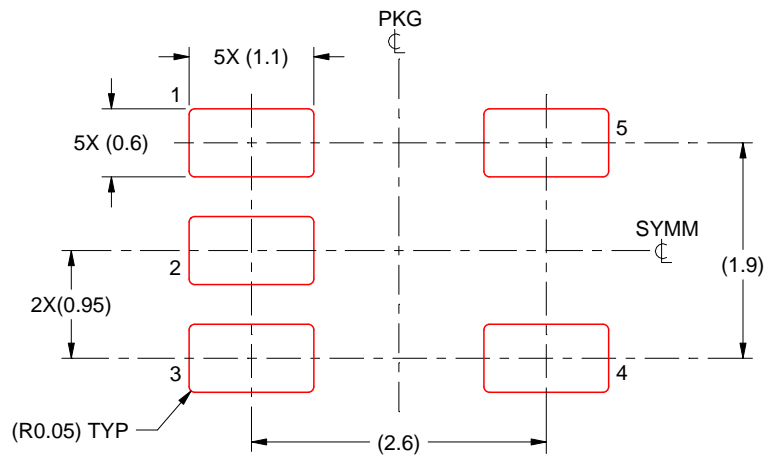
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D   11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5)   PLASTIC SMALL-OUTLINE PACKAGE

2,15 / 1,85

5   4

2,40 / 1,80

1,40 / 1,10

Pin 1
Index Area   1   2   3

0,65

5X 0,30 / 0,15

1,30

⊕ | 0,10 (M)

0,22 / 0,08

Gauge Plane
Seating Plane

0,15   0°–8°

0,46 / 0,26

1,10 / 0,80

⌒ | 0,10

Seating Plane

0,10 / 0,00

4093553-3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO-203 variation AA.