

## N-channel 400 V, 2.7 $\Omega$ typ., 2 A SuperMESH3™ Zener-protected Power MOSFET in a DPAK package

Datasheet — production data

### Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>w</sub>
STD3N40K3	400 V	< 3.4 $\Omega$	2 A	30 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

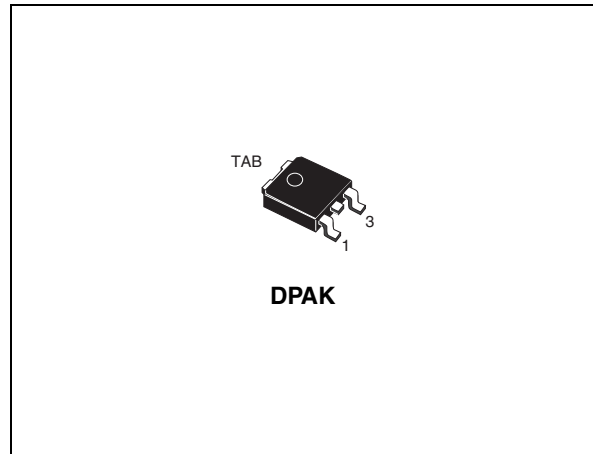


Figure 1. Internal schematic diagram

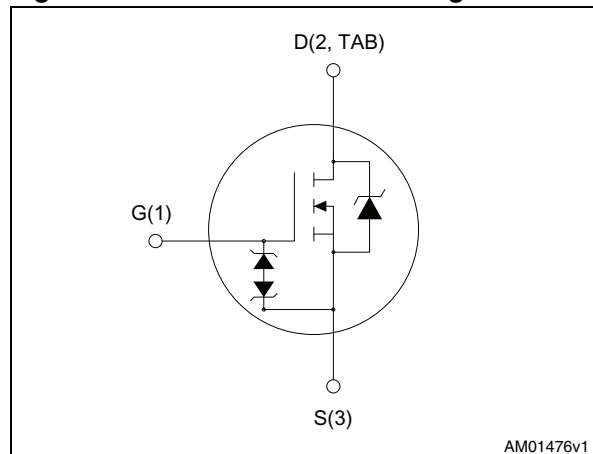


Table 1. Device summary

Order code	Marking	Package	Packaging
STD3N40K3	3N40K3	DPAK	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	400	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.2	A
$I_{DM}^{(1)}$	Drain current (pulsed)	8.0	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	45	mJ
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, R = 1.5 k $\Omega$ )	2500	V
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	12	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} < 2\text{ A}$ , di/dt = 400 A/ $\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.17	$^\circ\text{C/W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50	$^\circ\text{C/W}$

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	400			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 400 V V <sub>DS</sub> = 400 V, T <sub>C</sub> =125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> =0			±10	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 50 μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.9 A		2.7	3.4	Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iSS</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	165	-	pF
C <sub>oss</sub>	Output capacitance			17		
C <sub>rSS</sub>	Reverse transfer capacitance			3		
C <sub>oss(er)</sub> <sup>(1)</sup>	Equivalent output capacitance energy related	V <sub>DS</sub> =0 to 320 V, V <sub>GS</sub> =0	-	9	-	pF
C <sub>oss(tr)</sub> <sup>(2)</sup>	Equivalent output capacitance time related			14		
R <sub>g</sub>	Intrinsic gate resistance	f=1 MHz open drain	-	10	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 320 V, I <sub>D</sub> = 1.8 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 16</a> )	-	11	-	nC
Q <sub>gs</sub>	Gate-source charge			2		
Q <sub>gd</sub>	Gate-drain charge			7		

1. Is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>
2. Is defined as a constant equivalent capacitance giving the same storage energy as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn on delay time	$V_{DD} = 200\text{ V}$ , $I_D = 0.6$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )		7		ns	
$t_r$	Rise time			8		ns	
$t_{d(off)}$	Turn off delay time			-	18	-	ns
$t_f$	Fall time				14		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		1.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				7.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1.8\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	145		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$		490		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 17</a> )		7		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	166		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$		580		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 17</a> )		7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30		-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

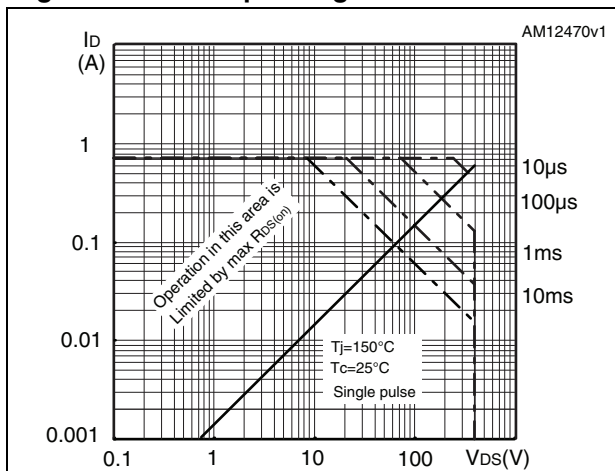


Figure 3. Thermal impedance

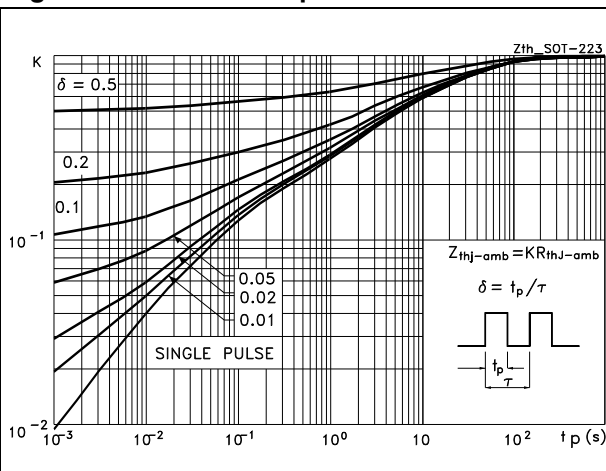


Figure 4. Output characteristics

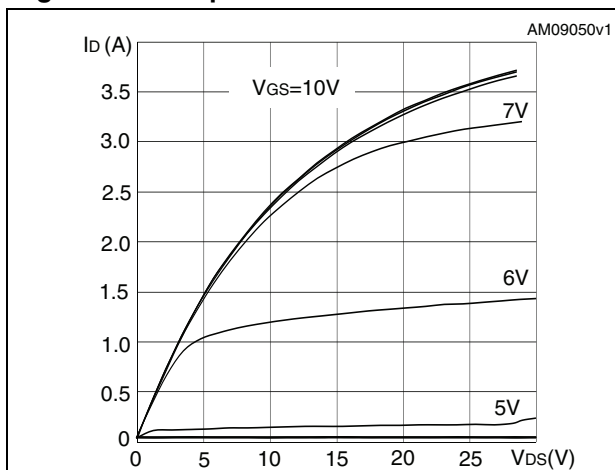


Figure 5. Transfer characteristics

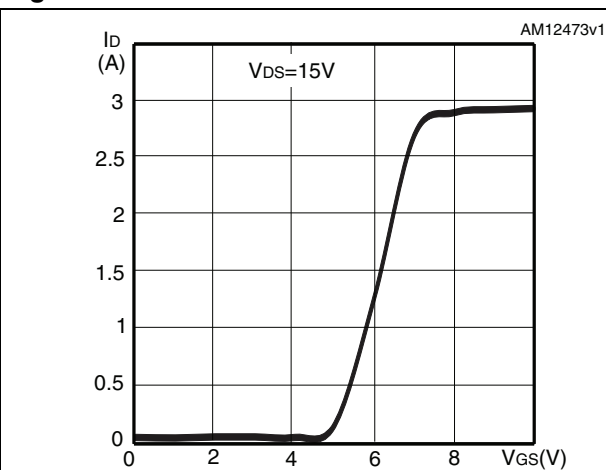


Figure 6. Gate charge vs gate-source voltage

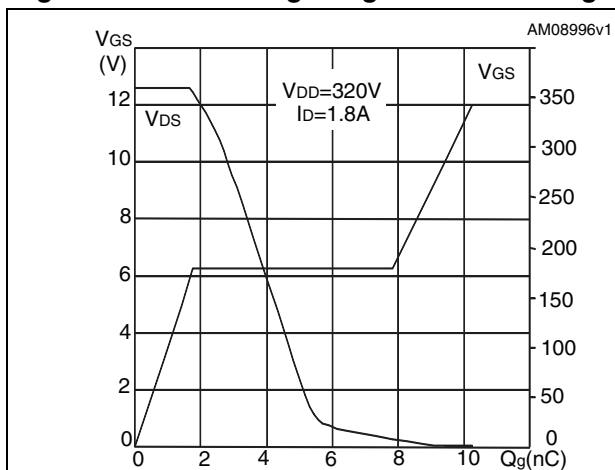


Figure 7. Static drain-source on-resistance

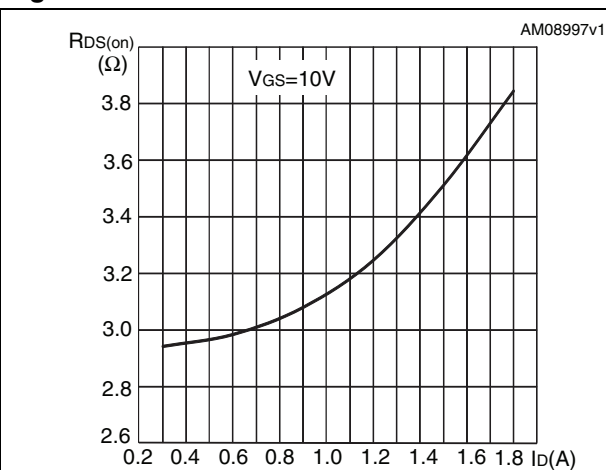


Figure 8. Capacitance variations

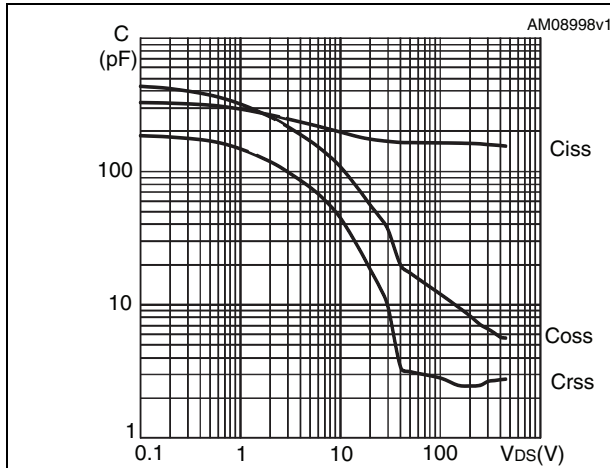


Figure 9. Output capacitance stored energy

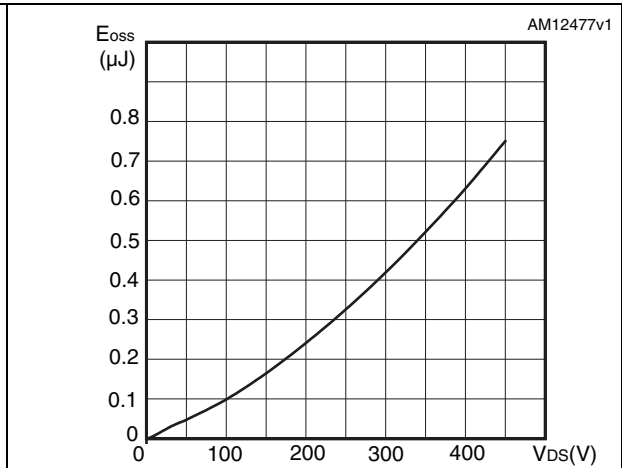


Figure 10. Normalized gate threshold voltage vs. temperature

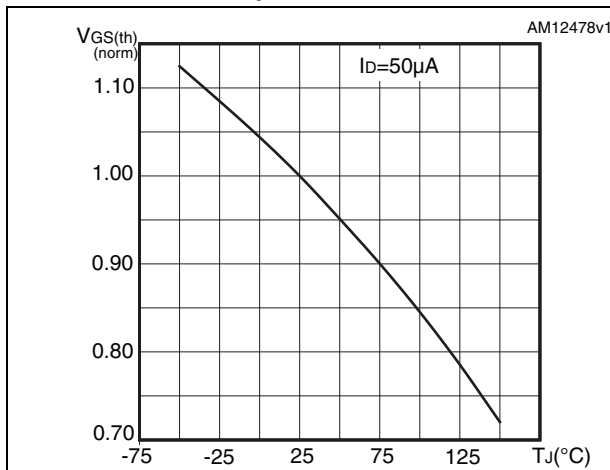


Figure 11. Normalized on-resistance vs. temperature

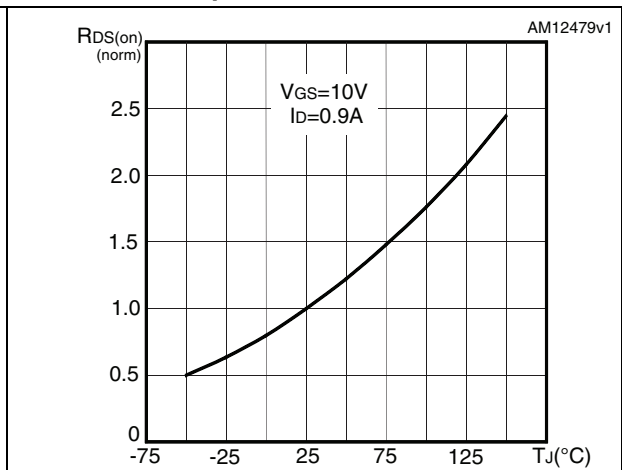


Figure 12. Source-drain diode forward characteristics

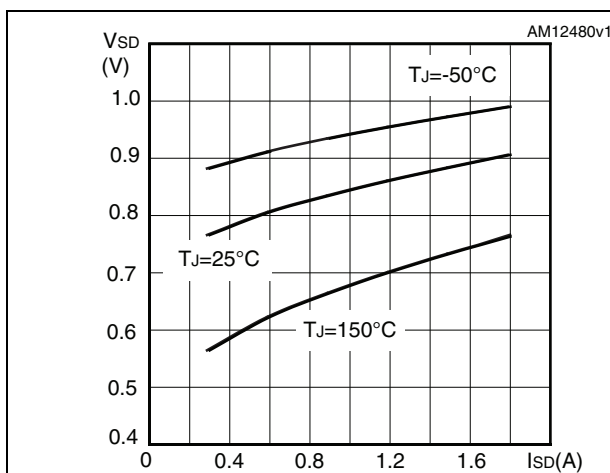


Figure 13. Normalized BV<sub>DSS</sub> vs. temperature

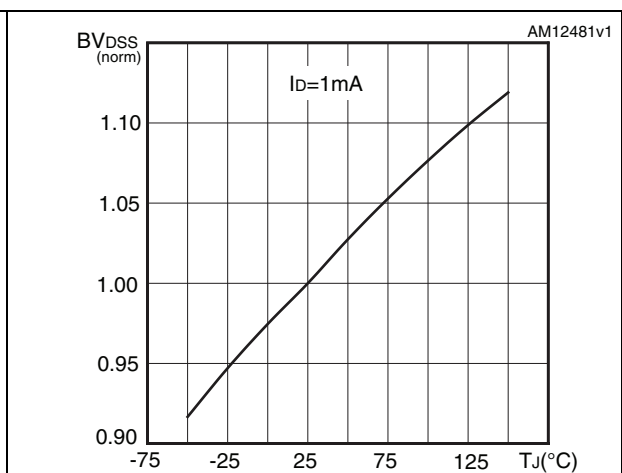
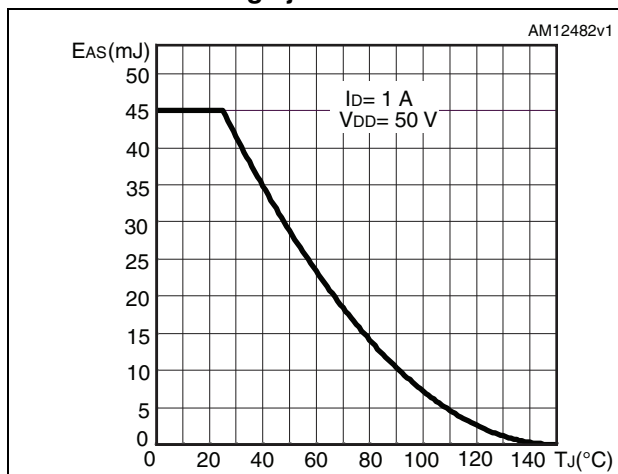


Figure 14. Maximum avalanche energy vs. starting Tj







## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) drawing

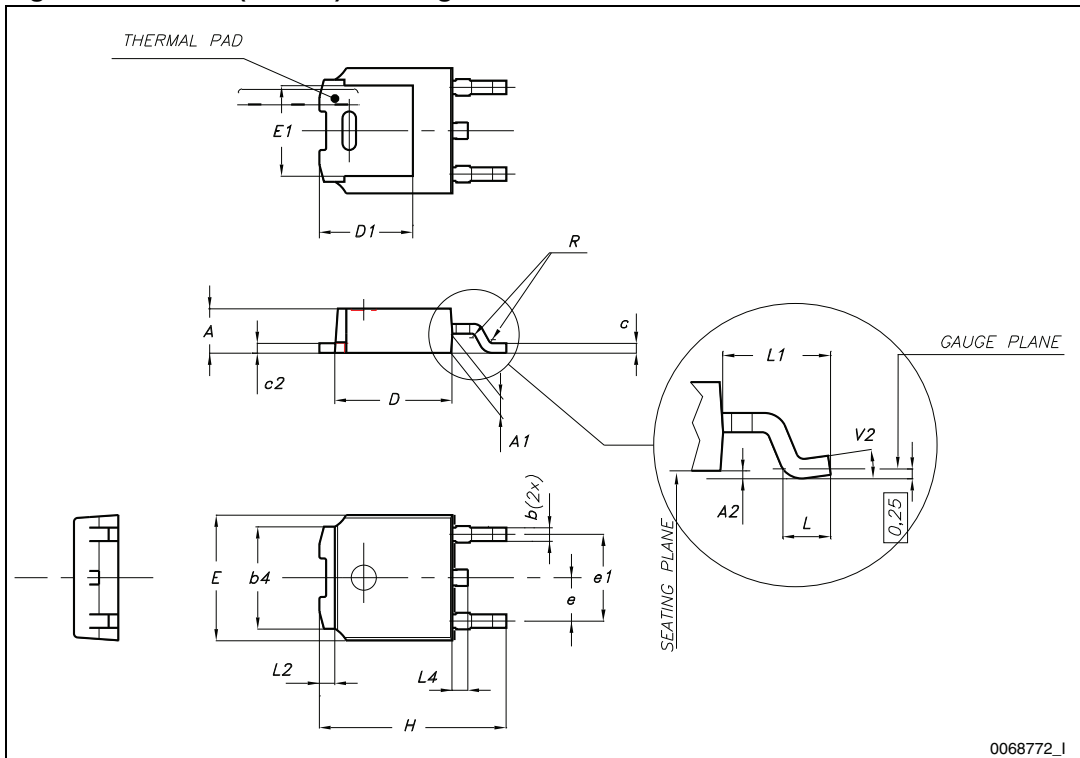
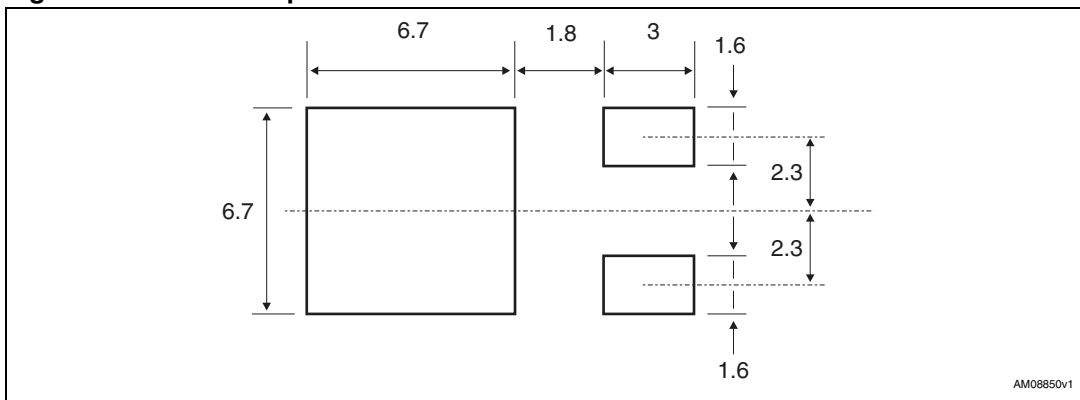


Figure 22. DPAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

## 5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 23. Tape for DPAK (TO-252)

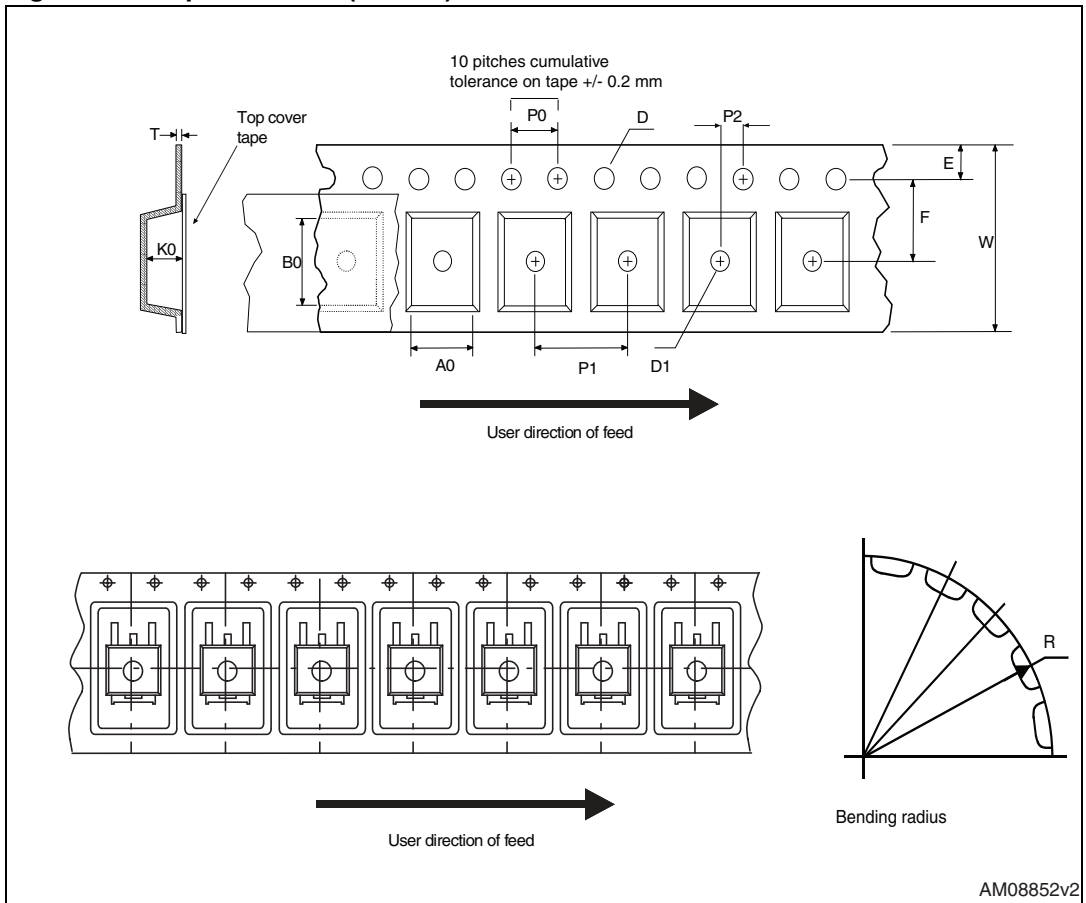
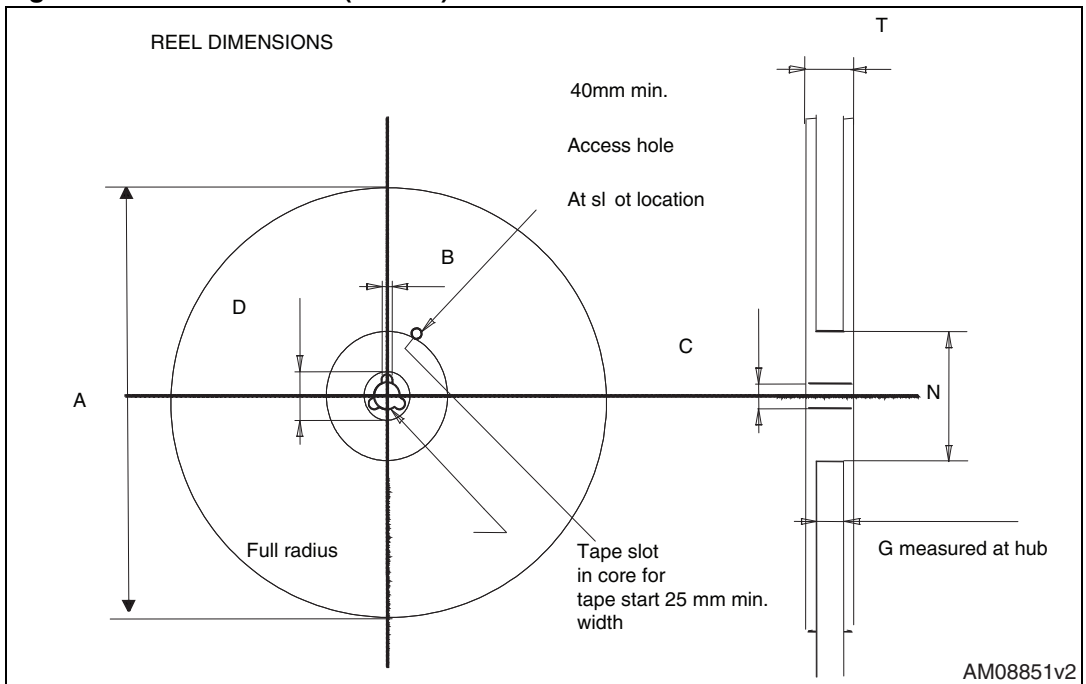


Figure 24. Reel for DPAK (TO-252)



## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Jul-2012	1	First release.

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