

DUAL N-CHANNEL ENHANCEMENT MODE MOSFET
Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	Package	I_D $T_A = +25^\circ\text{C}$
60V	8Ω @ $V_{GS} = 5V$	SOT363	170mA
	6Ω @ $V_{GS} = 10V$		200mA

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- DC-DC Converters
- Power Management Functions
- Battery Operated Systems and Solid-State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc

Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surface Mount Package
- ESD Protected Gate, 1KV (HBM)
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

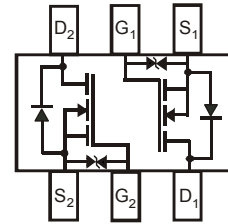
- Case: SOT363
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Solderable per MIL-STD-202, Method 208③
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)



SOT363



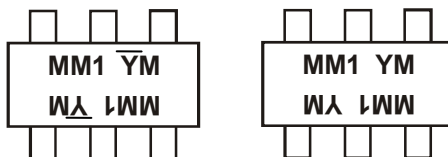
Top View


 Top View
Internal Schematic

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN65D8LDW-7	SOT363	3000/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

Marking Information


MM1= Product Type Marking Code
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 ȲM = Date Code Marking for CAT (Chengdu Assembly/ Test site)
 Y or Ȳ = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
Code	U	V	W	X	Y	Z	A	B	C	D	E	F
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic				Symbol	Value	Units
Drain-Source Voltage				V_{DSS}	60	V
Gate-Source Voltage				V_{GSS}	± 20	V
Continuous Drain Current (Note 5)	$V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	180	mA
			$T_A = +70^\circ\text{C}$		140	
Continuous Drain Current (Note 5)	$V_{GS} = 5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	150	mA
			$T_A = +70^\circ\text{C}$		120	
Continuous Drain Current (Note 6)	$V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	200	mA
			$T_A = +70^\circ\text{C}$		160	
Continuous Drain Current (Note 6)	$V_{GS} = 5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	170	mA
			$T_A = +70^\circ\text{C}$		140	
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)				I_{DM}	800	mA

Thermal Characteristics

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	300	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	435	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 6)	P_D	400	mW
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	330	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	139	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
				5.0		
Gate-Body Leakage	I_{GSS}	—	—	± 5.0	μA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	—	8	Ω	$V_{GS} = 5.0\text{V}, I_D = 0.115\text{A}$
		—	—	6	Ω	$V_{GS} = 10.0\text{V}, I_D = 0.115\text{A}$
Forward Transconductance	g_{FS}	80	—	—	mS	$V_{DS} = 10\text{V}, I_D = 0.115\text{A}$
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	$V_{GS} = 0\text{V}, I_S = 115\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	22.0	—	pF	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	3.2	—		
Reverse Transfer Capacitance	C_{rss}	—	2.0	—		
Gate Resistance	R_G	—	79.9	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge $V_{GS} = 10\text{V}$	Q_g	—	0.87	—	nC	$V_{GS} = 10\text{V}, V_{DS} = 30\text{V}, I_D = 150\text{mA}$
Total Gate Charge $V_{GS} = 4.5\text{V}$	Q_g	—	0.43	—		
Gate-Source Charge	Q_{gs}	—	0.11	—		
Gate-Drain Charge	Q_{gd}	—	0.11	—		
Turn-On Delay Time	$t_{D(on)}$	—	3.3	—	nS	$V_{DD} = 30\text{V}, I_D = 0.115\text{A}, V_{GEN} = 10\text{V}, R_{GEN} = 25\Omega$
Turn-On Rise Time	t_r	—	3.2	—		
Turn-Off Delay Time	$t_{D(off)}$	—	12.0	—		
Turn-Off Fall Time	t_f	—	6.3	—		

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

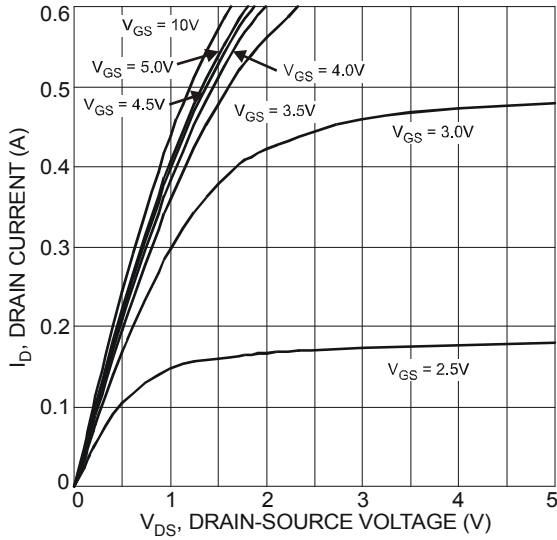


Fig.1 Typical Output Characteristic

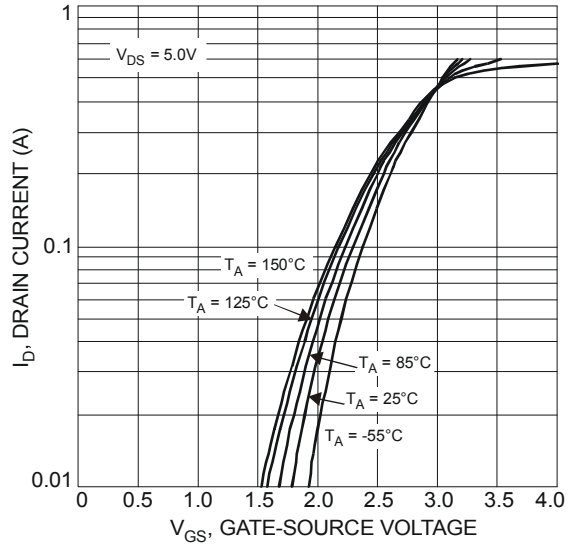


Fig.2 Typical Transfer Characteristics

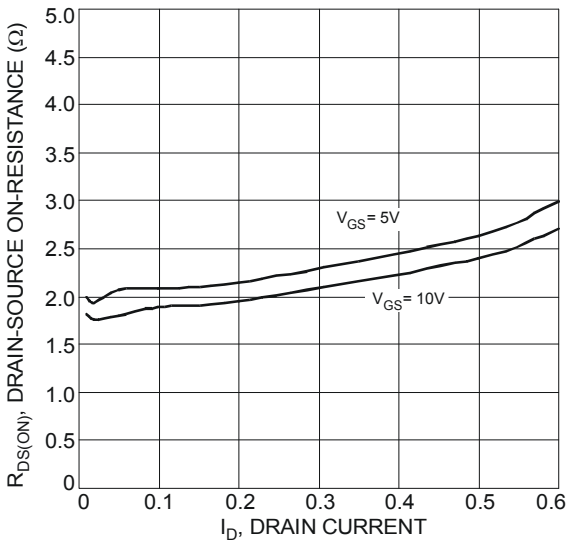


Fig.3 Typical On-Resistance vs. Drain Current and Temperature

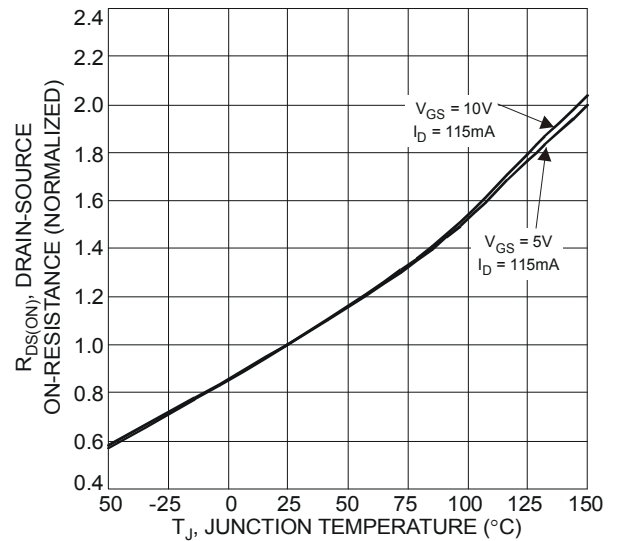


Fig.4 On-Resistance Variation with Temperature

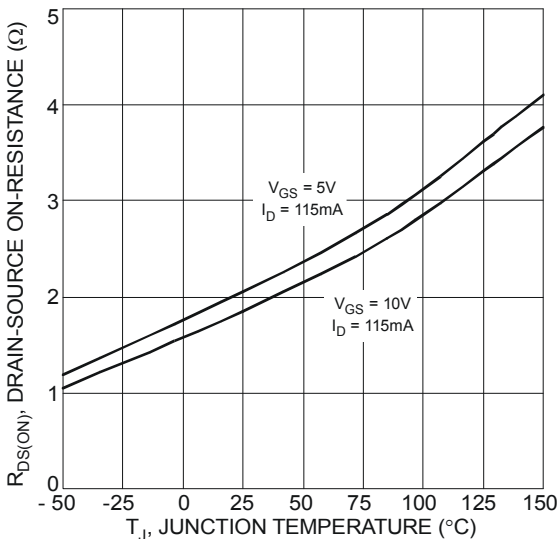


Fig.5 On-Resistance Variation with Temperature

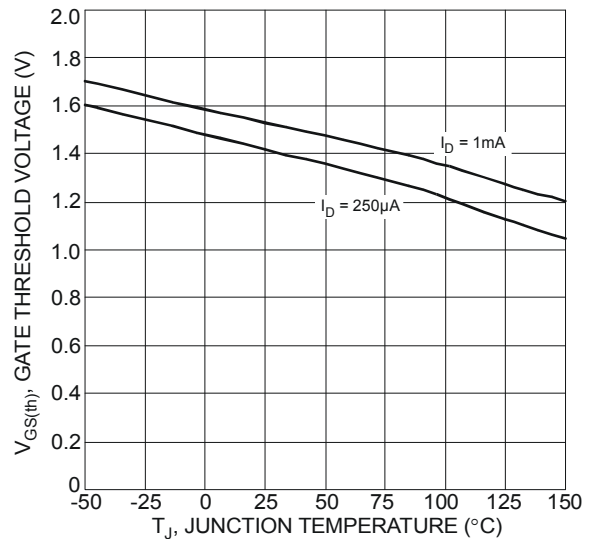


Fig.6 Gate Threshold Variation vs. Ambient Temperature

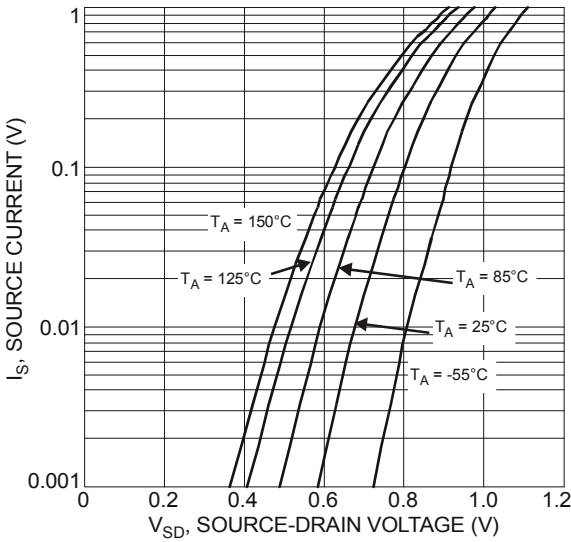


Fig. 7 Diode Forward Voltage vs. Current

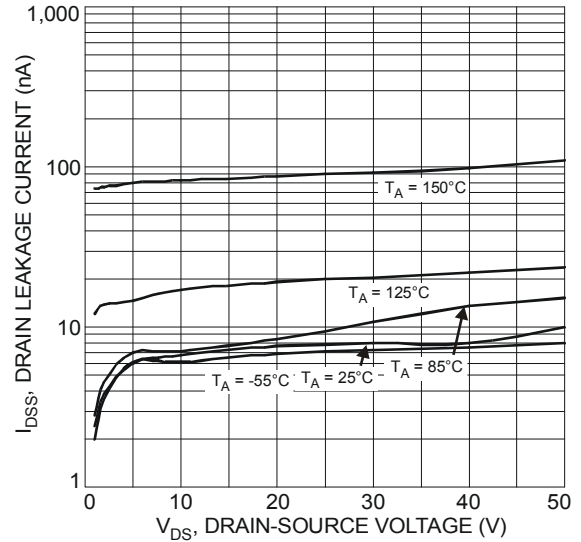


Fig. 8 Typical Drain-Source Leakage Current vs. Voltage

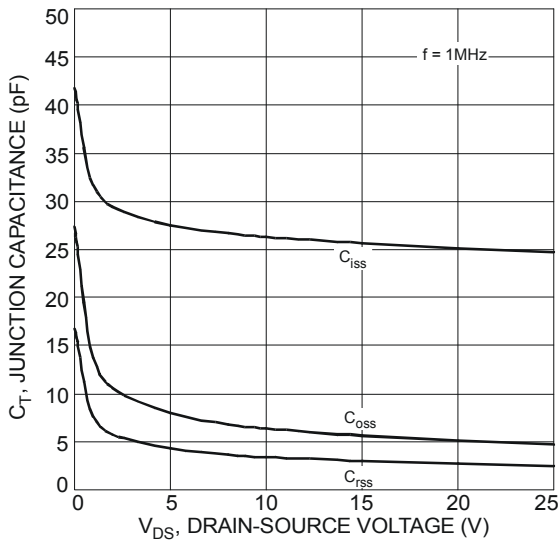


Fig. 9 Typical Junction Capacitance

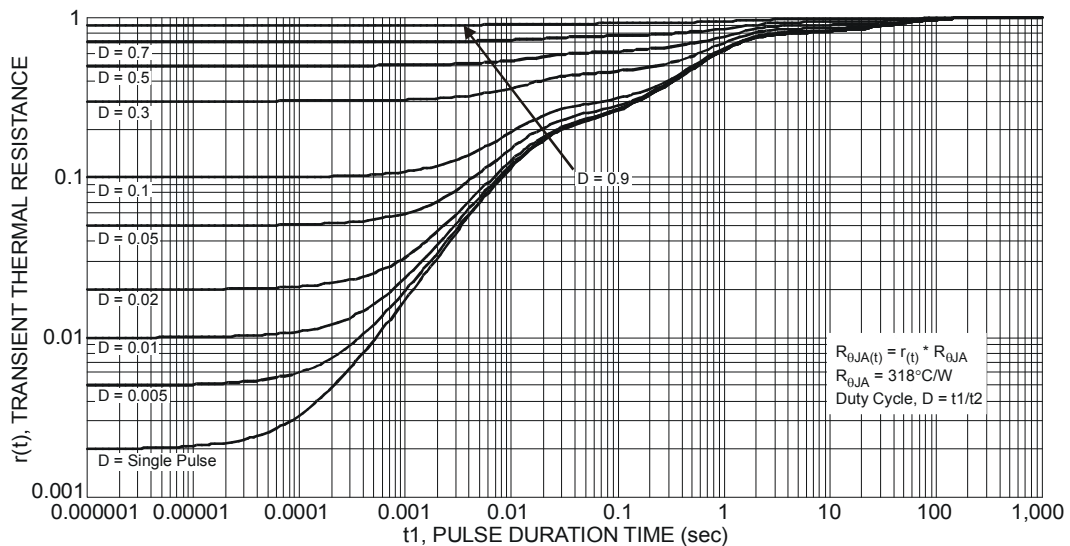
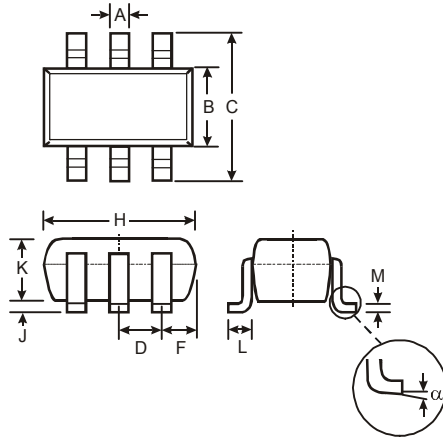


Fig. 10 Transient Thermal Resistance

$R_{\theta JA}(t) = r(t) * R_{\theta JA}$
 $R_{\theta JA} = 318^{\circ}\text{C/W}$
 Duty Cycle, $D = t1/t2$

Package Outline Dimensions

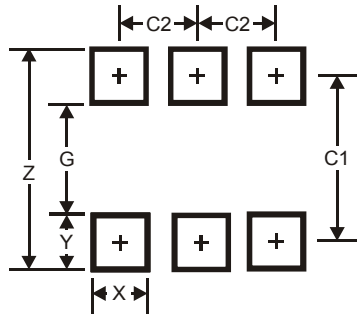
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SOT363			
Dim	Min	Max	Typ
A	0.10	0.30	0.25
B	1.15	1.35	1.30
C	2.00	2.20	2.10
D	0.65 Typ		
F	0.40	0.45	0.425
H	1.80	2.20	2.15
J	0	0.10	0.05
K	0.90	1.00	1.00
L	0.25	0.40	0.30
M	0.10	0.22	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	2.5
G	1.3
X	0.42
Y	0.6
C1	1.9
C2	0.65

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