RICOH

R1524x Series

200 mA 36 V Input Ultra Low Supply Current VR

No. EA-332-191108

OUTLINE

The R1524x is an ultra-low supply current voltage regulator featuring 200 mA output current and 36 V input voltage. This device consists of an Output Short-circuit Protection Circuit, an Over-current Protection Circuit, and a Thermal Shutdown Circuit in addition to the basic regulator circuits. The operating temperature range is from −40°C to 105°C, and the maximum input voltage is 36 V. All these features allow the R1524x to become an ideal power source of electric home appliances.

The output voltages are internally fixed at either of the following: 1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 3.4 V, 5.0 V, 5.5 V, 6.0 V, 6.4 V, 7.0 V, 8.0 V, 8.5 V and 9.0 V. The output voltage accuracy is ±0.6%.

The packages for this device range from high-density mounting to ultra high wattage. The R1524x is offered in five packages; a 5-pin SOT-23-5, a 5-pin SOT-89-5, a 6-pin HSOP-6J, a 6-pin DFN(PLP)1820-6, and an 8-pin HSOP-8E package.

FEATURES

- Input Voltage Range (Maximum Rating) ····· 3.5 V to 36 V (50 V)
- Operating Temperature Range ····· –40°C to 105°C
- Supply Current ····· Typ. 2.2 µA
- Standby Current ····· Typ. 0.1 µA
- Dropout Voltage ····· Typ. 0.6 V (I_{OUT} = 200 mA, V_{OUT} = 5.0 V)
- Output Voltage Range ····· 1.8 V / 2.5 V / 2.8 V / 3.0 V / 3.3 V / 3.4V / 5.0 V / 5.5 V / 6.0 V / 6.4 V / 7.0 V / 8.0 V / 8.5 V / 9.0 V
  *Contact Ricoh sales representatives for other voltages.
- Output Voltage Accuracy ····· ±0.6% (Ta = 25°C)
- Output Voltage Temperature-Drift Coefficient ····· Typ. ±60 ppm/°C
- Line Regulation ····· Typ. 0.01%/V (V_{SET} + 1 V ≤ V_{IN} ≤ 36 V)
- Built-in Output Short-circuit Protection Circuit ····· Typ. 80 mA
- Built-in Over-current Protection Circuit ····· Typ. 350 mA
- Built-in Thermal Shutdown Circuit ····· Thermal Shutdown Temperature: Typ. 160°C
- Ceramic capacitors are recommended to be used with this device ····· C_{OUT} = 0.1 µF or more
- Packages ····· SOT-23-5, SOT-89-5, HSOP-6J, DFN(PLP)1820-6, HSOP-8E

APPLICATIONS

- Power source for home appliances such as refrigerators, rice cookers, and electric hot-water pot.
- Power source for notebook PCs, digital TVs, cordless phones, and private LAN system.
- Power source for office equipment machines such as copiers, printers, facsimiles, scanners, and projectors.

SELECTION GUIDE

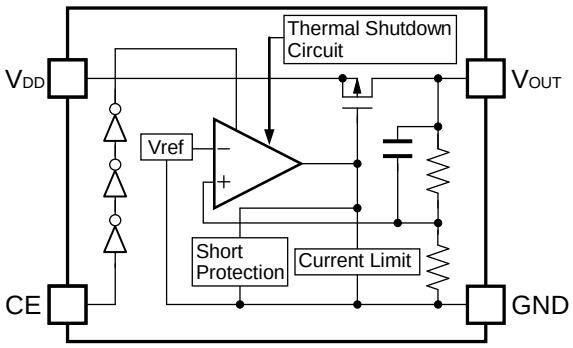
The set output voltage and the package type are user-selectable.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1524NxxxB-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes
R1524HxxxB-T1-FE	SOT-89-5	1,000 pcs	Yes	Yes
R1524SxxxB-E2-FE	HSOP-6J	1,000 pcs	Yes	Yes
R1524KxxxB-TR	DFN(PLP)1820-6	5,000 pcs	Yes	Yes
R1524SxxxH-E2-FE	HSOP-8E	1,000 pcs	Yes	Yes

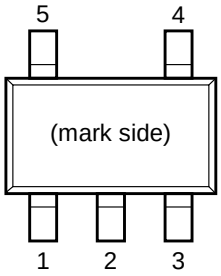
xxx: Specify the set output voltage (V_{SET})
1.8 V (018) / 2.5 V (025) / 2.8 V (028) / 3.0 V (030) / 3.3 V (033) / 3.4 V (034) / 5.0 V (050) / 5.5 V (055) / 6.0 V (060) / 6.4 V (064) / 7.0 V (070) / 8.0 V (080) / 8.5 V (085) / 9.0 V (090)
*Contact Ricoh sales representatives for other voltages.

BLOCK DIAGRAM

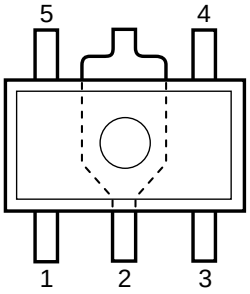


R1524x Block Diagram

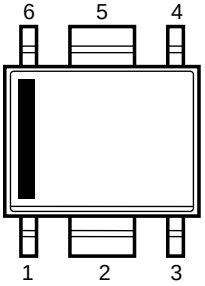
PIN DESCRIPTIONS



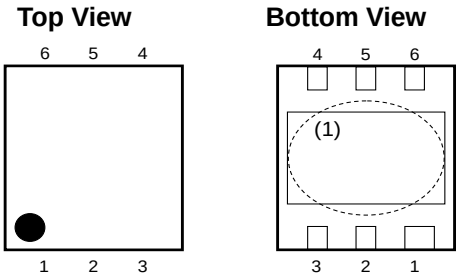
SOT-23-5 Pin Configuration



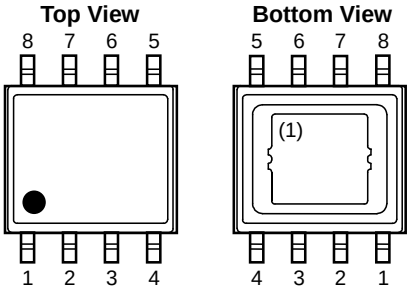
SOT-89-5 Pin Configuration



HSOP-6J Pin Configuration



DFN(PLP)1820-6 Pin Configuration



HSOP-8E Pin Configuration

SOT-23-5 Pin Descriptions

Pin No.	Symbol	Description
1	GND(2)	Ground Pin
2	GND(2)	Ground Pin
3	CE	Chip Enable Pin (Active-high)
4	V_{OUT}	Output Pin
5	V_{DD}	Input Pin

SOT-89-5 Pin Descriptions

Pin No.	Symbol	Description
1	V_{OUT}	Output Pin
2	GND(3)	Ground Pin
3	CE	Chip Enable Pin (Active-high)
4	GND(3)	Ground Pin
5	V_{DD}	Input Pin

(1) The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.
(2) The GND pin must be wired together when it is mounted on board.
(3) The GND pin must be wired together when it is mounted on board.

HSOP-6J Pin Descriptions

Pin No.	Symbol	Description
1	V_{OUT}	Output Pin
2	GND(1)	Ground Pin
3	CE	Chip Enable Pin (Active-high)
4	GND(1)	Ground Pin
5	GND(1)	Ground Pin
6	V_{DD}	Input Pin

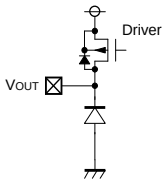
DFN(PLP)1820-6 Pin Descriptions

Pin No.	Symbol	Description
1	CE	Chip Enable Pin (Active-high)
2	NC	No Connection
3	GND	Ground Pin
4	V_{DD}	Input Pin
5	NC	No Connection
6	V_{OUT}	Output Pin

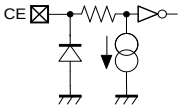
HSOP-8E Pin Descriptions

Pin No.	Symbol	Description
1	V_{OUT}	Output Pin
2	NC	No Connection
3	NC	No Connection
4	CE	Chip Enable Pin (Active-high)
5	GND	Ground Pin
6	NC	No Connection
7	NC	No Connection
8	V_{DD}	Input Pin

PIN EQUIVALENT CIRCUIT DIAGRAMS



V_{OUT} Pin



CE Pin

(1) The GND pin must be wired together when it is mounted on board.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item		Rating	Unit
V_{IN}	Input Voltage		−0.3 to 50	V
V_{IN}	Peak Input Voltage(1)		60	V
V_{CE}	Input Voltage (CE Pin)		−0.3 to 50	V
V_{OUT}	Output Voltage		−0.3 to V_{IN} + 0.3 ≤ 50	V
I_{OUT}	Output Current		300	mA
P_D	Power Dissipation(2) (JEDEC STD.51-7 Test Land Pattern)	SOT-23-5	660	mW
		SOT-89-5	2600	
		HSOP-6J	2700	
		DFN(PLP)1820-6	2200	
		HSOP-8E	2900	
Tj	Junction Temperature Range		−40 to 125	°C
Tstg	Storage Temperature Range		−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3.5 to 36	V
Ta	Operating Temperature Range	−40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Duration time: 200 ms
(2) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

C_{IN} = C_{OUT} = 0.1 µF, unless otherwise noted.

The specifications surrounded by ☐ are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1524x Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	V_{IN} = 14 V, I_{OUT} = 0 mA	V_{SET} ≤ 5.0 V		2.2	6.5	µA
			5.0 V < V_{SET}		2.5	6.8	
Istandby	Standby Current	V_{IN} = 36 V, V_{CE} = 0 V			0.1	1.0	µA
V_{OUT}	Output Voltage	V_{SET} + 1 V[1] ≤ V_{IN} ≤ 36 V, I_{OUT} = 1 mA	Ta = 25°C	×0.994		×1.006	V
			−40°C ≤ Ta ≤ 105°C	×0.984		×1.016	
ΔV_{OUT} /ΔI_{OUT}	Load Regulation	V_{IN} = V_{SET} + 3.0 V, 1 mA ≤ I_{OUT} ≤ 200 mA		Refer to the *Product-specific Electrical Characteristics*			
ΔV_{OUT} /ΔV_{IN}	Line Regulation	V_{SET} + 1 V[1] ≤ V_{IN} ≤ 36 V, I_{OUT} = 1 mA	V_{SET} < 3.3 V	-20	5	20	mV
			3.3 V ≤ V_{SET}	-0.02	0.01	0.02	%/V
V_{DIF}	Dropout Voltage	I_{OUT} = 200 mA		Refer to the *Product-specific Electrical Characteristics*			
I_{LIM}	Output Current Limit	V_{IN} = V_{SET} + 3.0 V		220	350		mA
I_{SC}	Short Current Limit	V_{IN} = 3.5 V, V_{OUT} = 0 V		60	80		mA
V_{CEH}	CE Pin Input Voltage, high	V_{IN} = V_{SET} + 1 V[1]		2.0		36	V
V_{CEL}	CE Pin Input Voltage, low	V_{IN} = 36 V		0		1.0	V
I_{PD}	CE Pull-down Current	V_{IN} = 36 V, V_{CE} = 2 V			0.2	0.6	µA
T_{TSD}	Thermal Shutdown Detection Temperature	Junction Temperature			160		°C
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature			135		°C

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

[1] V_{SET} ≤ 2.5 V, V_{IN} = 3.5 V

The specifications surrounded by ☐ are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1524x Product-specific Electrical Characteristics (Ta = 25°C)

Product Name	V_{OUT} (V) (Ta = 25°C)			V_{OUT} (V) (−40°C ≤ Ta ≤ 105°C)			$\Delta V_{OUT}/\Delta I_{OUT}$ (mV)			V_{DIF} (V)	
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	TYP.	MAX.
R1524x018x	1.7892	1.80	1.8108	1.7712	1.80	1.8288				1.6	2.5
R1524x025x	2.4850	2.50	2.5150	2.4600	2.50	2.5400					
R1524x028x	2.7832	2.80	2.8168	2.7552	2.80	2.8448				1.2	2.2
R1524x030x	2.9820	3.00	3.0180	2.9520	3.00	3.0480	-10	10	40		
R1524x033x	3.2802	3.30	3.3198	3.2472	3.30	3.3528					
R1524x034x	3.3796	3.40	3.4204	3.3456	3.40	3.4544				0.8	2.0
R1524x050x	4.9700	5.00	5.0300	4.9200	5.00	5.0800					
R1524x055x	5.4670	5.50	5.5330	5.4120	5.50	5.5880					
R1524x060x	5.9640	6.00	6.0360	5.9040	6.00	6.0960				0.6	1.2
R1524x064x	6.3616	6.40	6.4384	6.2976	6.40	6.5024					
R1524x070x	6.9580	7.00	7.0420	6.8880	7.00	7.1120	-18	18	72		
R1524x080x	7.9520	8.00	8.0480	7.8720	8.00	8.1280					
R1524x085x	8.4490	8.50	8.5510	8.3640	8.50	8.6360				0.5	1.3
R1524x090x	8.9460	9.00	9.0540	8.8560	9.00	9.1440					

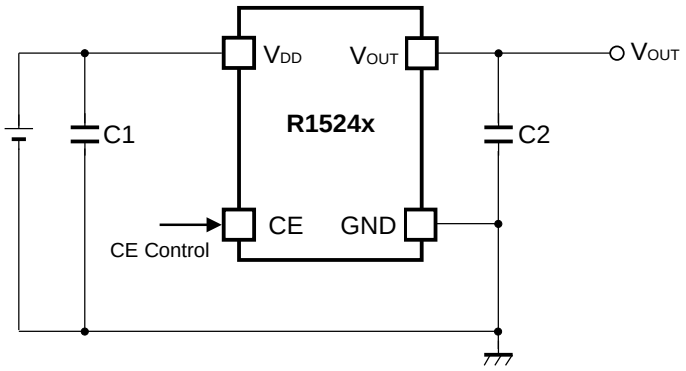
THEORY OF OPERATION

Thermal Shutdown

R1524x has a built-in thermal shutdown circuit, which stops the regulator operation if the junction temperature of this device increases to 160°C (Typ.) or higher. If the temperature drops to 135°C (Typ.) or lower, the regulator restarts the operation. Unless eliminating the overheating problem, the regulator turns on and off repeatedly and as a result, a pulse shaped output voltage is generated.

APPLICATION INFORMATION

TYPICAL APPLICATIONS



C1 = Ceramic 0.1 µF
C2 = Ceramic 0.1 µF

R1524x Typical Applications

TECHNICAL NOTES

Phase Compensation

In the R1524x, phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, make sure to use 0.1 µF or more of a capacitor (C2).

In case of using a tantalum type capacitor and the ESR (Equivalent Series Resistance) value of the capacitor is large, the output might be unstable. Evaluate the circuit including consideration of frequency characteristics.

Connect 0.1 µF or more of a capacitor (C1) between V_{DD} and GND, and as close as possible to the pins.

PCB Layout

For SOT-23-5 package type, wire the following GND pins together: No. 1 and No. 2

For SOT-89-5 package type, wire the following GND pins together: No. 2 and No. 4.

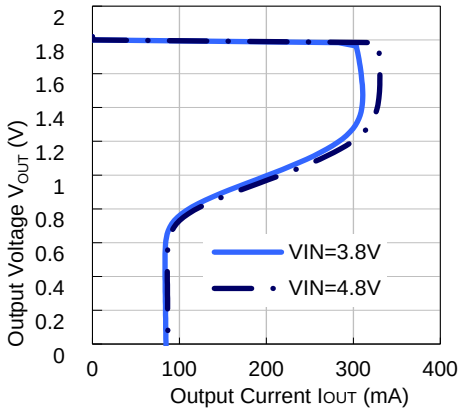
For HSOP-6J package type, wire the following GND pins together: No. 2, No. 4, and No. 5.

TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current (Ta = 25°C)

R1524x018B



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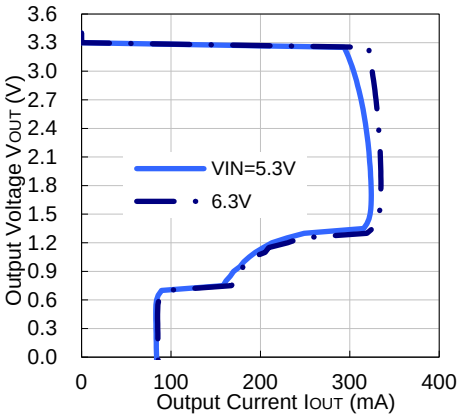

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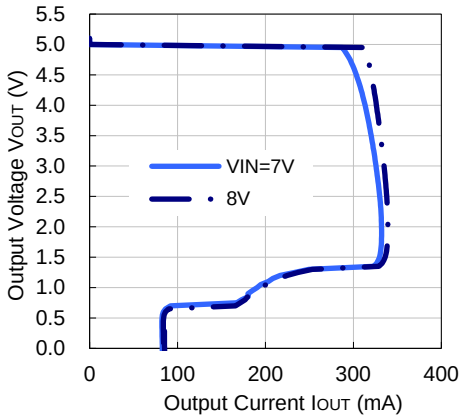

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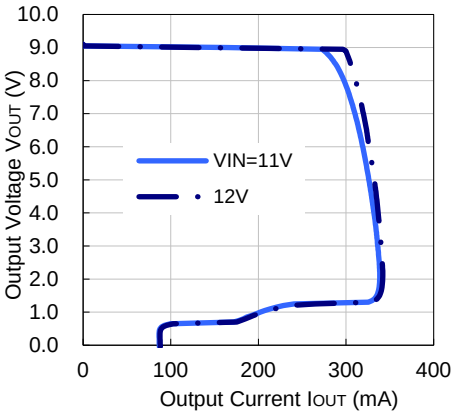
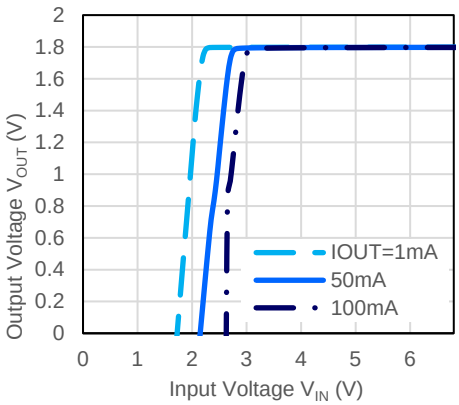


2) Output Voltage vs. Input Voltage (Ta = 25°C)

R1524x018B



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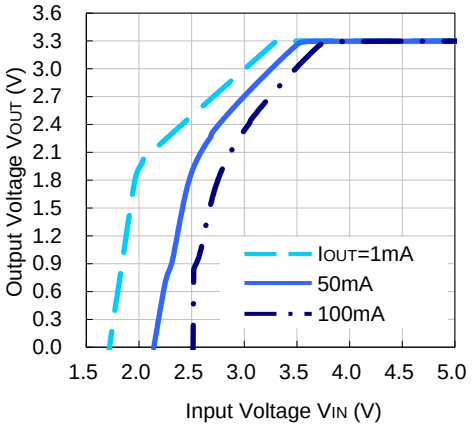

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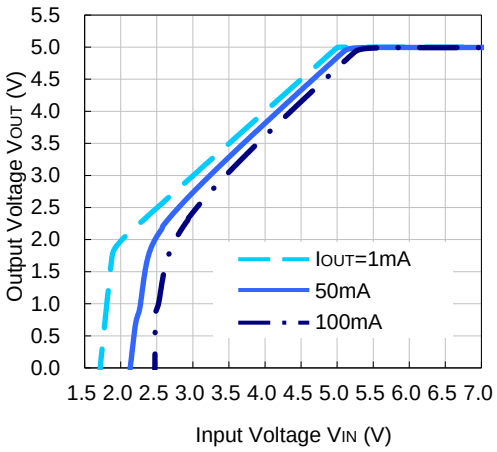

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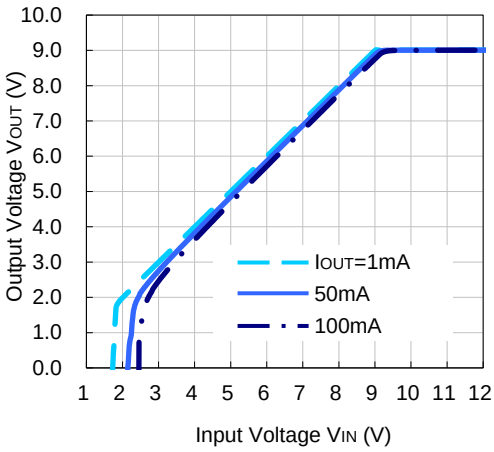
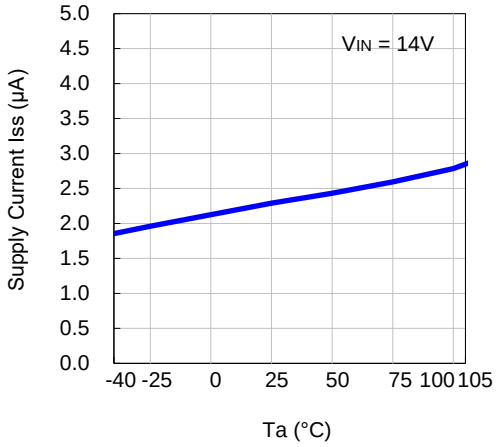


3) Supply Current vs. Temperature

R1524x018B



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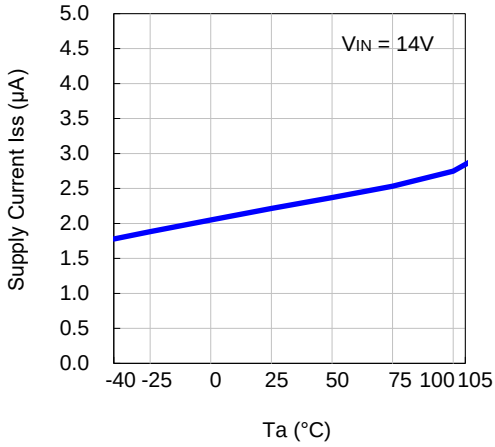

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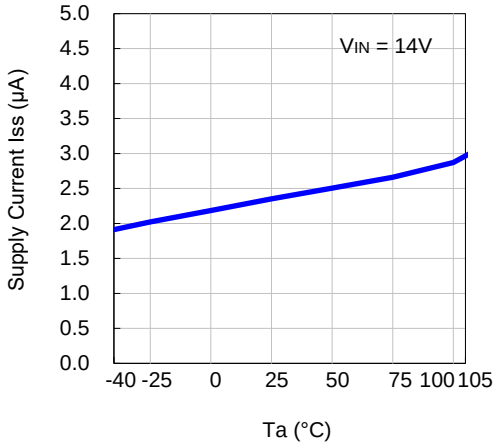

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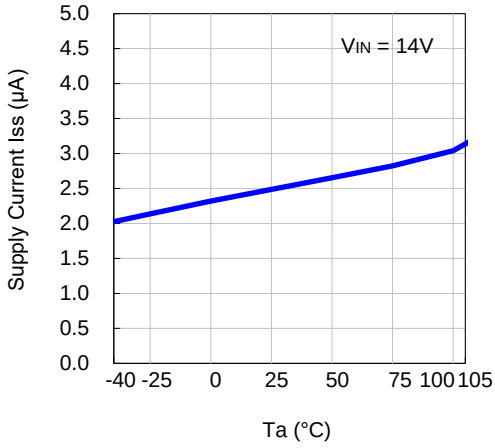
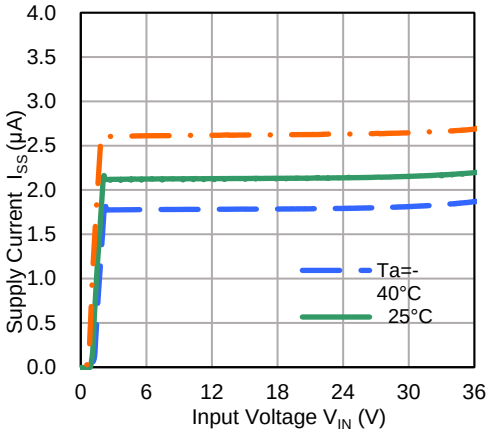


4) Supply Current vs. Input Voltage

R1524x018B



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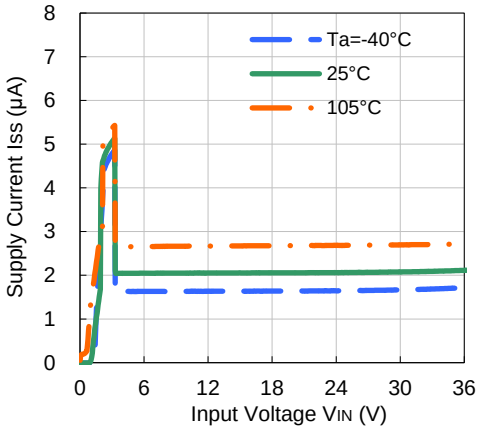
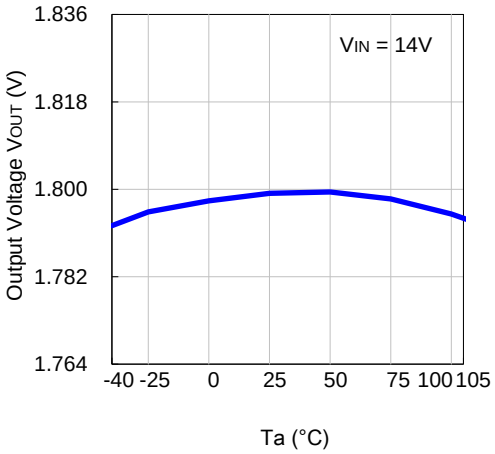


5) Output Voltage vs. Temperature (I_{OUT} = 1 mA)

R1524x018B



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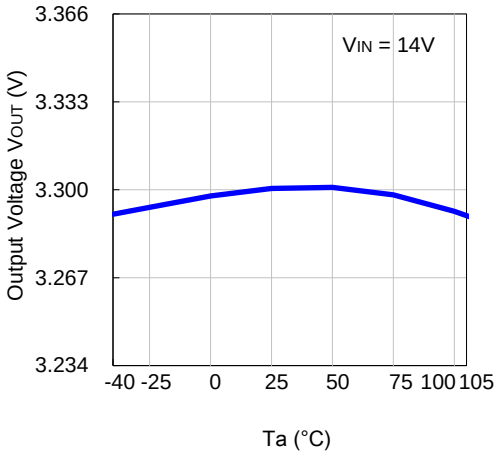

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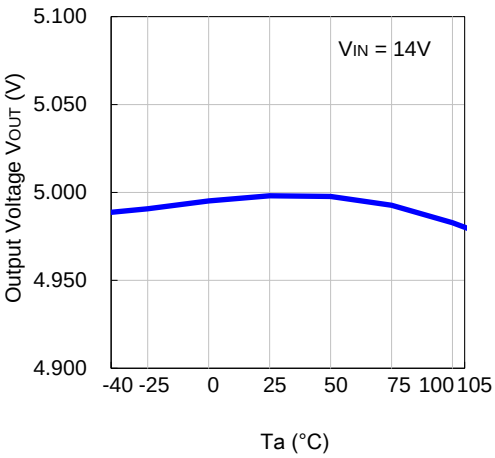

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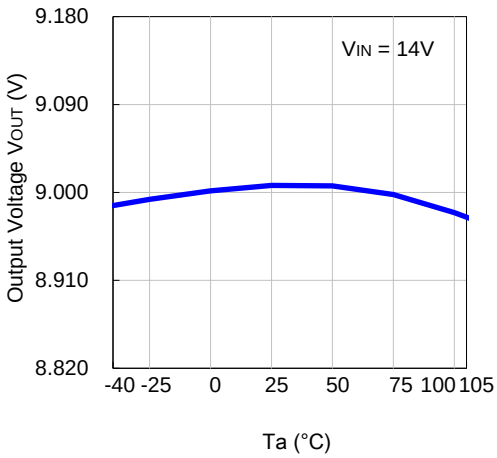
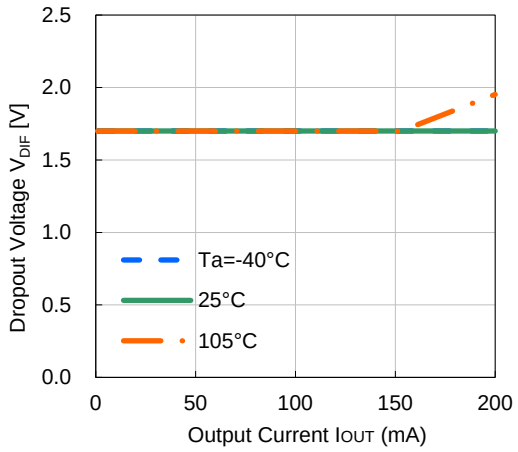
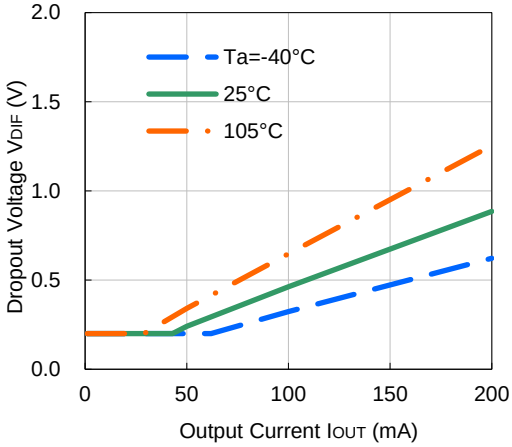


6) Dropout Voltage vs. Output Current

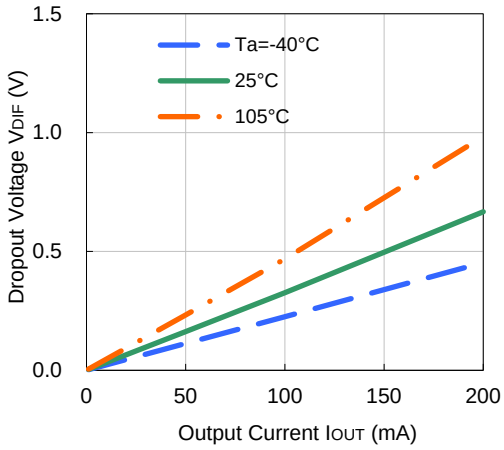
R1524x018B



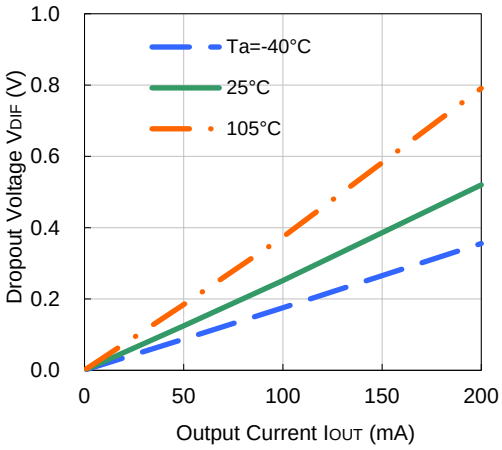
R1524x033B



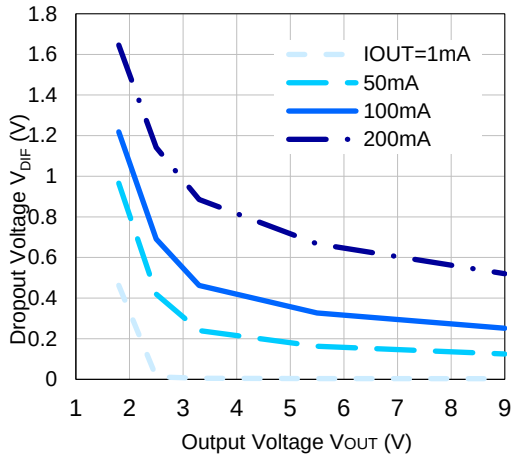
R1524x050B



R1524x090B

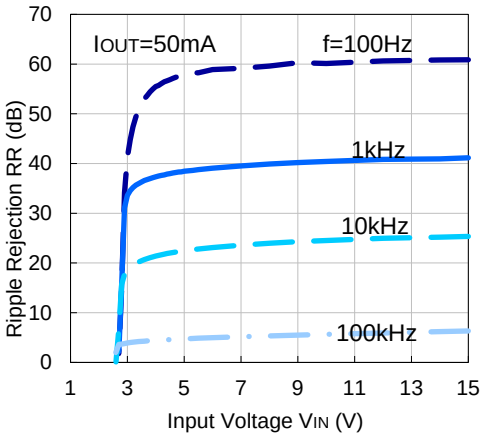


7) Dropout Voltage vs. Output Voltage (Ta = 25°C)



8) Ripple Rejection vs. Input Voltage (Ta = 25°C, Ripple = 0.2 Vpp)

R1524x018B



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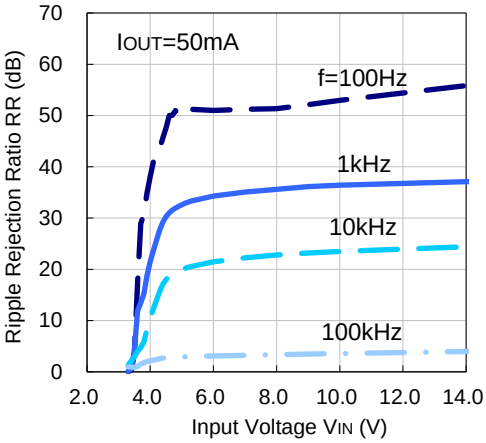

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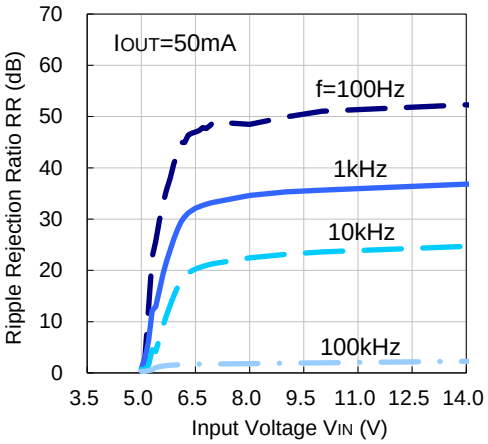
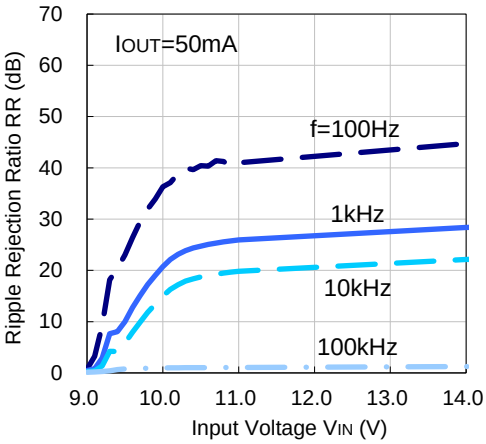
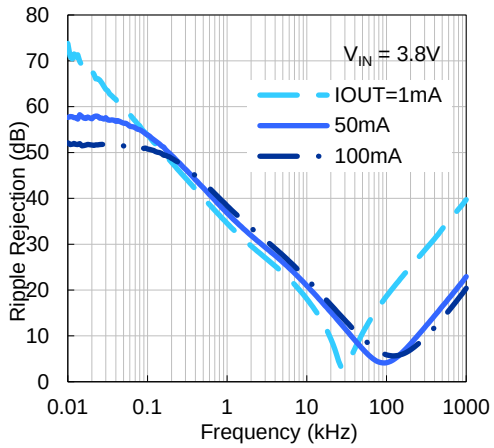


R1524x090B



9) Ripple Rejection vs. Frequency (Ta = 25°C, Ripple = 0.2 Vpp)

R1524x018B



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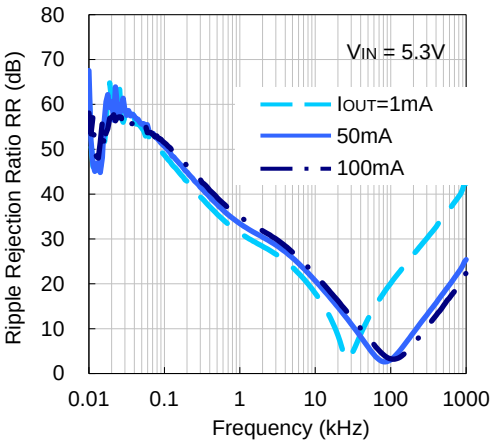

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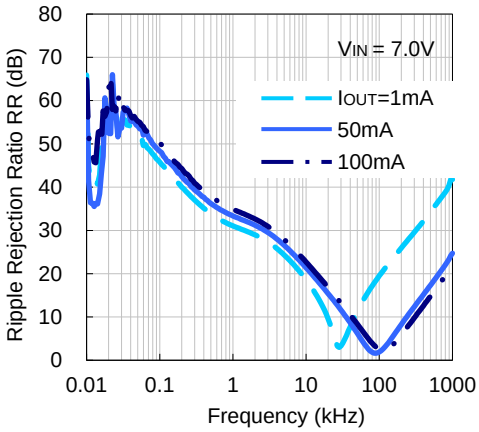

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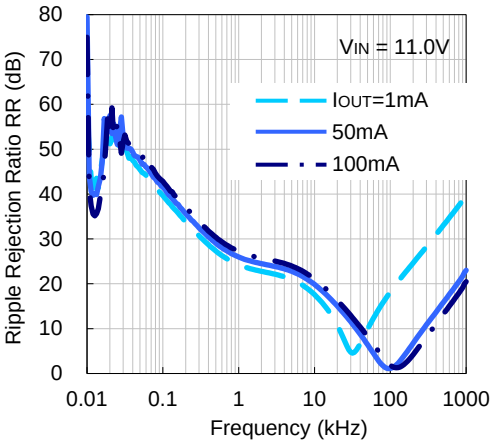
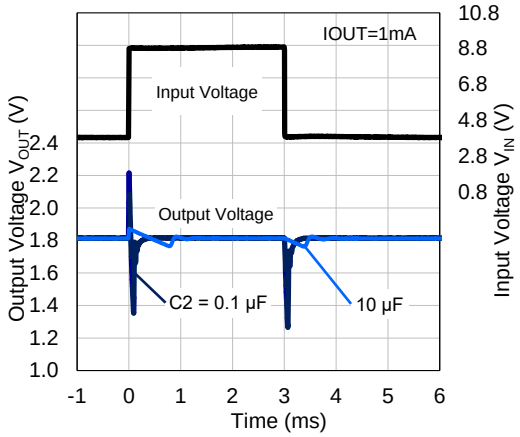


10) Input Transient Response (Ta = 25°C)

R1524x018B



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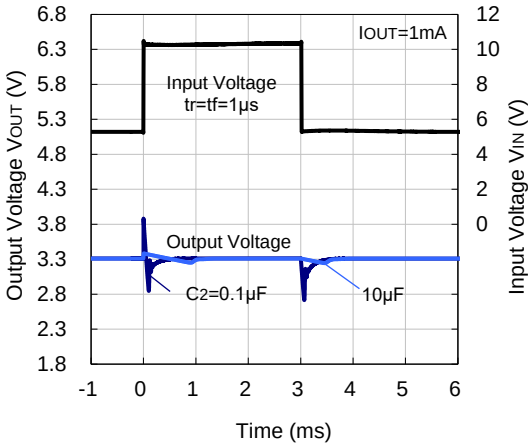

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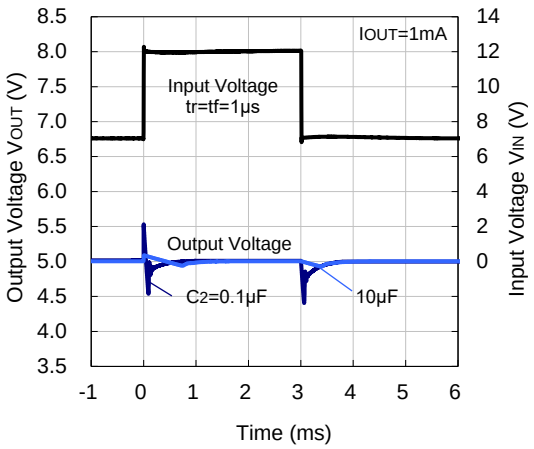
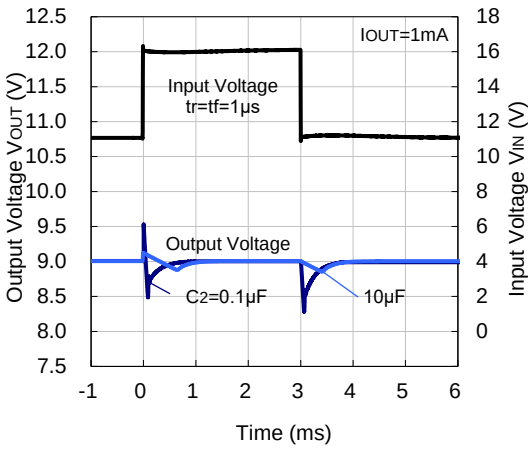
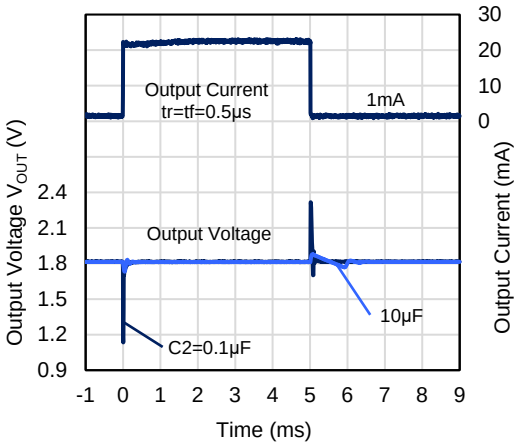


R1524x090B



11) Load Transient Response (Ta = 25°C)

R1524x018B



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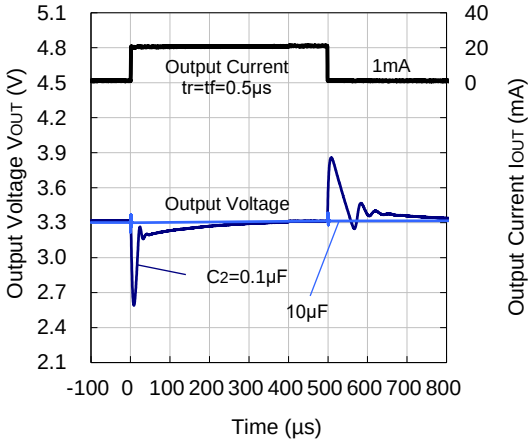
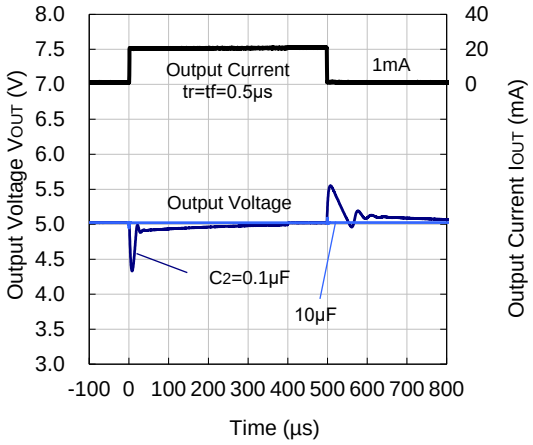


R1524x050B



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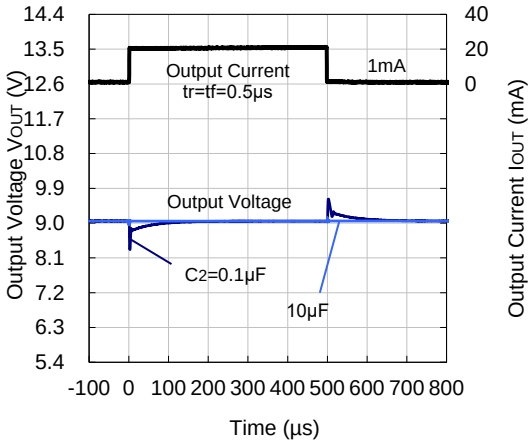
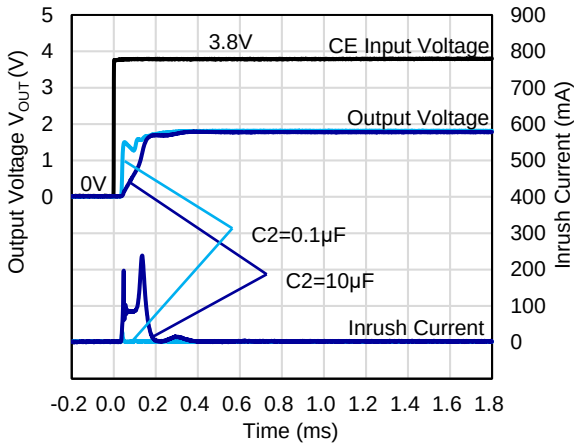
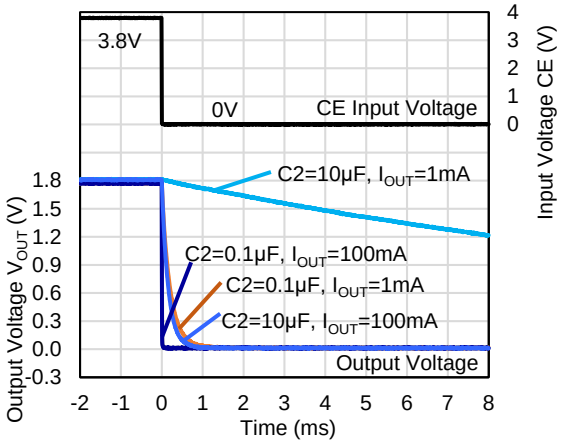


12) CE Transient Response (Ta = 25°C)

R1524x018B





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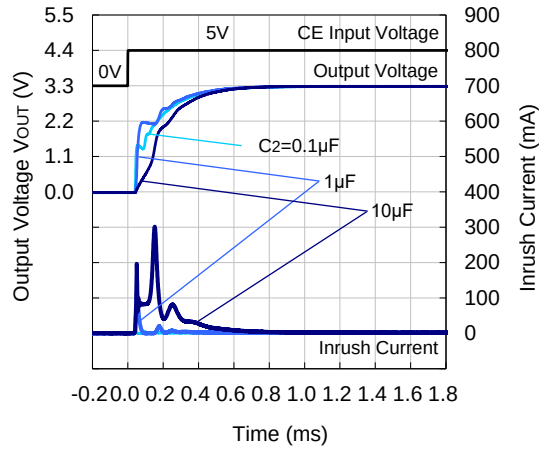

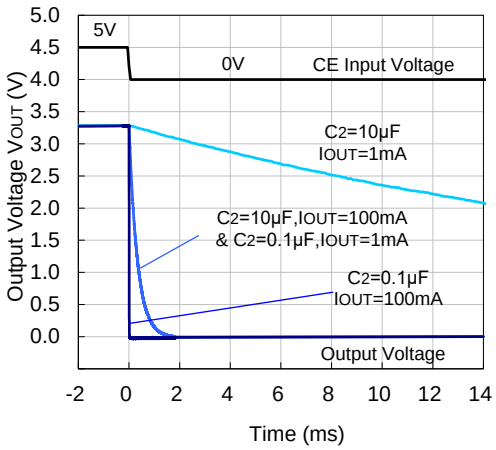

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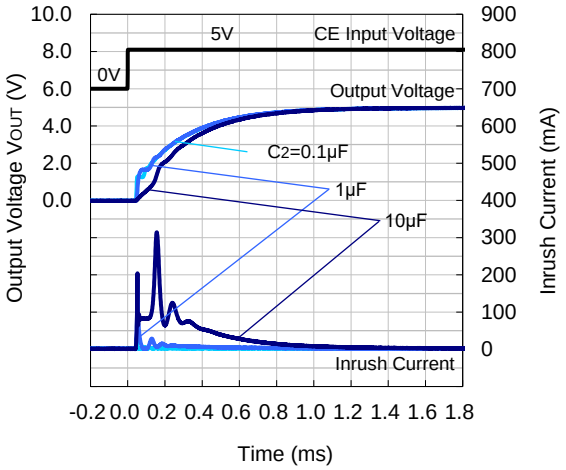

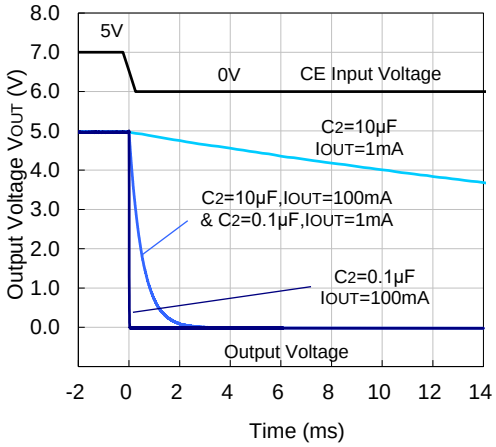

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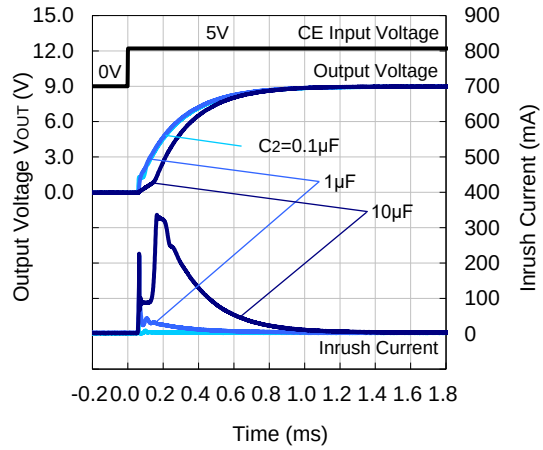
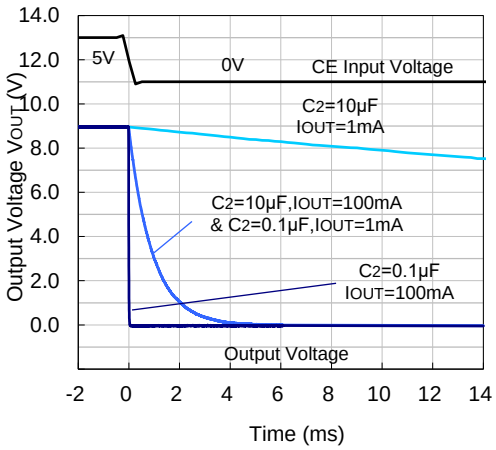
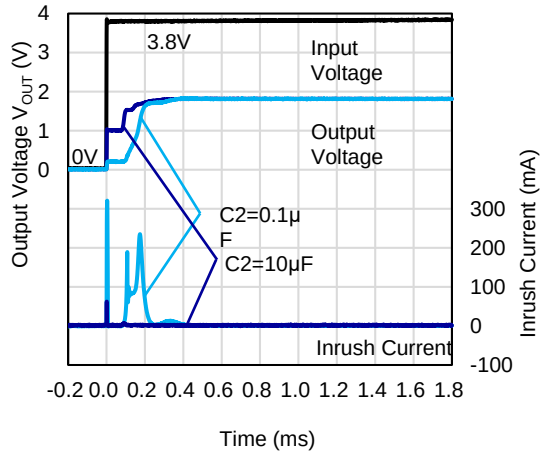




13) Power-on Transient Response (Ta = 25°C, V_{CE} = 5 V)

R1524x018B



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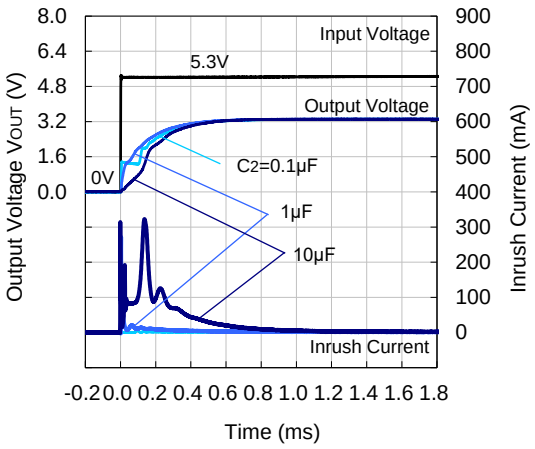

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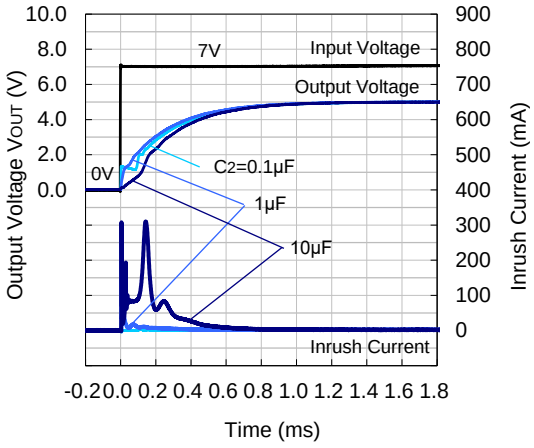

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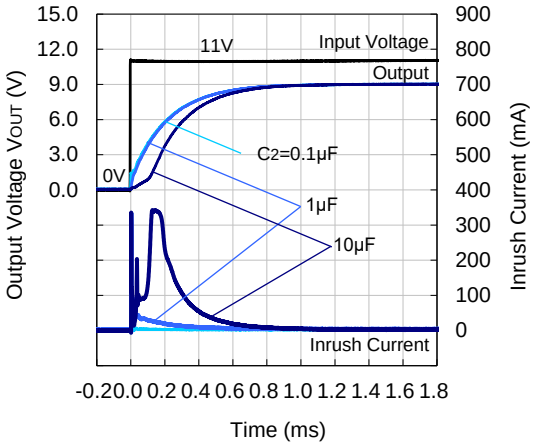
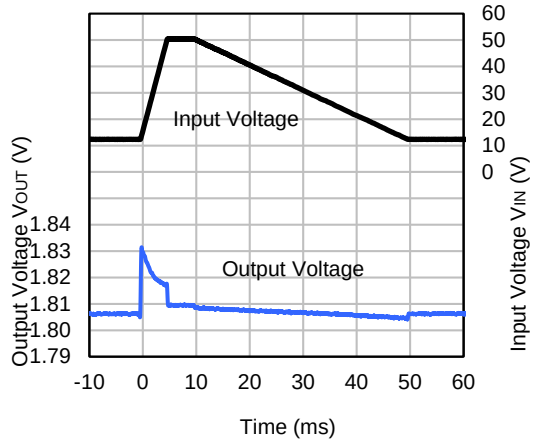


14) Load Dump (Ta = 25°C)

R1524x018B



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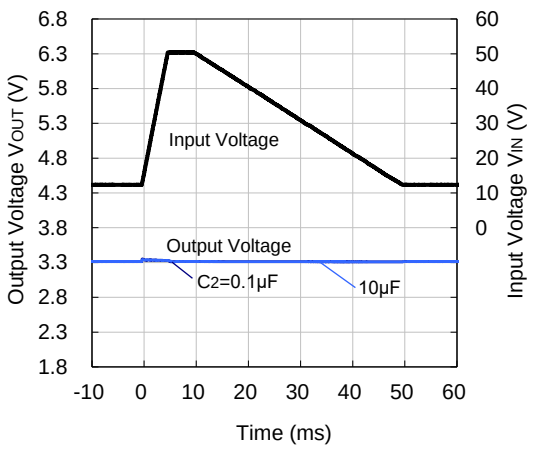

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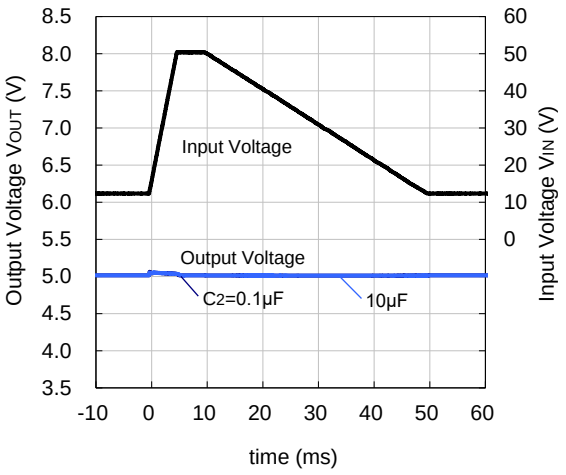
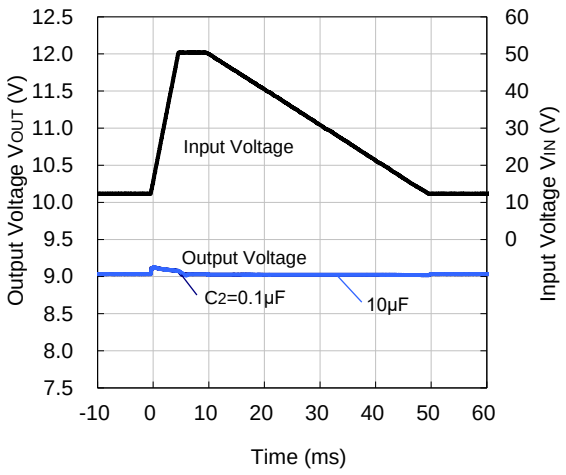
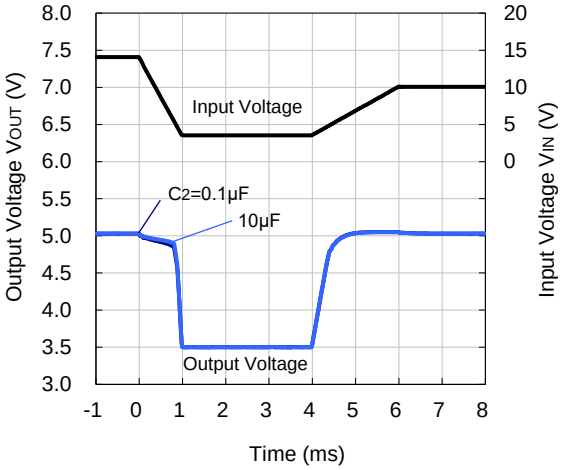


R1524x090B



15) Cranking (Ta = 25°C)

R1524x050B



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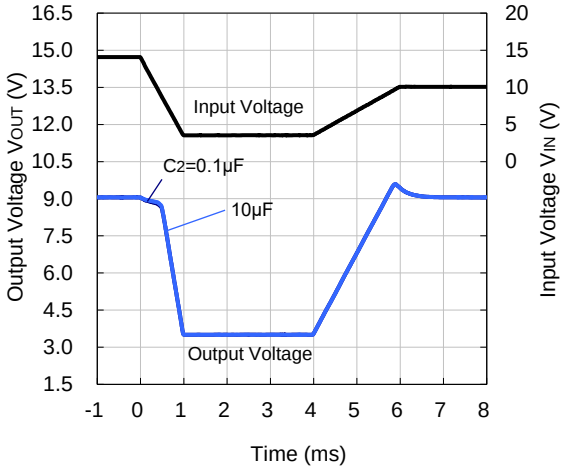
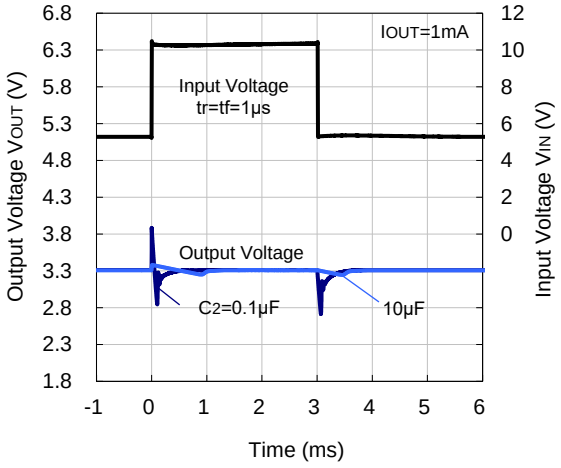


Input Transient/Load Transient vs. Output Capacity (C2)

R1524 performs a stable operation by using 0.1 µF of ceramic capacitor as the output capacitor. However, the variation of output voltage may not meet the demand of the system when input voltage and load current vary. In such cases, the variation of output voltage can be minimized significantly by using 10 µF or higher ceramic capacitor. When using an electrolytic capacitor for the output line, place the electrolytic capacitor outer side of the ceramic capacitor arranged close to the IC.

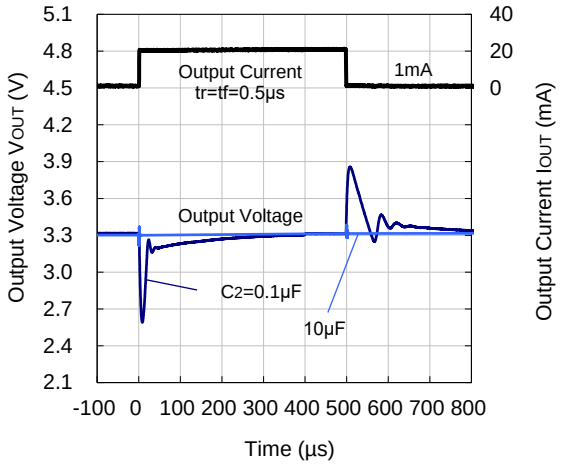
Input Transient Response

R1524x033B



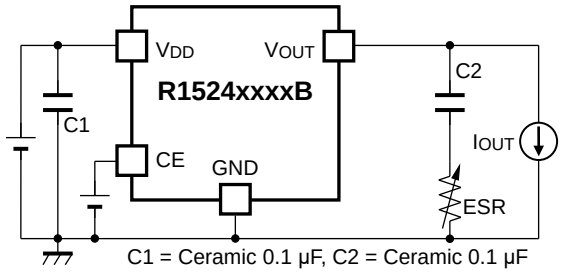
Load Transient Response

R1524x033B



ESR vs. Output Current

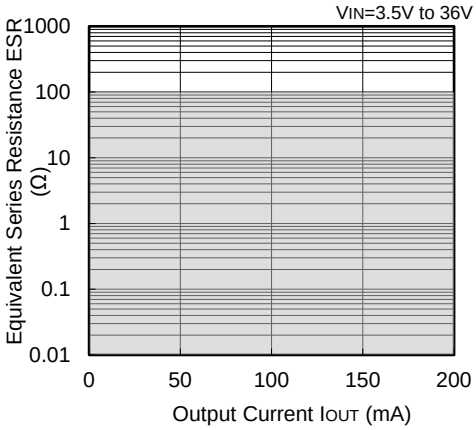
It is recommended that a ceramic type capacitor be used for this device. However, other types of capacitors having lower ESR can also be used. The relation between the output current (I_{OUT}) and the ESR of output capacitor is shown below.



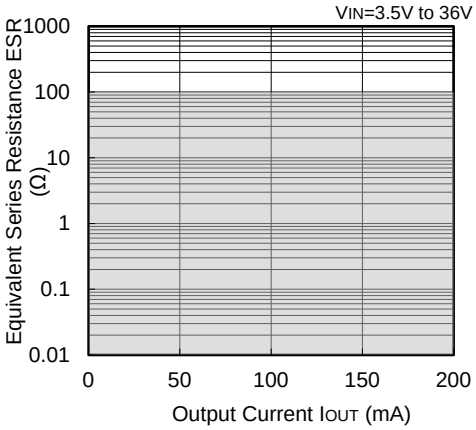
Measurement Conditions

Frequency Band: 10 Hz to 2 MHz
Measurement Temperature: −40°C to 105°C
Hatched area: Noise level is 40 µV (average) or below
Ceramic Capacitors: C1 = 0.1 µF, C2 = 0.1 µF

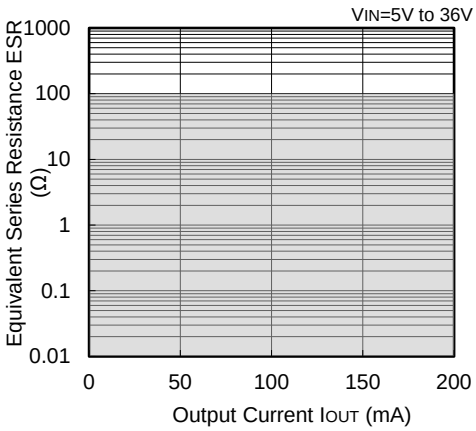
R1524x018B



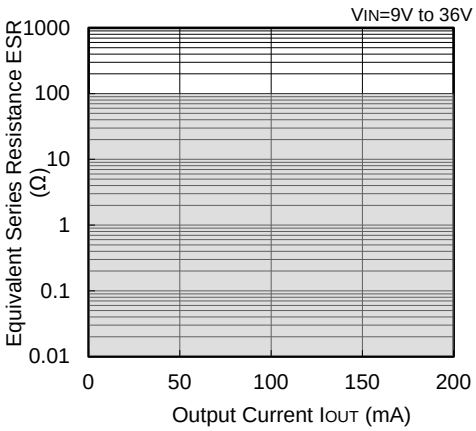
R1524x033B



R1524x050B



R1524x090B



Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

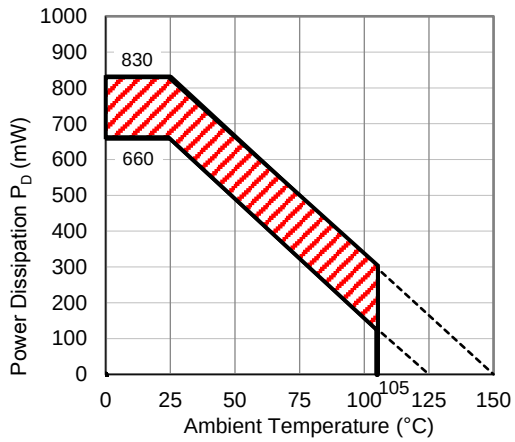
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 7 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

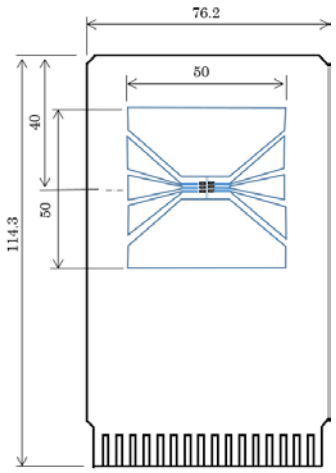
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



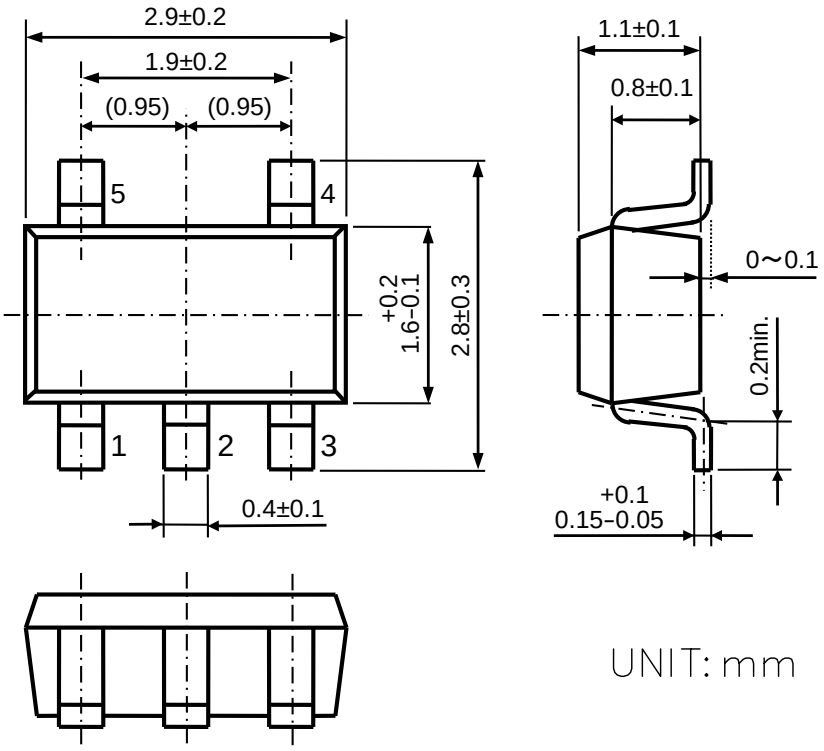
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



SOT-23-5 Package Dimensions

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

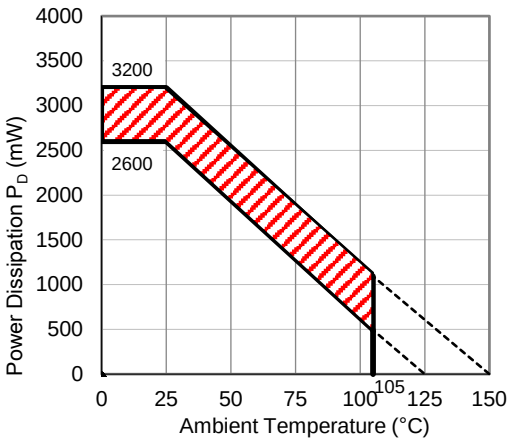
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 13 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

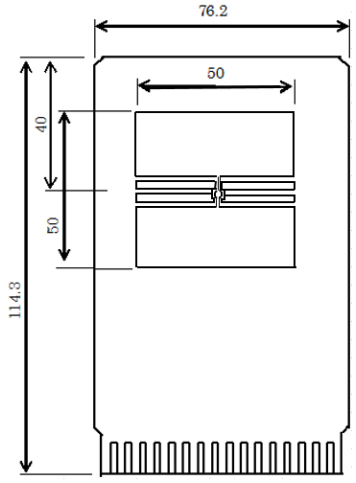
Item	Measurement Result
Power Dissipation	2600 mW
Thermal Resistance (θja)	θja = 38°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 13°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



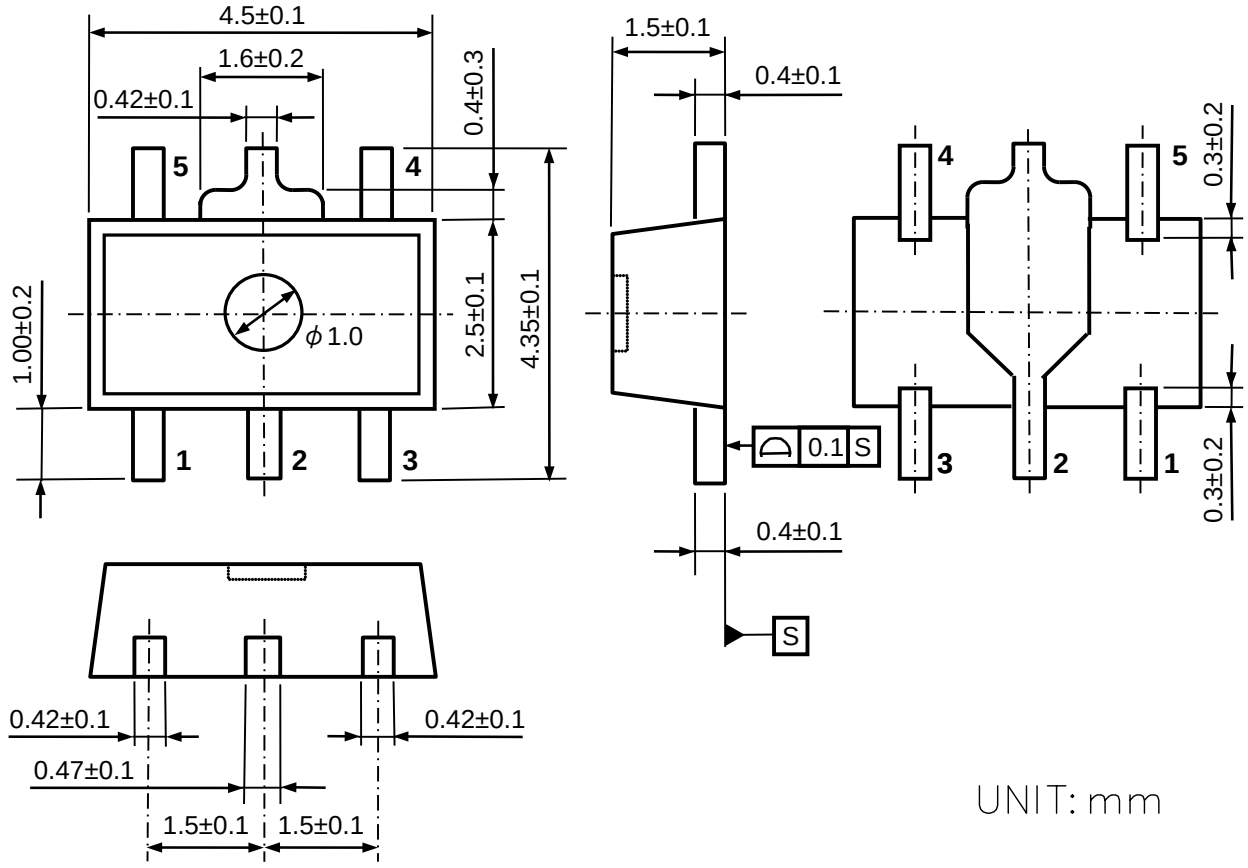
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



SOT-89-5 Package Dimensions

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

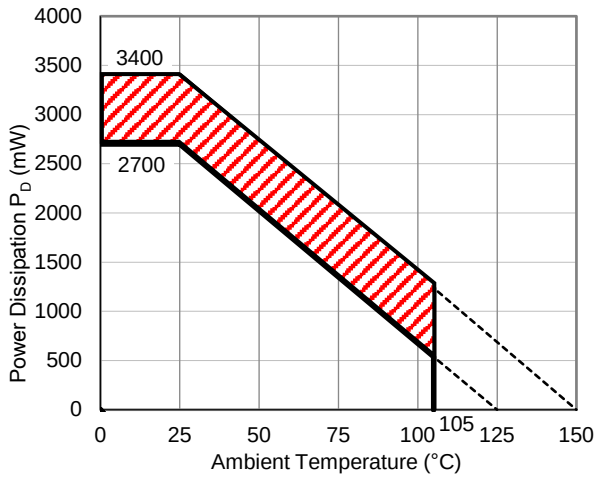
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 28 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

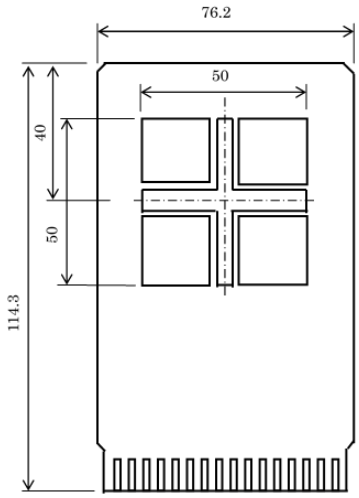
Item	Measurement Result
Power Dissipation	2700 mW
Thermal Resistance (θja)	θja = 37°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 7°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



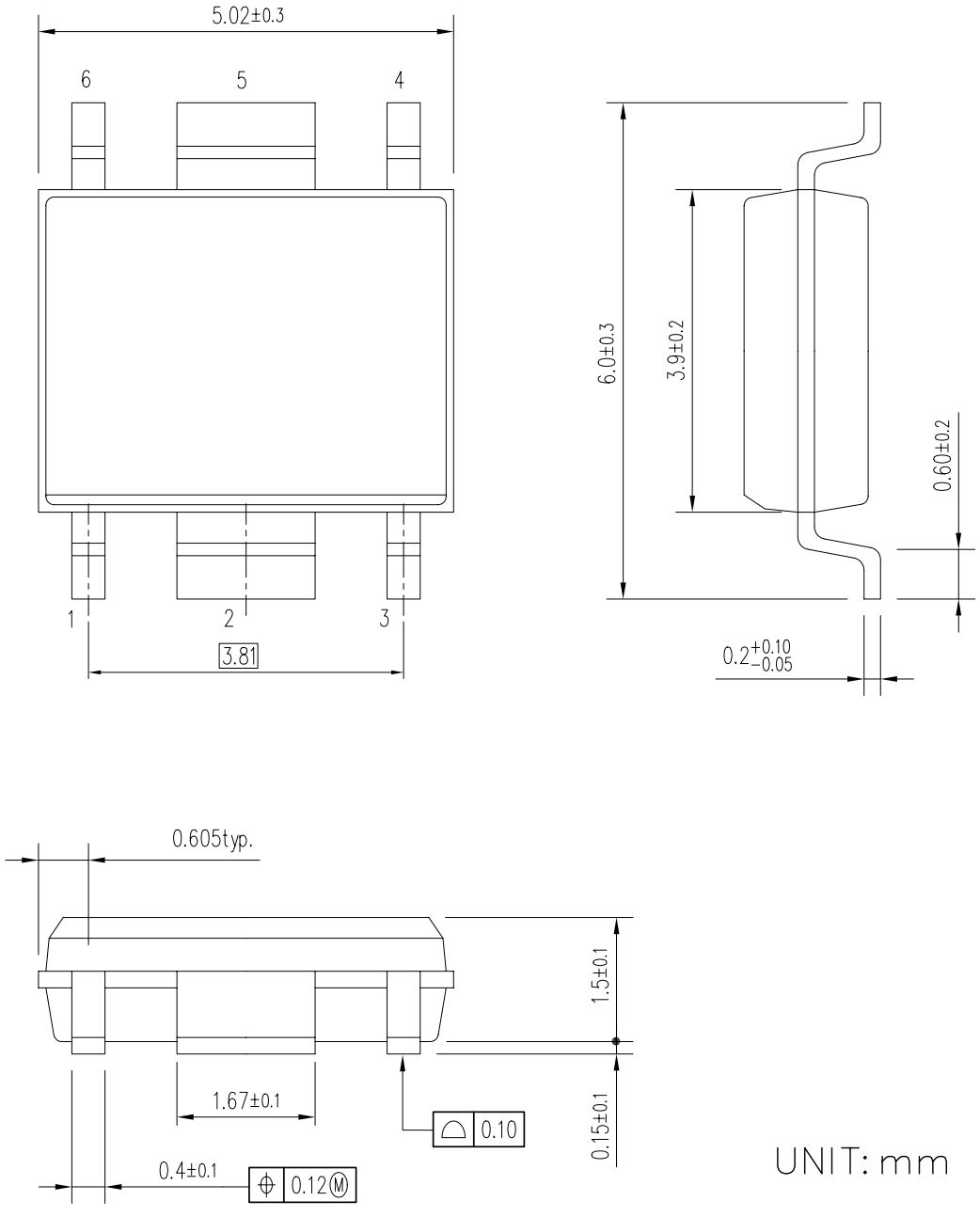
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



HSOP-6J Package Dimensions

Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

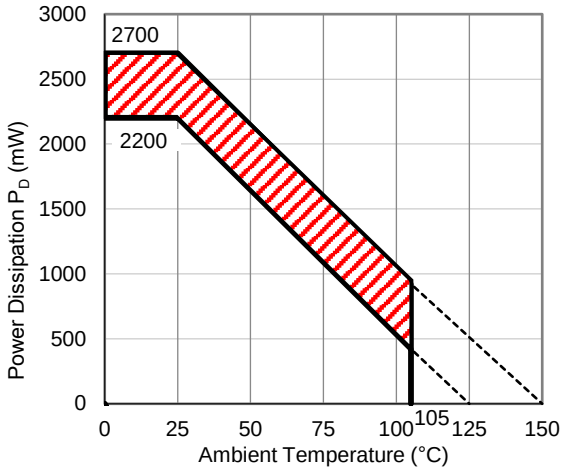
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.2 mm × 34 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

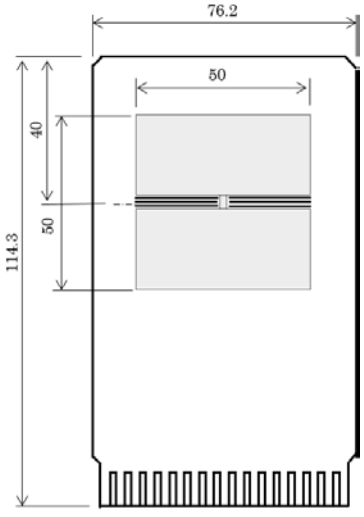
Item	Measurement Result
Power Dissipation	2200 mW
Thermal Resistance (θja)	θja = 45°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 18°C/W

θja: Junction-to–ambient thermal resistance.

ψjt: Junction–to-top of package thermal characterization parameter.



Power Dissipation vs. Ambient Temperature

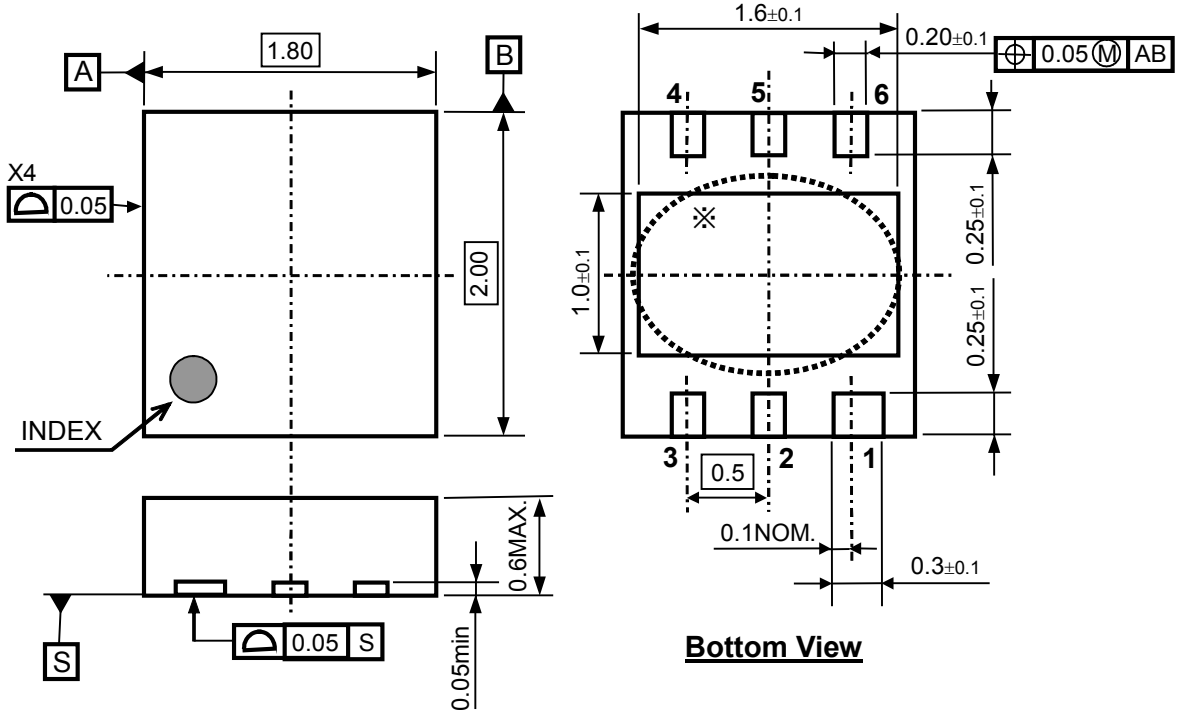


Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

Ver. A



DFN(PLP)1820-6 Package Dimensions (Unit: mm)

∗ The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

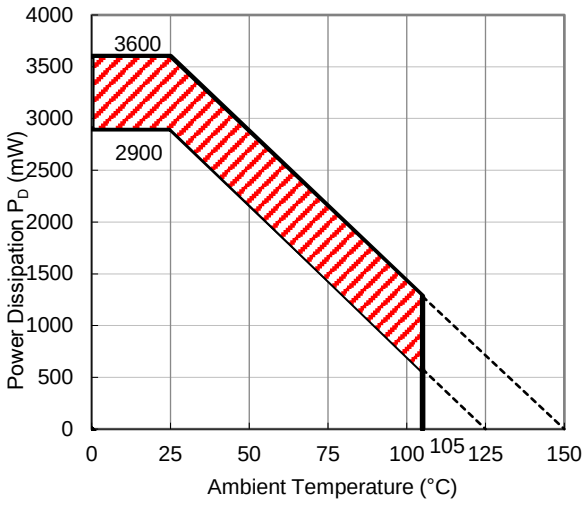
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

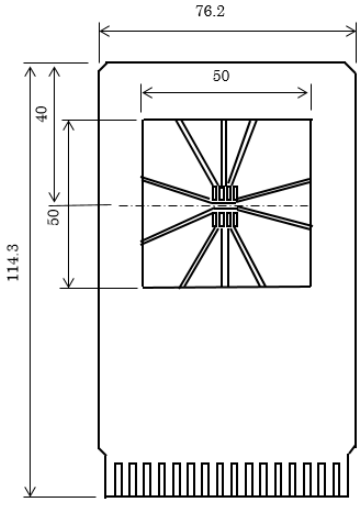
Item	Measurement Result
Power Dissipation	2900 mW
Thermal Resistance (θja)	θja = 34.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10 °C/W

θja: Junction-to–ambient thermal resistance.

ψjt: Junction–to-top of package thermal characterization parameter.



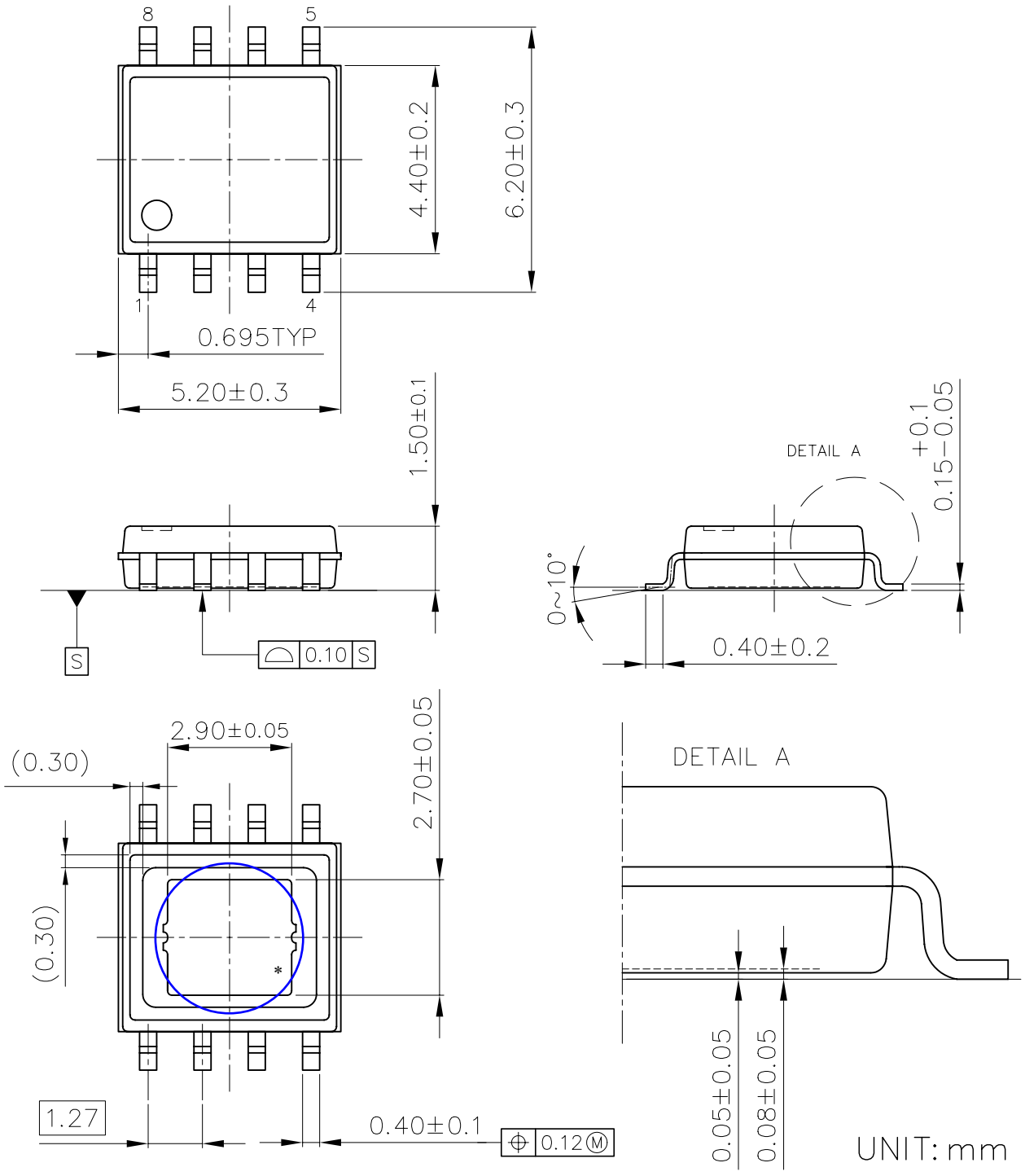
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years



HSOP-8E Package Dimensions

∗ The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

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