

N-channel 800 V, 2.75 Ω typ., 2 A MDmesh™ K5 Power MOSFET in a DPAK package

Datasheet - production data

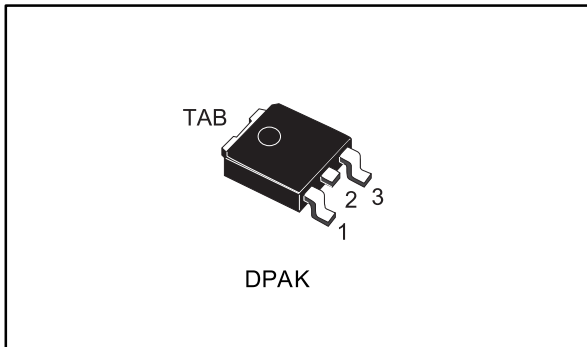
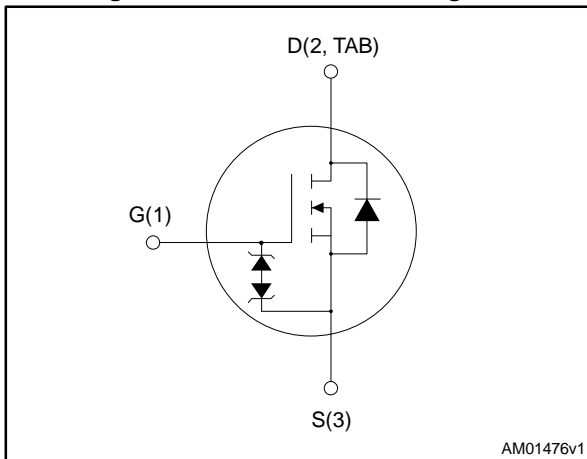


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max | I _D |
|------------|-----------------|-------------------------|----------------|
| STD3LN80K5 | 800 V | 3.25 Ω | 2 A |

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|---------|---------------|
| STD3LN80K5 | 3LN80K5 | DPAK | Tape and reel |

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|-------------|------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ °C}$ | 2 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ °C}$ | 1.25 | A |
| $I_D^{(1)}$ | Drain current (pulsed) | 8 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ °C}$ | 45 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 4.5 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | |
| T_{stg} | Storage temperature range | - 55 to 150 | °C |
| T_j | Operating junction temperature range | | |

Notes:

(1)Pulse width limited by safe operating area.

(2) $I_{SD} \leq 2\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$; $V_{DSpeak} < V_{(BR)DSS}$, $V_{DD} = 640\text{ V}$

(3) $V_{DS} \leq 640\text{ V}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case | 2.78 | °C/W |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 50 | °C/W |

Notes:

(1)When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 0.7 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$) | 155 | mJ |

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|-----------------------------------|--|------|------|------|------|
| V _{(BR)DSS} | Drain-source breakdown voltage | I _D = 1 mA, V _{GS} = 0 V | 800 | | | V |
| I _{DSS} | Zero gate voltage drain current | V _{DS} = 800 V, V _{GS} = 0 V | | | 1 | μA |
| | | V _{DS} = 800 V, V _{GS} = 0 V, T _C = 125 °C ⁽¹⁾ | | | 50 | μA |
| I _{GSS} | Gate body leakage current | V _{GS} = ± 20 V, V _{GS} = 0 V | | | ±10 | μA |
| V _{GS(th)} | Gate threshold voltage | V _{DS} = V _{GS} , I _D = 100 μA | 3 | 4 | 5 | V |
| R _{DS(on)} | Static drain-source on-resistance | V _{GS} = 10 V, I _D = 1 A | | 2.75 | 3.25 | Ω |

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|---------------------------------------|--|------|------|------|------|
| C _{iss} | Input capacitance | V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V | - | 102 | - | pF |
| C _{oss} | Output capacitance | | - | 11 | - | pF |
| C _{rss} | Reverse transfer capacitance | | - | 0.1 | - | pF |
| C _{otr} ⁽¹⁾ | Equivalent capacitance time related | V _{DS} = 0 to 640 V, V _{GS} = 0 V | - | 20 | - | pF |
| C _{oer} ⁽²⁾ | Equivalent capacitance energy related | | - | 7 | - | pF |
| R _G | Intrinsic gate resistance | f = 1 MHz, I _D = 0 A | - | 12 | - | Ω |
| Q _g | Total gate charge | V _{DD} = 640 V, I _D = 2 A, V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge behavior") | - | 2.63 | - | nC |
| Q _{gs} | Gate-source charge | | - | 0.91 | - | nC |
| Q _{gd} | Gate-drain charge | | - | 1.53 | - | nC |

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform") | - | 6.2 | - | ns |
| t_r | Rise time | | - | 7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 30 | - | ns |
| t_f | Fall time | | - | 26 | - | ns |

Table 8: Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 2 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 8 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 2\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 210 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 0.8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 7.6 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$, (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 345 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1.2 | | μC |
| I_{RRM} | Reverse recovery current | | - | 7.2 | | A |

Notes:

(1)Pulse width limited by safe operating area.

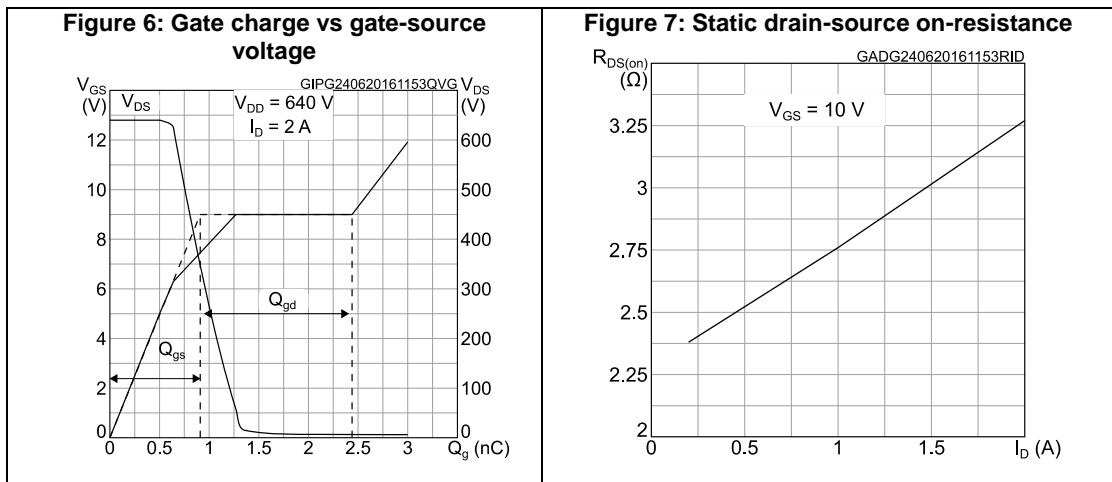
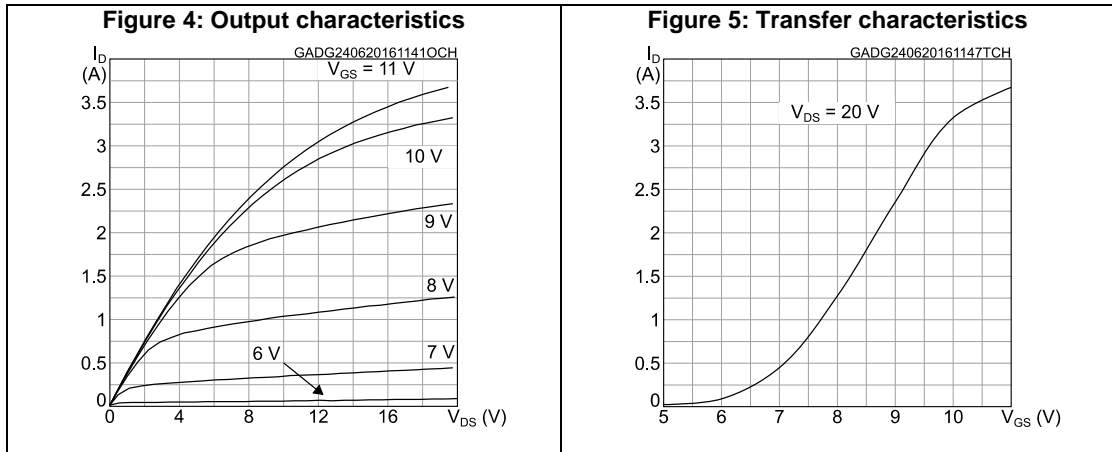
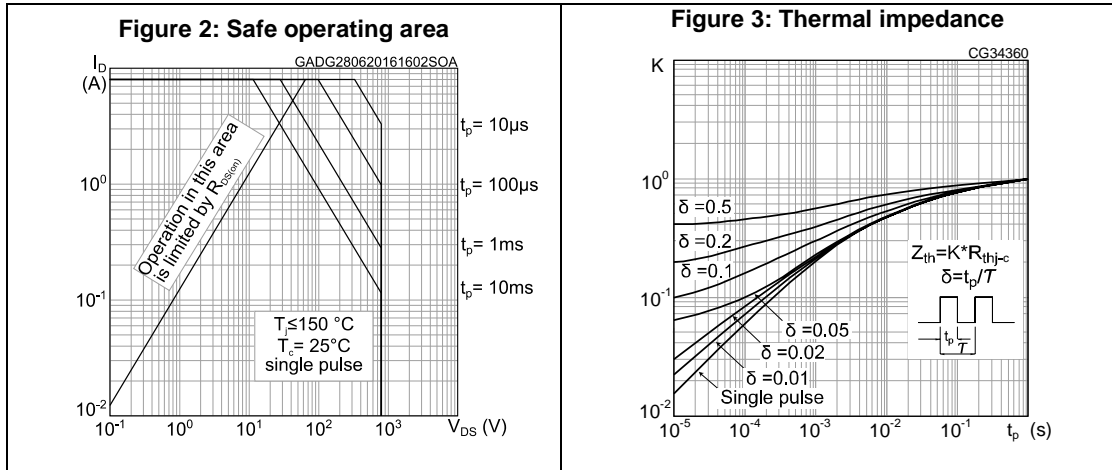
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

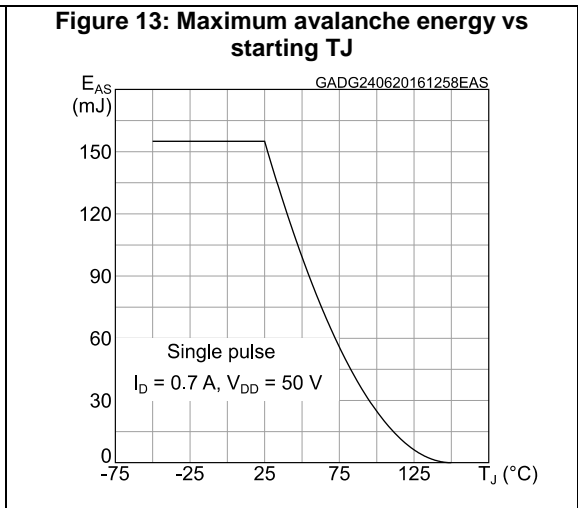
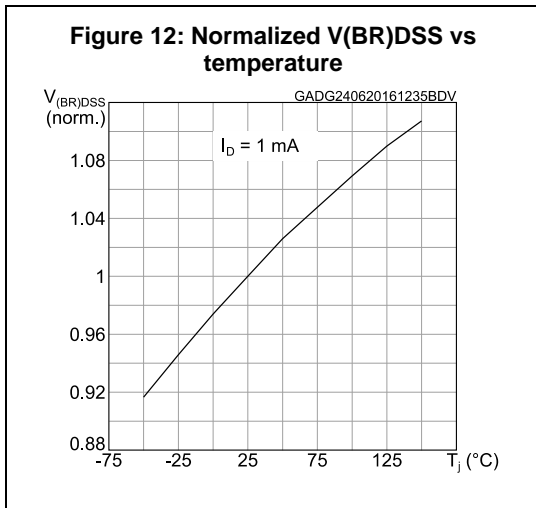
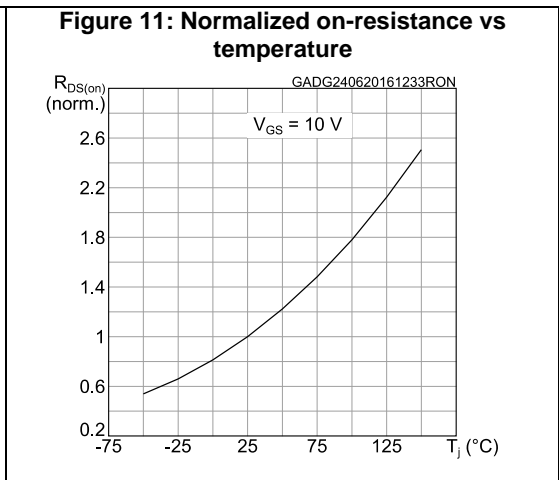
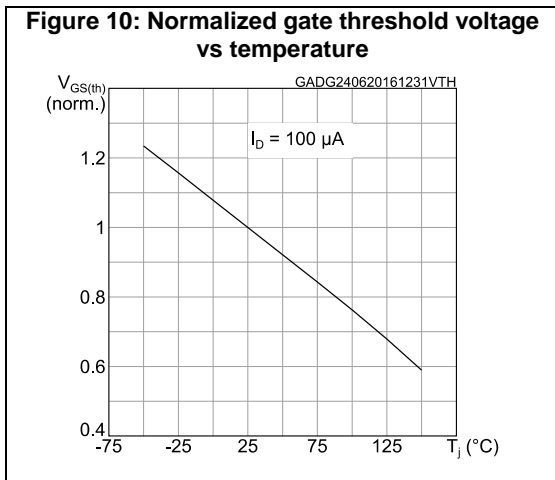
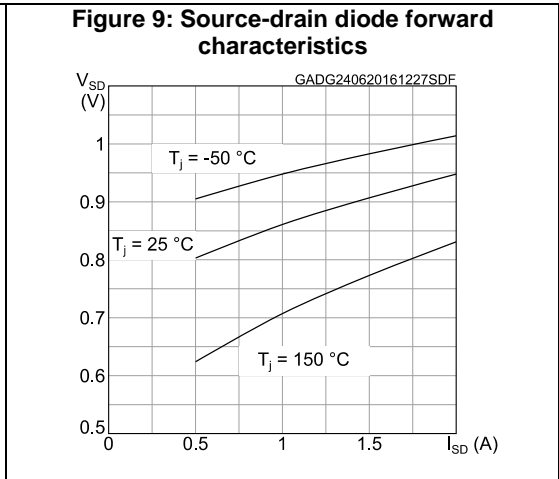
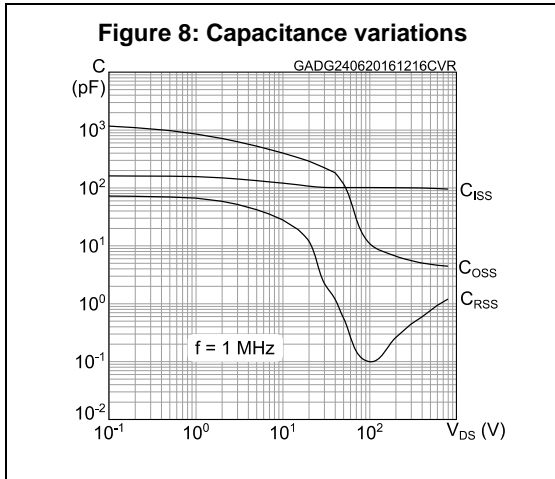
Table 9: Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$ | 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

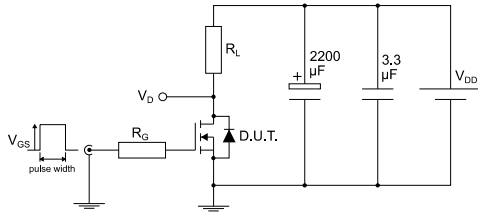
2.1 Electrical characteristics (curves)





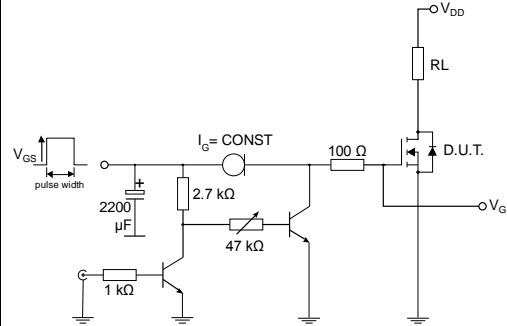
3 Test circuits

Figure 14: Test circuit for resistive load switching times



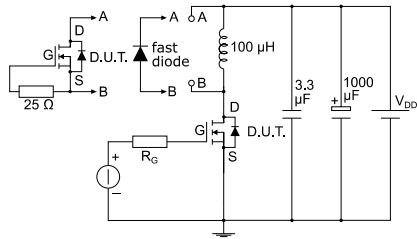
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Figure 15: Test circuit for gate charge behavior



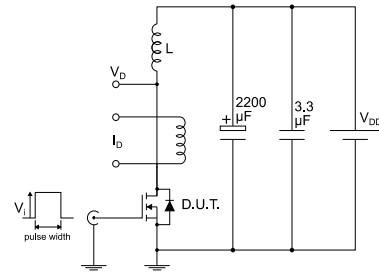
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Figure 16: Test circuit for inductive load switching and diode recovery times



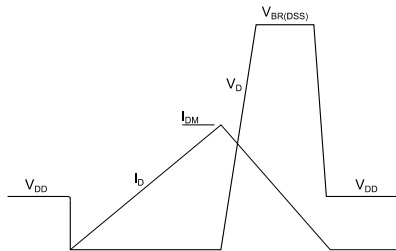
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Figure 17: Unclamped inductive load test circuit



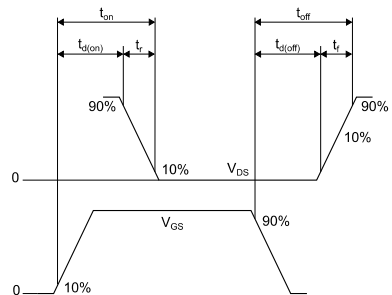
AM01471v1

Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK package information

Figure 20: DPAK (TO-252) type A package outline

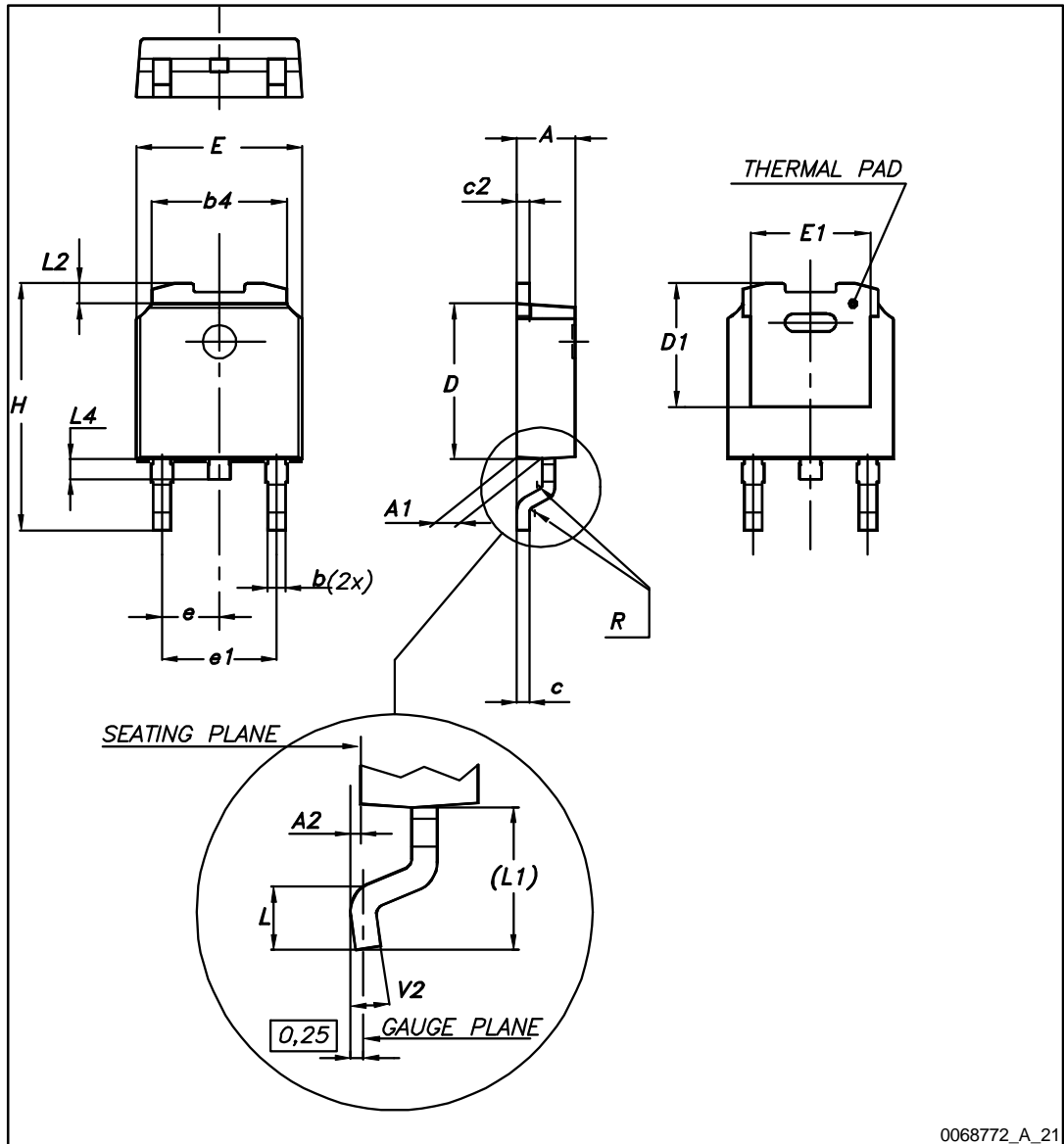
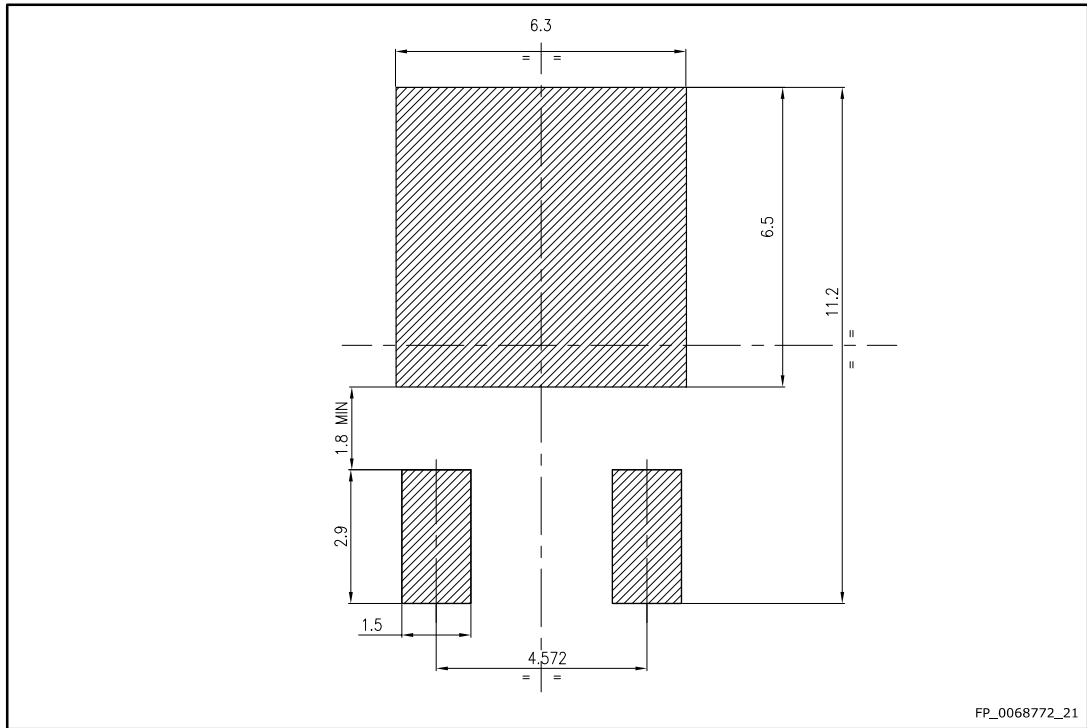


Table 10: DPAK (TO-252) type A mechanical data

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 4.60 | 4.70 | 4.80 |
| e | 2.16 | 2.28 | 2.40 |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| (L1) | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK packing information

Figure 22: DPAK (TO-252) tape outline

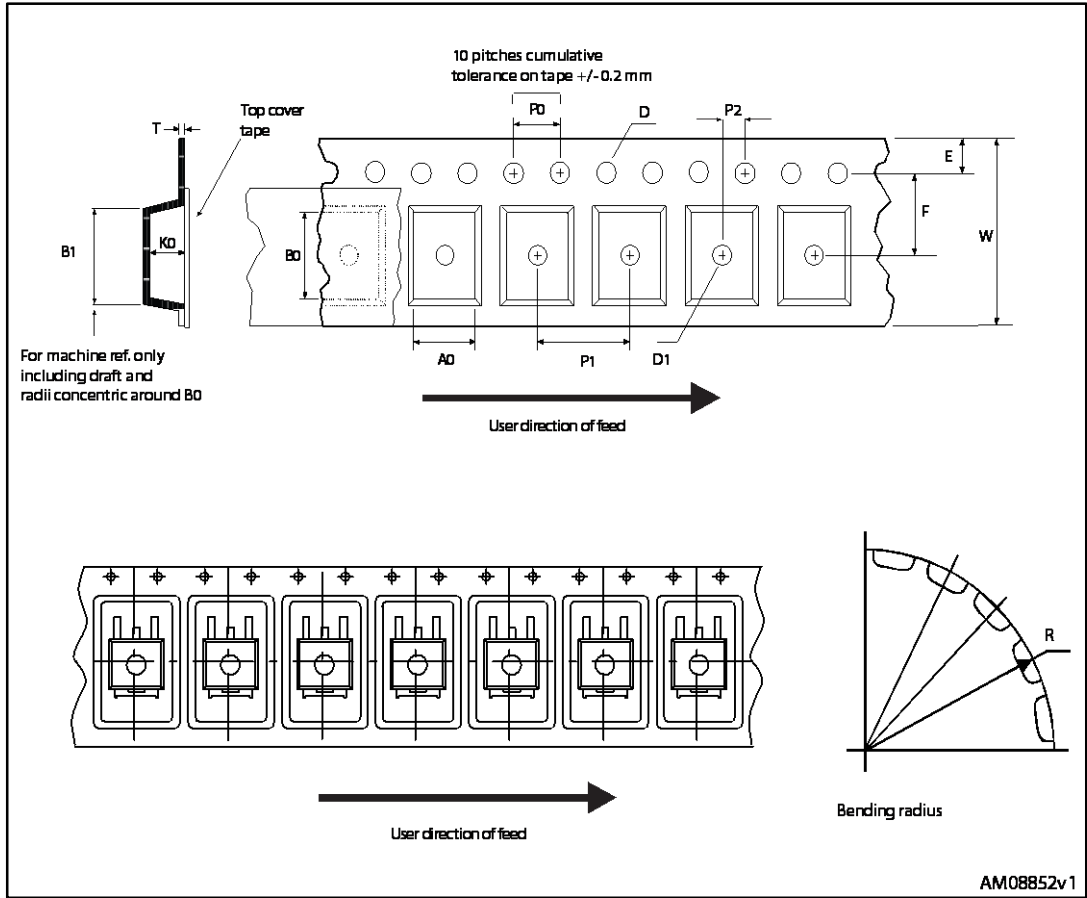


Figure 23: DPAK (TO-252) reel outline

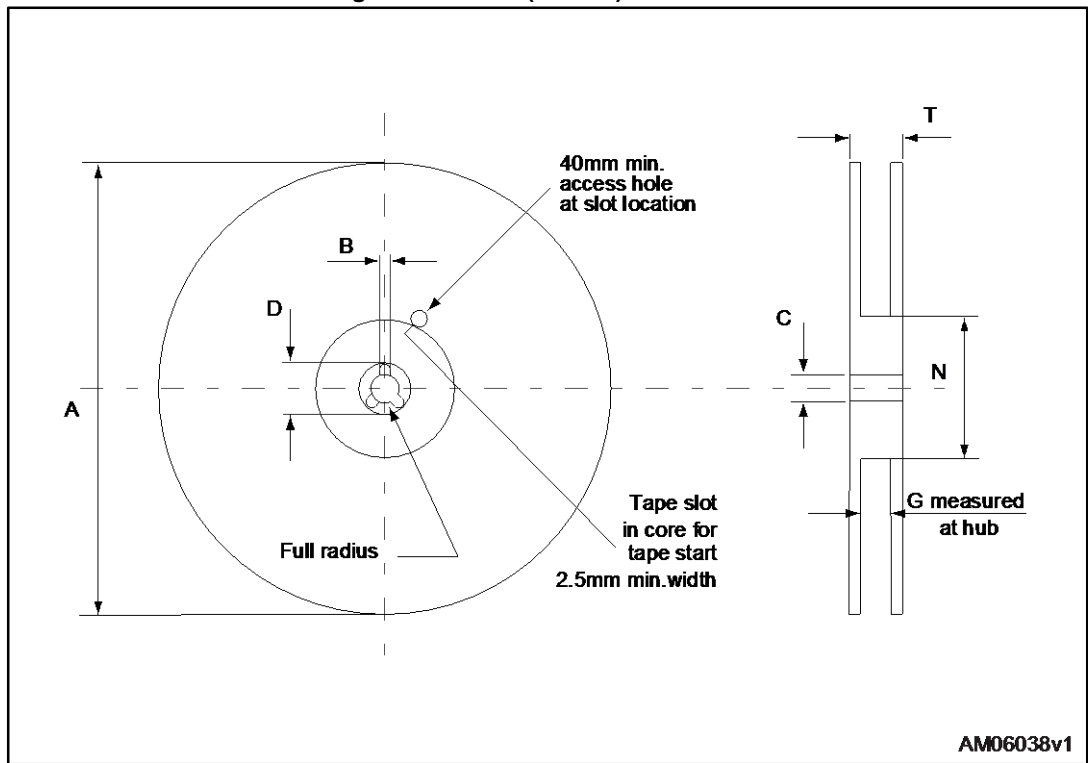


Table 11: DPAK (TO-252) tape and reel mechanical data

| Tape | | | Reel | | |
|------|------|------|-----------|------|------|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

5 Revision history

Table 12: Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 13-May-2015 | 1 | Initial release |
| 27-Jul-2016 | 2 | Updated title and features in cover page. Updated <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Document status promoted from preliminary to production data. Minor text changes. |

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