

- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS (5)
- Sink to Lead Creepage Dist. = 4.8mm
- Fully Avalanche Rated
- Lead-Free

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low onresistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

	HEXFET®	Power MOSFET
	V <sub>DSS</sub>	100V
G	R <sub>DS(on)</sub>	0.036Ω
	Ι <sub>D</sub>	24A



G	D	S
Gate	Drain	Source

Base Part Number	Baakaga Tupa	Standard Pack		Orderable Part Number
Base Fait Nulliber	Package Type	Form	Quantity	Orderable Part Nulliber
IRFI1310NPbF	TO-220 Full-Pak	Tube	50	IRFI1310NPbF

Absolute Maximu	Im Ratings		
Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	24	
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	17	Α
I <sub>DM</sub>	Pulsed Drain Current ①6	140	
P <sub>D</sub> @T <sub>C</sub> = 25°C	Maximum Power Dissipation	56	W
	Linear Derating Factor	0.37	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) 26	420	mJ
I <sub>AR</sub>	Avalanche Current ①⑥	22	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	5.6	mJ
dv/dt	Peak Diode Recovery dv/dt36	5.0	V/ns
TJ	Operating Junction and	-55 to + 175	
T <sub>STG</sub>	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

#### Thermal Resistance

Symbol	Parameter	Тур.	Max.	Units
$R_{ ext{ heta}JC}$	Junction-to-Case		2.7	°C 1.11
$R_{ heta JA}$	Junction-to-Ambient		65	°C/W



	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100				$V_{GS} = 0V, I_D = 250 \mu A$
$\Delta V_{(BR)DSS} / \Delta T_J$	Breakdown Voltage Temp. Coefficient		0.11			Reference to $25^{\circ}$ C, I <sub>D</sub> = 1mA (6)
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance			0.036		$V_{GS} = 10V, I_D = 13A$
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0		4.0		$V_{DS} = V_{GS}, I_D = 250 \mu A$
gfs	Forward Trans conductance	14				$V_{DS} = 25V, I_D = 22A$
913				25		$V_{DS} = 230$ , $T_D = 22$ K $V_{DS} = 100$ V, $V_{GS} = 0$ V
I <sub>DSS</sub>	Drain-to-Source Leakage Current			250	μA	$V_{DS} = 100 V, V_{GS} = 0V$ $V_{DS} = 80V, V_{GS} = 0V, T_J = 150^{\circ}C$
1	Gate-to-Source Forward Leakage			100		V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Reverse Leakage			-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge			120		I <sub>D</sub> = 22A
Q <sub>gs</sub>	Gate-to-Source Charge			15	nC	V <sub>DS</sub> = 80V
Q <sub>qd</sub>	Gate-to-Drain Charge			58		V <sub>GS</sub> = 10V , See Fig. 6 and 13④⑥
t <sub>d(on)</sub>	Turn-On Delay Time		11			$V_{DD} = 50V$
t <sub>r</sub>	Rise Time		56			I <sub>D</sub> =22A
t <sub>d(off)</sub>	Turn-Off Delay Time		45		ns	R <sub>G</sub> = 3.6Ω
t <sub>f</sub>	Fall Time		40			R <sub>D</sub> = 2.9Ω, See Fig. 10⊕᠖
L <sub>D</sub>	Internal Drain Inductance		4.5			Between lead, 6mm (0.25in.)
Ls	Internal Source Inductance		7.5			from package and center of die contact
C <sub>iss</sub>	Input Capacitance		1900			V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance		450		pF	V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance		230		рг	f = 1.0MHz, See Fig. 5⑥
С	Drain to Sink Capacitance		12			f = 1.0MHz
Source-Drain	Ratings and Characteristics					
	Parameter	Min.	Тур.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)			24		MOSFET symbol showing the
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			140	A	integral reverse
V <sub>SD</sub>	Diode Forward Voltage			1.3	V	$T_{J} = 25^{\circ}C, I_{S} = 13A, V_{GS} = 0V$ (4)
t <sub>rr</sub>	Reverse Recovery Time		180	270	ns	T <sub>J</sub> = 25°C ,I <sub>F</sub> = 22A
Q <sub>rr</sub>	Reverse Recovery Charge		1.2	1.8	μC	di/dt = 100A/µs ⊛᠖
t <sub>on</sub>	Forward Turn-On Time	Intrinsic	turn-on	time is	nealiaib	le (turn-on is dominated by $L_{s}+L_{p}$ )

Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Notes:

 $\odot\;$  Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

@ starting T<sub>J</sub> = 25°C, L = 1.0mH, R<sub>G</sub> = 25 $\Omega$ , I<sub>AS</sub> = 22A (See fig. 12)

 $\label{eq:ISD} \ensuremath{\mathbb{3}} \quad I_{SD} \leq 22A, \ di/dt \leq 180A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \ T_J \leq 175^\circ C.$ 

④ Pulse width  $\leq$  300µs; duty cycle  $\leq$  2%.

⑤ t=60s, *f*=60Hz

© Uses IRF1310N data and test conditions.



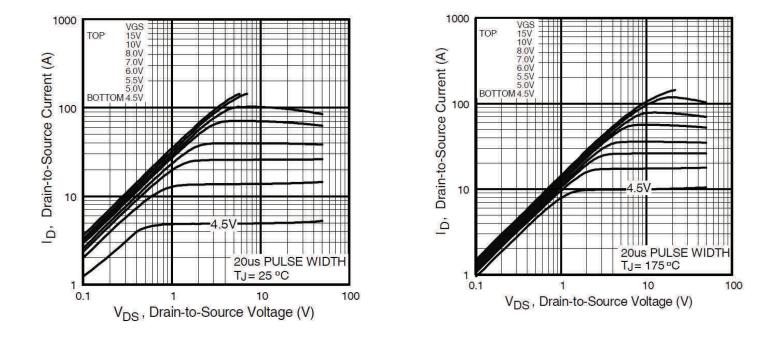


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

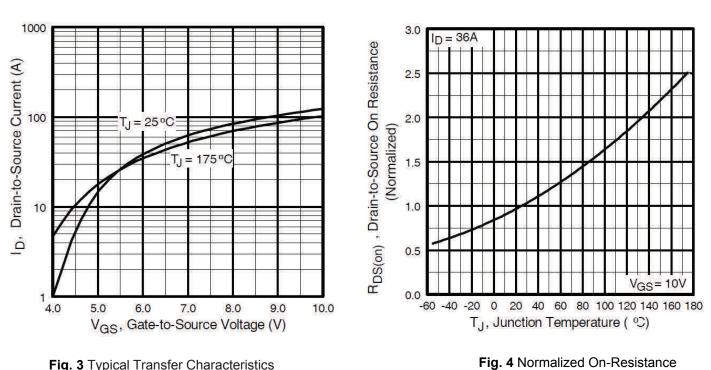
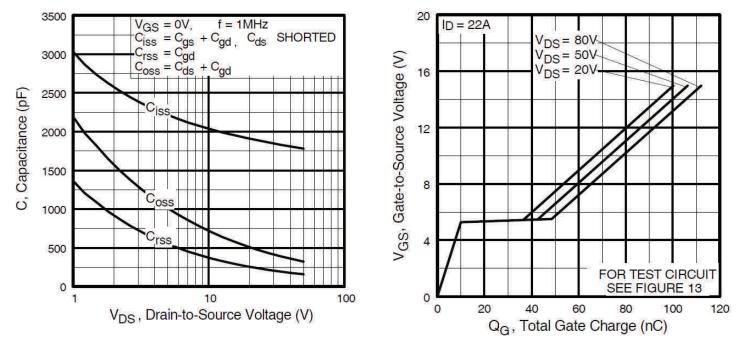
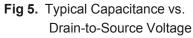


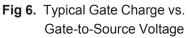
Fig. 3 Typical Transfer Characteristics

vs. Temperature









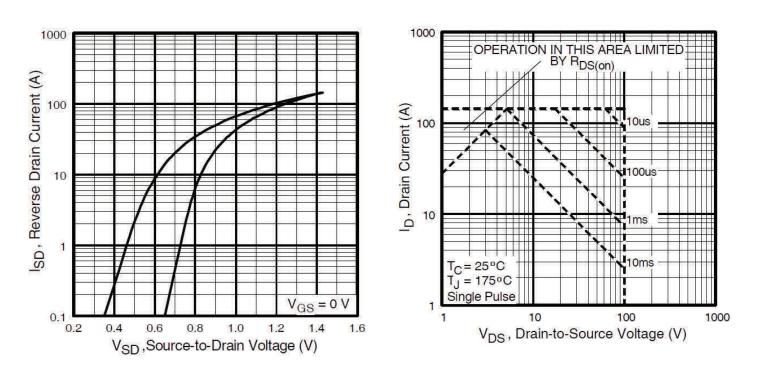


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

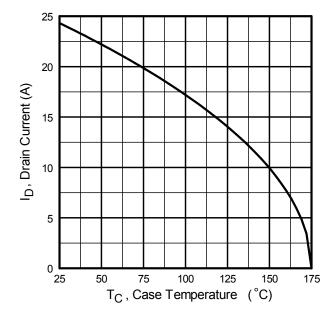


Fig 9. Maximum Drain Current vs. Case Temperature

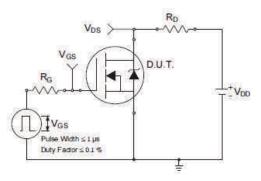


Fig 10a. Switching Time Test Circuit

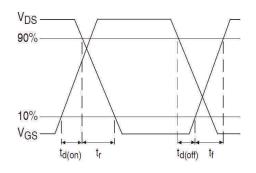


Fig 10b. Switching Time Waveforms

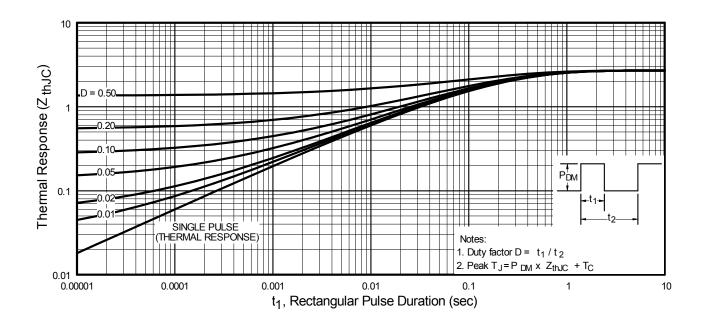


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

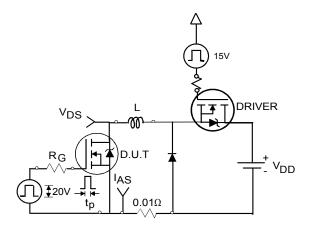


Fig 12a. Unclamped Inductive Test Circuit

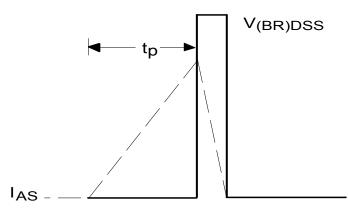


Fig 12b. Unclamped Inductive Waveforms

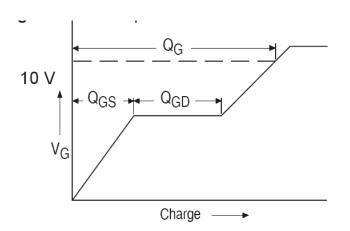


Fig 13a. Gate Charge Waveform

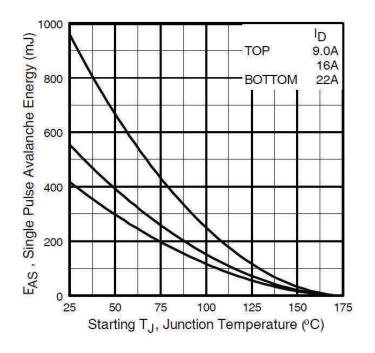


Fig 12c. Maximum Avalanche Energy vs. Drain Current

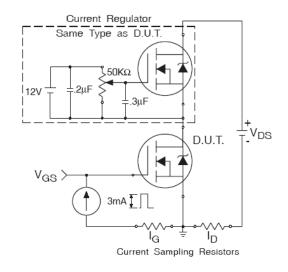
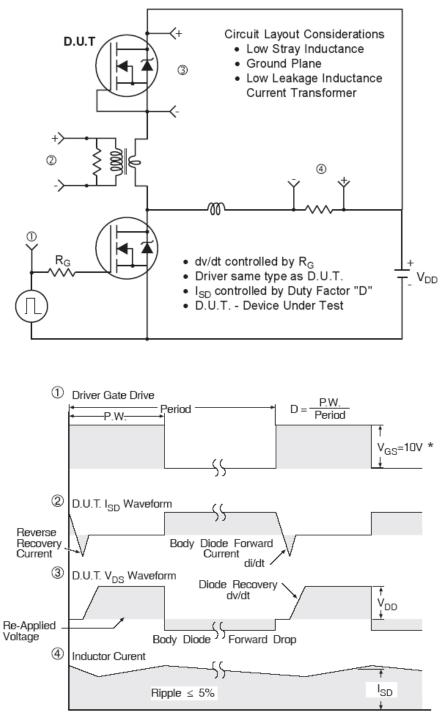
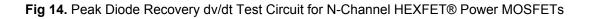


Fig 13b. Gate Charge Test Circuit

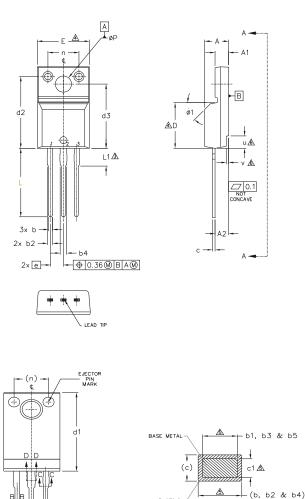


### Peak Diode Recovery dv/dt Test Circuit

\*  $V_{GS}$  = 5V for Logic Level Devices



### TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]. 2,0
- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST /4.d EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY. Ø.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

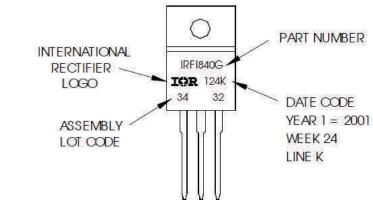
S Y M		DIMEN	ISIONS		N	
В	MILLIM	ETERS	INC	HES	O T E S	
O L	MIN.	MAX.	MIN.	MAX.	E S	
А	4.57	4.83	.180	.190		
A1	2.57	2.82	.101	.111		LEAD ASSIGNMENTS
A2	2.51	2.92	.099	.115		LEAD ASSIGNMENTS
b	0.61	0.94	.024	.037		
b1	0.61	0.89	.024	.035	5	HEXFET
b2	0.76	1.27	.030	.050		1 GATE
b3	0.76	1.22	.030	.048	5	2 DRAIN
b4	1.02	1.52	.040	.060		,
b5	1.02	1.47	.040	.058	5	3 SOURCE
С	0.33	0.63	.013	.025		
c1	0.33	0.58	.013	.023	5	
D	8.66	9.80	.341	.386	4	
d1	15.80	16.13	.622	.635		
d2	13.97	14.22	.550	.560		
d3	12.29	12.93	.484	.509		<u>IGBTs, CoPACK</u>
E	9.63	10.74	.379	.423	4	1 GATE
е	2.54 BSC		.100	BSC		2 COLLECTOR
L	13.21	13.72	.520	.540		
L1	3.10	3.68	.122	.145	3	3 EMITTER
n	6.05	6.60	.238	.260		
ØΡ	3.05	3.45	.120	.136		
u	2.39	2.49	.094	.098	6	
V	0.41	0.51	.016	.020	6	
Ø1	-	45°	-	45°		

### **TO-220 Full-Pak Part Marking Information**

EXAMPLE: THIS IS AN IRFI840G WITH ASSEMBLY LOT CODE 3432 ASSEMBLED ON WW 24, 2001 IN THE ASSEMBLY LINE "K"

SECTION B-B. C-C & D-D

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at http://www.irf.com/package/

VIEW A-A



Qualification Information						
Qualification Level		Industrial (per JEDEC JESD47F) <sup>†</sup>				
Moisture Sensitivity Level	TO-220 Full-Pak	N/A				
RoHS Compliant		Yes				

† Applicable version of JEDEC standard at the time of product release.

#### **Revision History**

Date	Comments
5/27/2016	<ul><li>Updated datasheet with corporate template.</li><li>Added disclaimer on last page.</li></ul>
04/27/2017	Corrected Package Outline on page 8.

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