Datasheet

DS000693

TMF8820/21/28

Multizone Time-of-Flight Sensor

v5-00 • 2022-Apr-14

Abstract

The TMF8820/21/28 is a dToF (direct time of flight) wide field of view optical distance sensor module achieving up to 5000 mm target detection distance and has up to 3x3, 4x4, 3x6 or 8x8 zones.

Content Guide

1 General Description

The TMF8820, TMF8821 & TMF8828 are a family of direct time-of-flight (dToF) sensors available in a small footprint modular package with integrated Vertical Cavity Surface Emitting Laser (VCSEL). The dToF device is based on SPAD, TDC and histogram technology and achieves 5000 mm detection range. Due to its lens on the SPAD, it supports 3x3, 4x4, 3x6 and 8x8 multizone output data and a very wide, dynamically adjustable, field of view. A multi-lens-array (MLA) inside the package above the VCSEL widens up the FoI (field of illumination). All processing of the raw data is performed on-chip and the TMF8820/21/28 provide distance information together with confidence values on its I^2C interface.

TMF8820	3x3 zones operation
TMF8821	3x3, 4x4 and 3x6 zones operation
TMF8828	3x3, 4x4, 3x6, and 8x8 zones operation

Information (only pertains to TMF8828)

The TMF8828 requires unique firmware (different from TMF8820/21/28) that will only operate on the TMF8828. The TMF8828 has two operating modes. It can operate as a TMF8820/21/28 (3x3, 4x4, or 3x6 zones) or in the TMF8828 mode which has 8x8 zones. In the TMF8828 mode, the device implements the 8x8 zone functionality as a sequence of four time-multiplexed measurements of 4x4 zones (like TMF8821). As such, the factory calibration sequence, loading the calibration data, reading the result measurements, and the optional histogram readouts must be performed four times in sequence by the host (please see the Host Driver Communication manual for details). The maximum measurement cycle rate in the TMF8828 mode is 15 Hz with 125 k iterations. Slower cycle rates with an increased number of iterations are possible.

1.1 Key Benefits & Features

The benefits and features of TMF8820/21/28, Multizone Time-of-Flight Sensor, are listed below:

Figure 1:
Added Value of Using TMF8820/21/28

Benefits	Features
Small footprint fits within narrow bezel applications	Modular package - 2.0 mm x 4.6 mm x 1.4 mm
Detecting objects in a very wide field of view	63º FoI/FoV

Benefits	Features
Enable new applications like click to focus, object tracking, presence detection	TMF8828: Multizone with 3x3, 4x4, 3x6 and 8x8 zones TMF8821: Multizone with 3x3, 4x4 and 3x6 zones TMF8820: Multizone with 3x3 zones
Within ±3% / ±10 mm of measurement (accuracy); no multipath and no multiple object problems as for iToF	Time-to-Digital Converter (TDC) Direct Time-of-Flight Measurement
Better accuracy detects reliably closest object Minimum distance 10 mm Maximum distance 5000 mm	Single Photon Avalanche Photodiode (SPAD) Histogram based architecture
No complex calibration	Dynamic cover glass calibration
Compensates for dirt on glass	Reliable operation under demanding use cases
Improved accuracy over temperature and life	Reference SPAD
Make better decisions	Distance and signal quality reported
Class 1 eye safe	Fast VCSEL driver with protection
Integration flexibility	I^3C tolerant - operate on a shared I^2C / I^3C bus
Longer battery life	141 mW power consumption at 30 Hz operation 8 µA power consumption standby current (keep memory) 2 µA power-down current consumption (EN=0)

1.2 Applications

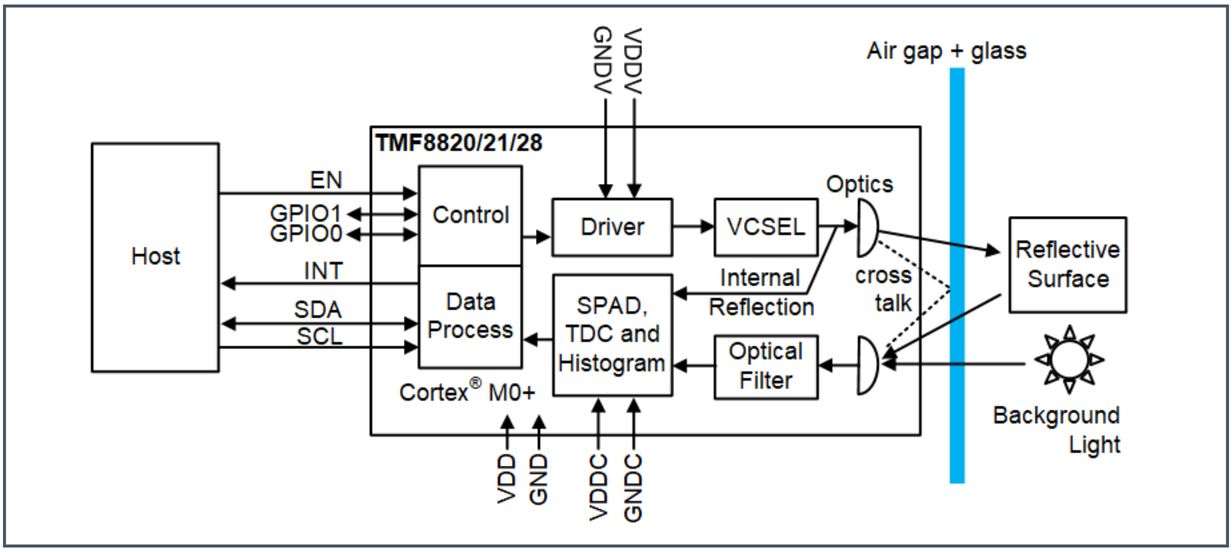
The device is ideal for use with applications including:

- Distance measurement for camera autofocus - Laser Detect Autofocus - LDAF (mobile phone)
- Presence detection (computing and communication)
- Object detection and collision avoidance (robotics)
- Light curtain (industrial)

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of TMF8820/21/28



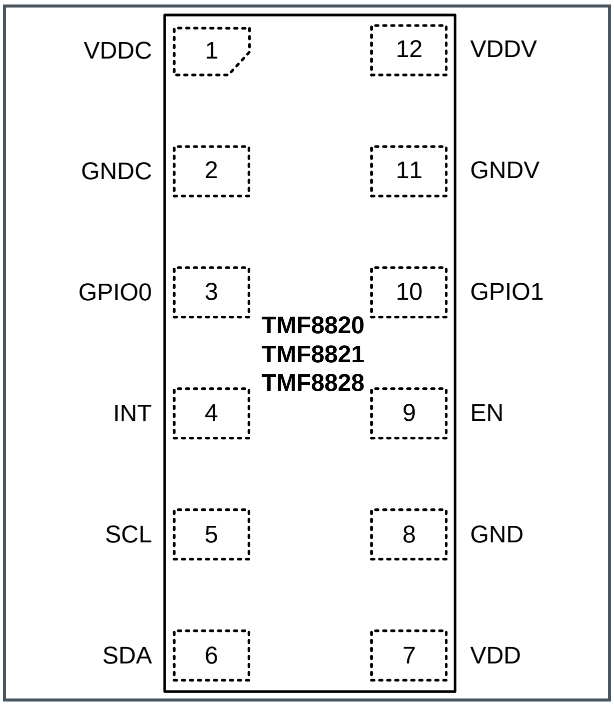
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity	Note
TMF8820-1AM	Optical Module	8-digit tracecode	Tape & Reel (7’’ reels)	500 pcs/reel	3x3 zones
TMF8820-1A			Tape & Reel (13’’ reels)	4000 pcs/reel	
TMF8821-1AM			Tape & Reel (7’’ reels)	500 pcs/reel	3x3, 4x4 and 3x6 zones
TMF8821-1A			Tape & Reel (13’’ reels)	4000 pcs/reel	
TMF8828-1AM			Tape & Reel (7’’ reels)	500 pcs/reel	3x3, 4x4, 3x6 and 8x8 zones
TMF8828-1A			Tape & Reel (13’’ reels)	4000 pcs/reel	

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Locations Top Through View (not to scale)



3.2 Pin Description

Figure 4:
Pin Description of TMF8820/21/28

Pin Number	Pin Name	Pin Type(1)	Description
1	VDDC	PWR	Charge pump supply voltage (3 V) – connect all VDD pins together; add a capacitor GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3V) to GND
2	GNDC	GND	Charge pump ground; connect all ground pins together
3	GPIO0	I/O	General purpose input/output; default tristate; connect to GND if not used
4	INT	OD	Interrupt. Open-drain output; connect to GND if not used
5	SCL	IN	I^2C serial clock
6	SDA	I/O	I^2C serial data
7	VDD	PWR	Chip supply voltage (3 V) – connect all VDD pins together; add a capacitor GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) to GND
8	GND	GND	Chip ground; connect all ground pins together
9	EN	IN	Enable input active high; setting to low forces the device into shutdown and all memory content is lost; connect to VDD if not used
10	GPIO1	I/O	General purpose input/output; default tristate; connect to GND if not used
11	GNDV	GND	VCSEL ground; connect all ground pins together
12	VDDV	PWR	VCSEL supply voltage (3 V) – connect all VDD pins together; add a capacitor GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) to GND

(1) Explanation of abbreviations:

IN	Digital input pin
I/O	Digital Input output pin
OD	Open drain output pin
GND	ground supply pin
PWR	Power Supply pin

Information

SDA, SCL, INT and EN have no diode to any VDD supply. Therefore even with VDD=0 V they do not block the interrupt line or I^2C bus.

GPIO0 and GPIO1 are push/pull output and have a diode to VDD; therefore if VDD is not powered, GPIO0 and GPIO1 shall not be driven from outside.

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of TMF8820/21/28

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DDMAX}	3 V Supply Voltage to Ground	-0.3	3.6(1)	V	Pins VDDV, VDDC, VDD
V_{GND}	Ground	0.0		V	Pins GNDV, GNDC, GND
V_{IOMAX}	Digital I/O Terminal Voltage	-0.3	3.6	V	SCL, SDA, INT and EN; has no internal diode to VDD
$V_{IO\_GPIO\_MAX}$	Interface Digital I/O terminal voltage	-0.3	VDD+0.3 max 3.6	V	GPIO0, GPIO1 has an internal diode to VDD
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JEDEC JESD78E
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	JS-001-2017
ESD_{CDM}	Electrostatic Discharge CDM	± 500		V	JEDEC JS-002-2018
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020(2)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h with T_A<30 °C and RH_{NC}<60%

(1) Limit supply rise to 1 V/µs
(2) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100 % Sn)

5 Electrical Characteristics

Device parameters are guaranteed at nominal conditions unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of TMF8820/21/28

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	3 V supply voltage	Pins VDDV, VDDC and VDD	2.7	3.0	3.3	V
VIO	I/O supply voltage	Supply voltage for external pull-up for SCL, SDA and INT.	1.62	1.8	3.3	V
T_{AMB}	Operating ambient temperature		-30	23	70	°C
Current Consumption						
I_{POWER_DOWN}	Power down current	Pin EN=0; state: power down; T_{AMB}=23°C		2	10	µA
$I_{STANDBY}$	Standby current	Current consumption for PON=0, wakeup by special I^2C command, only retention RAM keeps content; state: standby; I/O pins not toggling Only register 0xE0 (ENABLE) accessible by I^2C interface when in this mode.		8		µA
$I_{STANDBY\_TIMED}$	Standby timed current	Current consumption for waiting for measurement period to expire. goto_standby_timed = 1, low_power_osc_on = 1 Only register 0xE0 (ENABLE) accessible by I^2C interface when in this mode		34		µA
I_{WAIT}	Wait current	Wakeup by I^2C or timer, all memories keep content, CPU off, oscillator on; state: wait		216		µA
I_{ACTIVE}	Active current	Current consumption for CPU running at 80 MHz, VCSEL and TDC off state: active – histogram processing		2.8		mA
$I_{ACTIVE\_RANGING}$	Active current for ranging (VCSEL emitting light)	Current consumption for CPU running at 80 MHz, VCSEL and TDC on state: active – ranging		57		mA
Average Current Consumption for Running Application						
$P_{RANGING\_AVG}$	Average power consumption	Default settings with 550 k iterations, 3x3 mode, output data rate 30 Hz		141		mW
$P_{RANGING\_AVG\_LP}$	Average power consumption low power	Output data rate 30 Hz, 3x3 mode, 50 k iterations		19		mW

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/O Levels – Over Temperature and Supply						
I_{LEAK}	Leakage current to VDD or GND	SDA, SCL, GPIO0/1, EN, INT	-5		5	µA
V_{IH}	Input voltage high	SDA, SCL, GPIO0/1, EN	1.26		3.3	V
V_{IL}	Input voltage low	SDA, SCL, GPIO0/1, EN	0		0.54	V
V_{OL2mA}	Output voltage low	SDA, INT, 2 mA sink	0		0.36	V
V_{OL4mA}	Output voltage low	SDA. INT, 4 mA sink	0		0.6	V
I_{DRIVE_H}	Output current high	1 V applied on GPIO0/1	3.6			mA
I_{DRIVE_L}	Output current low	1 V applied on GPIO0/1	3.6			mA
Timings – over Temperature and Supply						
f_{clk}	RC oscillator	All internal timings are derived from this clock	4.85	5	5.15	MHz
f_{CPUclk}	Maximum operating frequency of CPU	The CPU can be switched between fclk and fclk*16		fclk * 16 (80 MHz)		MHz
$VCSEL_{CLK}$	Clock frequency of VCSEL clock			17.77		MHz
t_{POR}	Power on time	EN=1 to ready for I²C command			2	ms
$t_{FW\_DOWNLOAD}$	Time to download firmware	For 1 MHz I²C speed [TMF8820/21]		50		ms
		For 1 MHz I²C speed [TMF8828]		100		ms
$t_{FIRST\_MEAS\_COLD}$	Time from cold start to first measurement	From EN=0->1 (power down) to first measurement result; default settings (33 ms)		190		ms
$t_{FIRST\_MEAS\_WARM}$	Time from warm start to first measurement	From standby to first measurement result; default settings (33 ms)		60		ms
$t_{SWITCH\_to\_8820/8821}$	Time to switch to TMF8820/21 mode	From command 0x65 to CMD_STAT to first measurement result [TMF8828]		65		ms
$t_{SWITCH\_to\_8828}$	Time to switch to TMF8828 mode	From command 0x6C to CMD_STAT to first measurement result [TMF8828]		115		ms
I²C Interface – over Temperature and Supply						
f_{SCLK}	SCL clock frequency		0	400	1000	kHz
t_{BUF}	Bus free time between a STOP and START		0.5			µs
$t_{HD:STA}$	Hold time (Repeated) Start		0.26			µs
t_{LOW}	LOW period of SCL Clock		0.5			µs
t_{HIGH}	HIGH period of SCL clock		0.26			µs
$t_{SU:STA}$	Setup time for a Repeated START		0.26			µs
$t_{HD:DAT}$	Data hold time		0			µs
$t_{SU:DAT}$	Data setup time		50			ns
t_R	Rise time of both SDA and SCL		20		120	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_F	Fall time of both SDA and SCL		20		120	ns
Optical Parameters						
FoI	Field of view of the illuminator main area	Diagonal, FWHM(3) of radiant intensity	See section 7.5.2			
Optical Multizone Parameters						
$SPAD_X$	Delta in angle of single SPAD in x	In optical center		2.4		degrees
$SPAD_Y$	Delta in angle of single SPAD in y(1)	In optical center		5.6		degrees
Optical Stack Requirements						
$GLASS_{TRANSPARENCY}$	Glass transparency @ 940 nm	The device can work with IR inked or clear glass	85	90		%
$XTALK_{SYSTEM}$	System Crosstalk	Measured in final application	See ams OSRAM optical design guide			

(1) Due to SPADs with too high dark count, which are disabled by production test (screamer detection), need to use always at least two SPADs next to each other.

(2) FWHM – full width half maximum.

6 Typical Operating Characteristics

Following operating characteristics are measured with calibrated devices with full optical stack. The ambient light is measured on the target. The data is perpendicular scaled for the non-center zones.

Figure 7:
350 Lux Fluorescent Light 18% Grey Card 3x3, 33°x32° FoV Center Zone, 30 Hz

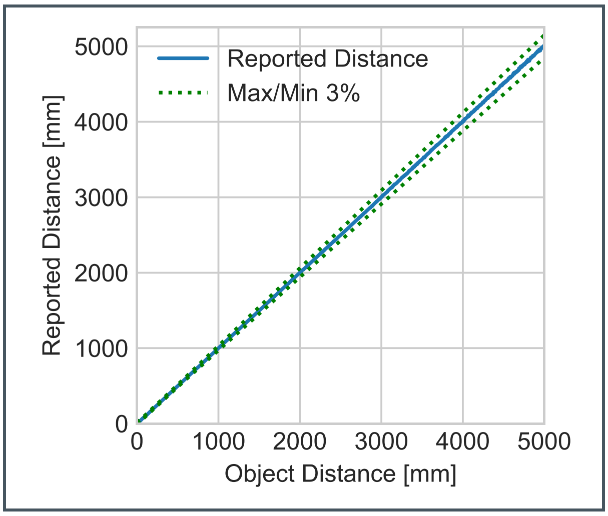


Figure 8:
Figure 7 Zoomed to 0 mm – 1000 mm

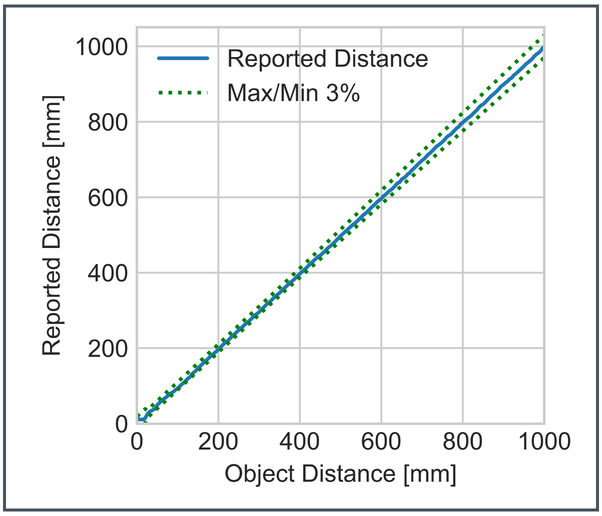


Figure 9:
350 Lux Fluorescent Light 18% Grey Card 3x3, 33°x32° FoV, Edge Zone, 30 Hz

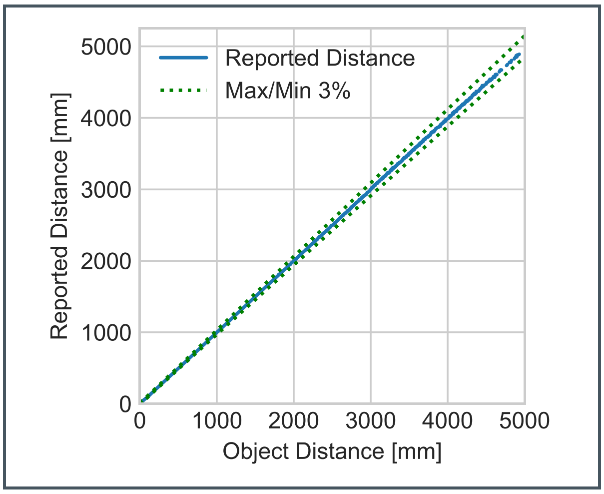


Figure 10:
350 Lux Fluorescent Light 18% Grey Card 3x3, 33°x32° FoV, Corner Zone, 30 Hz

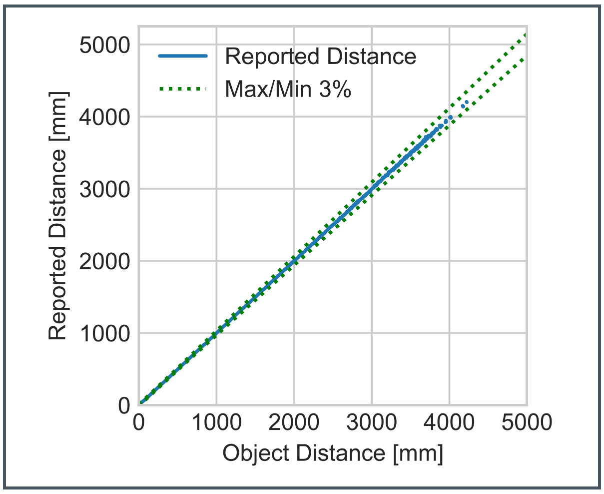


Figure 11:
140 Lux HAL (1 Lux sunlight) 18% Grey Card 3x3, 33°x32° FoV Center Zone, 30 Hz

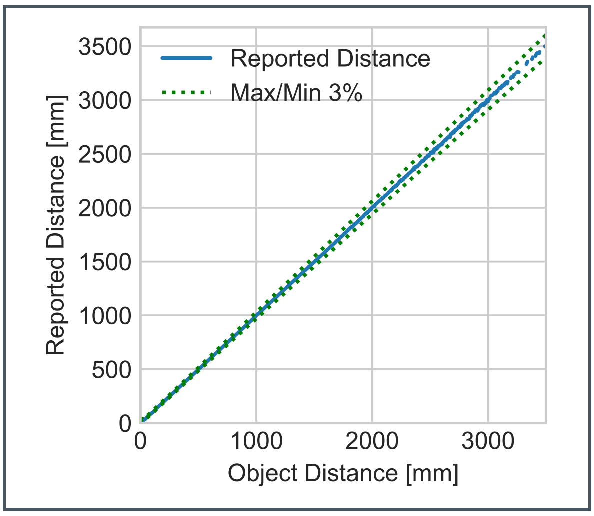


Figure 12:
700 Lux HAL (5 k Lux sunlight) 18% Grey Card 3x3, 33°x32° FoV Center Zone, 30 Hz

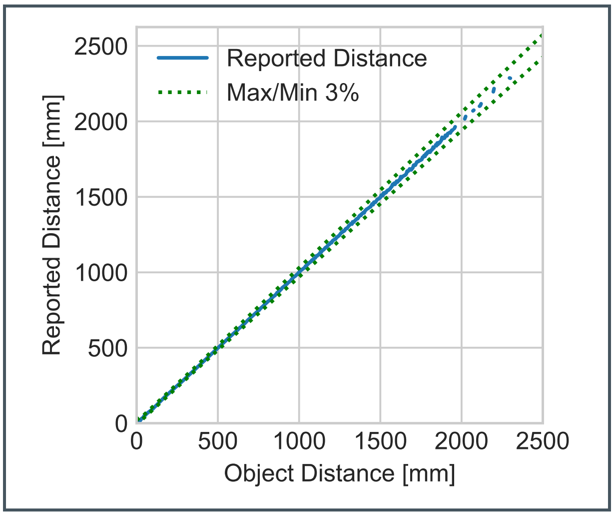


Figure 13:
1400 Lux HAL (10 k Lux sunlight) 18% Grey Card 3x3, 33°x32° FoV Center Zone, 30 Hz

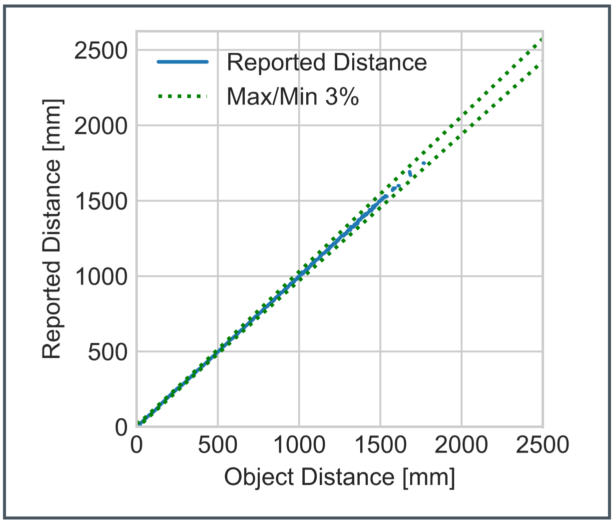
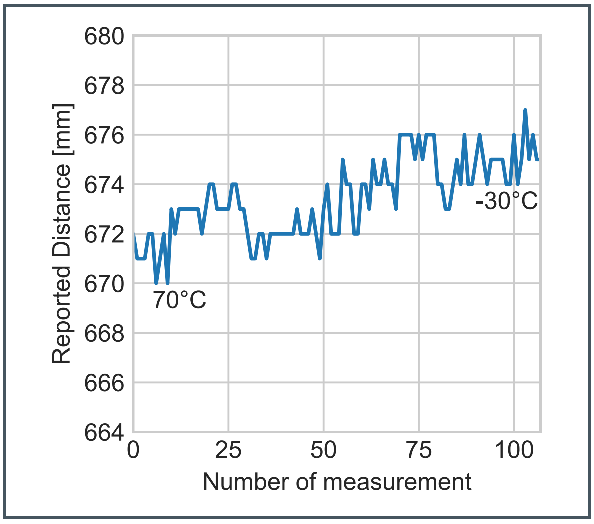


Figure 14:
Reported Distance During a Temperature Sweep from 70 °C to -30 °C with a Fixed Target in the Oven



6.1 4x4 Zones Operating Mode (only TMF8821 and TMF8828)

Figure 15:
350 Lux Fluorescent Light 18% Grey Card 4x4, 41°x52° FoV Center Zone, 15 Hz

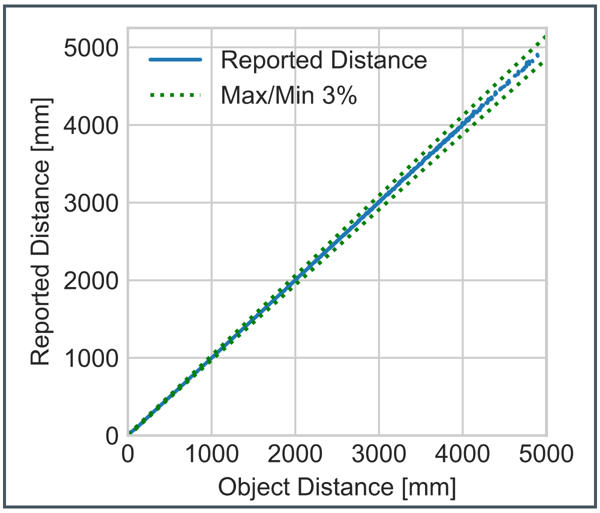


Figure 16:
Figure 15 Zoomed to 0 mm - 1000 mm

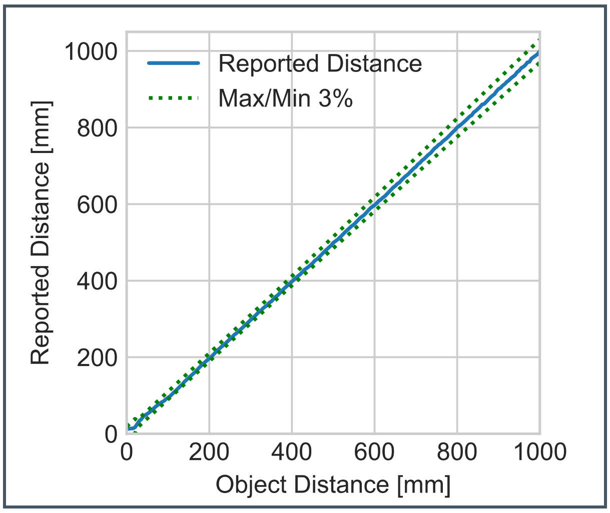


Figure 17:
350 Lux Fluorescent Light 18% Grey Card 4x4, 41°x52° FoV, Edge Zone, 15 Hz

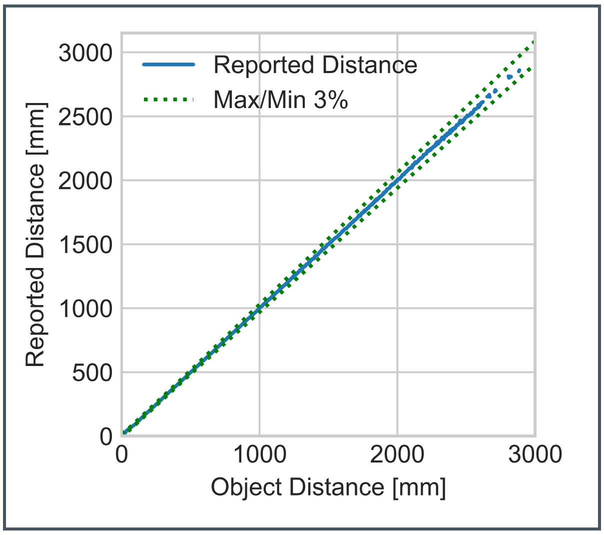
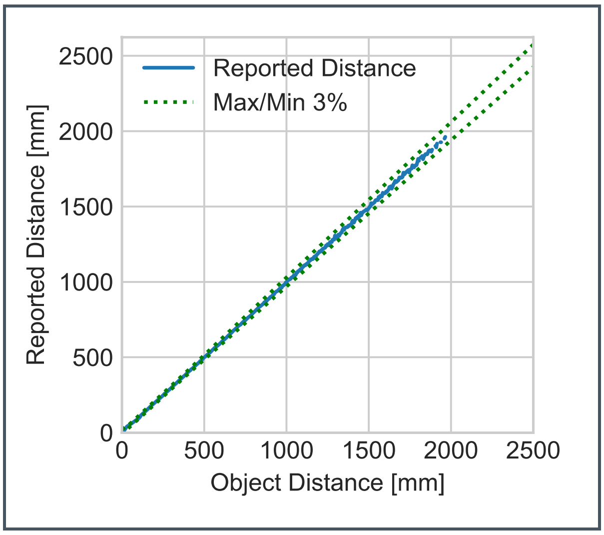


Figure 18:
350 Lux Fluorescent Light 18% Grey Card 4x4, 41°x52° FoV, Corner Zone, 15 Hz



6.2 8x8 Zones Operating Mode (only TMF8828)

Figure 19:
350 Lux Fluorescent Light 18% Grey Card 8x8, 41°x52° FoV Center Zone, 15 Hz

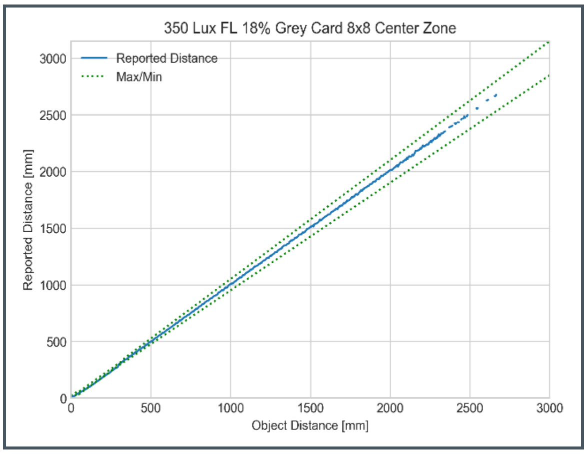


Figure 20:
Figure 19 Zoomed to 0 mm - 1000 mm

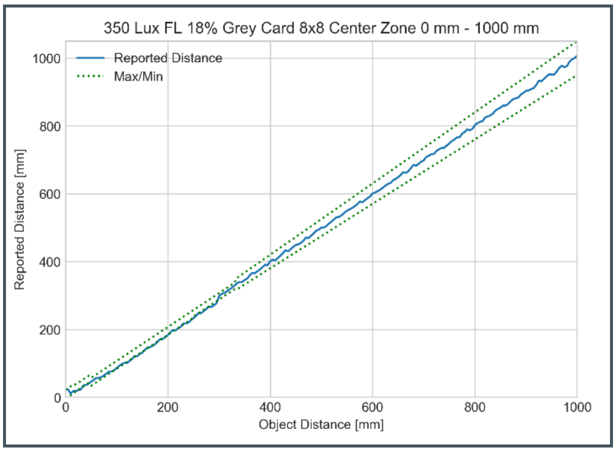


Figure 21:
350 Lux Fluorescent Light 18% Grey Card 8x8, 41°x52° FoV, Edge Zone, 15 Hz

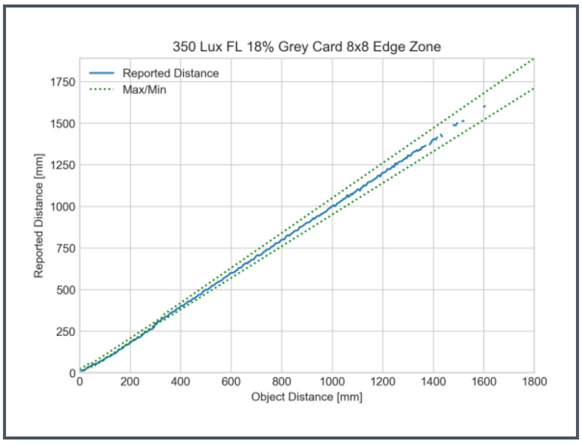
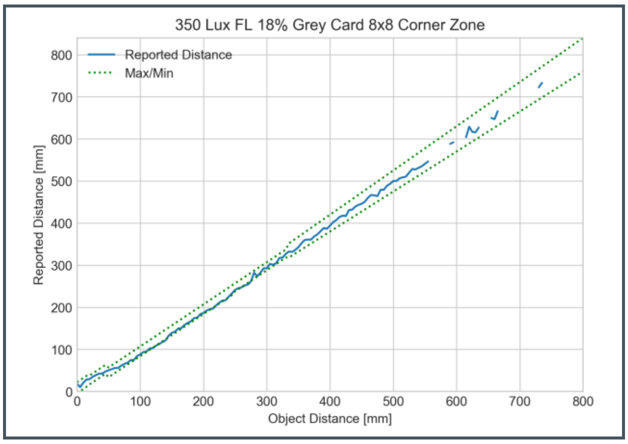


Figure 22:
350 Lux Fluorescent Light 18% Grey Card 8x8, 41°x52° FoV, Corner Zone, 15 Hz

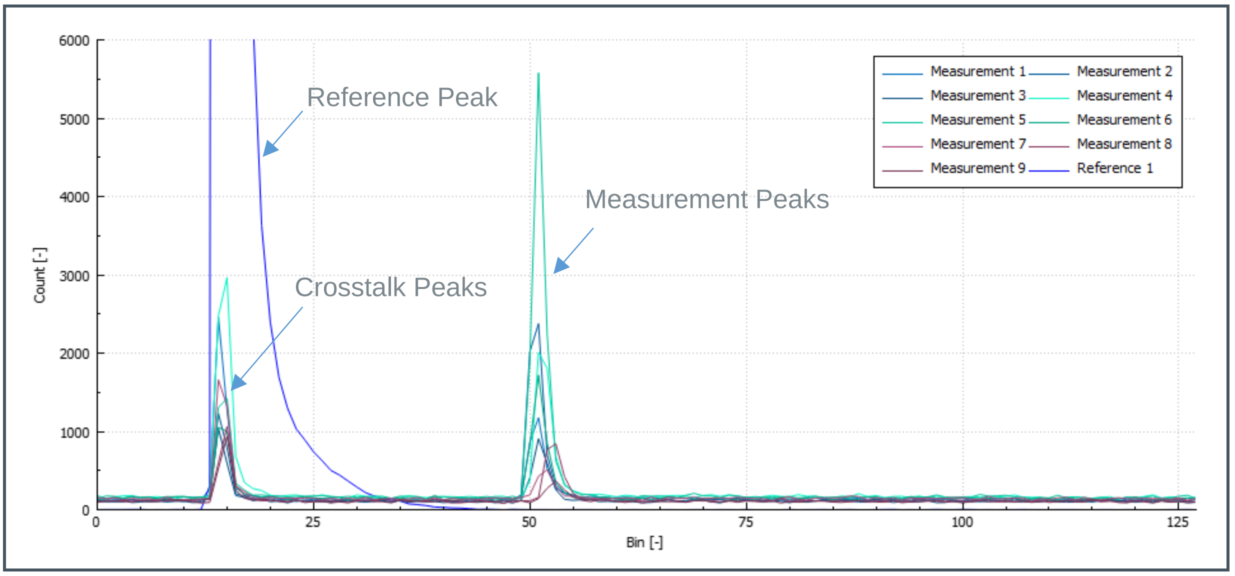


7 Functional Description

7.1 General Operating Description

The TMF8820/21/28 operating principle uses a pulse train of VCSEL pulses defined by the iteration setting. These pulses are spread using a MLA (micro lens array) to illuminate the FoI (field of illumination). An object reflects these rays back to the TMF8820/21/28 receiver optics lens and onto a SPAD (single photon avalanche detector) array. A TDC (time to digital converter) measures now the time from emission of these pulses to their arrival and accumulates the hits into bins inside a histogram. As TMF8820/21 sends 550 k pulses (default settings), the output of the TDC is a full histogram as shown in Figure 23:

Figure 23:
Example Target Histogram and Reference Histogram (Blue)



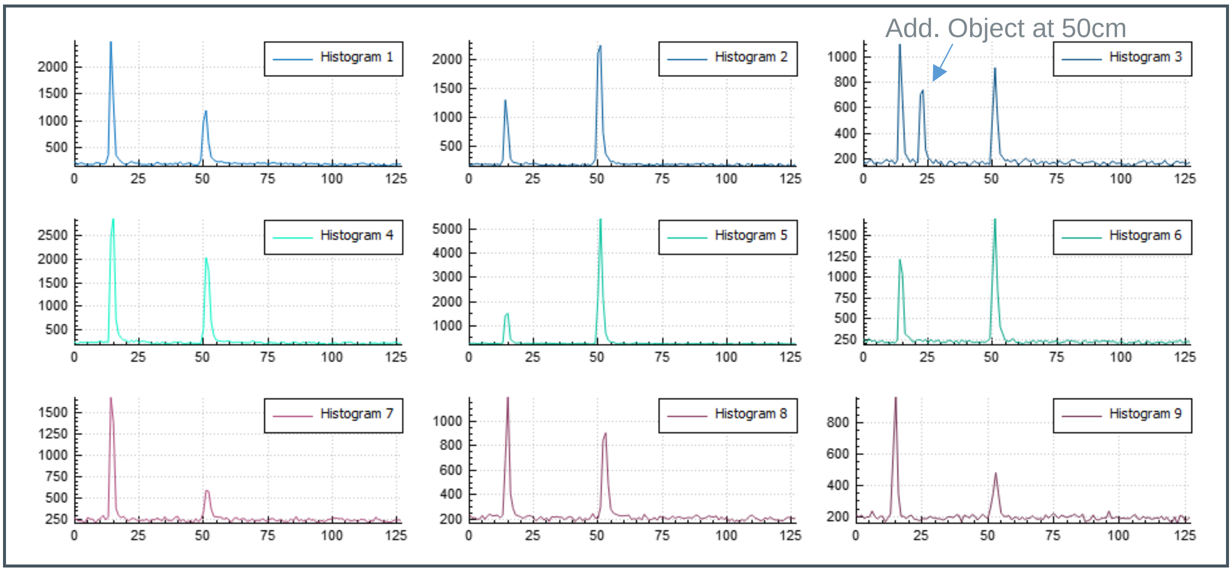
The large blue peak (clipped due to scaling for measurement peaks) in the histogram shows the reference peak histogram. A SPAD, which is located in the cavity of the VCSEL, generates this target peak. The target detection algorithm uses this peak together with the crosstalk peaks at bin 15 in the measurements channels to calculate zero distance. All measurement histograms show a crosstalk peak around bin 15 and the actual target peak at bin 50 – the algorithm has an internal calibration to calculate from bins to time, which the algorithm converts to distance using speed of light. In above example, the time from bin 15 to bin 50 represents a target distance of 2 m.

The internal processor (ARM M0+ ®) executes the ams OSRAM algorithm on these histograms to calculate the target distance of the object. The output of this calculation is the distance in [mm] presented on the I^2C interface for each of the zones.

7.1.1 Multizone / Multi-Object Functionality

The SPADs below the receiver lens are in focus of this lens. Therefore, depending on the location of the object, the different zones see different areas of the scene as shown in the raw histogram graph in Figure 24:

Figure 24:
Multizone Histograms Example

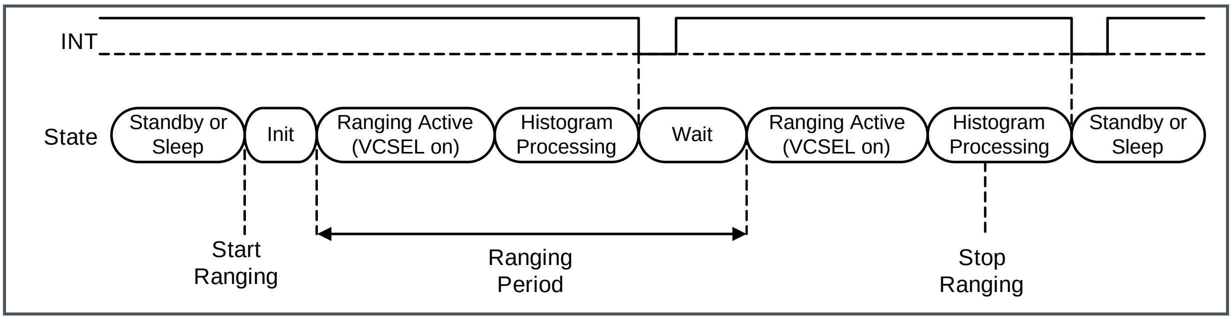


In zone3 (histogram 3) there is an additional object at 50 cm which is shown by a third peak in the histogram around bin 25. Zone3 outputs a first object at 50 cm and a second object at 2 m distance.

7.2 Timing Diagrams

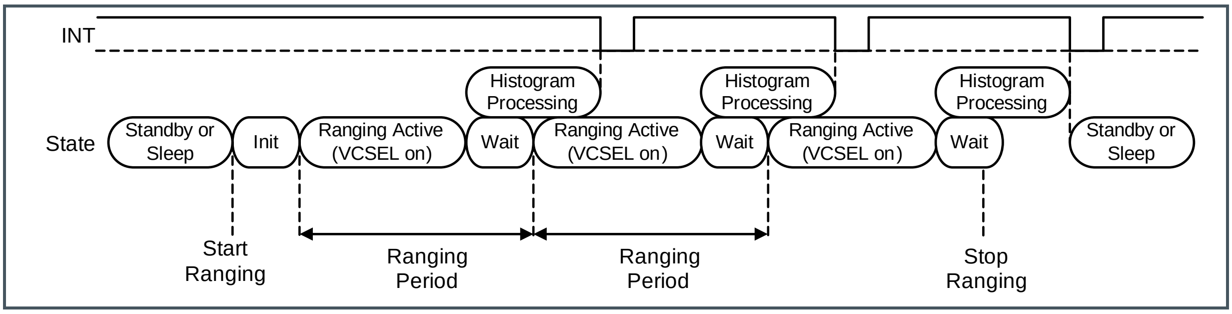
Following figure shows a typical target measurement timing diagram of TMF8820/21/28:

Figure 25:
Timing Diagram for Ranging Period > Ranging Active + Histogram Processing



If the ranging period is chosen shorter than the combined time of ranging active and histogram processing, the TMF8820/21/28 automatically runs histogram processing in parallel to ranging active:

Figure 26:
Timing Diagram for Ranging Period < Ranging Active + Histogram Processing



Note:
In time multiplex mode for TMF8821 (4x4 and 3x6) and TMF8828 (8x8), ranging active is executed 2 times for 3x6 and 4x4 respectively 4 times for 8x8 mode before an interrupt is sent after histogram processing. Each VCSEL burst uses the programmed number of iterations defined by register iterations[15:8] and iterations[7:0].

7.3 Calibration

To achieve the performance described in the next sections, the correct SPAD mask shall be set, iterations set to 4 M and calibration of the algorithm needs to be performed (cmd_stat = 0x20). The TMF8820/21/28 shall be embedded in the final application and the cover glass including the IR ink needs to be assembled. The calibration test shall be done in a housing with minimal ambient light and no target within 40 cm in field of view of the TMF8820/21/28.

Attention

Set number of iterations during calibration to 4 M to ensure accuracy. Read also the optical design guide (ODG) to have the system crosstalk level in the range defined by this document.

The TMF8820/21/28 generates a calibration data set, which needs to be stored on the host processor and reloaded after each power down or reset event.

It shall be ensured by the optical design that the optical crosstalk values are meeting the limits defined in the TMF8820/21/28 optical design guide (ODG).

Figure 27:
Calibration Data Measured Crosstalk Values (Little endian format = LSB first)

I²C Address (if appid=0x03, cid_rid=0x19 – Factory Calibration)	Offset in Calibration Data File	Meaning
0x2A-0x2B	0x06-0x07	Iterations used for calibration divided by 1024
Crosstalk values for zones 1-9; apply for non time multiplexed mode (3x3); also for the first measurement in time multiplexed mode (4x4 and 3x6); TMF8828 repeats 4x4 calibration 4 times		
0x5C-0x5F	0x38-0x3B	Crosstalk for reference channel – shall be ignored
0x60-0x63	0x3C-0x3F	Crosstalk for channel 1
0x64-0x67	0x40-0x43	Crosstalk for channel 2
0x68-0x6B	0x44-0x47	Crosstalk for channel 3
0x6C-0x6F	0x48-0x4B	Crosstalk for channel 4
0x70-0x73	0x4C-0x4F	Crosstalk for channel 5
0x74-0x77	0x50-0x53	Crosstalk for channel 6
0x78-0x7B	0x54-0x57	Crosstalk for channel 7
0x7C-0x7F	0x58-0x5B	Crosstalk for channel 8
0x80-0x83	0x5C-0x5F	Crosstalk for channel 9
Crosstalk values for zones 10-18 using channels 1-9 only for the second measurement in time multiplexed mode (4x4 and 3x6); TMF8828 repeats 4x4 calibration 4 times		
0xB4-0xB7	0x90-0x93	Crosstalk for reference channel; time multiplex – shall be ignored
0xB8-0xBB	0x94-0x97	Crosstalk for channel 1; time multiplex
0xBC-0xBF	0x98-0x9B	Crosstalk for channel 2; time multiplex
0xC0-0xC3	0x9C-0x9F	Crosstalk for channel 3; time multiplex
0xC4-0xC7	0xA0-0xA3	Crosstalk for channel 4; time multiplex
0xC8-0xCB	0xA4-0xA7	Crosstalk for channel 5; time multiplex
0xCC-0xCF	0xA8-0xAB	Crosstalk for channel 6; time multiplex
0xD0-0xD3	0xAC-0xAF	Crosstalk for channel 7; time multiplex
0xD4-0xD7	0xB0-0xB3	Crosstalk for channel 8; time multiplex
0xD8-0xDB	0xB4-0xB7	Crosstalk for channel 9; time multiplex
0xDC	0xB8	fc_status_during_cal - calibration status during factory calibration – copy of register 0x07 – 0x00 success, all other values are reporting an error during calibration

The host shall send the calibration data for the selected SPAD mask on each power-up of the TMF8820/21/28 and after each change of the SPAD mask using cmd_stat = 0x19, prior to execution of the ams OSRAM algorithm.

Attention

Calibration shall be done individually for all different SPAD masks used in operation of the device.

7.4 Algorithm Performance

The algorithm performance is measured using the driver supplied by ams OSRAM and using the latest firmware included in TMF882x_Driver_Linux_v*.zip. Download the latest firmware from **ams** website:

- For TMF8820 see https://ams.com/tmf8820
- For TMF8821 see https://ams.com/tmf8821
- For TMF8828 see https://ams.com/tmf8828

The driver automatically performs clock skew correction (use host clock to compensate for the TMF8820/21/28 internal clock drift) to achieve the accuracy.

See also section 9.5 for available drivers.

Performance parameters apply at nominal supply and temperature.

7.4.1 SPAD Mask and Mode Selection

The SPAD mask selection (register spad_map_id see Figure 113) defines the assignment of the SPADs to the individual zones – due to the lens above the SPADs, the FoV (field of view) of the sensor is also defined by the SPAD mask as shown in Figure 29.

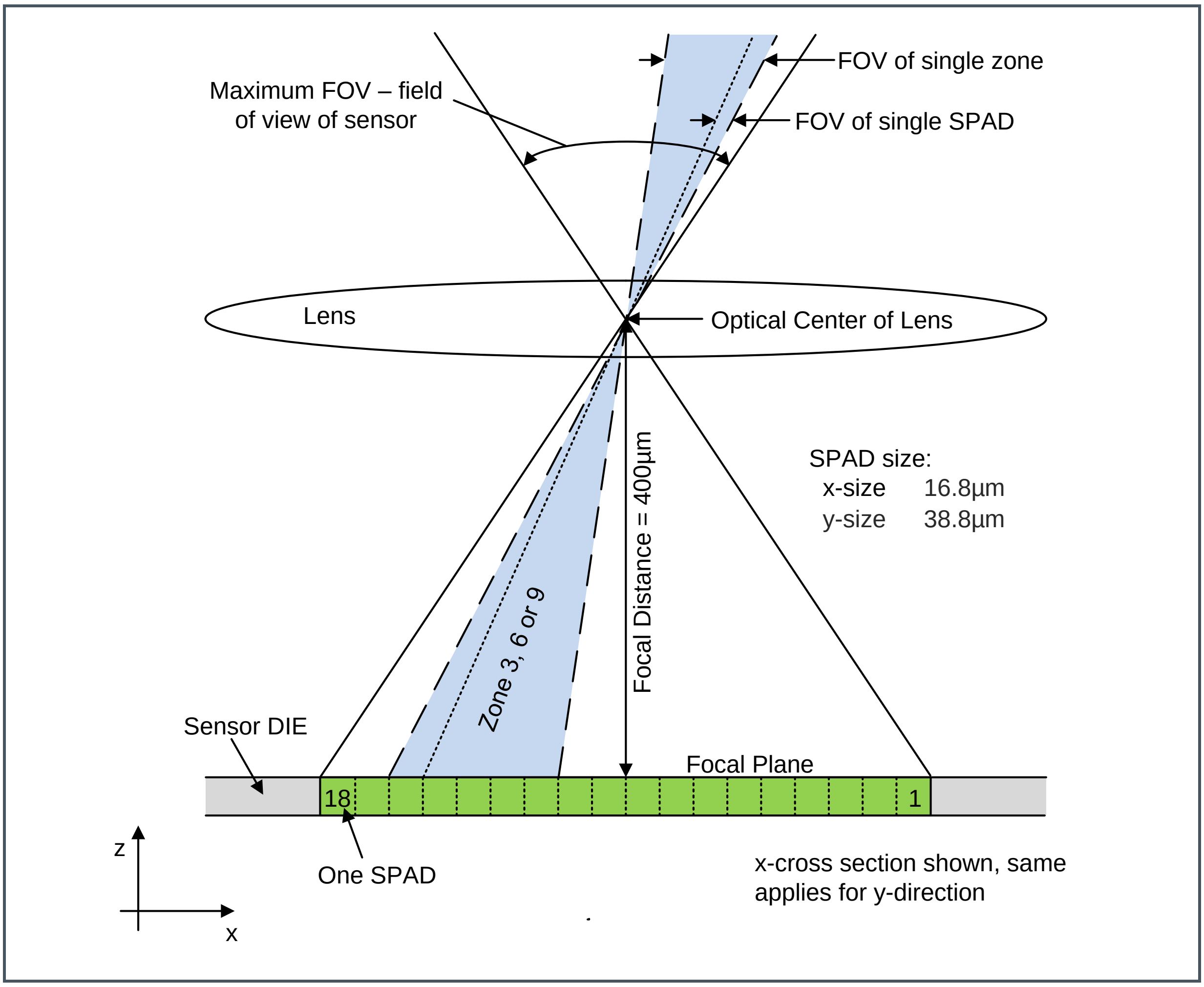
The ranging period shown in Figure 28 is depending on the operating mode, which is selected by spad_map_id and the iterations setting, set by register iterations. To achieve fastest ranging period set the report period in ms (register period) below ranging period to ensure that there will be no wait time.

Figure 28:
Ranging Period vs. Iterations and Operating Mode

Operating Mode	Iterations	Ranging Period With No Wait Time Programmed
3x3	50 k	6.1 ms
	550 k	32.2 ms
	4000 k	230 ms

Operating Mode	Iterations	Ranging Period With No Wait Time Programmed
3x6 or 4x4	50 k	13 ms
	550 k	65 ms
	4000 k	460 ms
8x8	50 k	26 ms
	550 k	129 ms
	4000 M	920 ms

Figure 29:
Relation of SPADs to FoV – Zone 3,6,9 from spad_map_id=1 (3x3 mode, 33°x32° FoV)



FoV of a SPAD or a zone can be calculated with, assuming center of zone is in optical center:

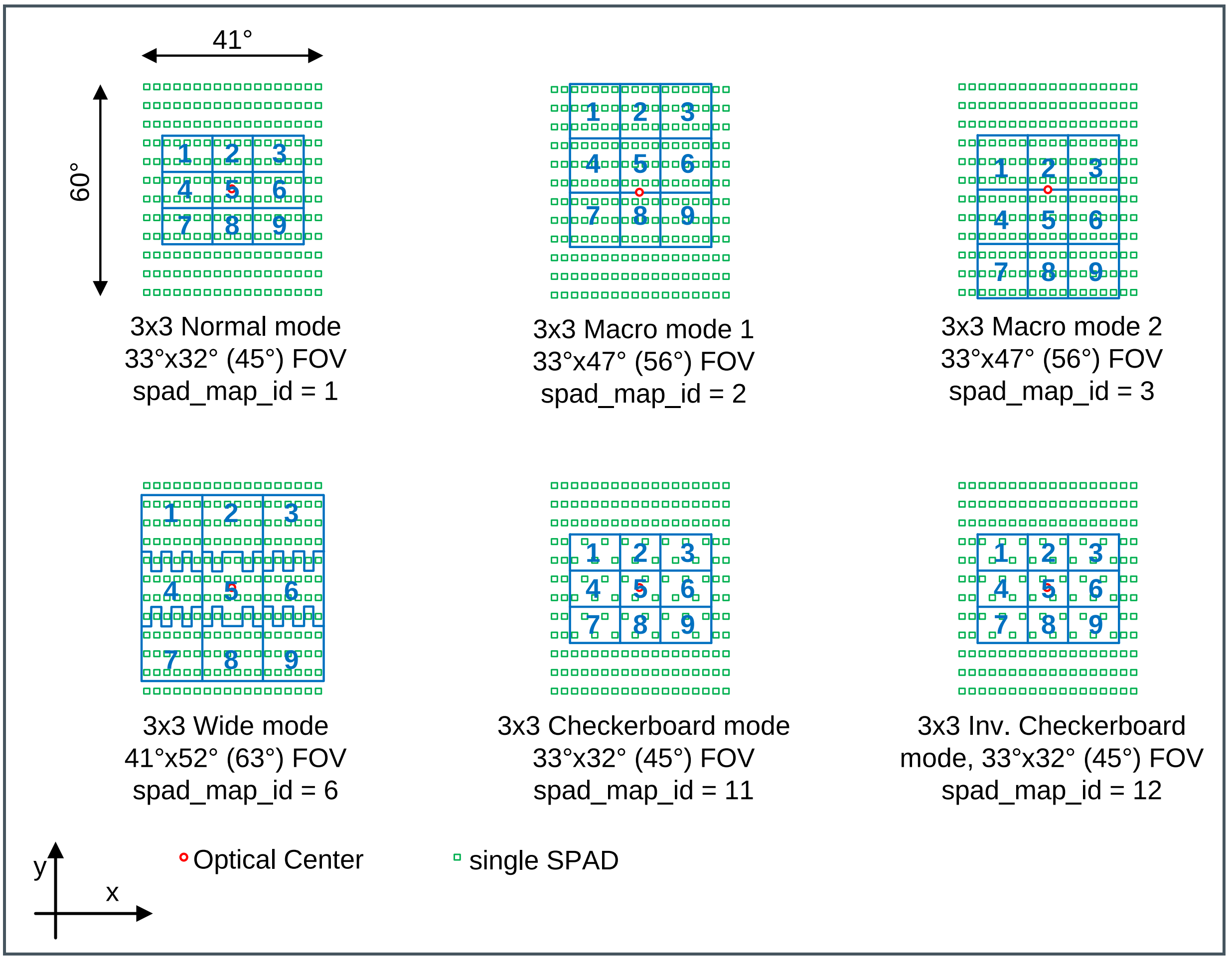
Equation 1:

$$FoV\ [°] = 2 * \text{atan} \frac{size\ of\ zone\ or\ SPAD}{2 * \ focal\ distance}$$

Where focal distance = 400 µm
Size of a single SPAD is 16.8 µm in x-direction and 38.8 µm in y-direction.

There are several pre-defined SPAD masks available as shown in Figure 113 and drawn in Figure 30 for 3x3 mode and Figure 31 for 4x4 and 3x6 mode and Figure 32 for 8x8 mode:

Figure 30:
Zones Configuration of Pre-Programmed SPAD Maps for 3x3 Mode Operation



Note: Use the checkerboard SPAD masks especially for high ambient light conditions.

Figure 31:
Zones Configuration of Pre-Programmed SPAD Maps for 4x4 and 3x6 Mode Operation

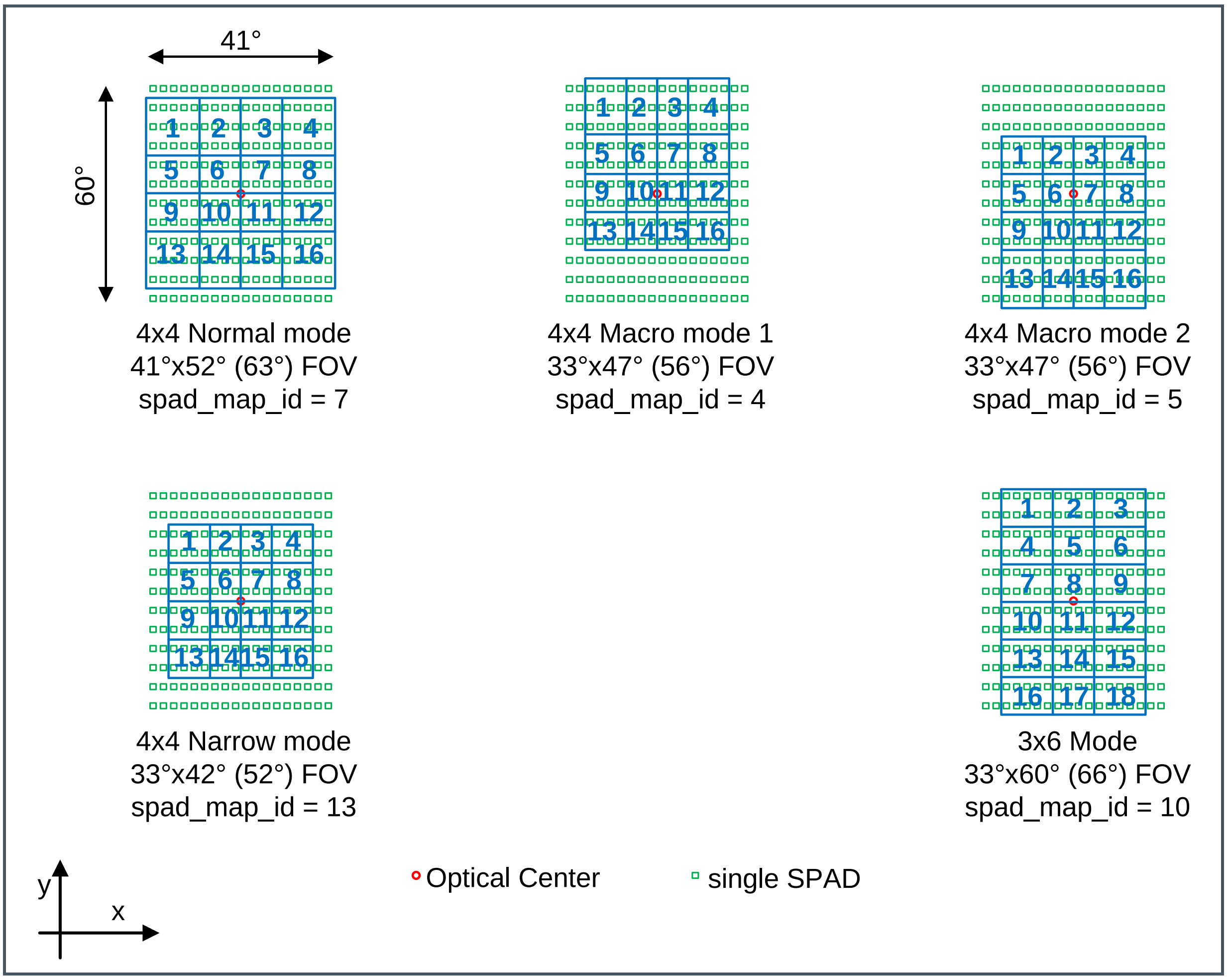
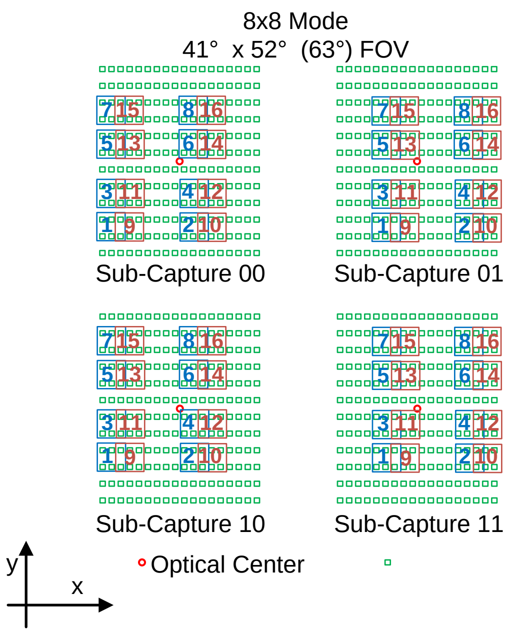


Figure 32:
Zones Configuration of Pre-Programmed SPAD Maps for 8x8 Mode Operation



Except in TMF8828 mode, the customer can design an own SPAD mask and assign SPADs to channels individually. In TMF8828 mode, the SPAD mask is fixed and cannot be changed. There are following constrains for these SPAD masks:

- Use spad_map_id=14 for single measurement up to 9 zones and spad_map_id=15 for time multiplexed measurement up to 18 zones
- The SPAD mask has a maximum size of 18x10.
- SPAD mapping and SPAD enable mask shall have the exact same size.
- Channel 0 is reserved for the reference channel and shall not be used in a SPAD mask.
- The resulting SPAD mask plus offset shall not exceed 18x12 – example: An 18x10 size SPAD mask has to have x_offset_2=0 (18 is already the limit) but can have a y-offset of +/-1 SPAD. Please note that the actual register value y_offset_2 is multiplied by 2 so, +2 or -2 is the actual value stored to y_offset_2 to obtain an offset of +1 respectively -1.
- In each used channel, there shall be at least two adjacent SPADs (can be in any direction).
- A single row shall not use channel 1 and channel 8 or 9 at the same time.
- There needs to be at least one channel per TDC enabled otherwise electrical calibration will fail - use at minimum channel (2 or 3) and (4 or 5) and (6 or 7) and (8 or 9)

A complete SPAD mask consists of an enable mask, where a '1' is an enabled SPAD and a '0' is used for a disabled SPAD, and a TDC channel selection mask where the number '1'…'9' assigns this SPAD to a TDC channel. See document TMF882X_Host_Driver_Communication*.pdf for detailed explanation how to download customized SPAD maps.

ams OSRAM recommends to program the SPAD mask through the device driver and read back the masks for verification.

Whenever the SPAD mask selection is changed, the current calibration is no longer valid – see section 7.3.

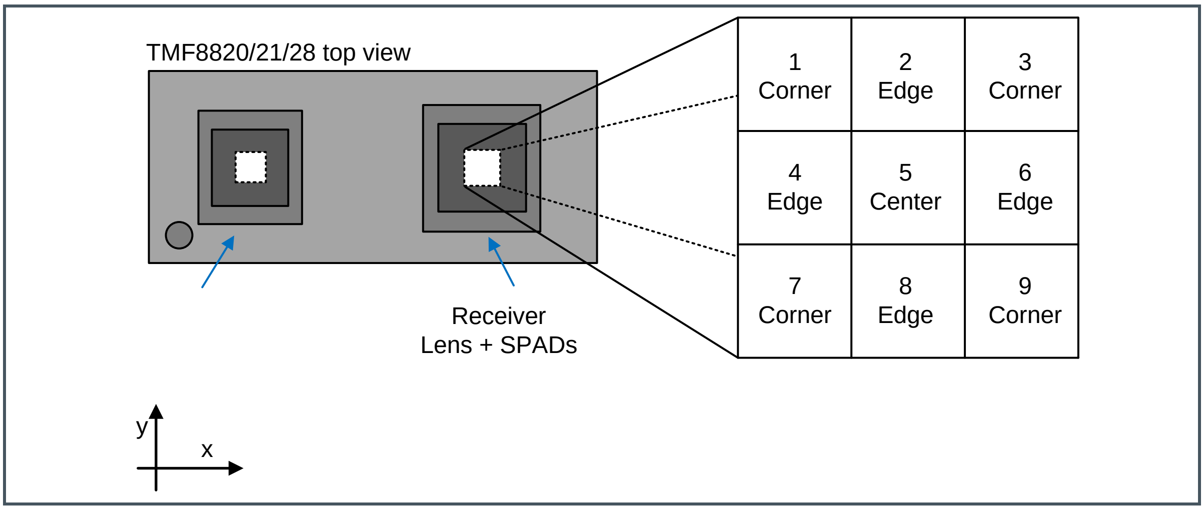
CAUTION

For a user defined SPAD mask ensure that each zone has at least two adjacent SPADs enabled. Otherwise, on some devices this zone might not see any target counts at all.

7.4.2 Performance in 3x3 Operating Mode

The algorithm reports distance information for each of the zone individually for the closest and the 2nd closest object in 1 mm steps. The algorithm performance is depending on the chosen zone:

Figure 33:
Zones Definition



For spad_map_id=1 (3x3 mode, 33°x32° FoV), calibration according to section 7.3, following performance parameters apply. The reported distance is the actual distance between the device and the actual measured zone – there is no perpendicular flat target correction applied. The target covers the full FoV of the device.

Figure 34:
Typical Maximum Distance in 3x3 Mode, 33°x32° FoV, 550 k Iterations (30 Hz output data rate), Light on the Target Only

Target Reflectivity %T at 940 nm	Zone	350 Lux LED Lighting	140 Lux Halogen(1)	700 Lux Halogen(2)	1400 Lux Halogen(3)
White target 90%	Center	5000 mm	4500 mm	2000 mm	1000 mm
	Edge	5000 mm	4000 mm	1800 mm	950 mm
	Corner	5000 mm	3000 mm	1500 mm	750 mm
Grey target 18%	Center	5000 mm	3000 mm	2000 mm	1500 mm
	Edge	4500 mm	2800 mm	1500 mm	1400 mm
	Corner	4000 mm	2000 mm	1400 mm	1200 mm

(1) 140 lux halogen light represents 1 k lux sunlight
(2) 700 lux halogen light represents 5 k lux sunlight
(3) 1400 lux halogen light represents 10 k lux sunlight

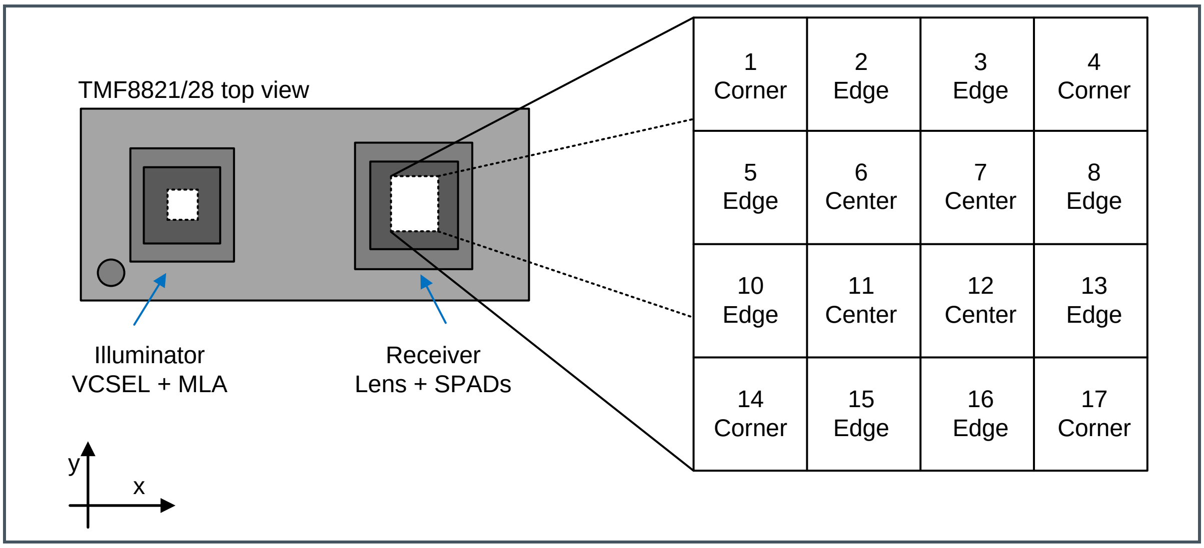
7.4.3 Performance in 4x4 Operating Mode – Only TMF8821 and TMF8828

Information

Please note that the zones for 4x4 operating mode are presented in zones 1-8 and 10-17; the result for zone 9 and 18 is not used.

The algorithm reports distance information for each of the zone individually for the closest and the 2nd closest object in 1 mm steps. The algorithm performance is depending on the chosen zone:

Figure 35:
Zones Definition (TMF8821 and TMF8828)



For spad_map_id=7 (4x4 mode, 41°x52° FoV), calibration according to section 7.3, following performance parameters apply. The reported distance is the actual distance between the device and the actual measured zone – there is no perpendicular flat target correction applied. The target covers the full FoV of the device.

Figure 36:
Typical Maximum Distance in 4x4 Mode, 41°x52° FoV, 550 k Iterations (15 Hz output data rate), Light on the Target Only

Target Reflectivity %T at 940 nm	Zone	350 Lux LED Lighting	140 Lux Halogen(1)	700 Lux Halogen(2)	1400 Lux Halogen(3)
White target 90%	Center	5000 mm	3500 mm	2000 mm	1000 mm
	Edge	3000 mm	1400 mm	900 mm	500 mm
	Corner	2900 mm	1300 mm	800 mm	400 mm
Grey target 18%	Center	4000 mm	2500 mm	1500 mm	1400 mm
	Edge	1500 mm	1200 mm	800 mm	700 mm
	Corner	1400 mm	1100 mm	700 mm	600 mm

(1) 140 lux HAL represents 1k lux sunlight
(2) 700 lux HAL represents 5k lux sunlight
(3) 1400 lux HAL represents 10k lux sunlight

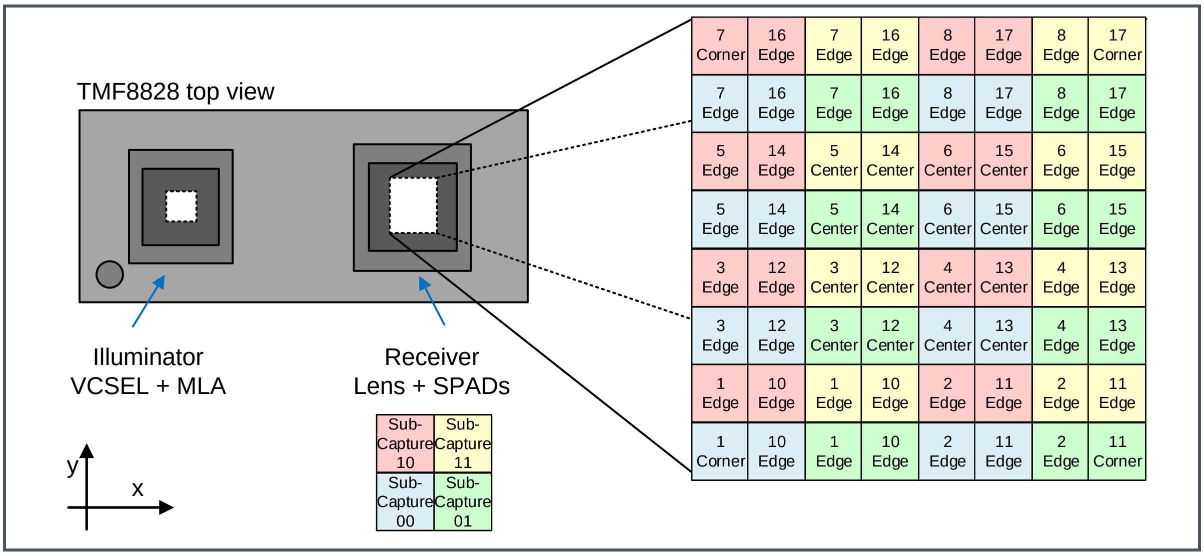
7.4.4 Performance in 8x8 Operating Mode – Only TMF8828

Information

Please note that the zones for 8x8 operating mode are presented in zones 1-8 and 10-17; the result for zone 9 and 18 is not used.

The algorithm reports distance information for each of the zone individually for the closest and the 2nd closest object in 1 mm steps. The algorithm performance is depending on the chosen zone:

Figure 37:
Zones Definition (TMF8828)



After calibration according to section 7.3, the following performance parameters apply. The reported distance is the actual distance between the device and the actual measured zone – there is no perpendicular flat target correction applied. The target covers the full FoV of the device.

Figure 38:
Typical Maximum Distance in 8x8 Mode, 41°x52° FoV, 125 k Iterations (15 Hz output data rate), Light on the Target Only

Target Reflectivity %T at 940 nm	Zone	350 Lux LED Lighting	140 Lux Halogen(1)	700 Lux Halogen(2)	1400 Lux Halogen(3)
White target 90%	Center	4400 mm	2000 mm	1300 mm	1000 mm
	Edge	1500 mm	900 mm	500 mm	400 mm
	Corner	900 mm	600 mm	300 mm	300 mm

Target Reflectivity %T at 940 nm	Zone	350 Lux LED Lighting	140 Lux Halogen(1)	700 Lux Halogen(2)	1400 Lux Halogen(3)
Grey target 18%	Center	2000 mm	1500 mm	1000 mm	800 mm
	Edge	800 mm	600 mm	400 mmm	300 mm
	Corner	500 mm	400 mm	300 mm	200 mm

(1) 140 lux HAL represents 1k lux sunlight
(2) 700 lux HAL represents 5k lux sunlight
(3) 1400 lux HAL represents 10k lux sunlight

7.4.5 Short Range High Accuracy Mode

From EVM release 3v52 onwards, the TMF8820/21/28 have a short range and high accuracy mode. This operating mode enhances the accuracy for a detection range up to 1000 mm.

Use this operating mode only if best accuracy for short range is needed as this operating mode reduces maximum detection distance as shown by Figure 34, Figure 36 and Figure 38 by approximately 50 % and clips it to 1000 mm but greatly enhances accuracy.

The mode can be enabled by setting of register active_range. Please download the relevant calibration data after switching the operating mode.

Figure 39:
Accuracy Short Range Mode of TMF8820/21/28

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{MIN}	Minimum detection distance	Grey target 18%		10		mm
		White target 90%		25		mm
$d_{ACCURACY3x3,4x4}$	Accuracy of detection for 3x3 and 4x4 mode	10 mm to 20 mm		± 10		mm
		20 mm to 200 mm		± 5		mm
		200 mm to 1000 mm; all except corner zones		± 2.0		%
		200 mm to 1000 mm; corner zones		± 2.5		%
$d_{ACCURACY8x8}$	Accuracy of detection for 8x8 mode	10 mm to 20 mm		± 10		mm
		20 mm to 40 mm		± 5		mm
		40 mm to 100 mm		-10/+5		mm
		100 mm to 200 mm		± 5		mm
		200 mm to 1000 mm; all except corner zones		± 2.0		%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		200 mm to 1000 mm; corner zones		± 3.0		%
$d_{PRECISION}$	Precision	± 2 sigma (95%), 350 lux LED lighting		2 mm + 0.5%		

Attention

The short range, high accuracy mode needs an individual calibration per SPAD map – see document TMF882X_Host_Driver_Communication*.pdf for detailed explanation of this calibration.

7.4.6 Accuracy / Precision Long Range Mode (default)

Figure 40:
Accuracy and Precision Parameters Long Range Mode (TMF8820/21 mode – 550 k iterations)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{MIN}	Minimum detection distance			10		mm
$d_{ACCURACY}$	Accuracy of detection	10 mm to 20 mm		± 19		mm
		20 mm to 50 mm, grey target		± 10		mm
		50 mm to 250 mm		± 15		mm
		250 mm to 333 mm		± 10		mm
		≥ 333 mm		± 3		%
$d_{PRECISION}$	Precision	± 2 sigma (95%), 350 lux LED lighting		2 mm + 0.5%		

Please note that above parameters are typical parameters and perpendicular flat target correction applied.

Figure 41:
Accuracy and Precision Parameters Long Range Mode (TMF8828 mode – 125 k iterations)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{MIN}	Minimum detection distance			10		mm
$d_{ACCURACY}$	Accuracy of detection	10 mm to 20 mm		-4/+22		mm

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		20 mm to 50 mm, grey target		-3/+18		mm
		50 mm to 250 mm		-16/+7		mm
		250 mm to 333 mm		-12/+7		mm
		≥ 333 mm		± 5		%
$d_{PRECISION}$	Precision	± 2 sigma (95%), 350 lux LED lighting		2 mm + 0.5%		

Please note that above parameters are typical parameters on clear cover glass and perpendicular flat target correction applied.

7.4.7 Confidence

For each detected target, the TMF8820/21/28 provides a confidence result. The confidence result is the signal to noise ratio (SNR) of the detected peak in the histogram.

Signal = Peak value in the histogram
Noise = Noise from the device and ambient light = sqrt (baseline level of histogram)

The confidence value is an 8-bit value which supports two encodings:

Linear Encoding

Selected by setting register bit logarithmic_confidence = 0.

The values for confidence represents directly SNR and are clipped at 255.

Logarithmic Encoding

Selected by setting register bit logarithmic_confidence = 1.

The values 0…40 represent directly SNR. Values above 40 are exponentially scaled with a growth rate of 5.36%.

Following c-like code fragment converts from the coded value ‘confidence’ to the actual value ‘exp_conf’:

```
#define CONF_BREAKPOINT        40

#define EXP_GROWTH_RATE      1.053676f
```

```
if (confidence <= CONF_BREAKPOINT)
        // confidence 0 - 40 are unchanged linear scale
        exp_conf = confidence;
else {
        // Exponential de-mapping
        uint32_t steps = confidence - CONF_BREAKPOINT;
        uint32_t exp_conf = (uint32_t)
                (CONF_BREAKPOINT* pow((double)EXP_GROWTH_RATE,(double)steps));
}
```

7.5 Typical Optical Characteristics

7.5.1 VCSEL

Internal protection ensures no single point of failure will cause the VCSEL to violate the Class 1 Laser Safety.

- Laser Safety Class 1

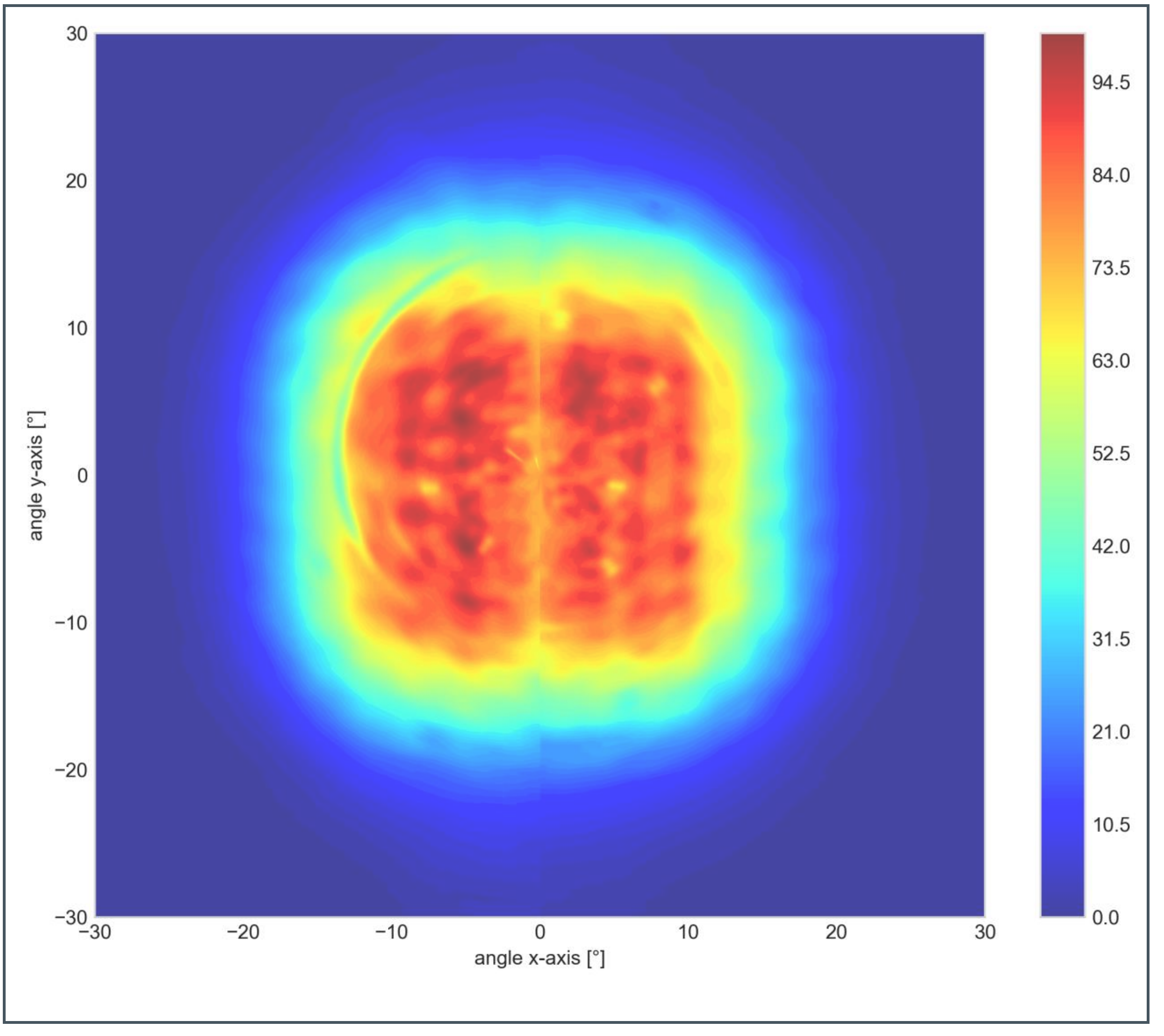
7.5.2 FoI / FoV

- VCSEL Field of Illumination (FoI)
  - 47x57º (70° diagonal calc.) full width from 5% of maximum up to max.
  - 41x47º (60° diagonal calc.) 1/e^2
  - 30x32º (43° diagonal calc.) FWHM

Information

The smaller value (x/y) for FoI is always into the direction of the SPADs.
FWHM … Full width half maximum

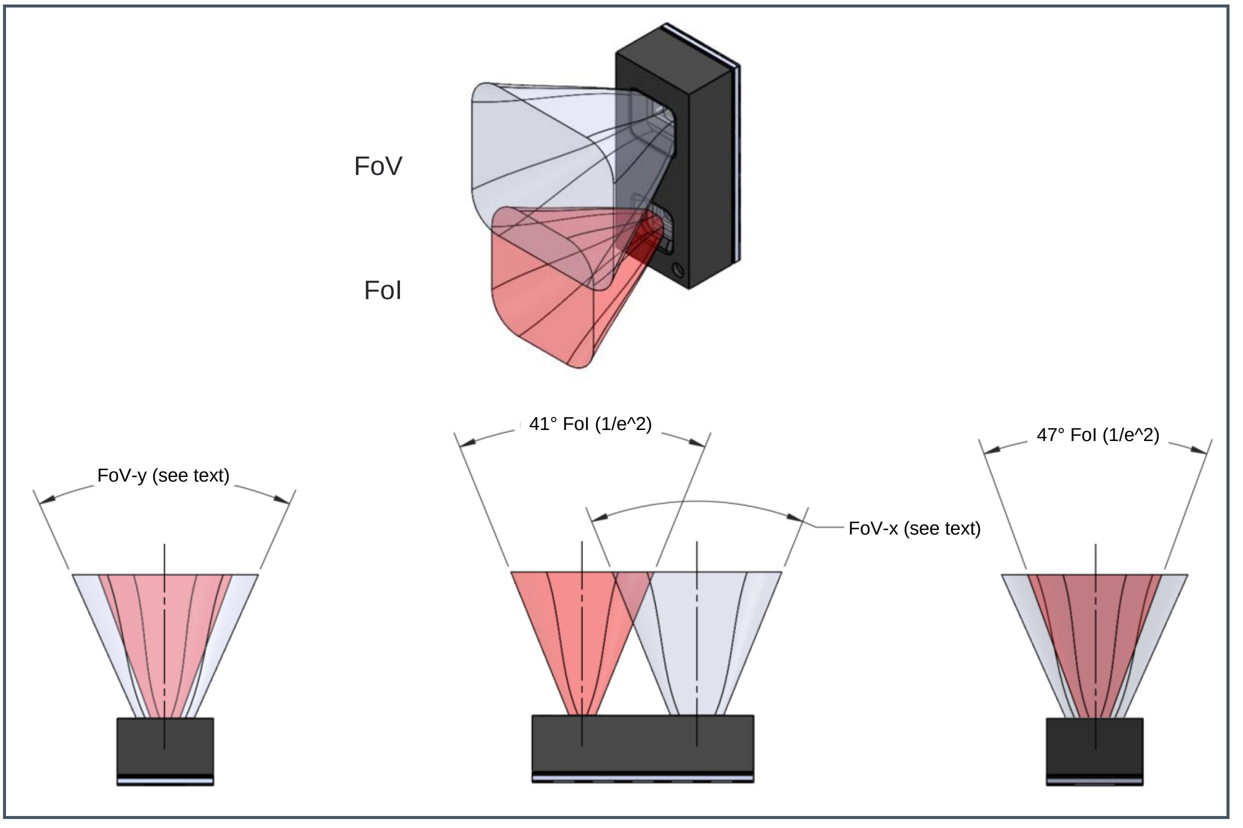
Figure 42:
Field of Illumination Shown in Pseudocolors in [%] of Max Range



The sensor field is view (FoV) depends on the chosen spad_map_id:

- dToF Sensor Field of View (FoV)   41x52º (63° diagonal calc.)   spad_map_id=6 or 7
  33x32º (45° diagonal calc.)   spad_map_id=1
  see Figure 30 and Figure 31 – fully customizable FoV.

Figure 43:
FoV/FoI of TMF8820/21/28



7.5.3 Optical Filter Characteristics

The on-chip optical filter blocks most of the ambient light and improves the performance especially with sunlight. It is possible to add another optical filter on top to even further improve sunlight performance.

- FWHM 92 nm
- Passband Center Wavelength 940 nm (filter only)

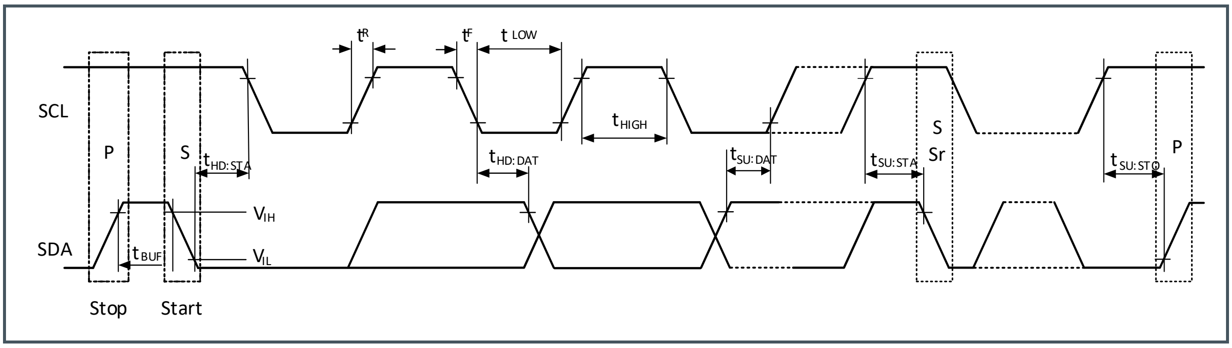
7.6 I²C Interface

The TMF8820/21/28 is controlled by an I²C bus, one interrupt pin and two GPIO pins.

Additionally see ams OSRAM device driver and/or application note TMF882X_Host_Driver_Communication_*.pdf for a detailed explanation of the I²C communication itself.

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing (default: 0x41) and standard, fast mode and fast mode plus modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Figure 44:
I²C Timings



The TMF8820/21/28 support following I²C operating modes:

- Standard mode – up to 100 kBit/s
- Fast-mode – up to 400 kBit/s
- Fast-mode-plus – up to 1 MBit/s

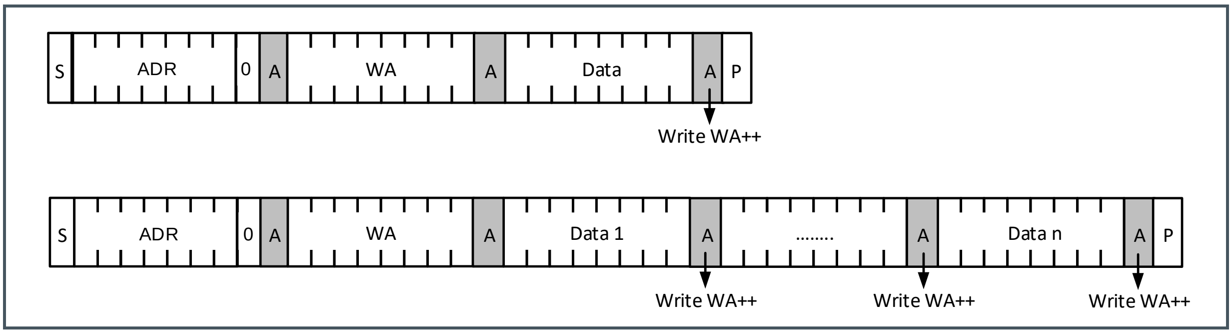
Figure 45:
I²C Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start (start condition end without preceding stop condition)	R	1-bit
ADR	Slave address 7 bits = default 0x41	R	Slave address
WA	Word address	R	8-bit
A	Acknowledge	W	1-bit
N	No Acknowledge	R	1-bit
Data	Data/write	R or W	8-bit
Data(n)	Data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Slave increment word address	R	During acknowledge

Internal to the device, an 8-bit buffer stores the register address location of the byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a P (Stop condition) and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

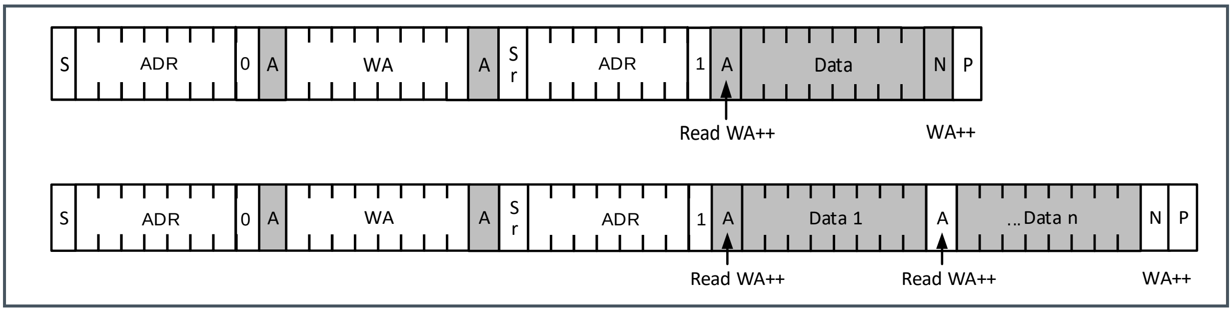
A Write transaction consists of a S, ADR, 0 (R/W flag), WA, Data (n), and P. Following each byte (9th clock pulse) the slave places an A or NA (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a P.

Figure 46:
Byte Write and Page Write Commands



A Read transaction consists of a S, ADR, 0 (R/W flag), WA, Sr, ADR, 1 (R/W flag), Data(n) and P. Following all but the final byte the master places an A (ACK) on the bus (9^{th} clock pulse). Termination of the Read transaction is indicated by a N (NACK) being placed on the bus by the master, followed by STOP.

Figure 47:
Random Read and Sequential Read Command (example shows 2 bytes)



The default I^2C address is 0x41. The address can be changed after power-up. Use the enable pin to enable only one device at a time to provide unique device addresses – see section 9.1.1.

The device is I^3C tolerant – therefore it can coexist with I^3C devices on the same bus. TMF8820/21/28 communicates in legacy I^2C mode of the I^3C bus.

Attention

During standby and standby timed mode, only register 0xE0 (ENABLE) is accessible by the I^2C interface.

8 Register Description

8.1 Register Overview

Please note that the I²C register table uses pages. Therefore, the content of the registers depends on the page select register app_id and cid_rid.

Figure 48:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
Any appid, any cid_rid – Registers always available									
0x00	**APPID**	appid							
0x01	**MINOR**	minor							
0xE0	**ENABLE**	0	cpu_ready	powerup_select					pon
0xE1	**INT_STATUS**	0	int7	int6	0	int4	0	int2	0
0xE2	**INT_ENAB**	0	int7_enab	int6_enab	0	int4_enab	0	int2_enab	0
0xE3	**ID**			0	0	1	0	0	0
0xE4	**REVID**						rev_id		
appid=0x03, any cid_rid - Main Application Registers									
0x02	**PATCH**	patch							
0x03	**BUILD_TYPE**	build							
0x04	**APPLICATION_STATUS**	app_status							
0x05	**MEASURE_STATUS**	measure_status							
0x06	**ALGORITHM_STATUS**	alg_status							
0x07	**CALIBRATION_STATUS**	fc_status							
0x08	**CMD_STAT**	cmd_stat							
0x09	**PREV_CMD**	prev_cmd							
0x10	**MODE (TMF8828 ONLY)**	mode							
0x0A	**LIVE_BEAT**	live_beat							
0x19	**ACTIVE_RANGE**	active_range							
0x1C	**SERIAL_NUMBER_0**	serial_number[7:0]							
0x1D	**SERIAL_NUMBER_1**	serial_number[15:8]							
0x1E	**SERIAL_NUMBER_2**	serial_number[23:16]							
0x1F	**SERIAL_NUMBER_3**	serial_number[31:24]							
0x20	**CONFIG_RESULT**	cid_rid							
0x21	**TID**	tid							
0x22	**SIZE_LSB**	size[7:0]							
0x23	**SIZE_MSB**	size[15:8]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
appid=0x03, cid_rid=0x10 – Measurement Results									
0x24	**RESULT_NUMBER**	number							
0x25	**TEMPERATURE**	temperature							
0x26	**NUMBER_VALID_RESULTS**	valid_results							
0x28	**AMBIENT_LIGHT_0**	ambient[7:0]							
0x29	**AMBIENT_LIGHT_1**	ambient[15:8]							
0x2A	**AMBIENT_LIGHT_2**	ambient[23:16]							
0x2B	**AMBIENT_LIGHT_3**	ambient[31:24]							
0x2C	**PHOTON_COUNT_0**	photon_count[7:0]							
0x2D	**PHOTON_COUNT_1**	photon_count[15:8]							
0x2E	**PHOTON_COUNT_2**	photon_count[23:16]							
0x2F	**PHOTON_COUNT_3**	photon_count[31:24]							
0x30	**REFERENCE_COUNT_0**	reference_count[7:0]							
0x31	**REFERENCE_COUNT_1**	reference_count[15:8]							
0x32	**REFERENCE_COUNT_2**	reference_count[23:16]							
0x33	**REFERENCE_COUNT_3**	reference_count[31:24]							
0x34	**SYS_TICK_0**	sys_tick[7:0]							
0x35	**SYS_TICK_1**	sys_tick[15:8]							
0x36	**SYS_TICK_2**	sys_tick[23:16]							
0x37	**SYS_TICK_3**	sys_tick[31:24]							
0x38	**RES_CONFIDENCE_0**	confidence0							
0x39	**RES_DISTANCE_0_LSB**	distance0[7:0]							
0x3A	**RES_DISTANCE_0_MSB**	distance0[15:8]							
0x3B	**RES_CONFIDENCE_1**	confidence1							
0x3C	**RES_DISTANCE_1_LSB**	distance1[7:0]							
0x3D	**RES_DISTANCE_1_MSB**	distance1[15:8]							
…	**…**								
0xA1	**RES_CONFIDENCE_35**	confidence35							
0xA2	**RES_DISTANCE_35_LSB**	distance35[7:0]							
0xA3	**RES_DISTANCE_35_MSB**	distance35[15:8]							
appid=0x03, cid_rid=0x16 – Configuration Page									
0x24	**PERIOD_MS_LSB**	period[7:0]							
0x25	**PERIOD_MS_MSB**	period[15:8]							
0x26	**KILO_ITERATIONS_LSB**	iterations[7:0]							
0x27	**KILO_ITERATIONS_MSB**	iterations[15:8]							
0x28	**INT_THRESHOLD_LOW_LSB**	int_threshold_low[7:0]							
0x29	**INT_THRESHOLD_LOW_MSB**	int_threshold_low[15:8]							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x2A	**INT_THRESHOLD_HIGH_LSB**	int_threshold_high[7:0]							
0x2B	**INT_THRESHOLD_HIGH_MSB**	int_threshold_high[15:8]							
0x2C	**INT_ZONE_MASK_0**	int_zone_mask[7:0]							
0x2D	**INT_ZONE_MASK_1**	int_zone_mask[15:8]							
0x2E	**INT_ZONE_MASK_2**							int_zone_mask[17:16]	
0x2F	**INT_PERSISTENCE**	int_persistence							
0x30	**CONFIDENCE_THRESHOLD**	confidence_threshold							
0x31	**GPIO_0**	driver_strength0			pre_delay0		gpio0		
0x32	**GPIO_1**	driver_strength1			pre_delay1		gpio1		
0x33	**POWER_CFG**	goto_standby_timed	low_pwr_osc_on	keep_pll_running		allow_osc_retrim	pulse_interrupt		
0x34	**SPAD_MAP_ID**					spad_map_id			
0x35	**ALG_SETTING_0**	logarithmic_confidence				distance_mode	distances		
0x36-0x38		Reserved – keep at 0							
0x39	**HIST_DUMP**								histogram
0x3A	**SPREAD_SPECTRUM**	Reserved – keep at 0					spread_spectrum_factor		
0x3B	**I2C_SLAVE_ADDRESS**	7bit_slave_address							0
0x3C	**OSC_TRIM_VALUE_LSB**	osc_trim_value[7:0]							
0x3D	**OSC_TRIM_VALUE_MSB**								osc_trim_value[8]
0x3E	**I2C_ADDR_CHANGE**					gpio_change_mask		gpio_change_value	
appid=0x03, cid_rid=0x17/0x18 – User defined SPAD Configuration									
0x24	**SPAD_ENABLE_FIRST**	spad_enable_first							
…	**…**								
0x41	**SPAD_ENABLE_LAST**	spad_enable_last							
0x42	**SPAD_TDC_FIRST**	spad_tdc_first							
…	**…**								
0x8C	**SPAD_TDC_LAST**	spad_tdc_last							
0x8D	**SPAD_X_OFFSET_2**	x_offset_2							
0x8E	**SPAD_Y_OFFSET_2**	y_offset_2							
0x8F	**SPAD_X_SIZE**	x_size							
0x90	**SPAD_Y_SIZE**	y_size							
appid=0x03, cid_rid=0x19 – Factory Calibration									
0x24	**FACTORY_CALIBRATION_FIRST**	factory_calibration_first – see section 7.3							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
…	**…**								
0x60-63	**CROSSTALK_ZONE1**	crosstalk_amplitude_zone1, 32-bit value, LSB first (little-endian)							
0x64-67	**CROSSTALK_ZONE2**	crosstalk_amplitude_zone2, 32-bit value, LSB first (little-endian)							
0x68-6B	**CROSSTALK_ZONE3**	crosstalk_amplitude_zone3, 32-bit value, LSB first (little-endian)							
0x6C-6F	**CROSSTALK_ZONE4**	crosstalk_amplitude_zone4, 32-bit value, LSB first (little-endian)							
0x70-73	**CROSSTALK_ZONE5**	crosstalk_amplitude_zone5, 32-bit value, LSB first (little-endian)							
0x74-77	**CROSSTALK_ZONE6**	crosstalk_amplitude_zone6, 32-bit value, LSB first (little-endian)							
0x78-7B	**CROSSTALK_ZONE7**	crosstalk_amplitude_zone7, 32-bit value, LSB first (little-endian)							
0x7C-7F	**CROSSTALK_ZONE8**	crosstalk_amplitude_zone8, 32-bit value, LSB first (little-endian)							
0x80-83	**CROSSTALK_ZONE9**	crosstalk_amplitude_zone9, 32-bit value, LSB first (little-endian)							
…	**…**								
0xB8-BB	**CROSSTALK_ZONE1_TMUX**	crosstalk_amplitude_zone1 time muxed, 32-bit value, LSB first (little-endian) – for 4x4 mode this represents the zone 10 as described in section 7.4.3							
0xBC-BF	**CROSSTALK_ZONE2_TMUX**	crosstalk_amplitude_zone2 time muxed, 32-bit value, LSB first (little-endian)							
0xC0-C3	**CROSSTALK_ZONE3_TMUX**	crosstalk_amplitude_zone3 time muxed, 32-bit value, LSB first (little-endian)							
0xC4-C7	**CROSSTALK_ZONE4_TMUX**	crosstalk_amplitude_zone4 time muxed, 32-bit value, LSB first (little-endian)							
0xC8-CB	**CROSSTALK_ZONE5_TMUX**	crosstalk_amplitude_zone5 time muxed, 32-bit value, LSB first (little-endian)							
0xCC-CF	**CROSSTALK_ZONE6_TMUX**	crosstalk_amplitude_zone6 time muxed, 32-bit value, LSB first (little-endian)							
0xD0-D3	**CROSSTALK_ZONE7_TMUX**	crosstalk_amplitude_zone7 time muxed, 32-bit value, LSB first (little-endian)							
0xD4-D7	**CROSSTALK_ZONE8_TMUX**	crosstalk_amplitude_zone8 time muxed, 32-bit value, LSB first (little-endian)							
0xD8-DB	**CROSSTALK_ZONE9_TMUX**	crosstalk_amplitude_zone9 time muxed, 32-bit value, LSB first (little-endian) – only used for 3x6 mode or customized SPAD maps							
0xDC	**CALIBRATION_STATUS_FC**	fc_status_during_cal - calibration status during factory calibration – copy of register 0x07 – 0x00 success, all other values are reporting an error during calibration							
…	**…**								
0xDF	**FACTORY_CALIBRATION_LAST**	factory_calibration_last							
appid=0x03, cid_rid=0x81 – Raw data Histograms									
0x24	**SUBPACKET_NUMBER**	subpacket_number							
0x25	**SUBPACKET_PAYLOAD**	subpacket_payload							
0x26	**SUBPACKET_CONFIG**								subpacket_config
0x27	**SUBPACKET_DATA0**	subpacket_data0							
…	**…**								
0xA6	**SUBPACKET_DATA127**	subpacket_data127							
appid=0x80 – Bootloader Registers									
0x08	**BL_CMD_STAT**	bl_cmd_stat							
0x09	**BL_SIZE**	bl_size							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x0A	**BL_DATA**	bl_data0 … bl_data127 - size depends on bl_cmd_stat – can be from 0 to 128							
…	**…**								
after data	**BL_CSUM**	bl_csum – actual location depends on bl_cmd_stat – can be from 0x0A to 0x8B							

8.2 Any app_id - Register Description for All Application IDs

8.2.1 APPID Register (Address 0x00)

Figure 49:
APPID Register

Addr: 0x00		APPID			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	appid	0	RO	Currently running application:	
				0x03	Measurement application running (=application major revision) Please allow 6 ms after RAMREMAP_RESET before reading this value.
				0x80	Bootloader running

8.2.2 MINOR Register (Address 0x01)

Figure 50:
MINOR Register

Addr: 0x01		MINOR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	minor	0	RO	Application minor or bootloader revision Please allow 6 ms after RAMREMAP_RESET before reading this value.

8.2.3 ENABLE Register (Address 0xE0)

Figure 51:
ENABLE Register

<table>
<tr><th>Addr: 0xE0</th><th></th><th>ENABLE</th><th></th><th></th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>6</td><td>cpu_ready</td><td>0</td><td>RO</td><td>CPU is ready to handle I^{2}C - if this bit is zero, then only the registers 0xE0 and above are useable, the memory mapped I^{2}C space is not used.
Bit gets set only explicitly by software, therefore a functional and running firmware is necessary for this bit to work.</td></tr>
<tr><td>5:4</td><td>powerup_select</td><td>0</td><td>R_PUSH</td><td>Select what to do at power up. Bits reside in always-on domain and survive standby mode. This bit is evaluated by software only and has no effect on the circuit.
See ams OSRAM driver how to change a running application and how to reset the TMF8820/21/28.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0</td><td>Default – start bootloader</td></tr><tr><td>1</td><td>Start bootloader but do not go to sleep</td></tr><tr><td>2</td><td>Start the application currently in RAM</td></tr><tr><td>3</td><td>Reserved, do not use</td></tr></table></td></tr>
<tr><td>0</td><td>pon</td><td>1</td><td>R_PUSH</td><td>1=Activate oscillator 0=Ask cpu to go to standby
Activating the oscillator is implemented in hardware. Whenever this register is '0' and a '1' is being written, the oscillator is being started and CPU receives a PON1 interrupt. It is implemented in the bootloader to execute a reset at this point, but the application goes to an IDLE state.
De-activating the oscillator is a software assisted process. It is important that the CPU powers down all modules properly before turning off the oscillator, therefore this is implemented in firmware. So writing a '0' to this register will trigger an internal CPU interrupt. The firmware, after powering down everything, sets the device into standby state.</td></tr>
</table>

8.2.4 INT_STATUS Register (Address 0xE1)

Figure 52:
INT_STATUS Register

Addr: 0xE1		INT_STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0		Reserved – leave at 0
6	int7	0	R_PUSH1	Interrupt status for one of the status registers has been set to a non-zero value Int7 status. If bit is asserted, and int7_enab is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear int7 condition.
5	int6	0	R_PUSH1	Interrupt status for a received command has been handled (successfully or error) Int6 status. If bit is asserted, and int6_enab is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear int6 condition.
4		0		Reserved – leave at 0
3	int4	0	R_PUSH1	Interrupt status for raw histogram is ready for readout Int4 status. If bit is asserted, and int4_enab is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear int4 condition.
2		0		Reserved – leave at 0
1	int2	0	R_PUSH1	Interrupt status for measurement result is ready for readout Int2 status. If bit is asserted, and int2_enab is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear int2 condition.
0		0		Reserved – leave at 0

8.2.5 INT_ENAB Register (Address 0xE2)

Figure 53:
INT_ENAB Register

Addr: 0xE2		INT_ENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7		0		Reserved – leave at 0
6	int7_enab	0	RW	Interrupt enable for one of the status registers has been set to a non-zero value

Addr: 0xE2		INT_ENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				0=Disabled, 1=Enabled; INT output is active if int7 flag is "1"
5	int6_enab	0	RW	Interrupt enable for a received command has been handled (successfully or error) 0=Disabled, 1=Enabled; INT output is active if int6 flag is "1"
4		0		Reserved – leave at 0
3	int4_enab	0	RW	Interrupt enable for raw histogram is ready for readout 0=Disabled, 1=Enabled; INT output is active if int4 flag is "1"
2		0		Reserved – leave at 0
1	int2_enab	0	RW	Interrupt enable for measurement result is ready for readout 0=Disabled, 1=Enabled; INT output is active if int2 flag is "1"
0		0		Reserved – leave at 0

8.2.6 ID Register (Address 0xE3)

Figure 54:
ID Register

Addr: 0xE3		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:0	id	08	RO	Chip ID, reads 08h – do not rely on register bits 6 and 7 of this register.

8.2.7 REVID Register (Address 0xE4)

Figure 55:
ID Register

Addr: 0xE4		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2:0	rev_id	NA	RO	Chip revision ID

8.3 appid=0x03, any cid_rid - Main Application Registers

Following registers are only available if appid=0x03 (=measurement application). These registers are always available for appid=0x03 independently of register cid_rid.

8.3.1 PATCH Register (Address 0x02)

Figure 56:
PATCH Register

Addr: 0x02		PATCH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	patch	0	RO	Application patch revision Please allow 6 ms after RAMREMAP_RESET before reading this value.

8.3.2 BUILD_TYPE Register (Address 0x03)

Figure 57:
BUILD_TYPE Register

Addr: 0x03		BUILD_TYPE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	build	0	RO	Application build revision Please allow 6 ms after RAMREMAP_RESET before reading this value.

8.3.3 APPLICATION_STATUS Register (Address 0x04)

Figure 58:
APPLICATION_STATUS Register

Addr: 0x04		APPLICATION_STATUS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	app_status	0	RO	Status information about the application	
				Value	**Description**
				0x00	SUCCESS - application has no error

Addr: 0x04	APPLICATION_STATUS				
Bit	Bit Name	Default	Access	Bit Description	
				0x01	ERR_BIST - histogram RAM BIST returned more than 1 error in at least 1 TDC RAM and cannot be repaired
				0x02	ERR_APP_CANT_STOP_MEASURE - the application could not terminate the measurement state machine. A hard shut-down of the measurement state machine was done
				0x03	ERR_APP_TIMER_OUT_OF_RANGE - upon wakeup from timed sleep the timer value was out of range. Internal program error (maybe RAM lost content)
				0x04	ERR_UNEXPECTED_RESET - host triggered a CPU reset or SW did call SystemReset
				0x05	WARNING_NO_FUSES_FOUND - fuses have not been programmed

8.3.4 MEASURE_STATUS Register (Address 0x05)

Figure 59:
MEASURE_STATUS Register

Addr: 0x05	MEASURE_STATUS				
Bit	Bit Name	Default	Access	Bit Description	
7:0	measure_status	0	RO	Status information about the measurement	
				Value	**Description**
				0x00	SUCCESS – measurement state machine has no error
				0x11	ERR_MEASURE_VCSEL - VCSEL eye safety failed
				0x12	ERR_MEASURE_BDV - failed to find a breakdown voltage
				0x13	Deprecated
				0x14	Deprecated
				0x15	ERR_MEASURE_CFG_TOO_MANY - tried to set a third configuration
				0x16	ERR_MEASURE_NOT_STARTED - tried to start a measurement before configuring the state machine

Addr: 0x05	MEASURE_STATUS				
Bit	Bit Name	Default	Access	Bit Description	
				0x17	ERR_MEASURE_BUFFER_RETURN - tried to return a buffer twice to the state machine
				0x18	ERR_MEASURE_TDC_LOCKUP - when this error code is set, the TDC locked up due to a wrong setting of the Spread Spectrum.

8.3.5 ALGORITHM_STATUS Register (Address 0x06)

Figure 60:
ALGORITHM_STATUS Register

Addr: 0x06	ALGORITHM_STATUS				
Bit	Bit Name	Default	Access	Bit Description	
7:0	alg_status	0	RO	Status information about the algorithm	
				Value	**Description**
				0x00	SUCCESS - Algorithm has no error
				0x21	ERR_ALGORITHM_EC_FAILED - Algorithm could not perform electrical calibration (e.g. no two peaks found)
				0x22	ERR_ALGORITHM_EC_BUFFER_ERROR – Electrical calibration function was called, but no buffer was provided
				0x23	ERR_ALGORITHM_EC_CFG_MISMATCH_ERROR – Electrical calibration function got mismatched config index

8.3.6 CALIBRATION_STATUS Register (Address 0x07)

Figure 61:
CALIBRATION_STATUS Register

Addr: 0x07	CALIBRATION_STATUS				
Bit	Bit Name	Default	Access	Bit Description	
7:0	fc_status	0	RO	Status about the factory calibration (fc)	
				Value	**Description**
				0x00	SUCCESS - fc has no error

Addr: 0x07		CALIBRATION_STATUS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				0x31	WARNING_NO_FACTORY_CALIBRATION - No factory calibration available, device performance may be degraded
				0x32	WARNING_FACTORY_CALIBRATION_DOES_NOT_MATCH_SPAD_MASK - Factory calibration and SPAD mask do not correlate, device performance may be degraded

8.3.7 CMD_STAT Register (Address 0x08)

Figure 62:
CMD_STAT Register

Addr: 0x08		CMD_STAT			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	cmd_stat	0	RW	Host writes to this register a command. Commands have the value range 0x10...0xFF. Device writes to this register a status. Status have the value range 0x00…0x0F	
				Value	**Description**
				0x10	CMD_MEASURE - Measure: start a cyclic measurement according to the configuration
				0x11	CMD_CLEAR_STATUS - Clear Status: clear all status registers (note that a new measurement clears them as well)
				0x12	CMD_GPIO – GPIO - configure GPIO pins according to the configuration
				0x13	CMD_RESERVED_EC - Reserved, do not use
				0x14	CMD_RESERVED_AH - Reserved, do not use
				0x15	CMD_WRITE_CONFIG_PAGE - Write Configuration page (whatever page has been loaded to registers 0x20 and following will be written to the device)
				0x16	CMD_LOAD_CONFIG_PAGE_COMMON - Load Configuration Page 0 - common configuration

Addr: 0x08		CMD_STAT			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				0x17	CMD_LOAD_CONFIG_PAGE_SPAD_1 - Load Configuration Page 1 - SPAD configuration
				0x18	CMD_LOAD_CONFIG_PAGE_SPAD_2 - Load Configuration Page 2 - SPAD configuration alternate measurement
				0x19	CMD_LOAD_CONFIG_PAGE_FACTORY_CALIB - Load Configuration Page 3 - factory calibration
				0x20	CMD_FACTORY_CALIBRATION - Perform Factory Calibration
				0x21	CMD_I2C_SLAVE_ADDRESS - Command that sets the device's I²C slave address to the address specified in config page common (see registers I2C_SLAVE_ADDRESS and I2C_ADDR_CHANGE)
				0x65	Force device to TMF8820/TMF8821 mode via a cold start (TMF8828 only)
				0x6C	Force device to TMF8828 mode via a cold start (TMF8828 only)
				0xFE	CMD_RESET - Reset: a software system reset shall be executed
				0xFF	CMD_STOP - Stop: Abort any ongoing measurement
				Status Results (0x00-0x0F)	
				0x00	STAT_OK - Ok, command accepted and successfully executed
				0x01	STAT_ACCEPTED - Command accepted and being executed, must send a STOP command to halt continues execution
				0x02	STAT_ERR_CONFIG - ERROR configuration not accepted, ready to accept new command
				0x03	STAT_ERR_APPLICATION - ERROR application encountered a severe error and stopped (more details see register APPLICATION_STATUS), ready to accept new command
				0x04	STAT_ERR_WAKEUP_TIMED - ERROR wakeup timed, severe internal error, device should be power cycled

Addr: 0x08		CMD_STAT			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				0x05	STAT_ERR_RESET_UNEXPECTED - ERROR unexpected reset, severe internal error, device should be power cycles
				0x06	STAT_ERR_UNKNOWN_CMD - ERROR unknown command
				0x07	STAT_ERR_NO_REF_SPAD - ERROR after screamer masking no reference SPAD is selected anymore, change your enable mask
				0x08	reserved
				0x09	STAT_ERR_UNKNOWN_CID - ERROR tried to write a config page with unknown CID, ready to accept new command
				0x0a	STAT_WARNING_CONFIG_SPAD_1_NOT_ACCEPTED - WARNING writing of config SPAD 1 page was ignored, as pre-selected SPAD mask is configured in common page
				0x0b	STAT_WARNING_CONFIG_SPAD_2_NOT_ACCEPTED - WARNING writing of config SPAD 2 page was ignored, as pre-selected SPAD mask, or single user defined is configured in common page
				0x0c	STAT_WARNING_OSC_TRIM_NOT_ACCEPTED - WARNING new osc trim value was ignored, as allow_osc_retrim was not set in register POWER_CONFIG
				0x0d	STAT_WARNING_I2C_ADDRESS_NOT_ACCEPTED - WARNING did not accept new I^2C address, as GPIOs did not match switching condition
				0x0e	STAT_ERR_UNKNOWN_MODE - ERROR this mode is not supported, read to accept a new command

8.3.8 PREV_CMD Register (Address 0x09)

Figure 63:
PREV_CMD Register

Addr: 0x09		PREV_CMD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	prev_cmd	0	RO	The previously executed command by the device - RO to host

8.3.9 MODE Register (Address 0x10)

Figure 64:
MODE Register

Addr: 0x10		MODE			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	mode	0	RO	Currently running application:	
				0x00	TMF8820/21/28 mode
				0x08	TMF8828 mode

8.3.10 LIVE_BEAT Register (Address 0x0A)

Figure 65:
LIVE_BEAT Register

Addr: 0x0A		LIVE_BEAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	live_beat	0	RO	A free running counter that counts every time the application wakes up from sleep (WFI/WFE) the value will be reset to 0 every time the device wakes up from standby or standby-timed

8.3.11 ACTIVE_RANGE Register (Address 0x19)

Figure 66:
ACTIVE_RANGE Register

Addr: 0x19		ACTIVE_RANGE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	active_range	Depends on EVM release	RW	The register switches between short range and long range mode – see section 7.4.5 Short Range High Accuracy Mode - and is only implemented for EVM release 3v52 or higher. 0x00 Accuracy mode not supported (default if function is not supported) 0x6E Short range mode 0x6F Long range mode (default if function is supported)

8.3.12 SERIAL_NUMBER_0 Register (Address 0x1C)

Figure 67:
SERIAL_NUMBER_0 Register

Addr: 0x1C		SERIAL_NUMBER_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	serial_number[7:0]	NA	RO	Serial number bits 0-7

8.3.13 SERIAL_NUMBER_1 Register (Address 0x1D)

Figure 68:
SERIAL_NUMBER_1 Register

Addr: 0x1D		SERIAL_NUMBER_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	serial_number[15:8]	NA	RO	Serial number bits 8-15

8.3.14 SERIAL_NUMBER_2 Register (Address 0x1E)

Figure 69:
SERIAL_NUMBER_2 Register

Addr: 0x1E		SERIAL_NUMBER_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	serial_number[23:16]	NA	RO	Serial number bits 16-23

8.3.15 SERIAL_NUMBER_3 Register (Address 0x1F)

Figure 70:
SERIAL_NUMBER_3 Register

Addr: 0x1F		SERIAL_NUMBER_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	serial_number[31:24]	NA	RO	Serial number bits 24-31

8.3.16 CONFIG_RESULT Register (Address 0x20)

CONFIG_RESULT is the paging register, which defines what content is accessible in registers 0x24-0xDF.

Figure 71:
CONFIG_RESULT Register

Addr: 0x20		CONFIG_RESULT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	cid_rid	0	RO	This register defines the content of registers 0x24-0xDF; this is a page selection and the actual content is paged into registers 0x24-0xDF This register is modified using command triggered by setting register cmd_stat – do not change this register directly. **Value** **Description** 0x10 MEASUREMENT_RESULT - result record of a measurement 0x16 COMMON_CID - COMMON configuration page

Addr: 0x20		CONFIG_RESULT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				0x17 — SPAD_1_CID – User defined SPAD configuration page 1 (first measurement in time multiplexed mode)
				0x18 — SPAD_2_CID – User defined SPAD configuration page 2 (2nd measurement in time multiplexed mode)
				0x19 — FACTORY_CALIBRATION_CID - factory calibration page ID
				0x81 — HIST_RAW_CID: Raw data histogram

8.3.17 TID Register (Address 0x21)

Figure 72:
TID Register

Addr: 0x21		TID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	tid	0	RO	Transaction ID register; changes on every transaction

8.3.18 SIZE_LSB Register (Address 0x22)

Figure 73:
SIZE_LSB Register

Addr: 0x22		SIZE_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	size[7:0]	0	RO	LSB of total packet size – together with SIZE_MSB register define the size of the payload starting from register 0x24 onwards

8.3.19 SIZE_MSB Register (Address 0x23)

Figure 74:
SIZE_MSB Register

Addr: 0x23		SIZE_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	size[15:8]	0	RO	MSB of total packet size – together with SIZE_LSB register define the size of the payload starting from register 0x24 onwards

8.4 appid=0x03, cid_rid=0x10 – Measurement Results

Following registers are only available if appid=0x03 and cid_rid=0x10 – measurement results.

8.4.1 RESULT_NUMBER Register (Address 0x24)

Figure 75:
RESULT_NUMBER Register

Addr: 0x24		RESULT_NUMBER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	number	0	RO	Running counter or results

Information

Please note that in the TMF8828 mode, the lower 2 bits of RESULT_NUMBER (1:0) report SUB-CAPTURE and the upper 6 bits (7:2) are the running counter of results.

8.4.2 TEMPERATURE Register (Address 0x25)

Figure 76:
TEMPERATURE Register

Addr: 0x25		TEMPERATURE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	temperature	0	RO	Temperature of the sensor DIE in °Celsius, range is -128..127

8.4.3 NUMBER_VALID_RESULTS Register (Address 0x26)

Figure 77:
NUMBER_VALID_RESULTS Register

Addr: 0x26		NUMBER_VALID_RESULTS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	valid_results	0	RO	How many zones have reported 1 or 2 results (also no-target counts as a valid result here)

8.4.4 AMBIENT_LIGHT_0 Register (Address 0x28)

Figure 78:
AMBIENT_LIGHT_0 Register

Addr: 0x28		AMBIENT_LIGHT_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ambient[7:0]	0	RO	Summed IR ambient light received by all channels bits 0-7 Note: This is not a linear measurement of the IR light received

8.4.5 AMBIENT_LIGHT_1 Register (Address 0x29)

Figure 79:
AMBIENT_LIGHT_1 Register

Addr: 0x29		AMBIENT_LIGHT_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ambient[15:8]	0	RO	Summed IR ambient light received by all channels bits 8-15 Note: This is not a linear measurement of the IR light received

8.4.6 AMBIENT_LIGHT_2 Register (Address 0x2A)

Figure 80:
AMBIENT_LIGHT_2 Register

Addr: 0x2A		AMBIENT_LIGHT_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ambient[23:16]	0	RO	Summed IR ambient light received by all channels bits 16-23 Note: This is not a linear measurement of the IR light received

8.4.7 AMBIENT_LIGHT_3 Register (Address 0x2B)

Figure 81:
AMBIENT_LIGHT_3 Register

Addr: 0x2B		AMBIENT_LIGHT_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ambient[31:24]	0	RO	Summed IR ambient light received by all channels bits 24-31 Note: This is not a linear measurement of the IR light received

8.4.8 PHOTON_COUNT_0 Register (Address 0x2C)

Figure 82:
PHOTON_COUNT_0 Register

Addr: 0x2C		PHOTON_COUNT_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	photon_count[7:0]	0	RO	Summed weight of the target peak of the closest target and all targets within 10 cm of this target. Bits 0-7

8.4.9 PHOTON_COUNT_1 Register (Address 0x2D)

Figure 83:
PHOTON_COUNT_2 Register

Addr: 0x2D		PHOTON_COUNT_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	photon_count[15:8]	0	RO	Summed weight of the target peak of the closest target and all targets within 10 cm of this target. Bits 8-15

8.4.10 PHOTON_COUNT_2 Register (Address 0x2E)

Figure 84:
PHOTON_COUNT_2 Register

Addr: 0x2E		PHOTON_COUNT_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	photon_count[23:16]	0	RO	Summed weight of the target peak of the closest target and all targets within 10 cm of this target. Bits 16-23

8.4.11 PHOTON_COUNT_3 Register (Address 0x2F)

Figure 85:
PHOTON_COUNT_3 Register

Addr: 0x2F		PHOTON_COUNT_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	photon_count[31:24]	0	RO	Summed weight of the target peak of the closest target and all targets within 10 cm of this target. Bits 24-31

8.4.12 REFERENCE_COUNT_0 Register (Address 0x30)

Figure 86:
REFERENCE_COUNT_0 Register

Addr: 0x30		REFERENCE_COUNT_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reference_count[7:0]	0	RO	Weight of the reference channel peak bits 0-7

8.4.13 REFERENCE_COUNT_1 Register (Address 0x31)

Figure 87:
REFERENCE_COUNT_1 Register

Addr: 0x31		REFERENCE_COUNT_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reference_count[15:8]	0	RO	Weight of the reference channel peak bits 8-15

8.4.14 REFERENCE_COUNT_2 Register (Address 0x32)

Figure 88:
REFERENCE_COUNT_2 Register

Addr: 0x32		REFERENCE_COUNT_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reference_count[23:16]	0	RO	Weight of the reference channel peak bits 16-23

8.4.15 REFERENCE_COUNT_3 Register (Address 0x33)

Figure 89:
REFERENCE_COUNT_3 Register

Addr: 0x33		REFERENCE_COUNT_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reference_count[31:24]	0	RO	Weight of the reference channel peak bits 24-31

8.4.16 SYS_TICK_0 Register (Address 0x34)

Figure 90:
SYS_TICK_0 Register

Addr: 0x34		SYS_TICK_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sys_tick[7:0]	0	RO	System tick with a granularity of 5 MHz (200ns) - bits 0-7 do a blockread starting at 0x20 for correct update Correct timestamps will always have bit 0 set – if bit 0 is not set, the timestamp shall be ignored and not used for clock skew correction.

8.4.17 SYS_TICK_1 Register (Address 0x35)

Figure 91:
SYS_TICK_1 Register

Addr: 0x35		SYS_TICK_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sys_tick[15:8]	0	RO	System tick with a granularity of 5 MHz - bits 8-15 do a blockread starting at 0x20 for correct update

8.4.18 SYS_TICK_2 Register (Address 0x36)

Figure 92:
SYS_TICK_2 Register

Addr: 0x36		SYS_TICK_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sys_tick[23:16]	0	RO	System tick with a granularity of 5 MHz - bits 16-23 do a blockread starting at 0x20 for correct update

8.4.19 SYS_TICK_3 Register (Address 0x37)

Figure 93:
SYS_TICK_3 Register

Addr: 0x37		SYS_TICK_3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sys_tick[31:24]	0	RO	System tick with a granularity of 5 MHz - bits 24-31 do a blockread starting at 0x20 for correct update

8.4.20 RES_CONFIDENCE_0 Register (Address 0x38)

Figure 94:
RES_CONFIDENCE_0 Register

Addr: 0x38		RES_CONFIDENCE_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	confidence0	0	RO	Confidence rating of zone 1 Range 0-255 where 0 = No object detected 255 = Highest confidence

8.4.21 RES_DISTANCE_0_LSB Register (Address 0x39)

Figure 95:
RES_DISTANCE_0_LSB Register

Addr: 0x39		RES_DISTANCE_0_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	distance0[7:0]	0	RO	Distance result in [mm] of zone 1 bits 0-7

8.4.22 RES_DISTANCE_0_MSB Register (Address 0x3A)

Figure 96:
RES_DISTANCE_0_MSB Register

Addr: 0x3A		RES_DISTANCE_0_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	distance0[15:8]	0	RO	Distance result in [mm] of zone 1 bits 8-15

8.4.23 Other Confidence / Distance Results Register (Address 0x3B-0xA3)

Subsequent registers store the result for confidence, distance LSB and distance MSB in same order as RES_CONFIDENCE_0, RES_DISTANCE_0_LSB and RES_DISTANCE_0_MSB for zone 2 to the last zone of the selected mode (space reserved until register 0xA3).

8.5 appid=0x03, cid_rid=0x16 – Configuration Page

Following registers are only available if appid=0x03 and cid_rid=0x16 – configuration page.

8.5.1 PERIOD_MS_LSB Register (Address 0x24)

Figure 97:
PERIOD_MS_LSB Register

Addr: 0x24		PERIOD_MS_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	period[7:0]	33	RW	Measurement period in milliseconds – bits 0-7

8.5.2 PERIOD_MS_MSB Register (Address 0x25)

Figure 98:
PERIOD_MS_MSB Register

Addr: 0x25		PERIOD_MS_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	period[15:8]	0	RW	Measurement period in milliseconds – bits 8-15

8.5.3 KILO_ITERATIONS_LSB Register (Address 0x26)

Figure 99:
KILO_ITERATIONS_LSB Register

Addr: 0x26		KILO_ITERATIONS_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	iterations[7:0]	25	RW	Measurement iterations times 1024 – bits 0-7 e.g. 537 represents 549888 iterations

8.5.4 KILO_ITERATIONS_MSB Register (Address 0x27)

Figure 100:
KILO_ITERATIONS_MSB Register

Addr: 0x27		KILO_ITERATIONS_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	iterations[15:8]	2	RW	Measurement iterations times 1024 – bits 8-15 e.g. 537 represents 549888 iterations

8.5.5 INT_THRESHOLD_LOW_LSB Register (Address 0x28)

Figure 101:
INT_THRESHOLD_LOW_LSB Register

Addr: 0x28		INT_THRESHOLD_LOW_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_threshold_low[7:0]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the object distances is farer than int_threshold_low[mm] – Bits 0-7

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.6 INT_THRESHOLD_LOW_MSB Register (Address 0x29)

Figure 102:
INT_THRESHOLD_LOW_MSB Register

Addr: 0x29		INT_THRESHOLD_LOW_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_threshold_low[15:8]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the object distances is farer than int_threshold_low[mm] – Bits 8-15

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.7 INT_THRESHOLD_HIGH_LSB Register (Address 0x2A)

Figure 103:
INT_THRESHOLD_HIGH_LSB Register

Addr: 0x2A		INT_THRESHOLD_HIGH_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_threshold_high[7:0]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the object distances is closer than int_threshold_high[mm] – Bits 0-7

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.8 INT_THRESHOLD_HIGH_MSB Register (Address 0x2B)

Figure 104:
INT_THRESHOLD_HIGH_MSB Register

Addr: 0x2B		INT_THRESHOLD_HIGH_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_threshold_high[15:8]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the object distances is closer than int_threshold_high[mm] – Bits 8-15

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.9 INT_ZONE_MASK_0 Register (Address 0x2C)

Figure 105:
INT_ZONE_MASK_0 Register

Addr: 0x2C		INT_ZONE_MASK_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_zone_mask[7:0]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the objects enabled by int_zone_mask detects a target– Bits 0-7 Bit 0 – Zone 1 Bit 1 – Zone 2 … Bit 7 – Zone 8

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.10 INT_ZONE_MASK_1 Register (Address 0x2D)

Figure 106:
INT_ZONE_MASK_1 Register

Addr: 0x2D		INT_ZONE_MASK_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_zone_mask[15:8]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the objects enabled by int_zone_mask detects a target– Bits 8-15 Bit 0 – Zone 9

Addr: 0x2D		INT_ZONE_MASK_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				Bit 1 – Zone 10 … Bit 7 – Zone 16

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.11 INT_ZONE_MASK_2 Register (Address 0x2E)

Figure 107:
INT_ZONE_MASK_2 Register

Addr: 0x2E		INT_ZONE_MASK_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	int_zone_mask[17:16]	0	RW	If int_persistance>0 an interrupt for a result will only be raised if any of the objects enabled by int_zone_mask detects a target– Bits 16-17 Bit 0 – Zone 17 Bit 1 – Zone 18

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.12 INT_PERSISTENCE Register (Address 0x2F)

Figure 108:
INT_PERSISTENCE Register

Addr: 0x2F		INT_PERSISTENCE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	int_persistence	0	RW	Number of consecutive measurements that find a target inside the threshold range to trigger an interrupt 0 means each measurement that finds a target inside the threshold range will trigger an interrupt 1 means there have to be two consecutive measurements that find a target inside the threshold range will trigger an interrupt For interrupt masking function to work, also set distances=1 (register 0x35) and histogram=0 (register 0x39)

Information

Please note that in TMF8828 mode, the device does not have the ability to generate an interrupt based on threshold excursions and as such registers at addresses from 0x28 to 0x2F are ignored.

8.5.13 CONFIDENCE_THRESHOLD Register (Address 0x30)

Figure 109:
CONFIDENCE_THRESHOLD Register

Addr: 0x30		CONFIDENCE_THRESHOLD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	confidence_threshold	6	RW	Only objects which have a confidence level equal or higher than this will be reported

8.5.14 GPIO_0 Register (Address 0x31)

Figure 110:
GPIO_0 Register

<table>
<tr><th>Addr: 0x31</th><th></th><th colspan="4">GPIO_0</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">driver_strength0</td><td rowspan="6">0</td><td rowspan="6">RW</td><td colspan="2">Pin GPIO0 driver strength setting</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0</td><td>Default setting</td></tr>
<tr><td>1</td><td>2x driving strength</td></tr>
<tr><td>2</td><td>3x driving strength</td></tr>
<tr><td>3</td><td>4x driving strength</td></tr>
<tr><td rowspan="5">4:3</td><td rowspan="5">pre_delay0</td><td rowspan="5">0</td><td rowspan="5">RW</td><td colspan="2">Pin GPIO0 pre-delay setting only for gpio0=3 or 4</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0</td><td>No delay</td></tr>
<tr><td>1</td><td>GPIO0 is asserted 100 µs before the VCSEL pulse</td></tr>
<tr><td>2</td><td>GPIO0 is asserted 200 µs before the VCSEL pulse</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">gpio0</td><td rowspan="9">0</td><td rowspan="9">RW</td><td colspan="2">Pin GPIO0 configuration</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0</td><td>Tristate</td></tr>
<tr><td>1</td><td>Input active high</td></tr>
<tr><td>2</td><td>Input active low</td></tr>
<tr><td>3</td><td>Output active low when VCSEL is pulsing – do not set gpio1 to 3 or 4 if this is used</td></tr>
<tr><td>4</td><td>Output active high when VCSEL is pulsing – do not set gpio1 to 3 or 4 if this is used</td></tr>
<tr><td>5</td><td>Output always high</td></tr>
<tr><td>6</td><td>Output always low</td></tr>
</table>

8.5.15 GPIO_1 Register (Address 0x32)

Figure 111:
GPIO_1 Register

<table>
<tr><th colspan="2">Addr: 0x32</th><th colspan="3">GPIO_1</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>7:6</td><td>driver_strength1</td><td>0</td><td>RW</td><td>Pin GPIO1 driver strength setting<table><tr><th>Value</th><th>Description</th></tr><tr><td>0</td><td>Default setting</td></tr><tr><td>1</td><td>2x driving strength</td></tr><tr><td>2</td><td>3x driving strength</td></tr><tr><td>3</td><td>4x driving strength</td></tr></table></td></tr>
<tr><td>4:3</td><td>pre_delay1</td><td>0</td><td>RW</td><td>Pin GPIO1 pre-delay setting only for gpio0=3 or 4<table><tr><th>Value</th><th>Description</th></tr><tr><td>0</td><td>No delay</td></tr><tr><td>1</td><td>GPIO1 is asserted 100 µs before the VCSEL pulse</td></tr><tr><td>2</td><td>GPIO1 is asserted 200 µs before the VCSEL pulse</td></tr></table></td></tr>
<tr><td>2:0</td><td>gpio1</td><td>0</td><td>RW</td><td>Pin GPIO1 configuration<table><tr><th>Value</th><th>Description</th></tr><tr><td>0</td><td>Tristate</td></tr><tr><td>1</td><td>Input active high</td></tr><tr><td>2</td><td>Input active low</td></tr><tr><td>3</td><td>Output active low when VCSEL is pulsing – do not set gpio0 to 3 or 4 if this is used</td></tr><tr><td>4</td><td>Output active high when VCSEL is pulsing – do not set gpio0 to 3 or 4 if this is used</td></tr><tr><td>5</td><td>Output always high</td></tr><tr><td>6</td><td>Output always low</td></tr></table></td></tr>
</table>

8.5.16 POWER_CFG Register (Address 0x33)

Figure 112:
POWER_CFG Register

Addr: 0x33		POWER_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	goto_standby_timed	0	RW	If possible go to standby timed to save power when waiting for measurement period to expire (PERIOD_MS_*)
6	low_power_osc_on	0	RW	Use low power oscillator in standby timed mode
5	keep_pll_running	0	RW	In idle mode keep PLL running
4		0	RW	Reserved – keep at 0
3	allow_osc_retrim	0	RW	If set oscillator retrimming is allowed (register OSC_TRIM_VALUE_*)
2	pulse_interrupt	0	RW	If set the INT pin has pulse behavior and shall not be cleared by the host, if cleared it is a level interrupt that shall be cleared by the host before reading the results
1:0	reserved	0	RW	Reserved – keep at 0

8.5.17 SPAD_MAP_ID Register (Address 0x34)

Figure 113:
SPAD_MAP_ID Register

<table>
<tr><th>Addr: 0x34</th><th></th><th colspan="2">SPAD_MAP_ID</th><th colspan="2"></th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="7">3:0</td><td rowspan="7">spad_map_id</td><td rowspan="7">1</td><td rowspan="7">RW</td><td colspan="2">Select SPAD map, which defines FoV</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0</td><td>Reserved – do not use</td></tr>
<tr><td>1</td><td>3x3 normal mode 33°x32° FoV</td></tr>
<tr><td>2</td><td>3x3 macro 1 mode 33°x47° FoV off center (use macro 1 or macro 2 depending if camera is above or below TMF8820/21/28).</td></tr>
<tr><td>3</td><td>3x3 macro 2 mode 33°x47° FoV</td></tr>
<tr><td>4</td><td>Only TMF8821: 4x4 macro 1 mode 33°x47° FoV (use macro 1 or macro 2 depending if camera is above or below TMF8821).</td></tr>
</table>

Addr: 0x34		SPAD_MAP_ID			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				5	Only TMF8821: 4x4 macro 2 mode 33°x47° FoV
				6	3x3 wide mode 41°x52° FoV
				7	Only TMF8821: 4x4 normal mode 41°x52° FoV
				8-9	Reserved – do not use
				10	Only TMF8821: 3x6 mode, 33°x60° FoV
				11	3x3 mode 33°x32° FoV, checkerboard – disable 1st, 3rd, 5th… (use for high ambient light)
				12	3x3 mode 33°x32° FoV, inverted checkerboard – disable 2nd, 4th, 6th… (use for high ambient light)
				13	Only TMF8821: 4x4 narrow mode 33°x42° FoV
				14	User defined mode, single measurement mode using config_page_spad1 only
				15	Only TMF8821: User defined mode, time multiplexed measurement mode using config_page_spad1 and 2 (note: in TMF8828 mode, this bit will be set when read but the user cannot define the SPAD mask)

8.5.18 ALG_SETTING_0 Register (Address 0x35)

Figure 114:
ALG_SETTING_0 Register

Addr: 0x35		ALG_SETTING_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	logarithmic_confidence	0	RW	This bit defines the confidence value encoding – see section 7.4.7 0 … linear encoding 1 … logarithmic encoding
6:3		0	RW	Reserved – keep at 0
2	distances	1	RW	If set do report distance results

Addr: 0x35		ALG_SETTING_0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	reserved	0	RW	Reserved – keep at 0

Register 0x36-0x38 is reserved for future extensions – keep registers at default value of 0x00.

8.5.19 HIST_DUMP Register (Address 0x39)

Figure 115:
HIST_DUMP Register

Addr: 0x39		HIST_DUMP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	reserved	0	RW	Reserved – keep at 0
0	histogram	0	RW	If set dump 24-bit raw histograms; do not set if int_persistence > 0 See ams OSRAM device driver and/or application note TMF882X_Host_Driver_Communication_*.pdf for interpretation of this value.

8.5.20 SPREAD_SPECTRUM Register (Address 0x3A)

Figure 116:
SPREAD_SPECTRUM Register

Addr: 0x3A		SPREAD_SPECTRUM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	reserved	0	RW	Reserved – keep at 0
2:0	spread_spectrum_factor	0	RW	Spread spectrum configuration to avoid aliasing of far objects to closer distance – valid range 0…5. If set >0, this jitters the VCSEL pulses, which widens the frequency band for EMC emission. DO NOT SET HIGHER THAN 5.

Attention

Use the lastest firmware version to use the register spread_spectrum_factor.

8.5.21 I2C_SLAVE_ADDRESS Register (Address 0x3B)

Figure 117:
I2C_SLAVE_ADDRESS Register

Addr: 0x3B		I2C_SLAVE_ADDRESS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	7bit_slave_address	0x41	RW	I^2C slave 7-bit address, a change requires the command CMD_I2C_SLAVE_ADDRESS to be executed; see register I2C_ADDR_CHANGE (0x3E) for conditions for this change
0	reserved	0	RW	Reserved – keep at 0

8.5.22 OSC_TRIM_VALUE_LSB Register (Address 0x3C)

Figure 118:
OSC_TRIM_VALUE_LSB Register

Addr: 0x3C		OSC_TRIM_VALUE_LSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	osc_trim_value[7:0]	0	RW	Oscillator trim value is a 9-bit signed value – bits 0-7

8.5.23 OSC_TRIM_VALUE_MSB Register (Address 0x3D)

Figure 119:
OSC_TRIM_VALUE_MSB Register

Addr: 0x3D		OSC_TRIM_VALUE_MSB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	reserved			Reserved – keep at 0
0	osc_trim_value[8]	0	RW	Oscillator trim value is a 9-bit signed value – bit 8

8.5.24 I2C_ADDR_CHANGE Register (Address 0x3E)

Figure 120:
I2C_ADDR_CHANGE Register

Addr: 0x3E		I2C_ADDR_CHANGE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:2	gpio_change_mask	0	RW	See gpio_change_value
1:0	gpio_change_value	0	RW	The command CMD_I2C_SLAVE_ADDRESS will only be executed if (gpio_data & gpio_change_mask) == (gpio_change_value & gpio_change_mask) Where gpio_data = [state of GPIO1, state of GPIO0]

Note: If the I²C address change shall be done in any case, set gpio_change_mask = 0 and gpio_change_value = 0.

8.6 appid=0x03, cid_rid=0x17/0x18 – User Defined SPAD Configuration

Following registers are only available if appid=0x03 and cid_rid=0x17/0x18 – SPAD configuration. For cid_rid=0x17 these registers apply for non time multiplexed mode (3x3) or for the first measurement in time multiplexed mode (4x4 – only TMF8821). cid_rid=0x18 is only available in TMF8821 and used for the second measurement in time multiplexed mode (4x4).

Use ams OSRAM device driver to access these registers – they provide a high level interface to configure the SPAD mask.

Information

Please note that in TMF8828 mode, user defined SPAD masks are not available and any attempt to store a SPAD configuration will result in a warning in the status register.

8.6.1 SPAD_ENABLE_FIRST Register (Address 0x24)

Figure 121:
SPAD_ENABLE_FIRST Register

Addr: 0x24		SPAD_ENABLE_FIRST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	spad_enable_first	0	RW	Start of SPAD enable mask

8.6.2 SPAD_ENABLE_LAST Register (Address 0x41)

Figure 122:
SPAD_ENABLE_LAST Register

Addr: 0x41		SPAD_ENABLE_LAST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	spad_enable_last	0	RW	Start of SPAD enable mask

8.6.3 SPAD_TDC_FIRST Register (Address 0x42)

Figure 123:
SPAD_TDC_FIRST Register

Addr: 0x42		SPAD_ENABLE_FIRST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	spad_tdc_first	0	RW	Start of SPAD to TDC channel select mask

8.6.4 SPAD_TDC_LAST Register (Address 0x8C)

Figure 124:
SPAD_TDC_LAST Register

Addr: 0x8C		SPAD_ENABLE_LAST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	spad_tdc_last	0	RW	Start of SPAD to TDC channel select mask

8.6.5 SPAD_X_OFFSET_2 Register (Address 0x8D)

Figure 125:
SPAD_X_OFFSET_2 Register

Addr: 0x8D		SPAD_X_OFFSET_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	x_offset_2	0	RW	Signed offset in x-direction in Q1 from the FoV center (Q1 = signed number multiplied by 2)

8.6.6 SPAD_Y_OFFSET_2 Register (Address 0x8E)

Figure 126:
SPAD_Y_OFFSET_2 Register

Addr: 0x8E		SPAD_Y_OFFSET_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	y_offset_2	0	RW	Signed offset in y-direction in Q1 from the FoV center (Q1 = signed number multiplied by 2)

8.6.7 SPAD_X_SIZE Register (Address 0x8F)

Figure 127:
SPAD_X_SIZE Register

Addr: 0x8F		SPAD_X_SIZE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	x_size	0	RW	Size in full SPADs of the SPAD mask in x-direction (valid range is 1..18)

8.6.8 SPAD_Y_SIZE Register (Address 0x90)

Figure 128:
SPAD_Y_SIZE Register

Addr: 0x90		SPAD_Y_SIZE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	y_size	0	RW	Size in full SPADs of the SPAD mask in y-direction (valid range is 1..10)

8.7 appid=0x03, cid_rid=0x19 – Factory Calibration

Following registers are only available if appid=0x03 and cid_rid=0x19 – Factory calibration.

8.7.1 FACTORY_CALIBRATION_FIRST Register (Address 0x24)

Figure 129:
FACTORY_CALIBRATION_FIRST Register

Addr: 0x24		FACTORY_CALIBRATION_FIRST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	factory_calibration_first	0	RW	Start of factory calibration data block

For crosstalk registers see Figure 48.

8.7.2 CALIBRATION_STATUS_FC Register (Address 0xDC)

Figure 130:
CALIBRATION_STATUS_FC Register

Addr: 0xDC		CALIBRATION_STATUS_FC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fc_status_during_cal	0	RW	Calibration status during factory calibration – copy of register 0x07 – 0x00 success, all other values are reporting an error during calibration

8.7.3 FACTORY_CALIBRATION_LAST Register (Address 0xDF)

Figure 131:
FACTORY_CALIBRATION_LAST Register

Addr: 0xDF		FACTORY_CALIBRATION_LAST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	factory_calibration_last	0	RW	End of factory calibration data block

8.8 appid=0x03, cid_rid=0x81 – Raw Data Histograms

Following registers are only available if appid=0x03 and cid_rid=0x81 – Raw data histograms. ams OSRAM recommends to use ams OSRAM device driver how to use these registers.

8.8.1 SUBPACKET_NUMBER Register (Address 0x24)

Figure 132:
SUBPACKET_NUMBER Register

Addr: 0x24		SUBPACKET_NUMBER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	subpacket_number	0	RW	Subpacket number – see ams OSRAM device driver and/or application note TMF882X_Host_Driver_Communication_*.pdf for interpretation of this value

8.8.2 SUBPACKET_PAYLOAD Register (Address 0x25)

Figure 133:
SUBPACKET_PAYLOAD Register

Addr: 0x25		SUBPACKET_PAYLOAD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	subpacket_payload	0x80	RW	Size of payload – always 0x80

8.8.3 SUBPACKET_CONFIG Register (Address 0x26)

Figure 134:
SUBPACKET_CONFIG Register

Addr: 0x26		SUBPACKET_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	subpacket_config	0	RW	0 = No time multiplex or first timeslot of time multiplex 1 = Second timeslot of time multiplex (only TMF8821)

8.8.4 SUBPACKET_DATA0 Register (Address 0x27)

Figure 135:
SUBPACKET_DATA0 Register

Addr: 0x27		SUBPACKET_DATA0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	subpacket_data0	0	RW	First data byte of this subpacket – see ams OSRAM device driver and/or application note TMF882X_Host_Driver_Communication_*.pdf for interpretation of this value

8.8.5 SUBPACKET_DATA127 Register (Address 0xA6)

Figure 136:
SUBPACKET_DATA127 Register

Addr: 0xA6		SUBPACKET_DATA127		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	subpacket_data127	0	RW	Last data byte of this subpacket – see ams OSRAM device driver and/or application note TMF882X_Host_Driver_Communication_*.pdf for interpretation of this value

8.9 appid=0x80 – Bootloader Registers

Following registers are only available if appid=0x80 (Bootloader). ams OSRAM recommends to use ams OSRAM device driver to operate the bootloader.

8.9.1 BL_CMD_STAT (Address 0x08)

Figure 137:
BL_CMD_STAT Register

Addr: 0x08		BL_CMD_STAT			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	bl_cmd_stat	0	RW	Write: Bootloader Command – see section 8.9.5 Bootloader Commands Read: Bootloader Status:	
				0x00	STAT_READY - the last command executed successfully
				0x01	STAT_ERR_SIZE - the last command had a size mismatch
				0x02	STAT_ERR_CSUM - the last command had a faulty checksum or was unknown
				0x03	STAT_ERR_RANGE - the last command tried to access RAM out of range
				0x04	STAT_ERR_MORE - the last command caused an error and there is more information in the response

8.9.2 BL_SIZE (Address 0x09)

Figure 138:
BL_SIZE Register

Addr: 0x09		BL_SIZE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	bl_size	0	RW	Data size in bytes

8.9.3 BL_DATA (Address 0x0A-0x8A)

Figure 139:
BL_DATA Register

Addr: 0x0A-0x8A		BL_DATA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	bl_data0 … bl_data127	0	RW	Up to 128 data bytes for bootloader commands

8.9.4 BL_CSUM (Address after bl_data*)

The actual I^{2}C address of BL_SUM depends on the length of the payload (bl_data0-bl_data127); BL_SUM always is after the last data byte.

Note: If there is no databyte, BL_SUM address is 0x0A.

Figure 140:
BL_CSUM Register

Addr: After bl_data*		BL_CSUM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	bl_csum	0	RW	Checksum for Sum(Command + Data Size + Data itself) XOR 0xFF

8.9.5 Bootloader Commands

The following commands (bl_cmd_stat) are supported by the bootloader:

Figure 141:
Bootloader Commands

Command	Value	Meaning
RAMREMAP_RESET	0x11	Remap RAM to Address 0 and Reset
DOWNLOAD_INIT	0x14	Initialize for RAM download from host to TMF8820/21/28
RAM_BIST	0x2A	Build in self test of RAM (pattern test)
I2C_BIST	0x2C	Build in self test of I^{2}C RAM (pattern test)
W_RAM	0x41	Write RAM Region (Plain = not encoded into e.g. Intel Hex Records)

Command	Value	Meaning
ADDR_RAM	0x43	Set the read/write RAM pointer to a given address

RAMREMAP_RESET = Execute Program Downloaded to RAM

This command remaps the RAM to address 0 and performs a System reset. Before executing this command, set powerup_select = 2.

Command is performed immediately without any delay.

After this the application that is located in RAM will be running. If there is no valid application you will need to do a HW reset (toggle enable pin or power cycle).

Figure 142:
RAMREMAP_RESET

Address	Value	Meaning
BL_CMD_STAT	0x11	REMAP RAM to 0 and RESET
BL_SIZE	0	No parameters
BL_CSUM	0xEE	

DOWNLOAD_INIT

This command is used to initialize the download HW for secure devices.

Figure 143:
DOWNLOAD_INIT

Address	Value	Meaning
BL_CMD_STAT	0x14	Initialize the HW for download from host to TMF8820/21/28 RAM
BL_SIZE	1	
BL_DATA0	0..0xFF	Seed
BL_CSUM	0..0xFF	

RAM_BIST

This command is to perform a RAM pattern test on the main RAM region.

Figure 144:
RAM_BIST

Address	Value	Meaning
BL_CMD_STAT	0x2A	Start pattern testing on the RAM
BL_SIZE	0	
BL_CSUM	0xD5	

BL_CMD_STAT will report pass / fail of the test.

I2C_BIST

This command is to perform a RAM pattern test on the I^2C RAM region.

Figure 145:
I2C_BIST

Address	Value	Meaning
BL_CMD_STAT	0x2C	Start pattern testing on the I^2C RAM
BL_SIZE	0	
BL_CSUM	0xD3	

During execution of this test cpu_ready=0. Wait until cpu_ready=1 and then BL_CMD_STAT will report pass / fail of the test.

W_RAM

This command writes the given data to a defined RAM region. Note that the RAM pointer has first to be set by the command ADDR_RAM. After the command is successfully executed, the RAM pointer will point to the first byte after the written region.

Figure 146:
W_RAM

Address	Value	Meaning
BL_CMD_STAT	0x41	Write to main RAM
BL_SIZE	0..0x80	Number of bytes to be written
BL_DATA0	0..0xFF	1st byte to be written
BL_DATA1	0..0xFF	2nd byte to be written
…		

Address	Value	Meaning
BL_DATA127	0..0xFF	128th byte to be written (only if size was 0x80)
BL_CSUM	0..0xFF	The CSUM comes immediately after the data.

ADDR_RAM

This command is to specify the RAM pointer location for the next R_RAM or W_RAM command.

Figure 147:
ADDR_RAM

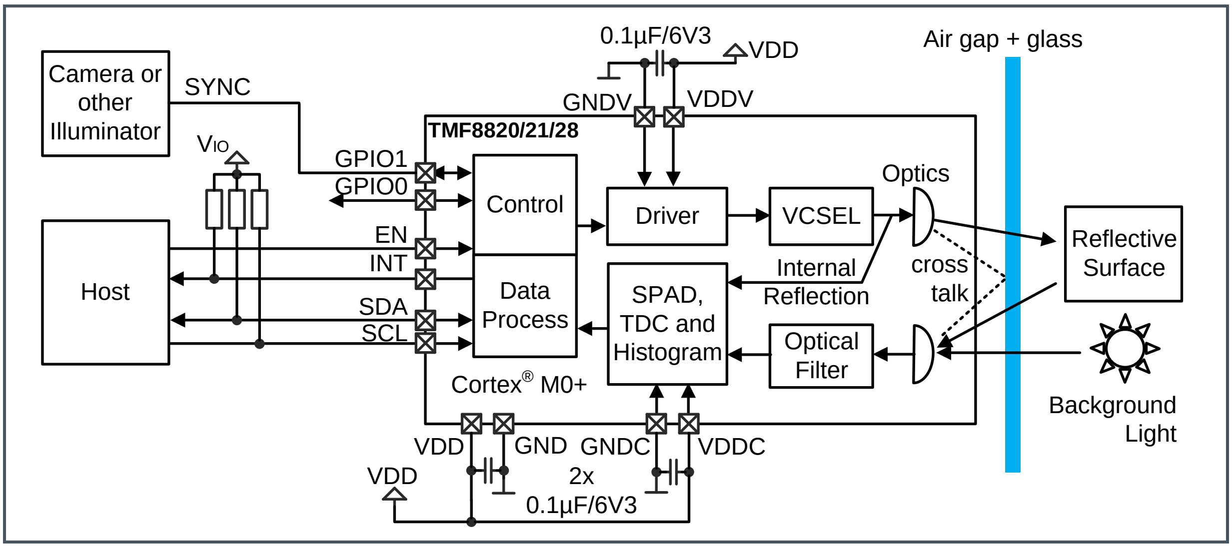
Address	Value	Meaning
BL_CMD_STAT	0x43	Specify the address of the next RAM read or write.
BL_SIZE	2	
BL_DATA0	0..0xFF	LSB of address in RAM
BL_DATA1	0..0xFF	MSB of address in RAM
BL_CSUM	0..0xFF	

9 Application Information

9.1 Schematic

The TMF8820/21/28 needs only 3 small 0402 external capacitors for operation:

Figure 148:
TMF8820/21/28 Application Schematic



The SYNC signal connected to GPIO1 can be used to immediately interrupt the TMF8820/21/28 VCSEL operation if the high power illuminator is operating or to sync to a camera operation. Ensure that SYNC does not exceed the VDD supply of TMF8820/21/28 as otherwise an internal protection diode will start conducting. On SYNC assertion, the VCSEL is immediately switched off (typically after 10 µs), on SYNC de-assertion the VCSEL operation is resumed.

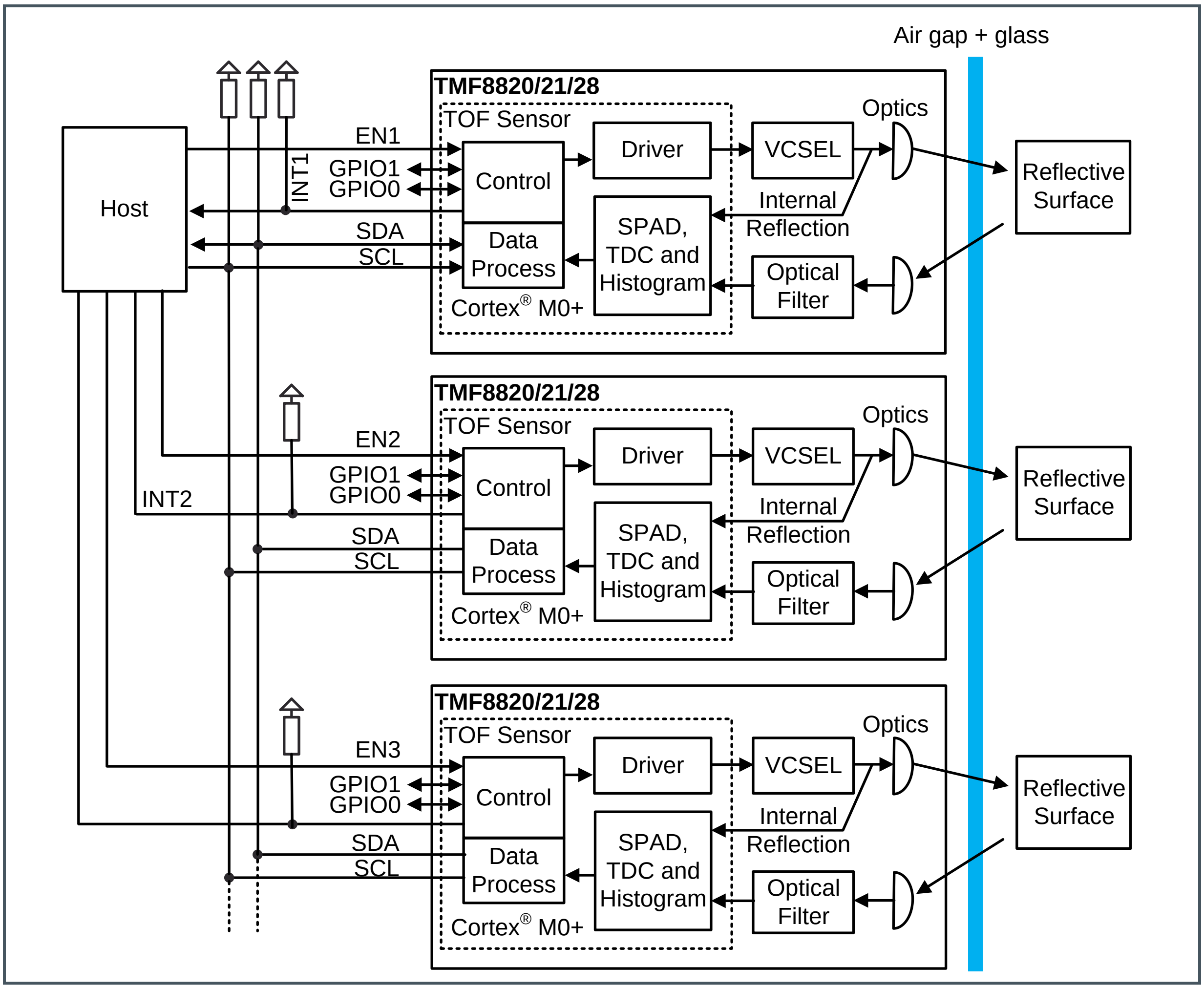
GPIO0 can be used as a general GPIO output signal.

The signals INT/SDA/SCL need an external pull-up resistor to the VIO supply (typically 1.8 V).

9.1.1 Operating Several TMF8820/21/28 Devices on a Single I²C Bus

Several TMF8820/21/28 devices can share a single I²C bus if there are dedicated enable (EN) connections to each of these devices.

Figure 149:
Sharing a Single I²C Bus for Operating Several TMF8820/21/28s



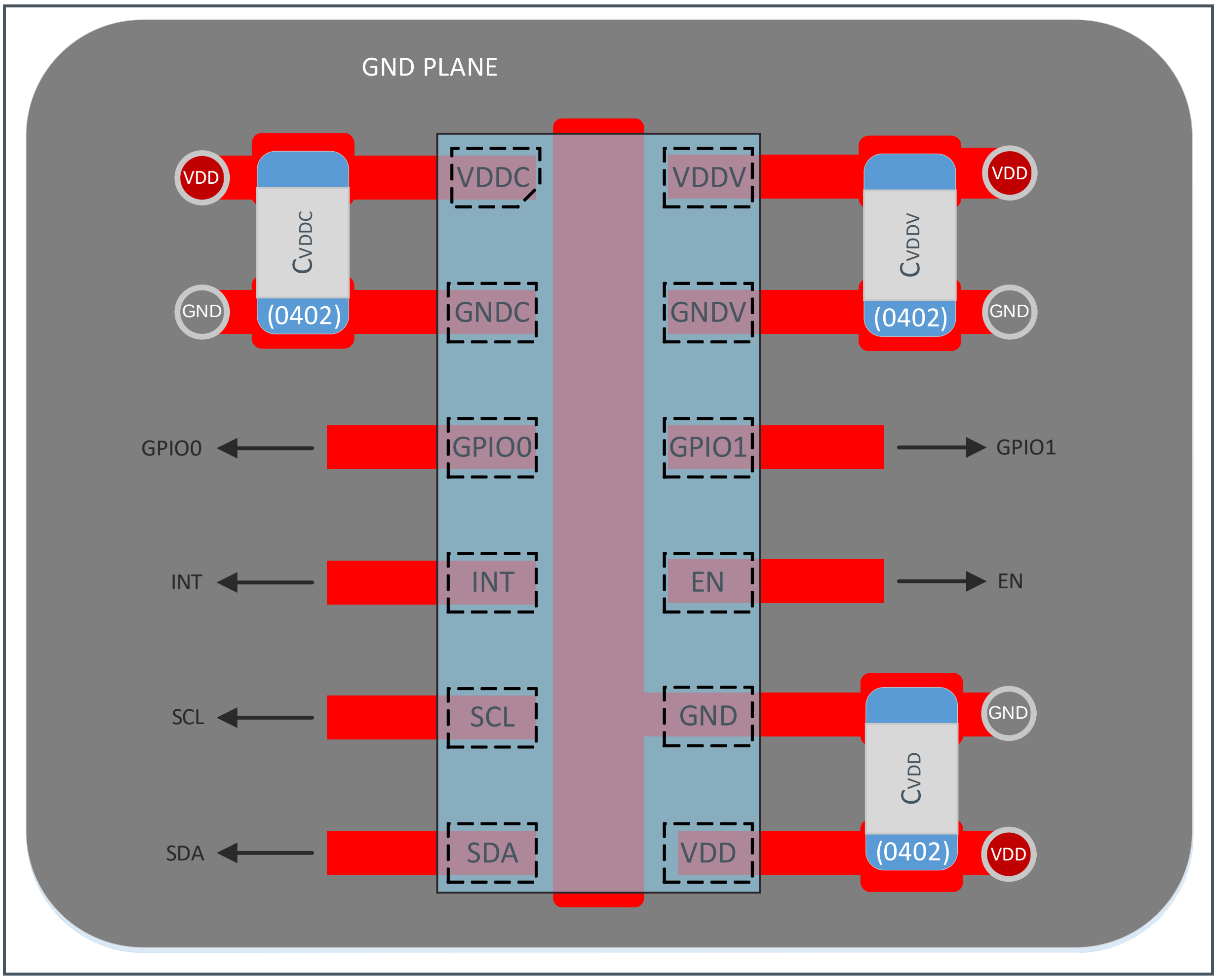
The procedure to initialize the devices to different I²C addresses is as follows:

1. Set EN1=0, EN2=0, EN3=0 (reset all devices)
2. Set EN1=1
3. Download firmware to first TMF8820/21/28
4. Reprogram I²C address for first TMF8820/21/28 using cmd_stat = CMD_I2C_SLAVE_ADDRESS where 7bit_slave_address(0x3B) = I²C address for first TMF8820/21/28; set gpio_change_mask = 0 and gpio_change_value = 0.
5. Set EN2=1

6. Download firmware to second TMF8820/21/28
7. Reprogram I^{2}C address for second TMF8820/21/28 using cmd_stat = CMD_I2C_SLAVE_ADDRESS where 7bit_slave_address(0x3B) = I^{2}C address for second TMF8820/21/28; set gpio_change_mask = 0 and gpio_change_value = 0.
8. Set EN3=1
9. Download firmware to third TMF8820/21/28
10. Reprogram I^{2}C address for third TMF8820/21/28 using cmd_stat = CMD_I2C_SLAVE_ADDRESS where 7bit_slave_address(0x3B) = I^{2}C address for third TMF8820/21/28; set gpio_change_mask = 0 and gpio_change_value = 0.
11. If there are further devices, repeat last three steps accordingly.

9.2 PCB Layout

Figure 150:
PCB Layout Recommendation



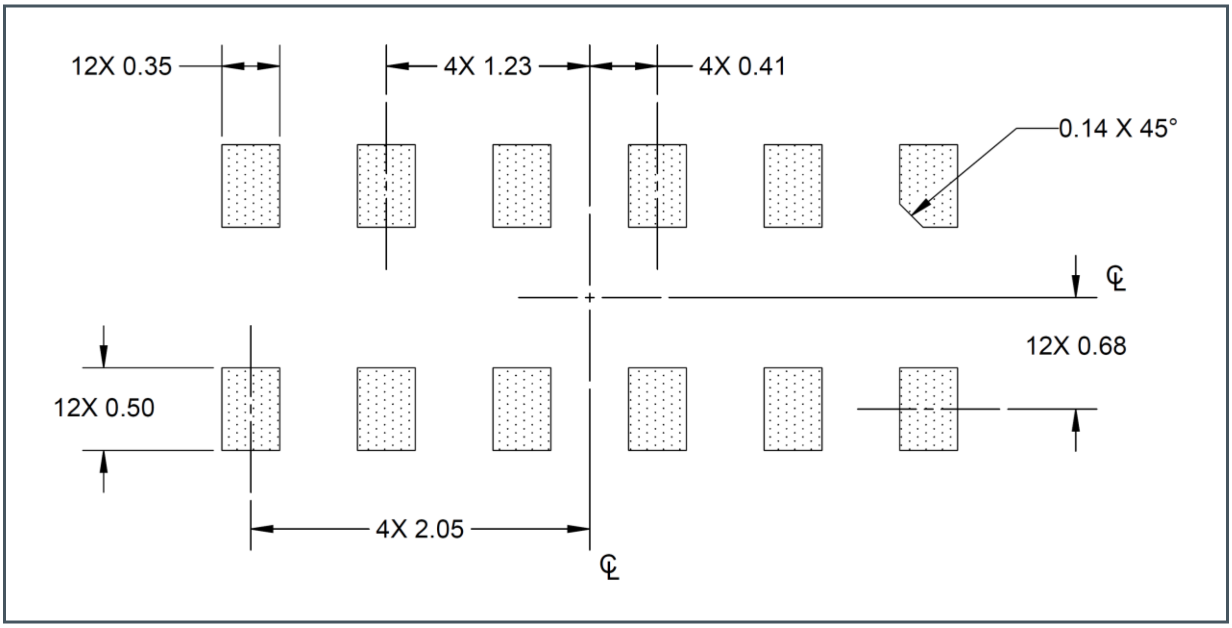
9.3 External Components

The TMF8820/21/28 only need three small 0402 sized capacitors for operation. Use GRM155R70J104KA01 (0402 X7R 0.1 µF 6.3 V) or capacitors with same or better performance for CVDDC, CVDD and CVDDV.

Add pull-up resistors (e.g. 10 kΩ) on pins SCL, SDA and INT.

9.4 PCB Pad Layout

Figure 151:
PCB Pad Layout



(1) All linear dimensions are in millimeters.
(2) Dimension tolerances are 0.05 mm unless otherwise noted.
(3) This drawing is subject to change without notice.

Use the PCB pad layout as a recommendation only. The actual pad layout shall be optimized for the customer production line.

9.5 Software Drivers

ams OSRAM recommends to use one of the available software drivers to operate the TMF8820/21/28. The drivers are available from the **ams** website:

- For TMF8820 see https://ams.com/tmf8820
- For TMF8821 see https://ams.com/tmf8821
- For TMF8828 see https://ams.com/tmf8828

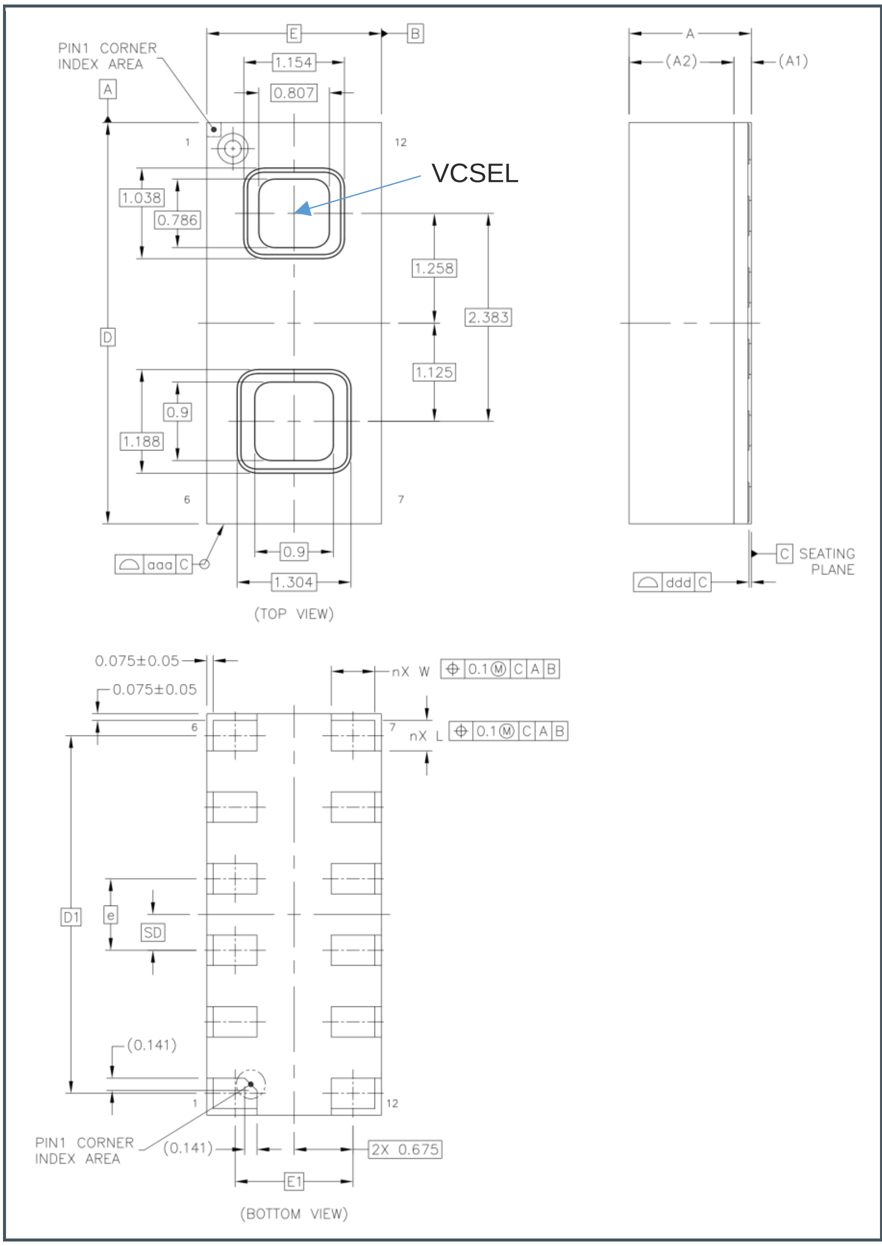
There are following drivers available:

Figure 152:
Available Drivers

Type	File	Explanation
Linux	TMF882x_Driver_Linux_v*.zip and TMF882x_Driver_Linux_Source_v*.zip	Use for any Linux system (e.g. Android) where the driver is running on the application processor. This is the driver running on TMF882x evaluation kit.
SDK	TMF882x_Driver_SDK_Source_v*.zip	Driver and several examples for using of the TMF8820/21/28 bundled inside a software development kit – the driver works out of the box using the tmf882x-mcu-shield-evm boards and an NXP LPC55S69-EVK, but should make porting to other hardware platforms easier.
MCU	TMF882x_Driver_MCU_Source_v*.zip	MCU driver – sometimes referenced as bare metal driver – the hardware functions for executing the I^2C routines can be easily replaced to simply port this driver to systems without operating system or systems not running Linux

10 Package Drawings & Markings

Figure 153:
OLGA12 Package Outline Drawing



Ref.	Min	Nom	Max
A	1.3	1.4	1.5
A1		0.2	REF
A2		1.2	REF
D		4.6	BSC
E		2	BSC
W	0.45	0.5	0.55
L	0.3	0.35	0.4
e		0.82	BSC
n		12	
D1		4.1	BSC
E1		1.35	BSC
SD		0.41	BSC
aaa		0.1	
ddd		0.08	

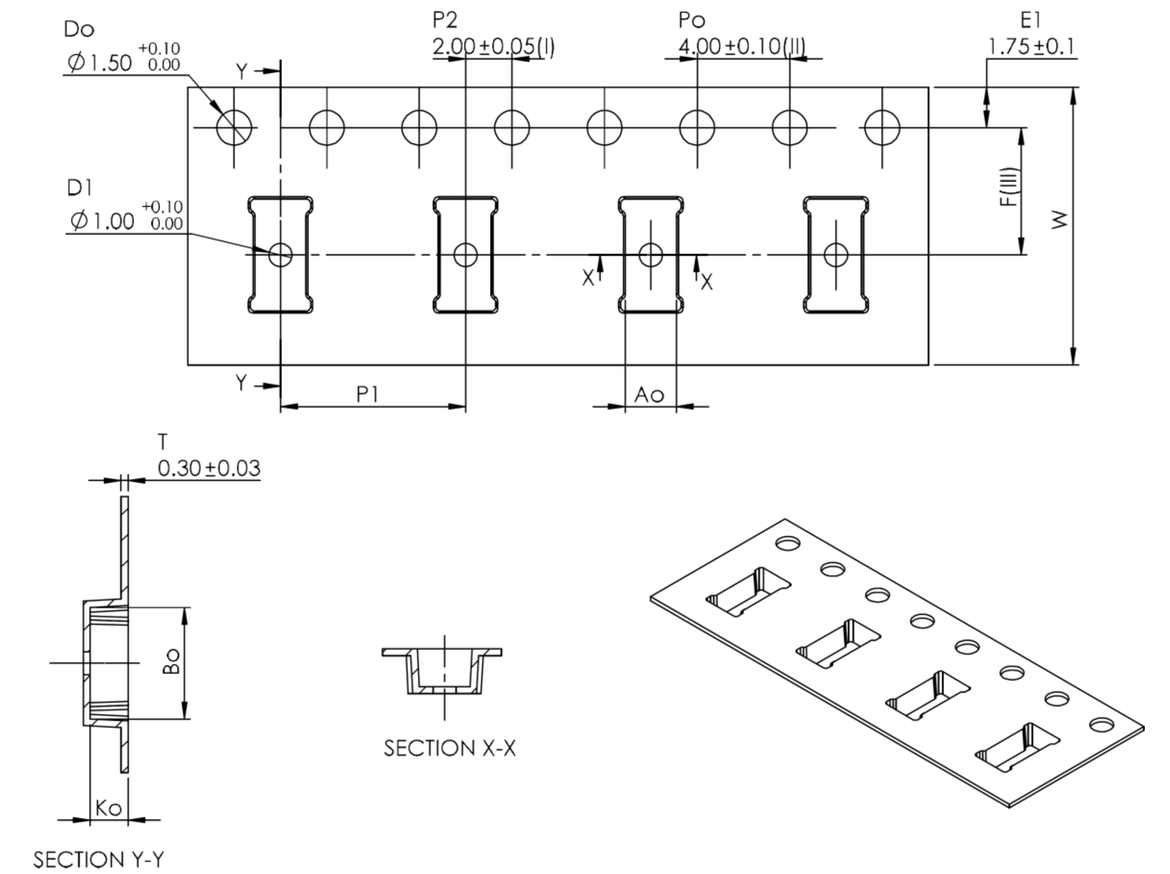
RoHS

Green

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) n is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.
(6) 8-digit tracecode only on bottom side of the package.

11 Tape & Reel Information

Figure 154:
Tape and Reel Drawing



Ao	2.20 +/-0.05
Bo	4.85 +/-0.05
Ko	1.65 +/-0.10
F	5.50 +/-0.05
P1	8.00 +/-0.10
W	12.00 +0.30/-0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

(1) All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
(2) The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
(3) Symbols on drawing A0, B0, and K0 are defined in ANSI EIA Standard 481-B 2001.
(4) There are two reel sizes available (see section Ordering Information)
i) 7'' reels: Each reel is 7 inch in diameter and contains 500 parts.
ii) 13'' reels: Each reel is 13 inch in diameter and contains 4000 parts.
(5) ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
(6) In accordance with EIA standard, device pin 1 is located next to sprocket holes in the tape.
(7) This drawing is subject to change without notice.

12 Soldering & Storage Information

12.1 Soldering Information

The package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components shall be limited to a maximum of three passes through this solder reflow profile.

Figure 155:
Solder Reflow Profile Graph

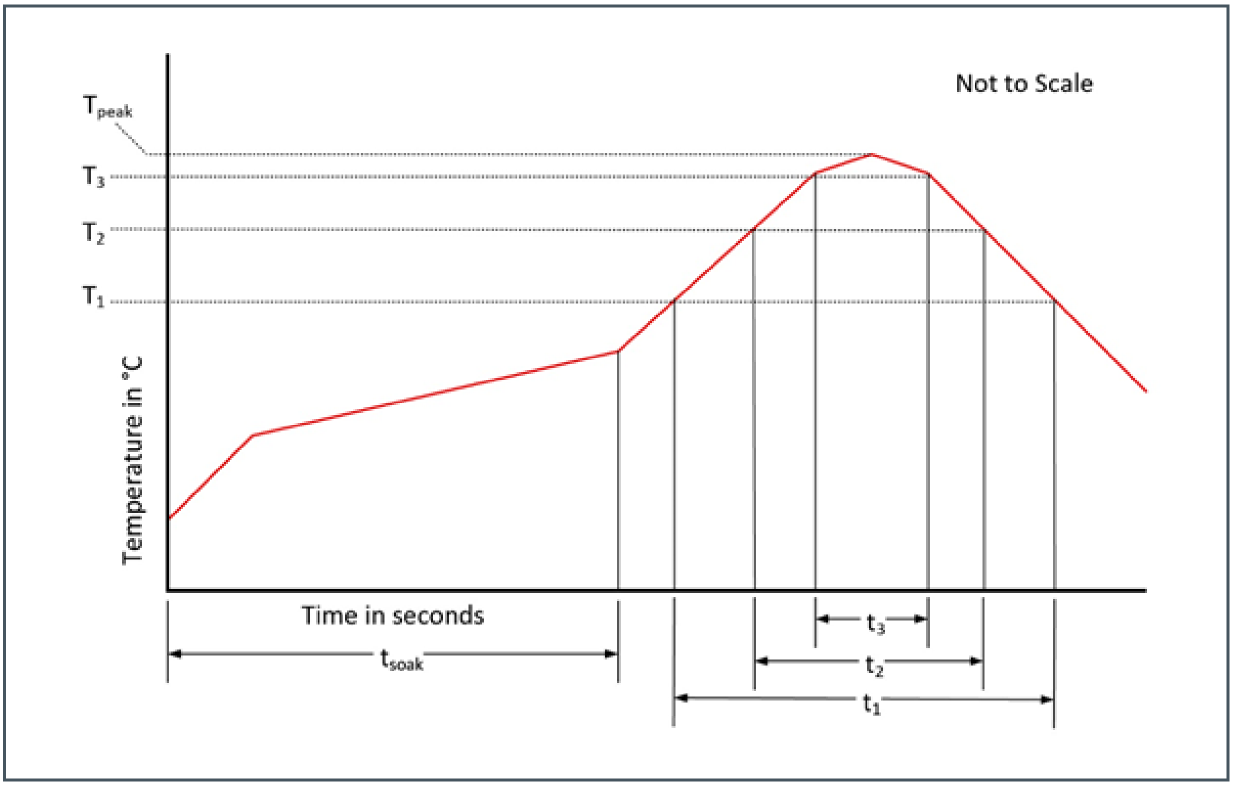


Figure 156:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T_1)	t_1	Max 60 s
Time above 230 °C (T_2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

12.2 Storage Information

12.2.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90 %

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30 °C
- Relative Humidity: <60 %

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

13 Laser Eye Safety

The TMF8820/21/28 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC / EN 60825-1:2014. This applies to the stand-alone device and the included software supplied by ams OSRAM. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions. Use outside of the recommended condition or any physical modification to the module during development could result in hazardous levels of radiation exposure.

Figure 157:
Laser Eye Safety Certificate

Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Example: Adding a converging lens on top of the TMF8820/21/28

14 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v5-00	Page
Used 1 MHz for firmware download	11
Minor updates with additional information (ranging flow in time multiplex, reference for latest firmware, timings in 8x8 mode, customized SPAD map creation)	19, 21, 22, 25
Added short range high accuracy mode	30
Removed live_gpio register	38
Added active_range register	38, 53
Added spread_spectrum	40, 48, 74
Clarified timing for readout of register appid, minor, patch and build	42, 46
Explained bl_cmd_stat error codes	82
Update software drivers and added SDK	91

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal Information

Devices sold by ams-OSRAM AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams-OSRAM AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams-OSRAM AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams-OSRAM AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams-OSRAM AG for each application. This product is provided by ams-OSRAM AG "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams-OSRAM AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams-OSRAM AG rendering of technical or other services.

RoHS Compliant & ams Green Statement

RoHS Compliant: The term RoHS compliant means that ams-OSRAM AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment EU 2015/863), including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams-OSRAM AG knowledge and belief as of the date that it is provided. ams-OSRAM AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams-OSRAM AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams-OSRAM AG and ams-OSRAM AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Headquarters
ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

Please visit our website at www.ams.com
Buy our products or get free samples online at www.ams.com/Products
Technical Support is available at www.ams.com/Technical-Support
Provide feedback about this document at www.ams.com/Document-Feedback
For sales offices, distributors and representatives go to www.ams.com/Contact
For further information and requests, e-mail us at ams_sales@ams.com