DDR4 LONGDIMM

4GB 1Rank*8 PC4-19200U-17

PN:KMKU4G8582400

DESCRIPTION

This document describes 512M x 64 one ranks 4GB DDR4-2400 CL17 1.2v SDRAM unbuffered DIMM product.

The product is based on 8C 512M x8-bit DDR4 FBGA components. The SPD is programmed follow JEDEC standard for 2400Mbps timing of 17-17-17 at 1.2v low power.

This product design specification reference JEDEC standard(*No. 21C DDR4 SDRAM UDIMM Design Specification*) raw-card A.

This 288-pin DIMM uses gold contact fingers and requires +1.2v power supply .

Features

•VDD = VDDQ = 1.2V ±60mV
• VPP = 2.5V, –125mV/+250mV
• On-die, internal, adjustable VREFDQ generation
• 1.2V pseudo open-drain I/O
• TC of 0°C to 85°C
– 64ms, 4096 cycle refresh at 0°C to 85°C
• 16 internal banks (x4, x8): 4 groups of 4 banks each
• 8n-bit prefetch architecture
• Programmable data strobe preambles
• Data strobe preamble training
• Command/Address latency (CAL)
• Multipurpose register READ and WRITE capability
• Write and read leveling
• Self refresh mode
• Low-power auto self refresh (LPASR)
• Temperature controlled refresh (TCR)
• Fine granularity refresh
• Self refresh abort
• Maximum power saving
• Output driver calibration
• Nominal, park, and dynamic on-die termination(ODT)
• Data bus inversion (DBI) for data bus
• Command/Address (CA) parity
• Databus write cyclic redundancy check (CRC)
• Per-DRAM addressability
• Post package repair (PPR) and soft post package repair (sPPR) modes
• JEDEC JESD-79-4 compliant

Addressing

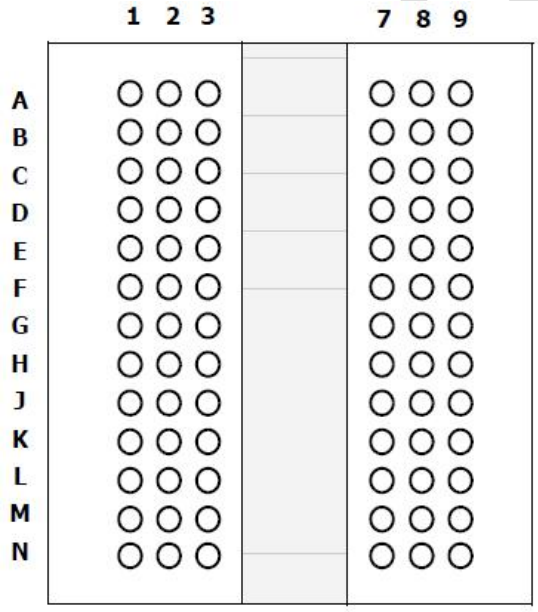
Parameter	512Meg x 8bit
Number of bank groups	4
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	32K (A[15:0])
Column addressing	1K (A[9:0])
Page size	1KB

Ordering Information

Memory Type	Density	Organization	Component Composition	#of ranks
DDR4 LONGDIMM 4G 2400	4GB	512Mx64bit	512X8 8c	1

x8 Package Ball out (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

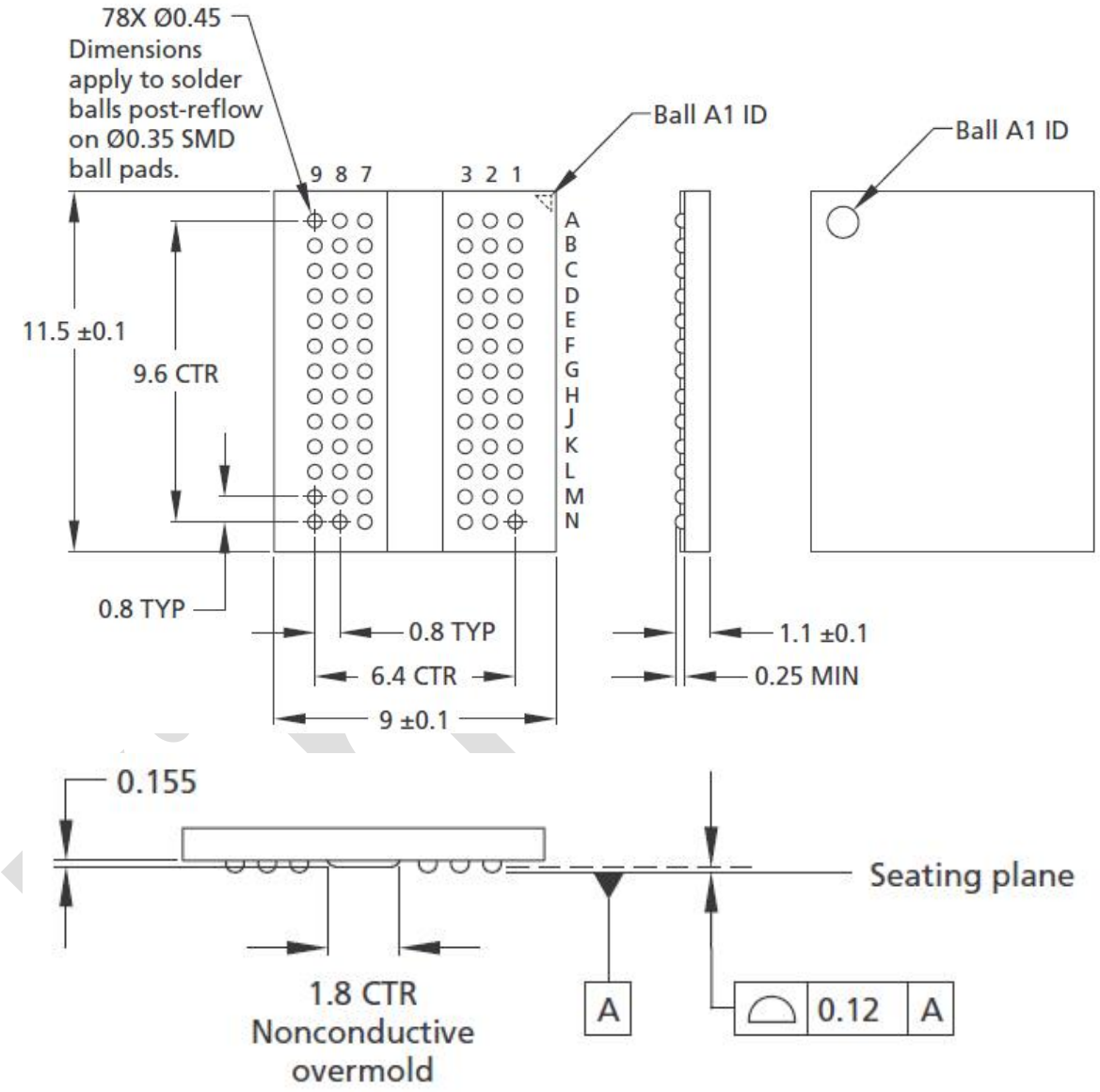


(Top View: See the balls through the Package)

○ Populated ball
+ Ball not populated

Package Dimensions

78Ball Fine Pitch Ball Grid Array Outline



Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
1	NC	145	NC	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	DM0_n,DBI_n,NC	151	VSS	78	EVENT_n	222	PARITY
8	NC	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	CS0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DM1_n,DBI1_n,NC	162	VSS	89	CS1_n	233	VDD
19	NC	163	DQS1_c	90	VDD	234	NC
20	VSS	164	DQS1_t	91	ODT1	235	NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	NC	237	NC,CS3_n,C1
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	DM4_n,DBI4_n,NC	243	VSS
29	DM2_n,DBI2_n,NC	173	VSS	100	NC	244	DQS4_c
30	NC	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45

37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Lable	Pin	Back Side Pin Label
39	VSS	183	DQ25	110	DM5_n,DBI5_n,NC	254	VSS
40	DM3_n,DBI3_n,NC	184	VSS	111	NC	255	DQS5_c
41	NC	185	DQS3_c	112	VSS	256	DQS3_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4,NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5,NC	119	DQ48	263	VSS
49	CB0,NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1,NC	121	DM6_n,DBI6_n,NC	265	VSS
51	DM8_n,DBI_n,NC	195	VSS	122	NC	266	DQS6_c
52	NC	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6,NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7,NC	126	DQ50	270	VSS
56	CB2,NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3,NC	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	ACT_n	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	DM7_n,DBI7_n,NC	276	VSS
62	ACT_n	206	VDD	133	NC	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12/BC_n	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A12/BC_n	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address input	SCL	I²C serial bus clock for SPD/TS and register
BA0, BA1	SDRAM bank select input	SDA	I²C serial data line for SPD/TS and register
BG0, BG1	Regsiter bank group select input	SA0–SA2	I²C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12 V	Optional Power Supply on socket but not used on RDIMM
CKE0, CKE1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0–CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. Address A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Input/Output Pin Functional Descriptions

Symbol	Type	Polarity	Function
CK0/#CK0 CK1/#CK1	IN		Clock: CK_t and CK_c are differential clock inputs. All address and control inputsignals are sampled on the
CKE0, CKE1	Input		Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input		Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS2_n and CS3_n are not used on UDIMMs.
C0, C1, C2	Input		Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. Not used on UDIMMs.
ODT0, ODT1	Input		On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM
ACT_n	Input		Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input		Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example,for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output		Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations.TDQS is not valid for UDIMMs.
BG0, BG1	Input		Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessedduring a MRS cycle. x4/x8 SDRAM configurations have BG0 and BG1. x16 based SDRAMs only have BG0.
BA0, BA1	Input		Bank Address Inputs: BA0 - BA1 define to which bankan Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input		Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write

			commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additionalfunctions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 SDRAM configuration.
A10 / AP	Input		Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If onlyone bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input		Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Symbol	Type	Polarity	Function
RESET_n	CMOS Input		Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output		Data Input/ Output: Bi-directional data bus. If CRC isenabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output		Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, toprovide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output		Termination Data Strobe: TDQS_t/TDQS_c are not valid for UDIMMs.
PARITY	Input		Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output		Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on-going DRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.
NC			No Connect: No on DIMM electrical connection is present.
VDD1	Supply		Power Supply: 1.2 V +/- 0.06 V
VSS	Supply		Ground
VPP	Supply		DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VTT2	Supply		Power Supply for termination of Address, Command and Control, VDD/2.
12 V	Supply		12 V supply not used on UDIMMs.
VDDSPD	Supply		Power supply used to power the I2C bus on the SPD-TSE.
VREFCA	Supply		Reference voltage for CA

Note:

1. For PC4 VDD 1.2V. For PC4L VDD is TBD.
2. For PC4 VTT is 0.06V. For PC4L VTT is TBD.

AC & DC Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	℃	1,2

Notes

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85ºC under all operating conditions.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.3V~1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3V~1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3V~3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3V~1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	℃	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the

measurement conditions, please refer to JESD51-2 standard.

3. VDD and VDDQ must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

4. VPP must be equal or greater than VDD/VDDQ at all times

DDR4-2400 Speed Bins

Speed Bin		DDR4-2400V		Unit
CL - nRCD - nRP		17-17-17		
Parameter	Symbol	min	max	
Internal read command to first data	t_{AA}	14.16	18.00	ns
Internal read command to first data with read DBI enabled	t_{AA_DBI}	tAA(min) + 3nCK	tAA(max) +3nCK	ns
ACT to internal read or write delay time	t_{RCD}	14.16	-	ns
PRE command period	t_{RP}	14.16	-	ns
ACT to PRE command period	t_{RAS}	32	9 x tREFI	ns
ACT to ACT or REF command period	t_{RC}	46.16	-	ns

PCB

General

* Board size：5250 x 1230 mil ±6 mil
* Thickness：55 ±4 mil
* Panel：5 pieces PCB per panel
* 8-layer board
* Impedance: 40/55 Ohm ±10% (Single-ended), 83/93 Ohm ±15% (Differential).
* Pin count：288 PIN

PCB Material

* Glass Epoxy FR4 LF, .UL 94V-0, BP ML

Plating

*Edge Connector Plating: Nickel Followed by gold

- Nickel Plating Thickness: 120 u" min.
- Surface treatment:
  Gold Plating: 3u" min.
  SMT PAD: average 2~3u".

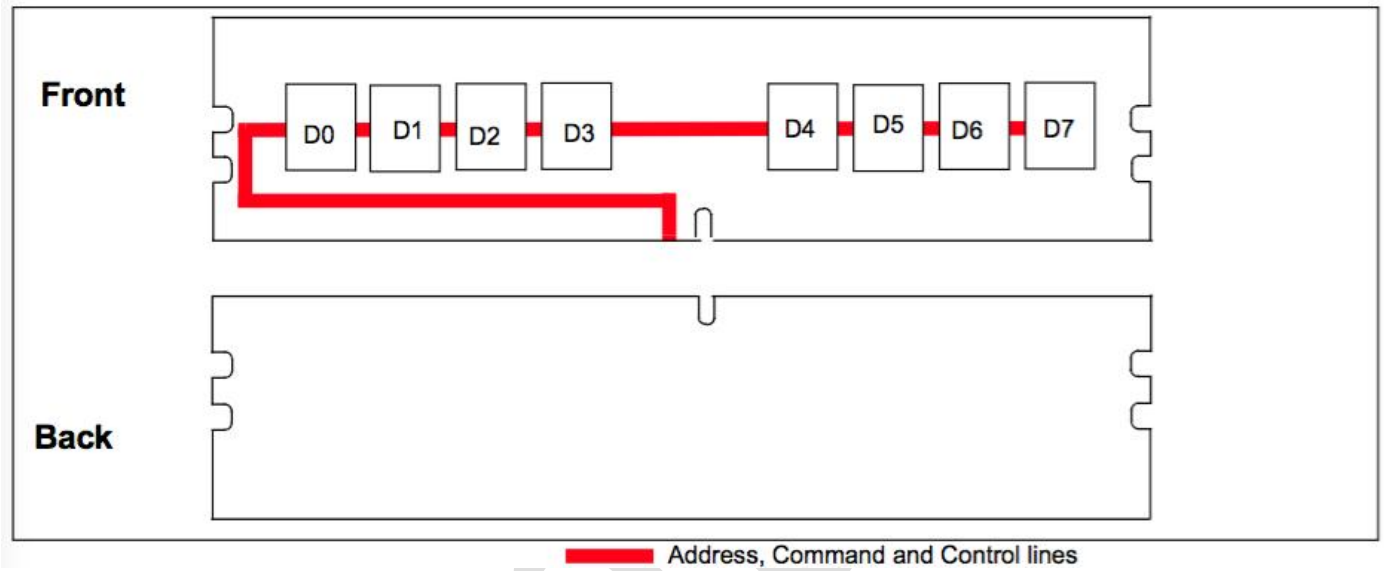
Reference:

*JEDEC Raw Card Version A

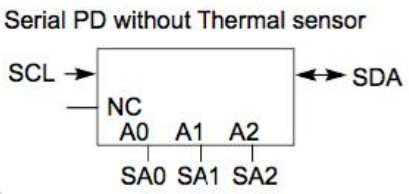
Raw Card	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# of Banks in SDRAM BA/BG	# Address bits row/col
A	4GB	512Mx64	4 Gbit	512 M x 8	8	1	FBGA	1/1	15/10[1]

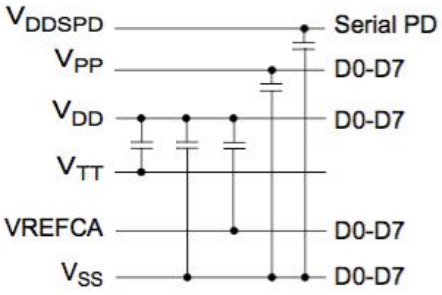
Functional Block Diagram

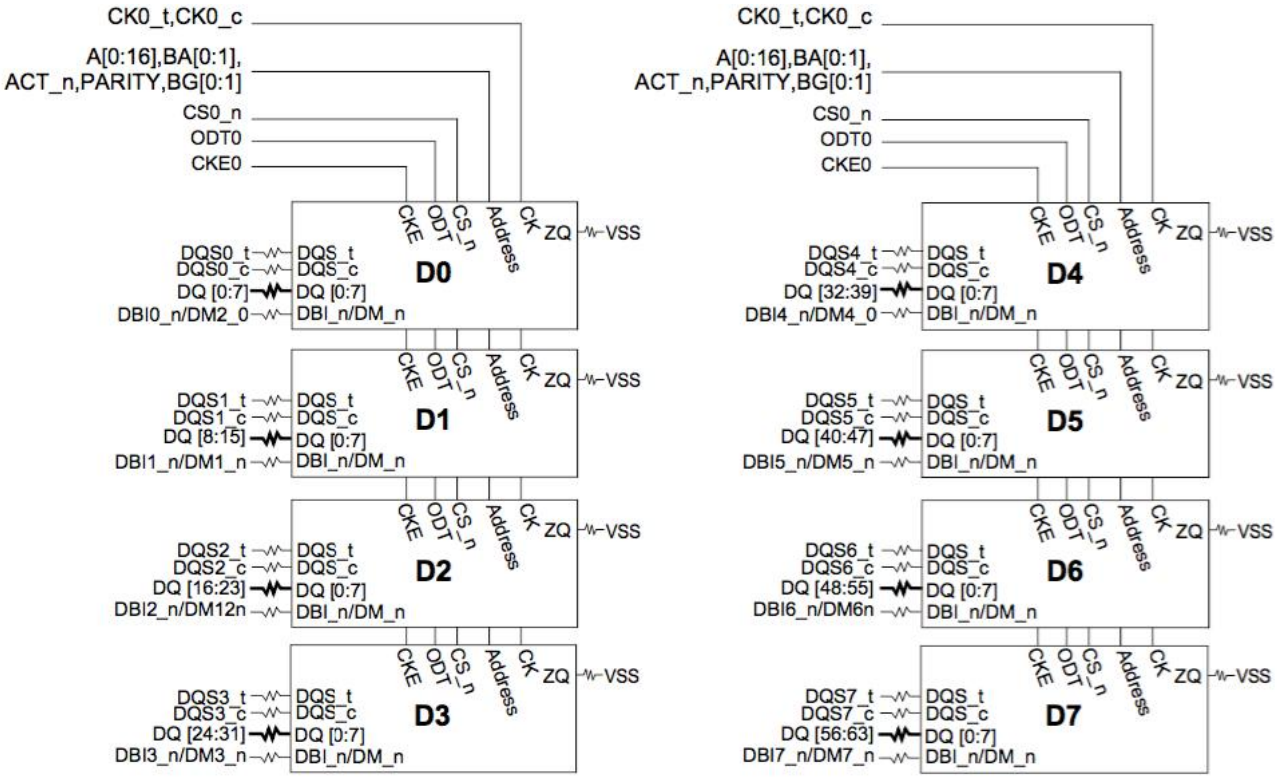
- x64 DIMM, populated as two physical ranks of x8 DDR4 SDRAMs



x64 DIMM, populated as one package rank of x8 DDR4 SDRAMs (Part 2 of 2)



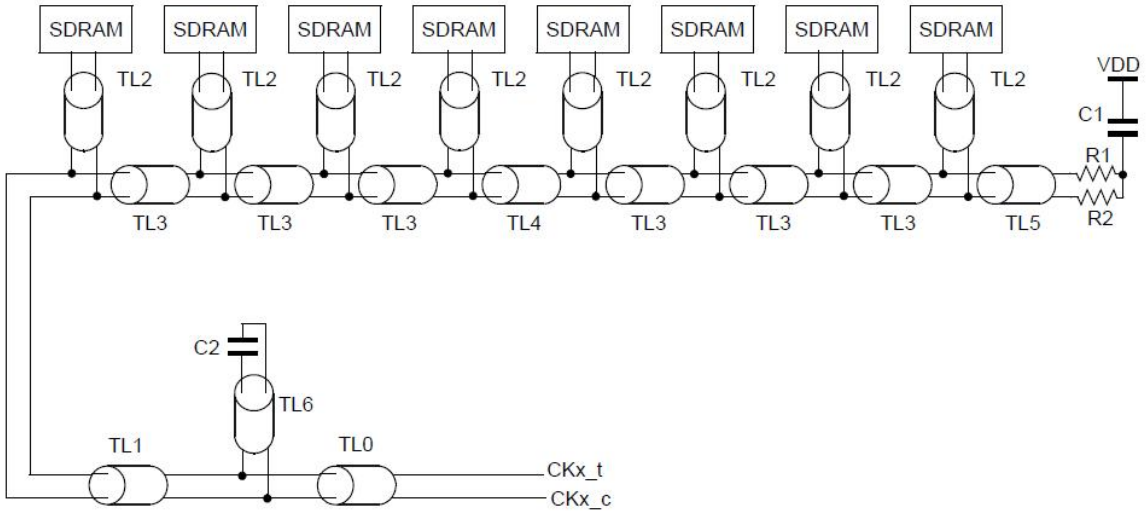




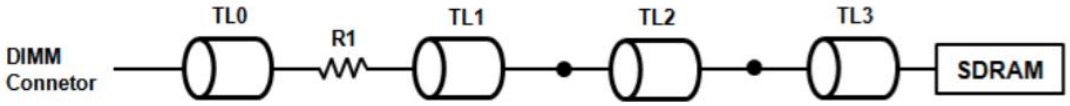
Note 1 Unless otherwise noted, resistor values are 15 ± 5%.

Note 2 ZQ resistors are 240 ± 1%. For all other resistor values refer to the appropriate wiring diagram.

- Net Structure Routing for Clock to SDRAM Loads

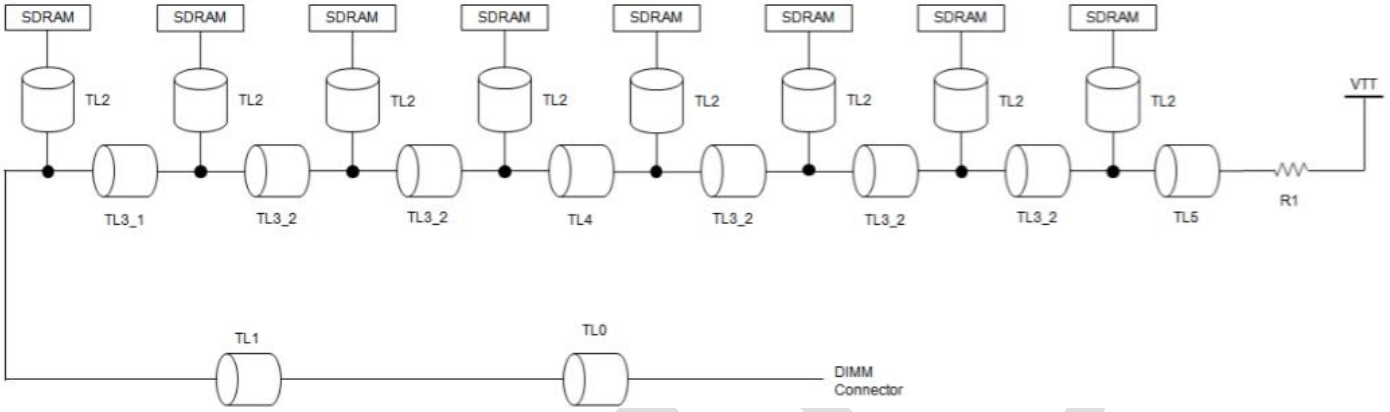


- Net Structure for DQ, DQS_t, DQS_c, DM_n/DBI_n

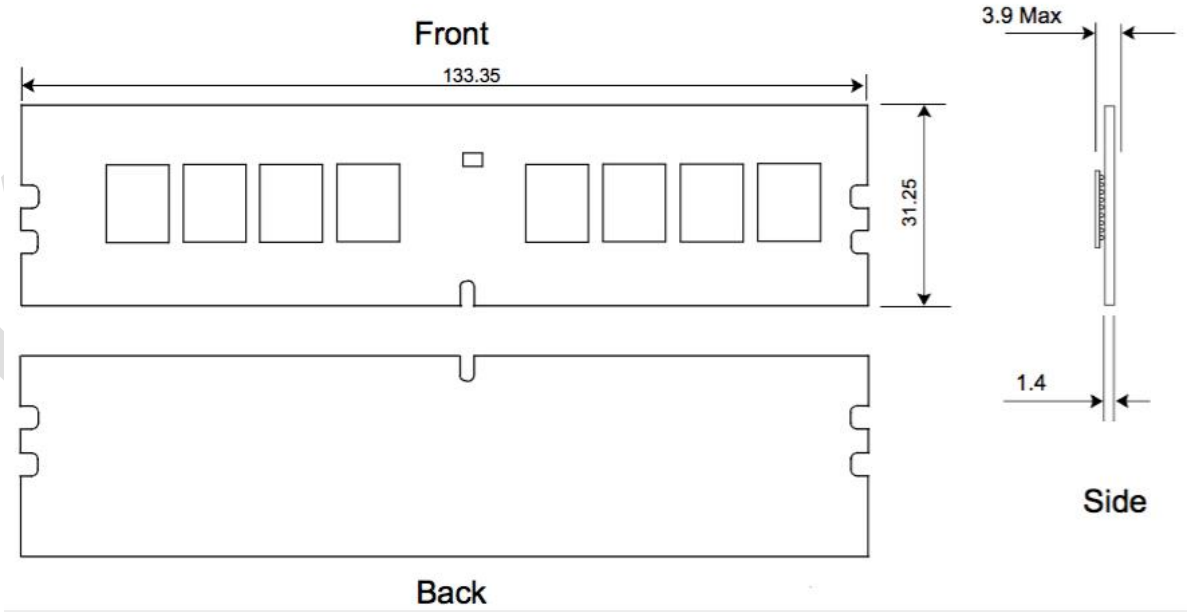


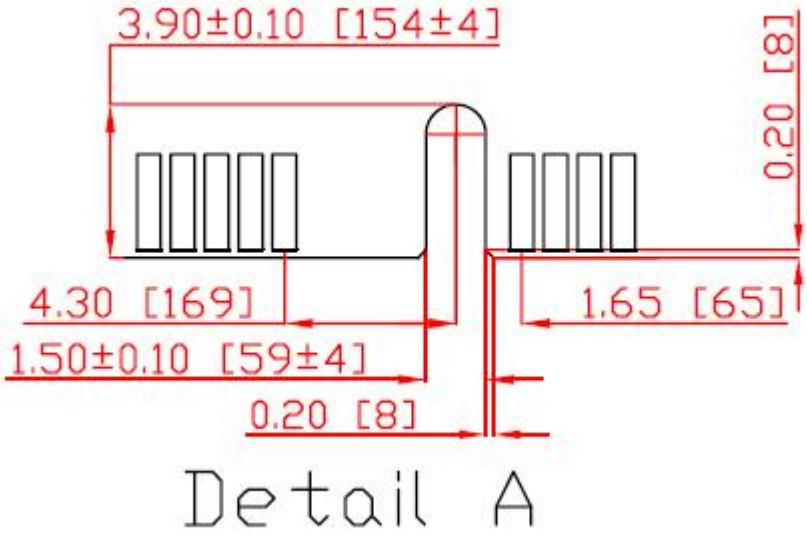
Resistor may be used as a test point

- Address and Command Net Structure Routing

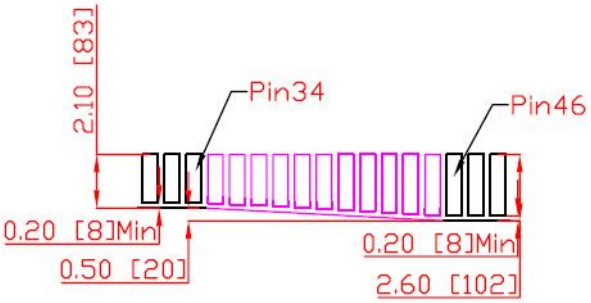


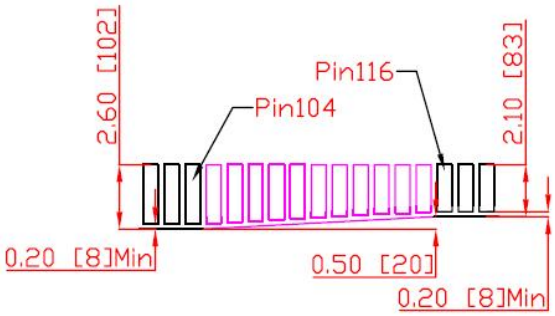
Module Dimensions



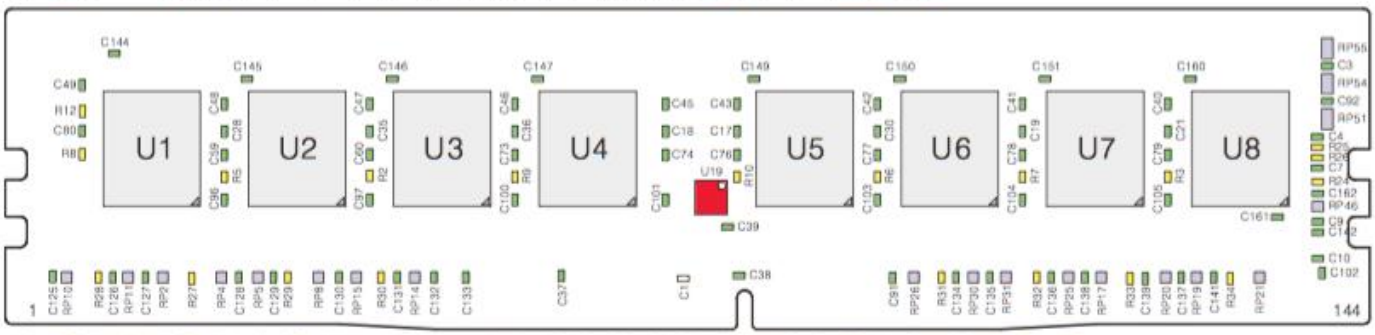

3.90±0.10 [154±4]
0.20 [8]
4.30 [169]
1.65 [65]
1.50±0.10 [59±4]
0.20 [8]

Detail A


2.10 [83]
Pin34
Pin46
0.20 [8]Min
0.50 [20]
0.20 [8]Min
2.60 [102]


2.60 [102]
Pin116
Pin104
2.10 [83]
0.20 [8]Min
0.50 [20]
0.20 [8]Min

TOP SIDE 1-RANK WITHOUT ECC



BOTTOM SIDE 1-RANK WITHOUT ECC