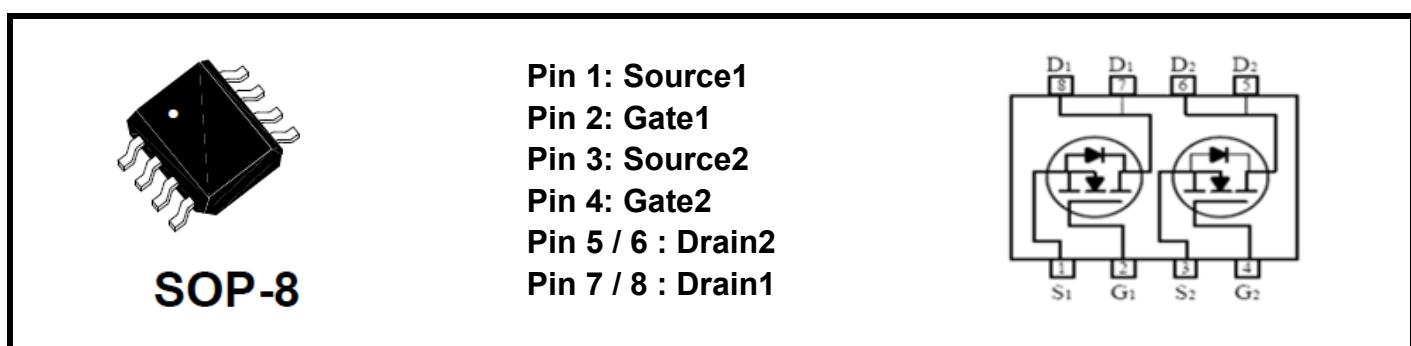


Dual N-Channel Enhancement-Mode MOSFET(20V, 6A)

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{D(on)} (m-ohm) Max
20V	6A	28 @ VGS = 4.5V, ID=6A
		40 @ VGS =2.5V, ID=5.2A

◆ Features

1. Advanced Trench Process Technology.
2. High Density Cell Design for Ultra Low On-Resistance.
3. Lead free product is acquired.
4. Surface mount Package.
5. RoHS Compliant.



◆ Ordering Information

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		2/4	1/3	5/6/7/8	
SM9926PRL	SM9926PRG	SOP-8	G	S	D	Tape Reel
SM9926X X X (1)Package Type (2)Packing Type (3)Lead Free						(1) P: SOP-8 (2) R: Tape Reel (3) G: Halogen Free; L: Lead Free



◆ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current (Continuous) ^a	6	A
I_{DM}	Drain Current (Pulsed) ^b	20	A
P_D	Total Power Dissipation @ $T_A=25^\circ\text{C}$	2.0	W
T_j, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (PCB mounted) ^c	62.5	$^\circ\text{C}/\text{W}$

a:Fused current that based on wire numbers and diameter

b:Repetitive Rating: Pulse width limited by the maximum junction temperature

c:1-in² 2oz Cu PCB board

◆ Electrical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$	-	-	± 100	nA
• On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.6	0.65	1.2	V
$R_{DS(\text{on})}$	Drain-Source On-State Resistance	$V_{GS}=4.5\text{V}, I_D=6.0\text{A}$	-	20	28	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=5.2\text{A}$	-	26	40	
• Dynamic Characteristics^d						
C_{iss}	Input Capacitance	$V_{DS}=8\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	-	522.3	-	pF
C_{oss}	Output Capacitance		-	98.48	-	
C_{rss}	Reverse Transfer Capacitance		-	74.69	-	
• Switching Characteristics^d						
Q_g	Total Gate Charge	$V_{DS}=10\text{V}, I_D=6\text{A}, V_{GS}=4.5\text{V}$	-	6.24	-	nC
Q_{gs}	Gate-Source Charge		-	1.64	-	
Q_{gd}	Gate-Drain Charge		-	1.34	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=10\text{V}, I_D=1\text{A}, V_{GEN}=4.5\text{V}, R_G=6\Omega$	-	10.4	-	nS
t_r	Turn-on Rise Time		-	4.4	-	
$t_{d(off)}$	Turn-off Delay Time		-	27.36	-	
t_f	Turn-off Fall Time		-	4.16	-	
• Drain-Source Diode Characteristics						
I_s	Maximum Diode Forward Current	$V_{GS}=0\text{V}, I_s=1.7\text{A}$	-	-	1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_s=1.7\text{A}$	-	-	1.2	V

Note: Pulse Test: Pulse Width $\leq 300\text{us}$, Duty Cycle $\leq 2\%$

d: Guaranteed by design: not subject to production testing

◆ Characteristics Curve

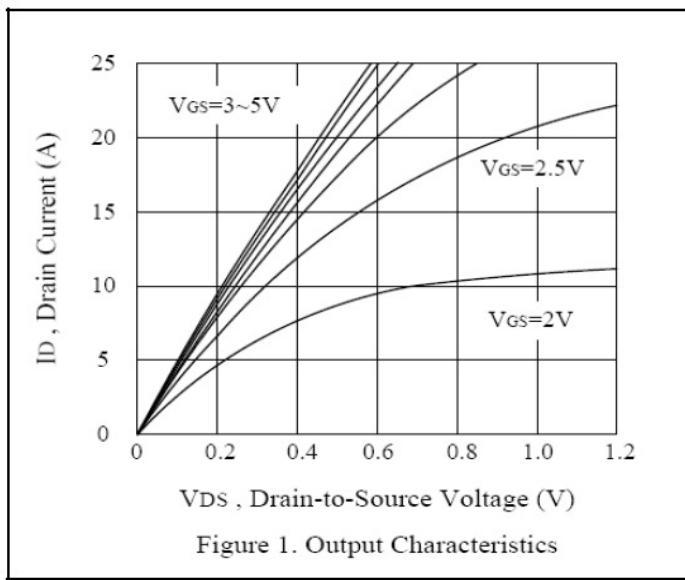


Figure 1. Output Characteristics

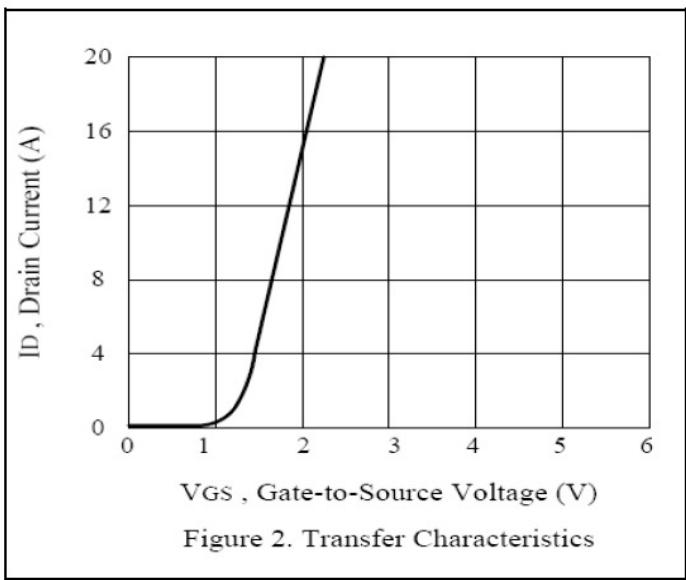


Figure 2. Transfer Characteristics

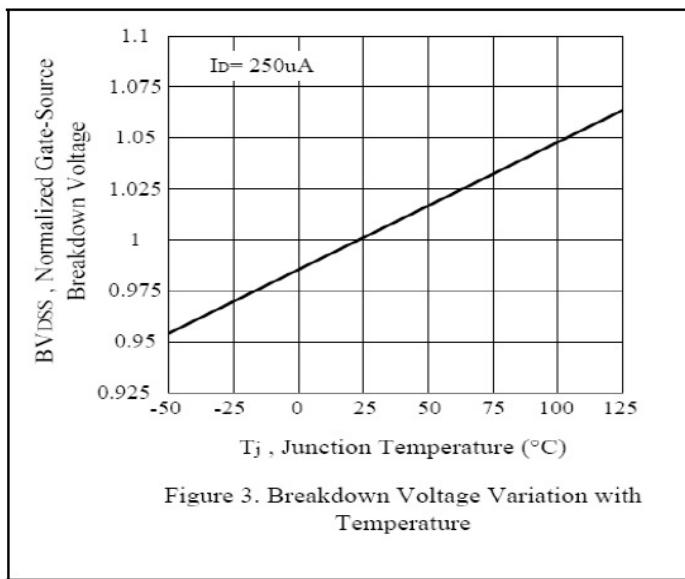


Figure 3. Breakdown Voltage Variation with Temperature

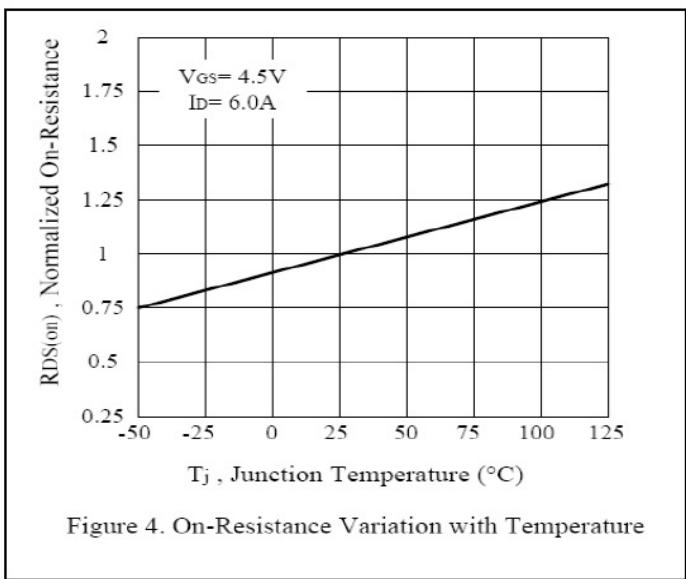


Figure 4. On-Resistance Variation with Temperature

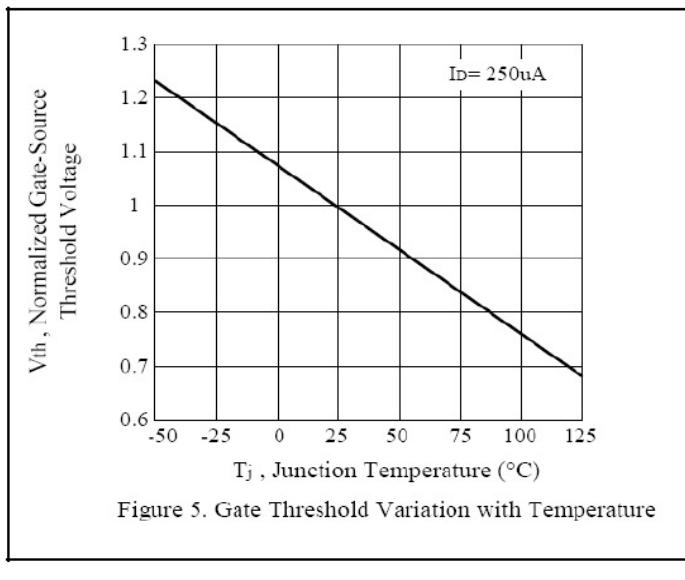


Figure 5. Gate Threshold Variation with Temperature

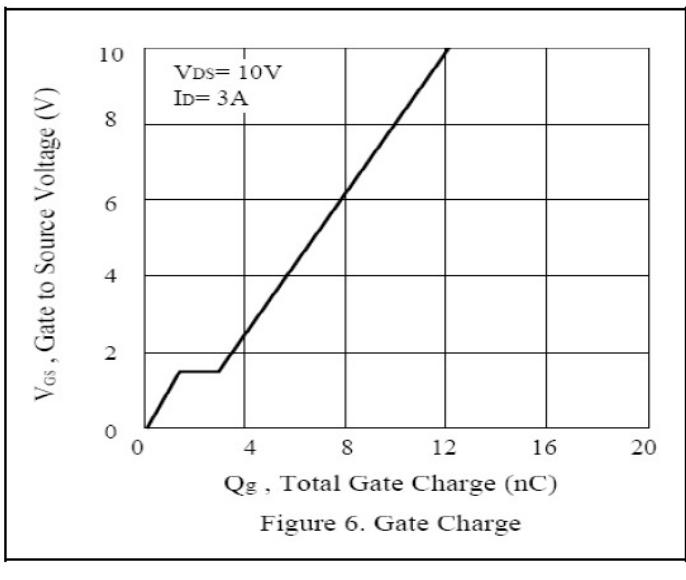


Figure 6. Gate Charge

◆ Characteristics Curve

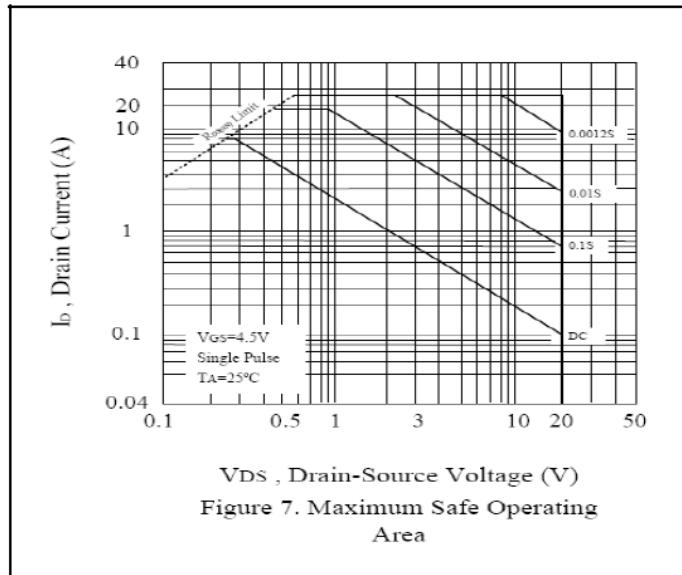


Figure 7. Maximum Safe Operating Area

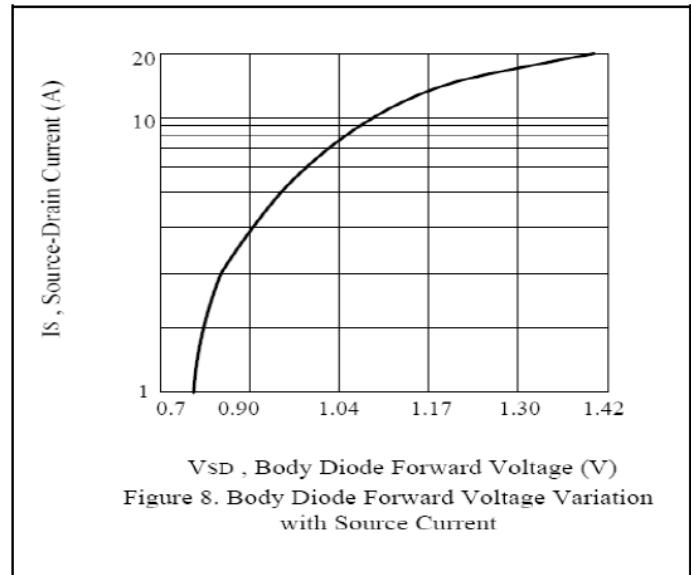


Figure 8. Body Diode Forward Voltage Variation with Source Current

