MT8395 AIoT Application Processor Datasheet

Version: 1.0
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Version History

Version	Date	Description
1.0	2022-02-10	First official release

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1 Introduction

The MT8395 is a highly integrated platform incorporating the following key features:

- Quad-core Arm® Cortex®-A78 processor
- Quad-core Arm Cortex-A55 processor
- Arm Mali™-G57 MC5 3D Graphics Accelerator (GPU) with Vulkan® 1.1, OpenGL ES 3.2 and OpenCL™ 2.2
- Dual-core AI Processor Unit (APU) Cadence® Tensilica® VP6 processor with AI Accelerator (AIA)
- Single-core Cadence HiFi 4 Audio Engine DSP
- LPDDR4X: Up to 16GB, with memory data rate up to LPDDR4X-4266
- Display output supporting 4K60 + 4K60 resolution
- Image processing: 48MP @ 30fps for single camera capture; 16MP + 16MP @ 30fps for dual camera capture
- Video encoding: 4K @ 60 fps with HEVC/H.264
- Video decoding: 4K @ 90 fps with AV1/VP9/HEVC/H.264

Figure 1-1 shows the functional block diagram of the device.

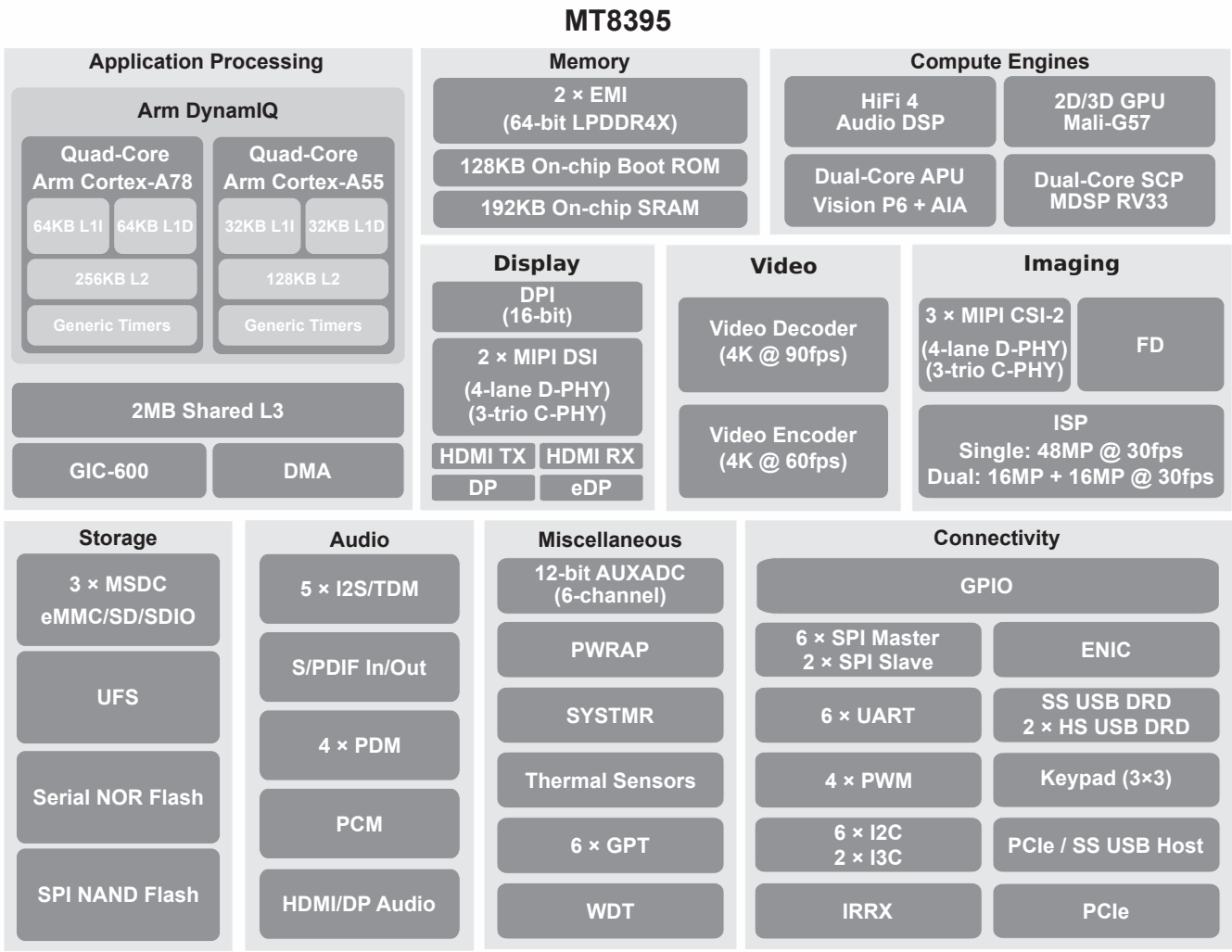


Figure 1-1 Functional Block Diagram

NOTE: Hardware components may work differently on different operating systems.

PRELIMINARY INFORMATION

1.1 Features Overview

Table 1-1 presents a summary of the device feature.

Table 1-1 Device Features

Feature		MT8395
Processors		
Quad-core Arm Cortex-A78	A78	2200 MHz
Quad-core Arm Cortex-A55	A55	2000 MHz
Graphics Accelerator Mali G-57 MC5	GPU	880 MHz
HiFi 4 Digital Signal Processor	DSP	720 MHz
AI Processor Unit	APU	832 MHz
System Companion Processor	SCP	416 MHz
Memory		
External Memory Interface (LPDDR4X)	EMI	Up to 16GB LPDDR4X-4266
Storage		
Memory Card Controller eMMC™/SD®/SDIO	MSDC0	eMMC (1-/4-/8-bit)
	MSDC1	SD Card (1-/4-bit)
	MSDC2	SD/SDIO Card (1-/4-bit)
SPI NAND Flash Interface	SNFI	Yes
Serial NOR Flash Interface	SNOR	Yes
Universal Flash Storage	UFS	Yes (1-lane)
Display		
High-Definition Multimedia Interface Transmitter	HDMITX	Yes (HDMI™ 2.0b)
Digital Display Parallel Interface	DPI	16-bit
DisplayPort Interface	DPTX	Yes (DP 1.4)
Embedded DisplayPort Interface	EDPTX	Yes (eDP 1.4)
MIPI™ Display Serial Interface	DSI0	4-lane D-PHY, or 3-trio C-PHY
	DSI1	4-lane D-PHY, or 3-trio C-PHY
High-Definition Multimedia Interface Receiver	HDMIRX	Yes (HDMI™ 2.0b)
Imaging		
Image Signal Processor	ISP	Single camera: 48MP @ 30fps
		Dual camera: 16MP + 16MP @ 30fps
MIPI Camera Serial Interface 2	CSI0	2 × 4-lane D-PHY
	CSI1	1 × 4-lane D-PHY, or 2 × 2-lane D-PHY, or 1 × 3-trio C-PHY, or 2 × 2-trio C-PHY
Face Detection	FD	Yes
Warp Engine	WPE	Yes
JPEG Encoder	JPEG	Baseline encoding and decoding (250 MP/s)
Video		
Video Encoder	VENC	HEVC/H.264, 4K @ 60 fps
Video Decoder	VDEC	AV1/VP9/HEVC/H.264, 4K @ 90 fps
Audio		
Inter-IC Sound	I2S	4 (2 input, 2 output)
Time Division Multiplexed Interface	TDM	

Feature		MT8395
Pulse Code Modulation	PCM	1
Pulse Density Modulation (Decoder for DMIC)	PDM	4 x stereo
Digital Interface	SPDIF_IN	2
	SPDIF_OUT	1
Connectivity		
Inter-Integrated Circuit	I2C	6
	I3C	2(1)
Universal Asynchronous Receiver/Transmitter	UART	6
Infrared Receiver	IRRX	1
Serial Peripheral Interface	SPI	6 (master mode only)
		2 (slave mode only)
Universal Serial Bus	USB Port 0	SS USB 3.1 Gen1 DRD
	USB Port 1	SS USB 3.1 Gen1 Host(2)
	USB Port 2	USB 2.0 DRD
	USB Port 3	USB 2.0 DRD
KeyPad Scanner	KeyPad	3 × 3
General Purpose I/O pins	GPIO	144
Pulse Width Modulation	PWM	Up to 4
Peripheral Component Interconnect Express	PCIe Port 0	Gen3, 2-lane, RC/EP mode
	PCIe Port 1	Gen2, 1-lane, RC mode(2)
Gigabit Ethernet Network Interface Controller	ENIC	MII/RMII/RGMII
Miscellaneous		
PMIC Interface	PWRAP	Yes
Auxiliary ADC	AUXADC	12-bit, 6-channel
Timers	GPT	5 × 32-bit and 1 × 64-bit
	SYSTMR	64-bit
	WDT(3)	Yes
Thermal Controller	TCSYS	Yes

1. I3C0 and I3C1 support MIPI I3C® (SDR mode only).
2. USB Port 1 shares pins with PCIe Port 1.
3. The Watchdog Timer (WDT) is part of the Top Reset Generation Unit (TOPRGU).

1.2 Ordering Information

Table 1-2 presents the available ordering part numbers.

Table 1-2 Ordering Information

Part Number	Package	Operational Temperature Range
MT8395AV/ZA	MFC VFBGA	See Table 5-3 Recommended Operating Conditions

2 Preface

2.1 Pin Characteristics and Signal Descriptions Conventions

Table 2-1 describes the column headers in all Pin Characteristic and Signal Description tables in Section 4.2 Pin Characteristics and Section 3 Features Description.

Table 2-1 Column Headers Description

Column Name	Explanations
Ball Name	Logical name of the ball. Note that there may exist a selection of several signals for the same ball (aux mode).
Ball Location	Ball's physical location on the chip package
Signal Name	The name of the signal for the given aux mode
Type	Pin type when configured for the given aux mode: • AI: Analog input • AO: Analog output • AIO: Analog bi-directional pin • DI: Digital input • DO: Digital output • DIO: Digital bi-directional pin • P: Power • G: Ground
Description	Description of the signal
Aux. Function	Auxiliary function mode number: • 0 through 7 are possible alternative functions • An empty box means Not Applicable and the ball is dedicated to one function only
Reset State	Shows the Aux. function configured at the release of the SYSRSTB signal
Buffer Type	Describes the associated input/output buffer type
Power Domain	Indicates the voltage supply that powers the terminal IO buffers
PU/PD	Indicates the state of an internal pull-up or pull-down resistor at the release of the SYSRSTB signal: • OFF: Internal pull-up and pull-down are disabled • PU: Pull-up is enabled • PD: Pull-down is enabled • No: Pull-up and pull-down not available • Blank cell means "No"
IO Reset Value	Shows the IO state at the release of the SYSRSTB signal

2.2 Timing Conventions, Parameters, and Information

This section provides a general description of used symbols, adopted standards and terminology, and test process. All timing characteristics are valid over the represented operating conditions unless otherwise specified.

The interface clock frequency documented in this datasheet is the maximum clock frequency, which corresponds to the maximum programmable frequency on the particular output clock. The frequency defines the maximum limit supported by the device and does not consider into account any system limitation (layouts, connectors, and so forth).

The system designer should take into account these system considerations and the device timing characteristics as well and should determine properly the maximum frequency supported to transfer the data on the corresponding interface.

The timing parameter values do not include delays by board routes. Timing values may be adjusted by increasing/decreasing such delays. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

2.2.1 Timing Parameters and Information

Table 2-2 represents timing parameter symbols and descriptions used in the timing characteristic tables.

Table 2-2 Timing Parameters

Symbol	Description
f_{op}	Operating frequency
t_p	Period (cycle time)
t_d	Delay time
t_{dis}	Disable time
t_{en}	Enable time
t_h	Hold time
t_{su}	Setup time
Start	Start bit
t_t	Transition time
t_v	Valid time
t_w	Pulse duration
t_{FALL}	Fall time
t_{RISE}	Rise time
V_{OH}	High level output voltage
V_{OL}	Low level output voltage
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
V_{REF}	Reference voltage

2.2.2 Parameter Information

This datasheet provides timing values at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be also taken into account.

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

All rise and fall transition timing parameters are referenced correspondingly to 90% and 10% of the signal logical levels, unless otherwise specified.

2.3 Abbreviations

A

AE
Auto Exposure

AER
Advanced Error Reporting

AES
Advanced Encryption Standard

AF
Auto Focus

AFBC
Arm Frame Buffer Compression

AI
Artificial Intelligence

AIA
AI Accelerators

ALLM
Auto Low Latency Mode

APB
Advanced Peripheral Bus

APC
Address Protection Controller

API
Application Programming Interface

APU
AI Processor Unit

ASP
Advanced Simple Profile

ASPM
Active State Power Management

ASSR
Alternative Scrambler Seed Reset

ASTC
Adaptive Scalable Texture Compression

AWB
Auto White Balance

AXI
Advanced eXtensible Interface

B

BBC
British Broadcasting Corporation

bps
Bits Per Second

C

CABC
Content Adaptive Backlight Control

CAMSYS
Camera Imaging Subsystem

CBP
Constrained Baseline Profile

CBS
Credit-Based Shaper

CCC
Common Command Code

CDM
Charged Device Model

CEC
Consumer Electronics Control

CKSQ
Clock Squarer

CLK
Clock

CMDQ
Command Queue

CPHA
Clock Phase

CPOL
Clock Polarity

CPU
Central Processor Unit

CRC
Cyclic Redundancy Check

CSC
Color Space Conversion

CSI
Camera Serial Interface

CSMA/CD
Carrier Sense Multiple Access with Collision Detection

CV
Computer Vision

D

DAA
Dynamic Address Assignment

DCM
Dynamic Clock Management

DDC
Display Data Channel

DE
Data Enable

DISP_AAL
Display Adaptive Ambient Light

DISP_CCORR
Display Color Correction

DISP_COLOR
Display Color

DISP_DITHER
Display Dither

DISP_GAMMA
Display GAMMA

DISP_MUTEX
Display MUTEX

DISP_OVL
Display Overlay

DISP_PWM
Display Pulse Width Modulation

DISP_RDMA
Display Data Path Read DMA

DISP_WDMA
Display Write Direct Memory Access

DL
Downlink

DLA
Deep Learning Accelerator

DMA
Direct Memory Access

DPI
Display Parallel Interface

DQS
Data Strobe

DR
Dynamic Range

DRAM
Dynamic Random-Access Memory

DRAMC
Dynamic Random-Access Memory Controller

DRE
Dark Region Enhancement

DRM
Digital Rights Management

DSD
Direct Stream Digital

DSI
Display Serial Interface

DVFS
Dynamic Voltage and Frequency Scaling

DVI
Digital Visual Interface

E

eARC
Enhanced Audio Return Channel

ECRC
Endpoint Cyclic Redundancy Check

EDID
Extended Display Identification Data

eDMA
Enhanced Direct Memory Access

EEE
Energy Efficient Ethernet

EMI
External Memory Interface

ENIC
Ethernet Network Interface Controller

EOTF
Electro-Optical Transfer Function

EP
Endpoint

F

FD
Face Detection

FHD OSD
Full High-Definition On-Screen Display

fps
Frames Per Second

FPU
Floating-Point Unit

FSM
Finite State Machine

G

GIC
Generic Interrupt Controller

GPIO
General-Purpose Input/Output

GPU
Graphics Processor Unit

H

HBM
Human Body Model

HDCP
High-bandwidth Digital Content Protection

HDMI
High-Definition Multimedia Interface

HDR
High Dynamic Range

HEIF
High Efficiency Image File Format

HEVC
High Efficiency Video Coding

HLG
Hybrid Log Gamma

HP
High Profile

HPD
Hot Plug Detect

HS
High-Speed

HSYNC/HSync
Horizontal Synchronization

HW
Hardware

I

I2C
Inter-Integrated Circuit

I2S
Inter-IC Sound

ICMP
Internet Control Message Protocol

IDK
Integration Development Kit

IP
Internet Protocol

IRRX
Infrared Receiver

ISP
Image Signal Processor

L

L1PMSS
L1 Power Management Substates

LCM
Liquid Crystal Monitor

LDO
Low Dropout

LFSR
Linear Feedback Shift Register

LPC
Linear Pulse Code

LPF
Low-Pass Filter

LPM
Lower Power Management

LSB
Least Significant Bit

LSP
Low Saturation Protection

LTR
Latency Tolerance Reporting

LUT
Look-up Table

LVTS
Low Voltage Thermal Sensor

M

MACs
Multiply-Accumulate operations

MCDI
MultiCore Deep Idle

MCLK
Master Clock

MCUSYS
Microcontroller Unit System

MDIO
Management Data Input/Output

MDP
Multimedia Data Path

MDP_FG
Multimedia Data Path Film Grain

MDP_OVL
MDP Overlay

MDP_RDMA
Multimedia Data Path Read DMA

MDP_RSZ
Multimedia Data Path Resizer

MDP_TDSHP
Multimedia Data Path 2D Sharpness

MDP_WROT
Multimedia Data Path Rotation

MHL
Mobile High-Definition Link

MISO
Master Input to Slave Output

MMU
Memory Management Unit

MOSI
Master Output to Slave Input

MP
Main Profile

MPU
Memory Protection Unit

MSDC
MMC and SD Controller

MSI
Message Signaled Interrupt

MUX
Multiplexer

N

NN
Neural Network

O

OETF
Optical-Electro Transfer Function

OTG
On-The-Go

P

PBC
Peaking by Color

PCB
Printed Circuit Board

PCM
Pulse Code Modulation

PD
Photo Detector

PDM
Pulse Density Modulation

PIO
Programmed Input/Output

PIPE
Physical Interface for PCI Express

POR
Power On Reset

PQ
Perceptual Quantizer

PWM
Pulse Width Modulation

PWRAP
PMIC Wrapper

R

RC
Root Complex / Rate Control

RDMA
Read Direct Memory Access

RF
Radio Frequency

RH
Relative Humidity

ROI
Region of Interest

RTC
Real-Time Counter

RX
Receiver

S

SAR
Successive Approximation Register

SAV
Start of Active Video

SCK
Serial Clock

SCLTM
Smart Contrast Local Tone Mapping

SCPSYS
System Companion Processor + System Power Manager

SDM
Sigma-Delta Modulation

SDR
Single Data Rate / Standard Dynamic Range

SFD
Start Frame Delimiter

SIMD
Single Instruction Multiple Data

SNFI
SPI NAND Flash Interface

SP
Strict Priority

SPDIF
Digital Interface

SPI
Serial Peripheral Interface

SPM
System Power Management

SSC
Spread Spectrum Clocking

SW
Software

T

TCM
Tightly Coupled Memory

TCP
Transmission Control Protocol

TDM
Time Division Multiplexing

TE
Tearing Effect

TLB
Translation Lookaside Buffer

TMDS
Transition-Minimized Differential Signaling

TOPS
Tera Operations Per Second

TSMCU
Thermal Sensing Micro Circuit Unit

TX
Transmitter

U

UART
Universal Asynchronous Receiver/Transmitter

UDP
User Datagram Protocol

UFO
Universal FeynRules Output

UHD OSD
Ultra High Definition On-Screen Display

UI
Unit Interval

UL
Uplink

USB
Universal Serial Bus

V

VC
Virtual Channel

VDEC
Video Decoder

VENC
Video Encoder

VESA
Video Electronics Standards Association

VFPU
Vector Floating-Point Unit

VLIW
Very Long Instruction Word

VRR
Variable Refresh Rate

VSYNC/VSync
Vertical Synchronization

W

WDMA
Write DMA

WDT
Watchdog Timer

WPE
Warp Engine

WRR
Weighted Round Robin

X

xHCI
eXtensible Host Controller Interface

3 Features Description

The MT8395 device is a highly-integrated, powerful platform designed for a wide range of Artificial Intelligence (AI) and Internet of Things (IoT) use cases requiring high-performance edge processing, advanced multimedia and connectivity capabilities, multiple high-resolution cameras, connected touchscreen displays, and use of a multi-tasking High-Level Operating System (HLOS).

The highly-capable octa-core application processor utilizes the Arm® DynamIQ™ technology by combining high-performance Cortex-A78 and power-efficient Cortex-A55 cores, equipped with Arm Neon™ engine. The application processor offers the necessary processing power to support the latest OpenOS, along with its demanding applications such as smart home appliance, industrial IoT and other AI embedded devices. This content can be enhanced by the 2D/3D graphics accelerator (Arm Mali-G57 MC5 GPU) and then visualized on a high-resolution touchscreen display. To provide advanced multimedia applications and services such as streaming audio and video, the device features multi-standard video encoder and decoder engines, and an advanced audio subsystem.

The dual-core AI Processor Unit (APU) enables deep learning, Neural Network (NN) acceleration, and Computer Vision (CV) applications. The latter, combined with the up to 48MP camera, can clearly and accurately perform AI-vision functions such as facial recognition, object identification, scene analysis, optical character recognition and much more.

An extensive set of interfaces, connectivity, flexible storage and memory options further enhance the capabilities of the device and give product designers freedom to customize.

3.1 Application Processors

The device includes an Arm processor based subsystem (MCUSYS), which is responsible for running operating system and application programs in the device. It comprises two different Arm CPUs: four Cortex-A55 (*little*) cores and four Cortex-78 (*big*) cores, residing into a single cluster (Arm DynamIQ). This implementation provides different levels of power efficiency and computing power to satisfy a wide range of system power and performance requirements. The power efficiency of the four *little* cores (A55) is specially optimized to minimize the power consumption in daily usage scenarios and lightweight applications. For performance driven applications, the four powerful *big* cores (A78) can handle the heavy tasks and provide the best user experience under these scenarios.

The DynamIQ cluster also includes:

- Arm DynamIQ Shared Unit
- 2MB shared L3 memory for all CPU cores within the cluster

The MCUSYS includes Arm GIC-600 interrupt controller that provides interrupt support for all DynamIQ cores.

The MCUSYS supports Dynamic Voltage and Frequency Scaling (DVFS) technology allowing CPU cores to run at different frequency and voltage configurations for different application requirements. Besides DVFS, the power of each CPU core can be turned off individually when not used. In standby mode, the MCUSYS can be completely shut down to further save power consumption and optimize the battery usage on mobile devices.

3.1.1 Cortex-A78 Processor

The A78 processor (Arm Cortex-A78 MPCore) supports the following key features:

- Quad-core implementation (*big* cores)
- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with Armv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels (EL0 to EL3)
  - A64 instruction set
  - A32 instruction set (Arm instruction set in pre-Armv8 architectures)
  - T32 instruction set (Arm Thumb® instruction set in pre-Armv8 architectures)
- Support for various Arm extensions:
  - Armv8.1 extensions
  - Armv8.2 extensions

  - Armv8.3 (LDAPR instructions only)
  - Cryptography extensions
  - Reliability, Availability and Serviceability (RAS) extensions
- Arm Jazelle® technology
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- Level 1 (L1) and Level 2 (L2) cache memory with cache line length of 64 bytes:
  - 64KB L1 instruction cache (I-cache), L1I
  - 64KB L1 data cache (D-cache), L1D
  - 256KB private (not shared) L2 cache for each core
- Memory Management Unit (MMU):
  - 32-entry, fully-associative, L1 instruction micro Translation Lookaside Buffer (TLB)
  - 32-entry, fully-associative, L1 data micro TLB
  - 4-way, set-associative, 1024-entry unified main TLB
- Security:
  - Arm TrustZone®
  - Secure boot
- Debug:
  - Armv8 debug logic
  - Arm CoreSight™ architecture

3.1.2 Cortex-A55 Processor

The A55 processor (Arm Cortex-A55 MPCore) supports the following key features:

- Quad-core implementation (*little* cores)
- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with Armv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels (EL0 to EL3)
  - A64 instruction set
  - A32 instruction set
  - T32 instruction set
- Support for various Arm extensions:
  - Armv8.1 extensions
  - Armv8.2 extensions
  - Armv8.3 (LDAPR instructions only)
  - Cryptography extensions
  - RAS extensions
- Arm Jazelle technology
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- L1 and L2 cache memory with cache line length of 64 bytes:
  - 32KB L1 instruction cache (I-cache), L1I
  - 32KB L1 data cache (D-cache), L1D
  - 128KB private (not shared) L2 cache for each core
- MMU:
  - 15-entry, fully-associative, L1 instruction micro TLB
  - 16-entry, fully-associative, L1 data micro TLB
  - 4-way, set-associative, 1024-entry unified main TLB
- Security:
  - Arm TrustZone
  - Secure boot
- Debug:
  - Armv8 debug logic
  - Arm CoreSight architecture

3.2 Graphics Accelerator

The device graphics accelerator (GPU) is based on Arm Mali-G57 MC5 core. It is used to process extremely complicated graphics and perform general processing tasks assigned by the main application processor.

The GPU supports the following key features:

- An enhanced API feature set with high-performance support for both shader-based and fixed-function graphics APIs. The supported graphics and compute API industry standards are:
  - OpenGL ES 1.1, 2.0, 3.2
  - Vulkan 1.0, 1.1
  - OpenCL 1.0, 1.1, 1.2, 2.0, 2.1, 2.2
- Anti-aliasing capabilities
- An effective core for General Purpose computing on Graphics Processing Units (GPGPU) applications
- High memory bandwidth and low-power consumption for 3D graphics content
- Arm Frame Buffer Compression (AFBC), version 1.3
- Adaptive Scalable Texture Compression (ASTC)
- 8-bit, 10-bit and 16-bit YUV input and output formats
- Secure processing of Digital Rights Management (DRM) protected content
- Bus protocol:
  - 4 × 128-bit Arm AMBA® 4 ACE master interface for external memory access
  - 1 × 32-bit Arm AMBA 4 AXI slave interface for GPU configuration
- L2 cache:
  - 4 banks × 256KB
  - 4-way, set-associative
- Cache coherency support:
  - Within GPU
  - Between GPU and other system resources

3.3 Digital Signal Processor

The HiFi 4 Audio Engine Digital Signal Processor (DSP) is a highly optimized audio processor designed for efficient execution of audio and voice codecs and pre-/post-processing modules. It is a Single Instruction Multiple Data (SIMD) processor with ability to work in parallel on two 32-bit data items or four 16-bit data items. The Very Long Instruction Word (VLIW) architecture supports the execution of up to four operations in parallel.

The HiFi 4 DSP supports the following key features:

- Single-core implementation
- CPU architecture:
  - Four 32 × 32-bit Multiply-Accumulate operations (MACs) per cycle
  - Limited support for 72-bit accumulators
  - Limited support for eight 32 × 16-bit MACs
  - Four VLIW slots
  - Ability to issue two 64-bit loads per cycle
- Memory system:
  - Level 1: 32KB L1 I-cache + 128KB L1 D-cache
  - Level 2: 256KB L2 SRAM—Tightly Coupled Memory (TCM)
- No data retention support for pre-fetch buffer, I-cache, D-cache, ITag, and DTag
- Support for 25 interrupts
- Supports System Power Management (SPM) to control power sequence
- Dedicated UART (DSP_UART)
- Clock speeds:
  - 720 MHz at 0.75 V
  - 540 MHz at 0.65 V
  - 370 MHz at 0.6 V
  - 220 MHz at 0.55 V

3.4 AI Processor Unit

The AI Processor Unit System (APUSYS) is a highly efficient computing unit that is best suited for Artificial Intelligence (AI) and Computer Vision (CV) algorithms.

The APUSYS supports the following key features:

- Programmable APU for both AI and CV applications
  - 2 × APU implementation, to support simultaneously multiple applications. Each APU includes:
    - Cadence Vision P6 (VP6) core
    - L1 instruction memory: 64KB RAM + 128KB cache
    - L1 data memory: 128KB RAM + 128KB cache
    - Vector Floating-Point Unit (VFPU) to support high precision requirement applications
  - TOPS performance:
    - Fix 8: 0.85 TOPS
    - Fix 16: 0.21 TOPS
    - FP16: 0.11 TOPS
    - FP32: 0.05 TOPS
- AIA (or DLA—Deep Learning Accelerator) for high computation demanding Neural Network (NN) applications
  - 2 × AIA implementation, to provide more TOPS and support simultaneously multiple applications
  - TOPS performance:
    - Fix 8: 3.9 TOPS
    - Fix 16: 2.0 TOPS
    - FP 16: 2.0 TOPS
  - Simultaneous pipelined HW function block (CONV/ACT/POOL)
  - Support for Android NN asymmetric quantized data format
  - Support for compressed weight to reduce DRAM bandwidth
- APUSYS memory subsystem
  - 1MB TCM as second level (L2) data memory
  - 2 × eDMA engines for reduced-overhead data movement and format conversion
  - AXI path from MCUSYS to APUSYS TCM to reduce DRAM bandwidth

3.5 System Companion Processor

The System Companion Processor (SCP) is a processor subsystem that includes two MDSP RV33 processors and a variety of peripherals. The special design of the SCP makes it suitable for running applications such as Voice wake-up, Sensor HUB and future tasks when the entire device is in suspend mode. The SCP is connected to an infra bus and therefore can access DRAM, audio SRAM and other hardware resources through it.

3.5.1 MDSP RV33 Features

The MDSP RV33 is a low-power DSP for sensor/voice/audio applications. It supports the following key features:

- 32-bit integer core
- Single-precision Floating-Point Unit (FPU)
- RISC-V compatible instruction set
- 6-stage pipeline
- L1 cache memory system:
  - 32KB I-cache
  - 32KB D-cache
- AXI interface and prefetch

3.5.2 SCP Features

The SCP supports the following key features:

- Two MDSP RV33 cores
- 32KB Shared L1 TCM
- 768KB Shared L2 TCM
- An AXI master interface for device memory and register access
- An AXI master interface for device DRAM access

- An AHB master interface for audio memory and register access
- An AXI slave interface for configuration by MCUSYS
- Interprocessor interrupt to MCUSYS
- Serial audio interface to support Voice wake-up
- 6 × 32-bit down-count timers per core, with selectable clock source
- Interrupt controller per core
- Support of 12-input external interrupt with debounce function
- 2 × I2C
- 2 × I3C
- 3 × SPI
- 2 × UART
- 8-bit GPIO
- Direct path to PMIC wrapper
- Watchdog timer

3.5.3 SCP Signal Descriptions

Table 3-1 presents SCP signal descriptions.

Table 3-1 SCP Signal Descriptions

Signal Name	Type	Description	Ball Location
SCP_I3C0(1)			
SCP_SCL0	DIO	SCP I3C clock 0	AM28
SCP_SDA0	DIO	SCP I3C data 0	AK27
SCP_I2C1(1)			
SCP_SCL1	DIO	SCP I2C clock 1	AL28, AL27
SCP_SDA1	DIO	SCP I2C data 1	AM29, AL29
SCP_I2C2(1)			
SCP_SCL2	DIO	SCP I2C clock 2	AU18, AL9
SCP_SDA2	DIO	SCP I2C data 2	AT18, AM10
SCP_I3C3(1)			
SCP_SCL3	DIO	SCP I3C clock 3	AT11
SCP_SDA3	DIO	SCP I3C data 3	AL10
SCP_SPI0			
SCP_SPI0_CK	DO	SCP SPI0 serial clock	F32
SCP_SPI0_CS	DO	SCP SPI0 chip select	F31
SCP_SPI0_MI	DI	SCP SPI0 master input / slave output	G31
SCP_SPI0_MO	DO	SCP SPI0 master output / slave input	G32
SCP_SPI1_A			
SCP_SPI1_A_CK	DO	SCP SPI1 serial clock	AU23
SCP_SPI1_A_CS	DO	SCP SPI1 chip select	AT22
SCP_SPI1_A_MI	DI	SCP SPI1 master input / slave output	AR23
SCP_SPI1_A_MO	DO	SCP SPI1 master output / slave input	AT23
SCP_SPI1_B			
SCP_SPI1_B_CK	DO	SCP SPI1 serial clock	AP14
SCP_SPI1_B_CS	DO	SCP SPI1 chip select	AL12
SCP_SPI1_B_MI	DI	SCP SPI1 master input / slave output	AR12
SCP_SPI1_B_MO	DO	SCP SPI1 master output / slave input	AK12
SCP_SPI2			
SCP_SPI2_CK	DO	SCP SPI2 serial clock	AP17
SCP_SPI2_CS	DO	SCP SPI2 chip select	AT18
SCP_SPI2_MI	DI	SCP SPI2 master input / slave output	AL17

Signal Name	Type	Description	Ball Location
SCP_SPI2_MO	DO	SCP SPI2 master output / slave input	AU18
SCP_UART			
TP_UCTS1_AO	DI	SCP UART1 clear to send (active low)	AT10
TP_UCTS2_AO	DI	SCP UART2 clear to send (active low)	AP24
TP_URTS1_AO	DO	SCP UART1 request to send (active low)	AM8
TP_URTS2_AO	DO	SCP UART2 request to send (active low)	AM25
TP_URXD1_AO	DI	SCP UART1 receive data	AN8
TP_URXD2_AO	DI	SCP UART2 receive data	AN24
TP_UTXD1_AO	DO	SCP UART1 transmit data	AR8
TP_UTXD2_AO	DO	SCP UART2 transmit data	AN25
SCP_GPIO			
TP_GPIO0_AO	DIO	SCP GPIO0	H31
TP_GPIO1_AO	DIO	SCP GPIO1	G34
TP_GPIO2_AO	DIO	SCP GPIO2	J31
TP_GPIO3_AO	DIO	SCP GPIO3	G33
TP_GPIO4_AO	DIO	SCP GPIO4	G35
TP_GPIO5_AO	DIO	SCP GPIO5	H33
TP_GPIO6_AO	DIO	SCP GPIO6	H32
TP_GPIO7_AO	DIO	SCP GPIO7	H34
SCP Command Signals			
SCP_VREQ_VAO	DO	SCP to PMIC normal voltage request	AT15
Voice Wake-up			
VOW_CLK_MISO	DI	Voice wake-up interface clock	AU17
VOW_DAT_MISO	DI	Voice wake-up interface data	AK15

1. These pins must be connected to an external pull-up 4.7 kΩ and to an external pull-up 2.2 kΩ for FS+ and HS modes.

3.6 Memory

The device connects to external memories using External Memory Interface (EMI) controller and two Dynamic Random-Access Memory Controllers (DRAMC) with DDR PHY. EMI is a sophisticated communication interface between external memories and the device.

The EMI controller processes requests from the device masters and issues commands to the DRMAC. There are two EMI controllers. Each has the following key features:

- Prevents DRAM stall, data overflow, and underflow
- Allows gating its own clock when idle
- Connection to two DRAMCs
- Command schedule options:
  - Starvation control
  - Bandwidth regulator
  - Latency regulator
  - High priority
  - Page hit control
  - Read and write turn around prevent control
- Dedicated AXI connection ports:
  - 2 × 128-bit read and write ports to the MCUSYS
  - 2 × 128-bit read and write ports to the multimedia modules
  - 3 × 128-bit read and write ports to the GPU, APU, and peripherals
  - 1 × 128-bit read and write port to the Audio system

Each DRAMC processes EMI commands and controls the external memory. It has the following key features:

- Contains integrated DDR PHY
- Supports the following DDR memory type:
  - 16-bit LPDDR4X at 4266 MT/s
- Schedules and issues DRAM bus commands
- Keeps the integrity of DRAM bus timings
- Supports power-down and self-refresh
- Supports clock stop
- Support of input DQS/DQ timing calibration for PVT variation
- Supports read/write command out of order control
- Supports LPDDR4X byte mode
- Supports per-bank refresh

3.6.1 EMI Signal Descriptions

Table 3-2 presents EMI signal descriptions.

Table 3-2 EMI Signal Descriptions

Signal Name	Type	Description	Ball Location
EMI0—Calibration Resistor, Reset Output, Voltage Reference			
EMI0_EXTR(1)	AIO	EMI0 DRAM output driving calibration resistor	B3
EMI0_RESET_N	DO	EMI0 DRAM reset output	D29
EMI0_TP(2)	AIO	EMI0 DRAM voltage reference, connected to ½ AVDDQ_EMI0	H19
EMI0 Command/Address Bus—EMI0_CA[5:0]			
EMI0_CA0	DO	EMI0 DRAM command/address output 0	B18
EMI0_CA1	DO	EMI0 DRAM command/address output 1	B17
EMI0_CA2	DO	EMI0 DRAM command/address output 2	A18
EMI0_CA3	DO	EMI0 DRAM command/address output 3	C20
EMI0_CA4	DO	EMI0 DRAM command/address output 4	A20
EMI0_CA5	DIO	EMI0 DRAM command/address output 5	D19
EMI0 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI0_CK_T	DO	EMI0 DRAM clock	E17
EMI0_CK_C	DO	EMI0 DRAM clock invert	F17
EMI0_CKE0	DO	EMI0 DRAM clock enable for rank 0	G21
EMI0_CKE1	DO	EMI0 DRAM clock enable for rank 1	G20
EMI0_CS0	DO	EMI0 DRAM chip select for rank 0	F19
EMI0_CS1	DO	EMI0 DRAM chip select for rank 1	E18
EMI0_DMI0	DIO	EMI0 DRAM data mask/inversion for DQ[7:0]	A28
EMI0_DMI1	DIO	EMI0 DRAM data mask/inversion for DQ[15:8]	A22
EMI0_DQS0_T	DIO	EMI0 DRAM data strobe for DQ[7:0]	C28
EMI0_DQS0_C	DIO	EMI0 DRAM data strobe invert for DQ[7:0]	D28
EMI0_DQS1_T	DIO	EMI0 DRAM data strobe for DQ[15:8]	E25
EMI0_DQS1_C	DIO	EMI0 DRAM data strobe invert for DQ[15:8]	F25
EMI0 Data Bus—EMI0_DQ[15:0]			
EMI0_DQ0	DIO	EMI0 DRAM data pin 0	E27
EMI0_DQ1	DIO	EMI0 DRAM data pin 1	F26
EMI0_DQ2	DIO	EMI0 DRAM data pin 2	A30
EMI0_DQ3	DIO	EMI0 DRAM data pin 3	E26
EMI0_DQ4	DIO	EMI0 DRAM data pin 4	C26
EMI0_DQ5	DIO	EMI0 DRAM data pin 5	B29
EMI0_DQ6	DIO	EMI0 DRAM data pin 6	B27

Signal Name	Type	Description	Ball Location
EMI0_DQ7	DIO	EMI0 DRAM data pin 7	A26
EMI0_DQ8	DIO	EMI0 DRAM data pin 8	A24
EMI0_DQ9	DIO	EMI0 DRAM data pin 9	B23
EMI0_DQ10	DIO	EMI0 DRAM data pin 10	F24
EMI0_DQ11	DIO	EMI0 DRAM data pin 11	E23
EMI0_DQ12	DIO	EMI0 DRAM data pin 12	D21
EMI0_DQ13	DIO	EMI0 DRAM data pin 13	D22
EMI0_DQ14	DIO	EMI0 DRAM data pin 14	B21
EMI0_DQ15	DIO	EMI0 DRAM data pin 15	B25
EMI1 Command/Address Bus—EMI1_CA[5:0]			
EMI1_CA0	DO	EMI1 DRAM command/address output 0	E15
EMI1_CA1	DO	EMI1 DRAM command/address output 1	C16
EMI1_CA2	DO	EMI1 DRAM command/address output 2	A15
EMI1_CA3	DO	EMI1 DRAM command/address output 3	C13
EMI1_CA4	DO	EMI1 DRAM command/address output 4	A13
EMI1_CA5	DO	EMI1 DRAM command/address output 5	B15
EMI1 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI1_CK_T	DO	EMI1 DRAM clock	E16
EMI1_CK_C	DO	EMI1 DRAM clock invert	D16
EMI1_CKE0	DO	EMI1 DRAM clock enable for rank 0	D14
EMI1_CKE1	DO	EMI1 DRAM clock enable for rank 1	C14
EMI1_CS0	DO	EMI1 DRAM chip select for rank 0	F14
EMI1_CS1	DO	EMI1 DRAM chip select for rank 1	F15
EMI1_DMI0	DIO	EMI1 DRAM data mask/inversion for DQ[7:0]	A5
EMI1_DMI1	DIO	EMI1 DRAM data mask/inversion for DQ[15:8]	A11
EMI1_DQS0_T	DIO	EMI1 DRAM data strobe for DQ[7:0]	C5
EMI1_DQS0_C	DIO	EMI1 DRAM data strobe invert for DQ[7:0]	D5
EMI1_DQS1_T	DIO	EMI1 DRAM data strobe for DQ[15:8]	D9
EMI1_DQS1_C	DIO	EMI1 DRAM data strobe invert for DQ[15:8]	E9
EMI1 Data Bus—EMI1_DQ[15:0]			
EMI1_DQ0	DIO	EMI1 DRAM data pin 0	C6
EMI1_DQ1	DIO	EMI1 DRAM data pin 1	E7
EMI1_DQ2	DIO	EMI1 DRAM data pin 2	A3
EMI1_DQ3	DIO	EMI1 DRAM data pin 3	D8
EMI1_DQ4	DIO	EMI1 DRAM data pin 4	E8
EMI1_DQ5	DIO	EMI1 DRAM data pin 5	A4
EMI1_DQ6	DIO	EMI1 DRAM data pin 6	B6
EMI1_DQ7	DIO	EMI1 DRAM data pin 7	A7
EMI1_DQ8	DIO	EMI1 DRAM data pin 8	A9
EMI1_DQ9	DIO	EMI1 DRAM data pin 9	B10
EMI1_DQ10	DIO	EMI1 DRAM data pin 10	D10
EMI1_DQ11	DIO	EMI1 DRAM data pin 11	F10
EMI1_DQ12	DIO	EMI1 DRAM data pin 12	E12
EMI1_DQ13	DIO	EMI1 DRAM data pin 13	C12
EMI1_DQ14	DIO	EMI1 DRAM data pin 14	B12
EMI1_DQ15	DIO	EMI1 DRAM data pin 15	B8
EMI2—Calibration Resistor, Reset Output, Voltage Reference			
EMI2_EXTR(1)	AIO	EMI2 DRAM output driving calibration resistor	AJ1

Signal Name	Type	Description	Ball Location
EMI2_RESET_N	DO	EMI2 DRAM reset output	B2
EMI2_TP(2)	AIO	EMI2 DRAM voltage reference, connected to ½ AVDDQ_EMI0	R7
EMI2 Command/Address Bus—EMI2_CA[5:0]			
EMI2_CA0	DO	EMI2 DRAM command/address output 0	N5
EMI2_CA1	DO	EMI2 DRAM command/address output 1	P5
EMI2_CA2	DO	EMI2 DRAM command/address output 2	P4
EMI2_CA3	DO	EMI2 DRAM command/address output 3	N3
EMI2_CA4	DO	EMI2 DRAM command/address output 4	N1
EMI2_CA5	DO	EMI2 DRAM command/address output 5	P3
EMI2 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI2_CK_T	DO	EMI2 DRAM clock	R4
EMI2_CK_C	DO	EMI2 DRAM clock invert	R5
EMI2_CKE0	DO	EMI2 DRAM clock enable for rank 0	R2
EMI2_CKE1	DO	EMI2 DRAM clock enable for rank 1	R1
EMI2_CS0	DO	EMI2 DRAM chip select for rank 0	M5
EMI2_CS1	DO	EMI2 DRAM chip select for rank 1	N4
EMI2_DMI0	DIO	EMI2 DRAM data mask/inversion for DQ[7:0]	E1
EMI2_DMI1	DIO	EMI2 DRAM data mask/inversion for DQ[15:8]	L1
EMI2_DQS0_T	DIO	EMI2 DRAM data strobe for DQ[7:0]	C3
EMI2_DQS0_C	DIO	EMI2 DRAM data strobe invert for DQ[7:0]	D3
EMI2_DQS1_T	DIO	EMI2 DRAM data strobe for DQ[15:8]	H4
EMI2_DQS1_C	DIO	EMI2 DRAM data strobe invert for DQ[15:8]	H5
EMI2 Data Bus—EMI2_DQ[15:0]			
EMI2_DQ0	DIO	EMI2 DRAM data pin 0	C1
EMI2_DQ1	DIO	EMI2 DRAM data pin 1	D2
EMI2_DQ2	DIO	EMI2 DRAM data pin 2	F3
EMI2_DQ3	DIO	EMI2 DRAM data pin 3	G5
EMI2_DQ4	DIO	EMI2 DRAM data pin 4	F5
EMI2_DQ5	DIO	EMI2 DRAM data pin 5	E4
EMI2_DQ6	DIO	EMI2 DRAM data pin 6	F2
EMI2_DQ7	DIO	EMI2 DRAM data pin 7	G1
EMI2_DQ8	DIO	EMI2 DRAM data pin 8	J1
EMI2_DQ9	DIO	EMI2 DRAM data pin 9	K2
EMI2_DQ10	DIO	EMI2 DRAM data pin 10	K5
EMI2_DQ11	DIO	EMI2 DRAM data pin 11	K4
EMI2_DQ12	DIO	EMI2 DRAM data pin 12	M3
EMI2_DQ13	DIO	EMI2 DRAM data pin 13	L4
EMI2_DQ14	DIO	EMI2 DRAM data pin 14	M2
EMI2_DQ15	DIO	EMI2 DRAM data pin 15	H2
EMI3 Command/Address Bus—EMI3_CA[5:0]			
EMI3_CA0	DO	EMI3 DRAM command/address output 0	U6
EMI3_CA1	DO	EMI3 DRAM command/address output 1	U5
EMI3_CA2	DO	EMI3 DRAM command/address output 2	U3
EMI3_CA3	DO	EMI3 DRAM command/address output 3	W3
EMI3_CA4	DO	EMI3 DRAM command/address output 4	W1
EMI3_CA5	DO	EMI3 DRAM command/address output 5	V3

Signal Name	Type	Description	Ball Location
EMI3 System Bus—Command, Chip Select, Data Mask, Data Strobe, Clock Signals			
EMI3_CK_T	DO	EMI3 DRAM clock	T4
EMI3_CK_C	DO	EMI3 DRAM clock invert	T5
EMI3_CKE0	DO	EMI3 DRAM clock enable for rank 0	U2
EMI3_CKE1	DO	EMI3 DRAM clock enable for rank 1	U1
EMI3_CS0	DO	EMI3 DRAM chip select for rank 0	V5
EMI3_CS1	DO	EMI3 DRAM chip select for rank 1	V4
EMI3_DMI0	DIO	EMI3 DRAM data mask/inversion for DQ[7:0]	AG1
EMI3_DMI1	DIO	EMI3 DRAM data mask/inversion for DQ[15:8]	AA1
EMI3_DQS0_T	DIO	EMI3 DRAM data strobe for DQ[7:0]	AG4
EMI3_DQS0_C	DIO	EMI3 DRAM data strobe invert for DQ[7:0]	AG3
EMI3_DQS1_T	DIO	EMI3 DRAM data strobe for DQ[15:8]	AC4
EMI3_DQS1_C	DIO	EMI3 DRAM data strobe invert for DQ[15:8]	AC5
EMI3 Data Bus—EMI3_DQ[15:0]			
EMI3_DQ0	DIO	EMI3 DRAM data pin 0	AH2
EMI3_DQ1	DIO	EMI3 DRAM data pin 1	AH1
EMI3_DQ2	DIO	EMI3 DRAM data pin 2	AF5
EMI3_DQ3	DIO	EMI3 DRAM data pin 3	AD4
EMI3_DQ4	DIO	EMI3 DRAM data pin 4	AE5
EMI3_DQ5	DIO	EMI3 DRAM data pin 5	AF3
EMI3_DQ6	DIO	EMI3 DRAM data pin 6	AF2
EMI3_DQ7	DIO	EMI3 DRAM data pin 7	AE1
EMI3_DQ8	DIO	EMI3 DRAM data pin 8	AC1
EMI3_DQ9	DIO	EMI3 DRAM data pin 9	AB2
EMI3_DQ10	DIO	EMI3 DRAM data pin 10	AB4
EMI3_DQ11	DIO	EMI3 DRAM data pin 11	AA5
EMI3_DQ12	DIO	EMI3 DRAM data pin 12	Y5
EMI3_DQ13	DIO	EMI3 DRAM data pin 13	Y3
EMI3_DQ14	DIO	EMI3 DRAM data pin 14	Y2
EMI3_DQ15	DIO	DRAM data pin 15	AD2

1. Connect this pin through an external 60.4 Ω (1%) resistor to GND.
2. If not used, it can be left unconnected.

3.6.2 LPDDR4X Interface

3.6.2.1 LPDDR4X Timing Characteristics

The EMI LPDDR4X timing characteristics are compliant with JEDEC Standard—JESD209-4.

3.6.2.2 LPDDR4X Application Guidelines

Table 3-3 presents supported LPDDR4X device combinations.

Table 3-3 LPDDR4X Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
2	2 × 16-bit	No	64-bit

Figure 3-1 shows the schematic connections for a 64-bit interface using 2 × 2 × 16-bit devices.

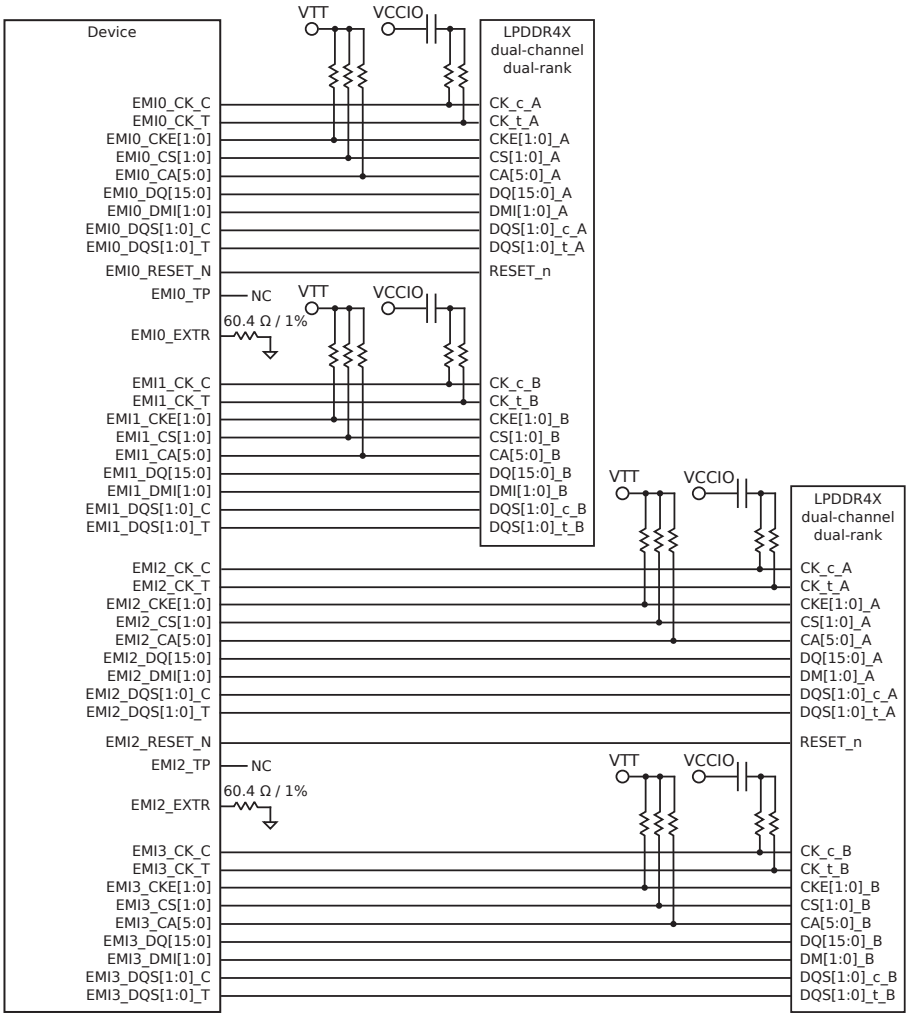


Figure 3-1 LPDDR4X Basic Schematic for 2 × 2 × 16-bit

3.7 Storage

3.7.1 Memory Card Controller (MSDC)

The Memory Stick and Secure Digital® (SD) card Controller (MSDC) offers a high throughput data transfers while power consumption and data security between device local hosts and memory cards are taken into consideration.

The MSDC interface fully supports:
- SD 3.0 (Secure Digital) memory card Specification
- SDIO 3.0 (Secure Digital Input Output) card Specification
- eMMC5.1 (embedded MultiMediaCard) Specification

The device has integrated 3 MSDC modules. MSDC0 is used as MMC™/eMMC interface, MSDC1 is used as SD interface, and MSDC2 is used as SD/SDIO interface. Each MSDC module supports the following key features:
- 32-bit access on AHB bus for control registers
- Basic DMA and linked-list based DMA modes

The MSDC0 controller fully supports:
- 64-bit data access on AXI bus
- 1-, 4-, 8-bit data bus width for eMMC
- Backwards compatibility with legacy MMC card
- High-speed Single Data Rate (SDR) mode
- High-speed Dual Data Rate (DDR) mode
- HS200 mode, SDR up to 200 MBps
- HS400 mode, DDR up to 400 MBps
- eMMC boot up mode
- Command Queue (CMDQ)
- Advanced Encryption Standard (AES)

The MSDC1 and MSDC2 controllers fully support:
- 32-bit data access on AHB bus
- 1-, 4-bit data bus width for SD card interface
- 1-, 4-bit data bus width for SDIO interface (MSDC2 only)
- Default Speed mode, data rate up to 12 MBps
- High-speed mode, data rate up to 25 MBps
- SDR12 mode, data rate up to 12 MBps
- SDR25 mode, data rate up to 25 MBps
- SDR50 mode, data rate up to 50 MBps
- SDR104 mode, data rate up to 100 MBps
- DDR50 mode, data rate up to 50 MBps

3.7.1.1 MSDC Signal Descriptions

Table 3-4 presents MSDC signal descriptions.

Table 3-4 MSDC Signal Descriptions

Signal Name	Type	Description	Ball Location
MSDC0			
MSDC0_CLK	DO	eMMC clock output	B36
MSDC0_CMD	DIO	eMMC command	C36
MSDC0_DAT0	DIO	eMMC data 0	D34
MSDC0_DAT1	DIO	eMMC data 1	D33
MSDC0_DAT2	DIO	eMMC data 2	D32
MSDC0_DAT3	DIO	eMMC data 3	C35
MSDC0_DAT4	DIO	eMMC data 4	D35
MSDC0_DAT5	DIO	eMMC data 5	E34

Signal Name	Type	Description	Ball Location
MSDC0_DAT6	DIO	eMMC data 6	E33
MSDC0_DAT7	DIO	eMMC data 7	E32
MSDC0_DSL	DI	eMMC data strobe input	A35
MSDC0_RSTB	DO	eMMC reset output	B35
MSDC1			
MSDC1_CLK	DO	SD card clock output	AU9
MSDC1_CMD	DIO	SD card command	AN8
MSDC1_DAT0	DIO	SD card data 0	AT6
MSDC1_DAT1	DIO	SD card data 1	AT7
MSDC1_DAT2	DIO	SD card data 2	AT8
MSDC1_DAT3	DIO	SD card data 3	AU8
MSDC2			
MSDC2_CLK	DO	SD card / SDIO clock output	G34
MSDC2_CLK_A	DO	SD card / SDIO clock output A	AL13
MSDC2_CMD	DIO	SD card / SDIO command	H31
MSDC2_CMD_A	DIO	SD card / SDIO command A	AP12
MSDC2_DAT0	DIO	SD card / SDIO data 0	G33
MSDC2_DAT0_A	DIO	SD card / SDIO data 0 A	AN12
MSDC2_DAT1	DIO	SD card / SDIO data 1	H33
MSDC2_DAT1_A	DIO	SD card / SDIO data 1 A	AT13
MSDC2_DAT2	DIO	SD card / SDIO data 2	G35
MSDC2_DAT2_A	DIO	SD card / SDIO data 2 A	AU14
MSDC2_DAT3	DIO	SD card / SDIO data 3	J31
MSDC2_DAT3_A	DIO	SD card / SDIO data 3 A	AP13

3.7.1.2 MSDC Signal Mapping

The communication protocol between controller and device is implemented through an advanced 11-signal or 6-signal bus. Details are provided in Table 3-5.

Table 3-5 MSDC Signal Mapping

No.	Name[3.7][1]	Type	eMMC	SD/SDHC	SDIO	Description
1	MSDC0/1/2_CLK	DO	CLK	CLK	SCLK	Clock
2	MSDC0_RSTB	DO	RCLK			Reset output
3	MSDC0/1/2_DAT0	DIO	DAT0	DAT0	DAT0	Serial data line bit 0
4	MSDC0/1/2_DAT1	DIO	DAT1	DAT1	DAT1	Serial data line bit 1
5	MSDC0/1/2_DAT2	DIO	DAT2	DAT2	DAT2	Serial data line bit 2
6	MSDC0/1/2_DAT3	DIO	DAT3	DAT3	DAT3	Serial data line bit 3
7	MSDC0_DAT4	DIO	DAT4			Serial data line bit 4
8	MSDC0_DAT5	DIO	DAT5			Serial data line bit 5
9	MSDC0_DAT6	DIO	DAT6			Serial data line bit 6
10	MSDC0_DAT7	DIO	DAT7			Serial data line bit 7
11	MSDC0/1/2_CMD	DIO	CMD	CMD	BS	Command/bus state
12	SD_WP[2]	I		WP		Write protection
13	SD_INS[2]	I	VSS2	VSS2	INS	Card insertion

1. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistors are required on the system board.

2. SD_WP and SD_INS signals are not provided by MSDC controller. These functions can be accomplished using GPIO pins, if needed.

3.7.1.3 MSDC Timing Characteristics

Table 3-6 and Figure 3-2 present the MSDC timing characteristics in Default Speed mode.

Table 3-6 MSDC Timing Characteristics (Default Speed mode)

No	Symbol	Parameter	Min	Max	Unit
Clock CLK (CLK rise and fall times are measured by min V_{IH} and max V_{IL}); C_{CARD} ≤ 10 pF					
DS1	f_{OP}	Operating frequency data transfer mode	0	25	MHz
	f_{OP_ID}	Operating frequency identification mode	100	400	kHz
DS2	$t_{w\_CLK\_L}$	Pulse duration, CLK low	10		ns
DS3	$t_{w\_CLK\_H}$	Pulse duration, CLK high	10		ns
DS4	t_{RISE_CLK}	Rise time, CLK		10	ns
DS5	t_{FALL_CLK}	Fall time, CLK		10	ns
Input DAT/CMD (referenced to CLK); C_{CARD} ≤ 10 pF					
DS6	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input	5		ns
DS7	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input	5		ns
Output DAT/CMD (referenced to CLK); C_L ≤ 40 pF					
DS8	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output during data transfer mode	0	14	ns
DS9	t_{d_DAT/CMD_ID}	Delay time, DAT/CMD output during identification mode	0	50	ns

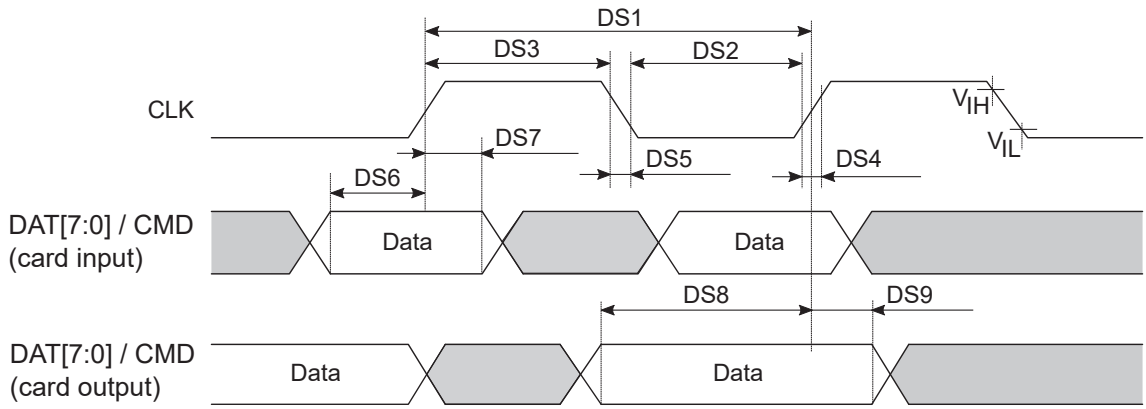


Figure 3-2 MSDC Timing Diagram (Default Speed mode)

Table 3-7 and Figure 3-3 present the MSDC timing characteristics in High Speed mode.

Table 3-7 MSDC Timing Characteristics (High Speed mode)

No	Parameter	Min	Max	Unit
Clock CLK (CLK rise and fall times are measured by min V_{IH} and max V_{IL}); C_{CARD} ≤ 10 pF				
HS1	f_{OP} Operating frequency data transfer mode	0	50	MHz
HS2	$t_{w\_CLK\_L}$ Pulse duration, CLK low	7		ns
HS3	$t_{w\_CLK\_H}$ Pulse duration, CLK high	7		ns
HS4	t_{RISE_CLK} Rise time, CLK		3	ns
HS5	t_{FALL_CLK} Fall time, CLK		3	ns
Input DAT/CMD (referenced to CLK); C_{CARD} ≤ 10 pF				
HS6	$t_{su\_DAT/CMD}$ Setup time, DAT/CMD input	6		ns
HS7	$t_{h\_DAT/CMD}$ Hold time, DAT/CMD input	2		ns

No	Parameter			Min	Max	Unit
Output DAT/CMD (referenced to CLK)						
HS8	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output(1)	$C_L \leq 40$ pF		14	ns
HS9	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output(1)	$C_L \geq 15$ pF	2.5		ns
	C_L	Total system capacitance for each line			40	pF

1. Valid during data transfer mode.

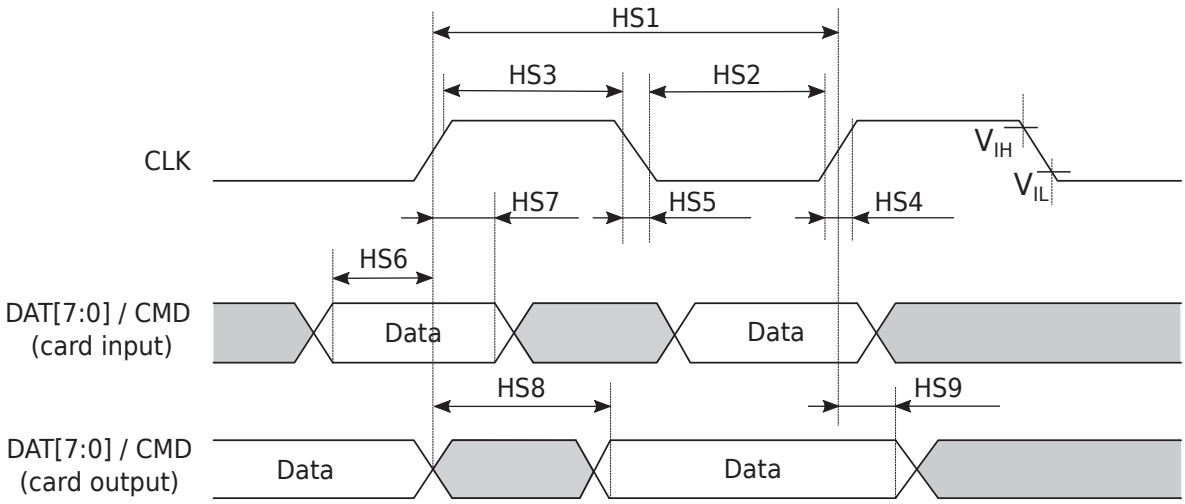


Figure 3-3 MSDC Timing Diagram (High Speed mode)

Table 3-8 and Figure 3-4 present the MSDC timing characteristics in SDR12, SDR25, SDR50, and SDR104 modes.

Table 3-8 MSDC Timing Characteristics (SDR12/SDR25/SDR50/SDR104 modes)

No.	Parameter		Min	Max	Unit
CLK output from host					
SDR121	t_C	Cycle time, CLK for SDR12		40	ns
		Cycle time, CLK for SDR25		20	ns
		Cycle time, CLK for SDR50		10	ns
		Cycle time, CLK for SDR104		4.8(4)	ns
SDR122	$t_{w\_CLK\_L}$	Pulse duration, CLK low	10		ns
SDR123	$t_{w\_CLK\_H}$	Pulse duration, CLK high	10		ns
	D	Duty Cycle, CLK	30	70	%
SDR124	t_{RISE_CLK}	Rise time, CLK		0.2 × SDR121(1)	ns
SDR125	t_{FALL_CLK}	Fall time, CLK		0.2 × SDR121(1)	ns
Host DAT/CMD input (referenced to CLK), V_{CT} = 0.975 V					
SDR126	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input for SDR50, C_{CARD} = 10 pF	3		ns
		Setup time, DAT/CMD input for SDR104, C_{CARD} = 10 pF	1.4		ns
SDR127	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input for SDR50, C_{CARD} = 5 pF	0.8		ns
		Hold time, DAT/CMD input for SDR104, C_{CARD} = 5 pF	0.8		ns
Host DAT/CMD output (referenced to CLK)					
SDR128	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output for SDR12/SDR25,		14	ns

No.	Parameter		Min	Max	Unit
		$t_C \geq 20.0$ ns, C_L = 40 pF, using driver type B			
		Delay time, DAT/CMD output for SDR50, $t_C \geq 10.0$ ns, C_L = 30 pF, using driver type B		7.5	ns
		Delay time, DAT/CMD output for SDR104	0	2	UI(2)
	$\Delta t_{d\_DAT/CMD}$	Delay variation due to temperature change after tuning for SDR104	-350	+1550	ps
SDR129	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output for SDR12/SDR25/SDR50, C_L = 15 pF	1.5		ns
SDR1210	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output for SDR104	0.6(3)		UI(2)

1. $t_{RISE\_CLK}/t_{FALL\_CLK}$ < 0.96 ns (max) at 208 MHz, C_{CARD} = 10 pF; $t_{RISE\_CLK}/t_{FALL\_CLK}$ < 2 ns (max) at 100 MHz, C_{CARD} = 10 pF. The absolute maximum value of t_{RISE_CLK} and t_{FALL_CLK} is 10 ns regardless of the clock frequency.
2. Unit Interval (UI) is one bit nominal time. For example, UI = 5 ns at 200 MHz.
3. $t_{h\_DAT/CMD}$ = 2.88 ns at 208 MHz
4. Maximum 208 MHz, V_{CT} = 0.975 V

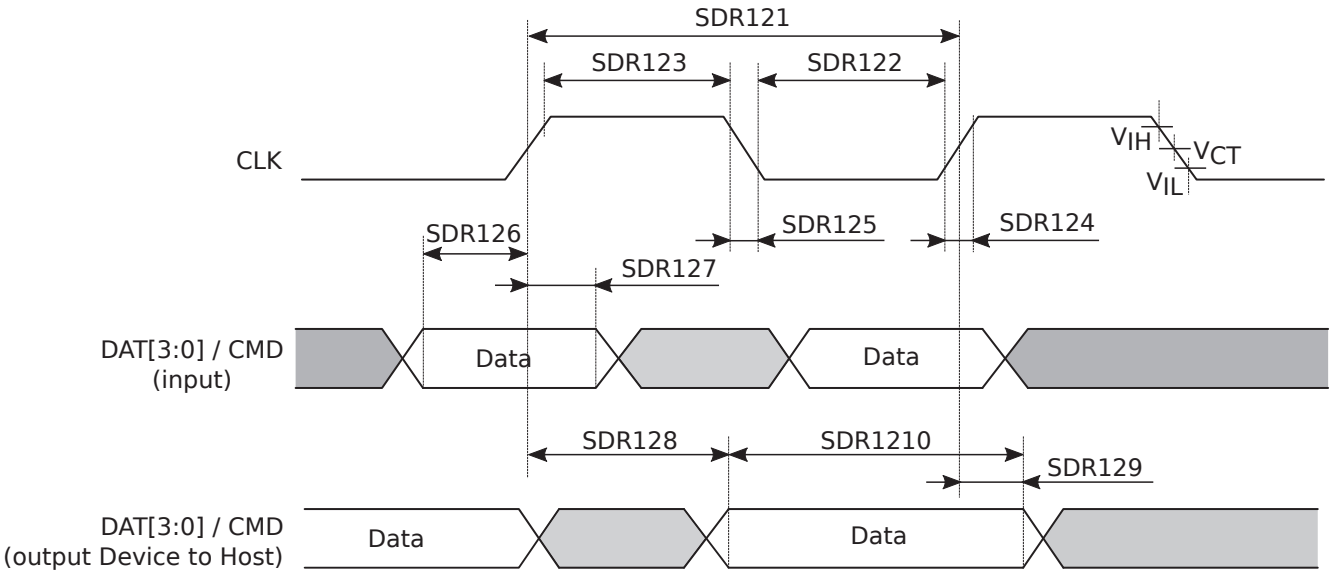


Figure 3-4 MSDC Timing Diagram (SDR12/SDR25/SDR50/SDR104 modes)

Table 3-9 and Figure 3-5 present the MSDC timing characteristics in DDR50 mode.

Table 3-9 MSDC Timing Characteristics (DDR50 mode)

No	Parameter			Min	Max	Unit
Input DAT/CMD (referenced to CLK rising and falling edge / rising edge); $C_{CARD} \leq 10$ pF						
DDR503	t_{su_CMD}	Setup time, CMD input		6		ns
	t_{su_DAT}	Setup time, DAT input		3		ns
DDR504	t_{h_CMD}	Hold time, CMD input		0.8		ns
	t_{h_DAT}	Hold time, DAT input		0.8		ns
Output DAT/CMD (referenced to CLK rising and falling edge / rising edge)						
DDR505	t_{d_CMD}	Delay time, CMD output(1)	$C_L \leq 30$ pF		13.7	ns
	t_{d_DAT}	Delay time, DAT output(1)	$C_L \leq 25$ pF		7	ns
DDR506	t_{h_CMD}	Hold time, CMD output	$C_L \geq 15$ pF	1.5		ns
	t_{h_DAT}	Hold time, DAT output	$C_L \geq 15$ pF	1.5		ns

1. Valid during data transfer mode.

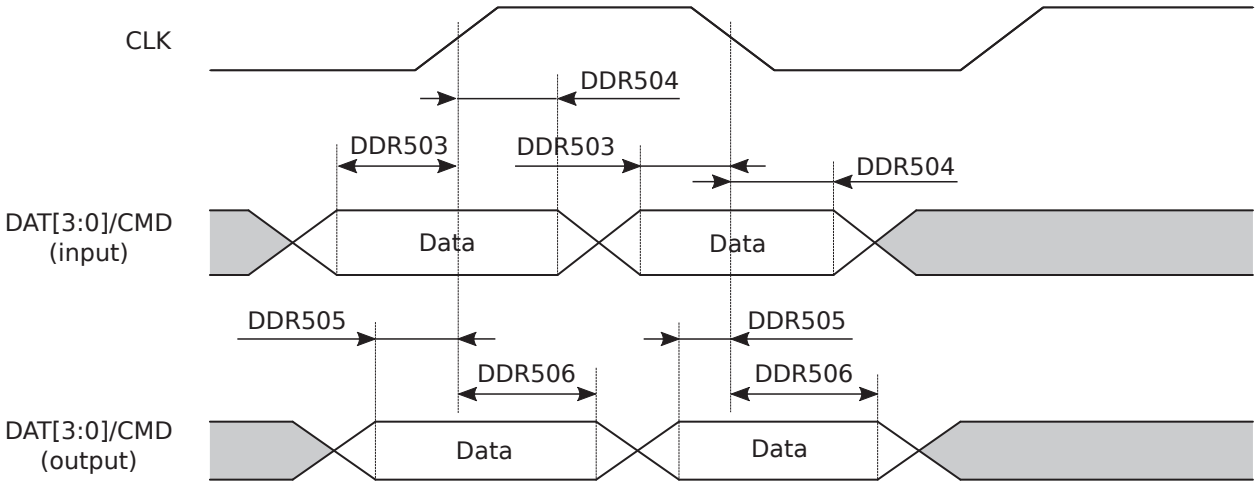


Figure 3-5 MSDC Timing Diagram (DDR50 mode)

Table 3-10 and Figure 3-6 present the MSDC timing characteristics in HS200 mode.

Table 3-10 MSDC Timing Characteristics (HS200 mode)

No	Parameter		Min	Max	Unit
Clock CLK					
HS2001	t_C	Cycle time, CLK	5		ns
HS2002	t_{RISE_CLK}	Rise time, CLK (C_{Device} ≤ 6 pF)		1(4)	ns
HS2003	t_{FALL_CLK}	Fall time, CLK (C_{Device} ≤ 6 pF)		1(4)	ns
	D	Duty Cycle, CLK	30	70	%
Input DAT/CMD; C_{Device} ≤ 6 pF					
HS2005	$t_{su\_DAT/CMD}$	Setup time, DAT/CMD input	1.4		ns
HS2006	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD input	0.8		ns
Output DAT/CMD					
HS2007	$t_{d\_DAT/CMD}$	Delay time, DAT/CMD output	0	2	UI(1)
	$\Delta t_{d\_DAT/CMD}$	Delay variation due to temperature change after tuning(2)	-350 (ΔT=-20°C)	1550 (ΔT=90°C)	ps
HS2008	$t_{h\_DAT/CMD}$	Hold time, DAT/CMD output	0.575(3)		UI(1)

1. Unit Interval (UI) is one bit nominal time. For example, UI = 5 ns at 200 MHz.
2. Total allowable shift of output valid window ($t_{h\_DAT/CMD}$) from last system tuning procedure $\Delta t_{d\_DAT/CMD}$ is 2600 ps for ΔT from -25 °C to 125 °C during operation.
3. The minimum value is equal to 2.88 ns at 208 MHz.
4. The absolute maximum value of t_{RISE_CLK} and t_{FALL_CLK} is 10 ns regardless of the clock frequency.

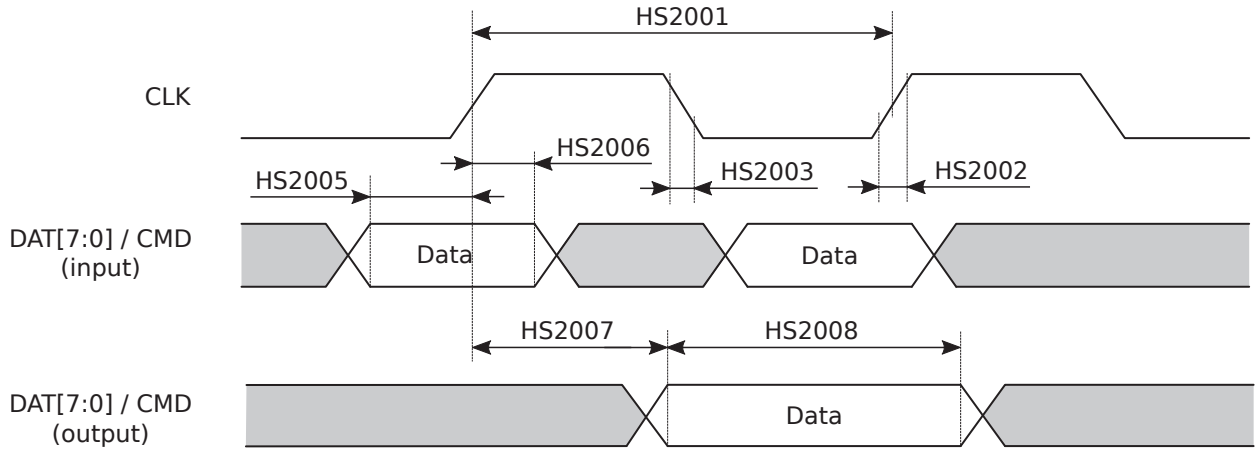


Figure 3-6 MSDC Timing Diagram (HS200 mode)

Table 3-11, Figure 3-7, and Figure 3-8 present the MSDC timing characteristics in HS400 mode.

Table 3-11 MSDC Timing Characteristics (HS400 mode)

No	Symbol	Parameter	Min	Max	Unit
Input CLK					
HS4001	t_{C_CLK}	Cycle time, CLK (with respect to V_T)	5		ns
	SR	Slew rate, with respect to V_{IH}/V_{IL}	1.125		V/ns
HS4002	t_{ck_dd}	Duty cycle distortion(1)	0	0.3	ns
HS4003	t_{W_CLK}	Pulse duration, CLK (with respect to V_T)	2.2		ns
Input DAT (referenced to CLK); with respect to V_{IH}/V_{IL}; (C_{Device} ≤ 6 pF)					
HS4004	t_{su_DAT}	Setup time, DAT input	0.4		ns
HS4005	t_{h_DAT}	Hold time, DAT input	0.4		ns
	SR	Slew rate	1.125		V/ns
Data Strobe					
HS4006	t_{C_CLK}	Cycle time, CLK (with respect to V_T)	5		ns
	SR	Slew rate (with respect to V_{OH}/V_{OL} and HS400 reference load)	1.125		V/ns
HS4007	t_{ds_dd}	Duty cycle distortion(2)	0	0.2	ns
HS4008	t_{W_CLK}	Pulse duration, CLK (with respect to V_T)	2		ns
	t_{RPRE}	Read preamble	0.4		t_{C_CLK}
	t_{RPST}	Read post-amble	0.4		t_{C_CLK}
Input DAT (referenced to Data Strobe); with respect to V_{OH}/V_{OL} and HS400 reference load					
HS4009	t_{RQ}	Output skew		0.4	ns
HS4010	t_{RQH}	Output hold skew		0.4	ns
	SR	Slew rate	1.125		V/ns

1. Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter and phase noise.
2. Allowable deviation from the input CLK duty cycle distortion (t_{ck_dd}). With respect to V_T. Includes jitter and phase noise.

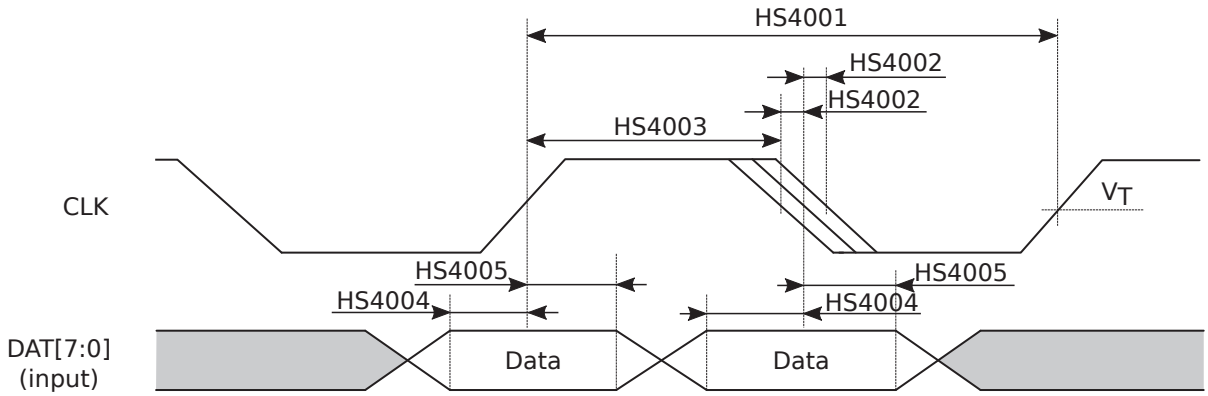


Figure 3-7 MSDC Timing Diagram (HS400 Input mode)

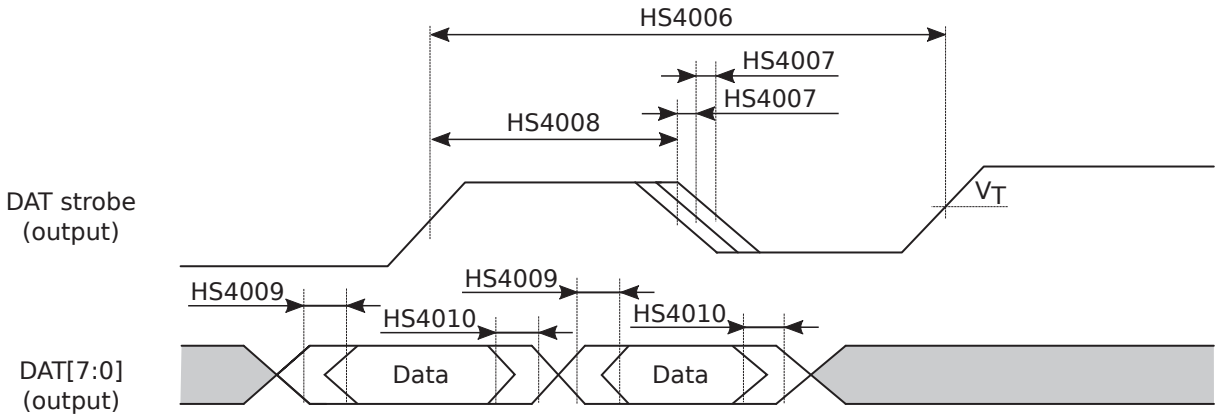


Figure 3-8 MSDC Timing Diagram (HS400 Output mode)

3.7.2 Universal Flash Storage (UFS)

The UFS controller is used for computing and mobile systems requiring low power consumption and high data throughput to store data in Non-Volatile Memory (NVM) devices. The UFS controller in the device is composed of three main modules: UFS Host Controller Interface (HCI), Unified Protocol (UniPro®) interface, and MIPI M-PHY® physical layer.

The UFS controller is compliant with the following standards:

- JEDEC Standard Universal Flash Storage (UFS), Version 2.1
- JEDEC Standard Universal Flash Storage Host Controller Interface (UFSHCI), Version 2.1
- MIPI Alliance Specification for UniPro, Version 1.6
- MIPI Alliance Specification for M-PHY, Version 3.1

The UFS controller supports the following key features:

- Single lane up to 5.8 Gbps (HS-G3 B-series)
- Pulse width modulation modes: PWM-G1 through PWM-G4
- High speed modes: HS-G1 through HS-G3 data rates
- Two high speed rate series: RATE A and RATE B
- MIPI UniPro test feature
- Auto-Hibernate function for power saving
- 32 configurable slots for Advanced Encryption Standard (AES)
- AES encryption and decryption engine for both XTS and CBC-ESSIV modes:
  - XTS mode: key sizes of 128/256 bits
  - CBC-ESSIV mode: key sizes of 128/192/256 bits

- Interfaces:
  - AHB slave interface
  - DMA AXI master interface with 36-bit address width

M-PHY main features:
- Supports 8b/10b line coding.
- Supports I2C interface for testing and debugging.
- M-PHY TX supports large amplitude only.

3.7.2.1 UFS Signal Descriptions

Table 3-12 presents UFS signal descriptions.

Table 3-12 UFS Signal Descriptions

Signal Name	Type	Description	Ball Location
UFS_MPHY_SCL	DI	UFS M-PHY serial clock	AL9
UFS_MPHY_SDA	DIO	UFS M-PHY serial data	AM10
UFS_RST_N	DO	UFS reset	A34
UFS_RX0N	AI	UFS negative differential receive data lane 0	B32
UFS_RX0P	AI	UFS positive differential receive data lane 0	B33
UFS_TX0N	AO	UFS negative differential transmit data lane 0	C31
UFS_TX0P	AO	UFS positive differential transmit data lane 0	C30
UFS_PLL_CKREF	DI	26 MHz clock input for UFS	G29
UFS_REFCK_OUT	DO	UFS reference clock output	F28

3.7.3 SPI NAND Flash Interface (SNFI)

The device includes one SPI NAND Flash Interface (SNFI) controller.

The SNFI controller supports the following key features:
- Error Checking and Correction (ECC) engine (BCH code acceleration allows 24-bit error correction)
- Programmable page size and spare size
- Programmable Flash Data Memory (FDM) data size and protected FDM data size
- Word/byte access through APB bus
- DMA for massive data transfer
- Latch sensitive interrupt (indicates the ready state for Read, Program and Erase operations)
- Programmable wait states
- Programmable command/address setup and hold times
- Programmable read enable hold time and write enable recovery time
- One chip select for SPI NAND flash parts
- Quad and Dual command modes
- Device clock, sample clock, and data skew adjustments

3.7.3.1 SNFI Signal Descriptions

Table 3-13 presents SNFI signal descriptions.

Table 3-13 SNFI Signal Descriptions

Signal Name	Type	Description	Ball Location
SNFI_CLK	DO	SNFI clock	AP22
SNFI_CS	DO	SNFI chip select	AN23
SNFI_HOLD	DIO	SNFI hold	AL8
SNFI_MISO	DIO	SNFI MISO	AP23
SNFI_MOSI	DIO	SNFI MOSI	AN22
SNFI_WP	DIO	SNFI write protection	AL7

3.7.3.2 SNFI Timing Characteristics

Table 3-14 and Figure 3-9 present the SNFI output timing characteristics.

Table 3-14 SNFI Output Timing Characteristics

No	Parameter	Description	Min	Typ	Max	Unit
SNFI01	F_{ck}	SNFI clock (SFCK) frequency	26		104	MHz
SNFI02	T_{ck}	SFCK period		1000 / SNFI01		ns
SNFI03	t_{CSS}	Chip select (SFCS) active setup time relative to SFCK		1.5 × SNFI02		ns
SNFI04	t_{CSH}	Chip select active hold time relative to SFCK		1.5 × SNFI02(1)		ns
SNFI05	t_{CLL}	Clock low pulse time		0.5 × SNFI02		ns
SNFI06	t_{CLH}	Clock high pulse time		0.5 × SNFI02		ns
SNFI07	t_{SUDAT}	Data output setup time	0.5 × SNFI02 - 1.5		0.5 × SNFI02 - 0.6	ns
SNFI08	t_{HDDAT}	Data output hold time	0.5 × SNFI02 - 1.5		0.5 × SNFI02 - 0.6	ns

1. Mac mode: use 1.5 × SNFI02. Reading NAND in auto mode: use 7.5 × SNFI02.

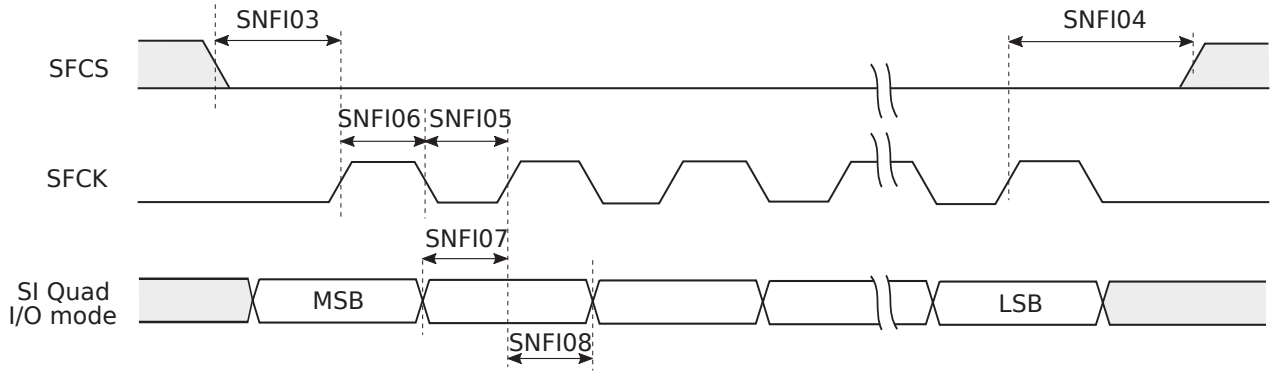


Figure 3-9 SNFI Output Timing Diagram

Table 3-15 and Figure 3-10 present the SNFI input timing characteristics.

Table 3-15 SNFI Input Timing Characteristics

No	Parameter	Description	Min	Max	Unit
SNFI09	t_v	Clock low to output valid require time	0	12	ns
SNFI10	t_{HO}	Output hold require time	0	SNFI09	ns

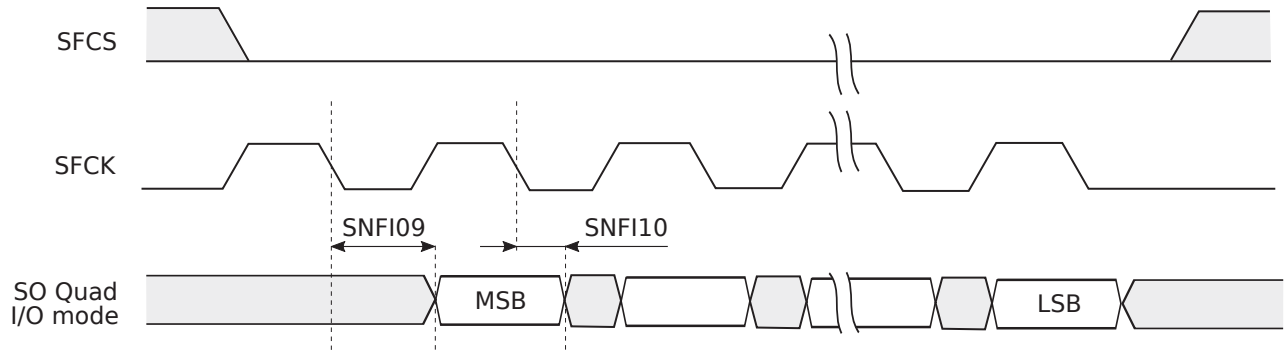


Figure 3-10 SNFI Input Timing Diagram

3.7.4 Serial NOR (SNOR) Flash Interface

The device includes one Serial NOR (SNOR) Flash Interface controller.

The SNOR controller supports the following key features:

- SPI bus compatible serial interface for common serial NOR flash devices
- 512-byte page programming buffer
- Multi-page program
- Single-bit SPI mode to transfer page program and 1-byte program
- 4-byte address mode and compatible 3-byte address mode
- Single-bit read mode
- Dual output and dual I/O read modes
- Quad output and quad I/O read modes
- Read of serial NOR flash data through Direct read mode, Programmed Input/Output (PIO) read mode, or DMA read mode
- For Direct read mode, the maximum supported capacity of serial NOR flash device is 2GB
- For PIO and DMA read modes, the maximum supported capacity of serial NOR flash device is 4GB

3.7.4.1 SNOR Signal Descriptions

Table 3-16 presents SNOR signal descriptions.

Table 3-16 SNOR Signal Descriptions

Signal Name	Type	Description	Ball Location
SPINOR_CK	DO	SNOR clock	AP22
SPINOR_CS	DO	SNOR chip select	AN23
SPINOR_IO0	DIO	SNOR I/O data 0 (MOSI)	AN22
SPINOR_IO1	DIO	SNOR I/O data 1 (MISO)	AP23
SPINOR_IO2	DIO	SNOR I/O data 2 (WP)	AL7
SPINOR_IO3	DIO	SNOR I/O data 3 (hold)	AL8

3.7.4.2 SNOR Timing Characteristics

Table 3-17 and Figure 3-11 present the SNOR timing characteristics.

Table 3-17 SNOR Timing Characteristics

No	Parameter[1]	Description	Min	Max	Unit
SNOR01	F_{ck}	SNOR clock (SF_SCLK) frequency		25	MHz
SNOR02	D	Duty Cycle, SF_SCLK	45	55	%

No	Parameter[1]	Description	Min	Max	Unit
SNOR03	t_{CLQx}	Input setup time	4.635		ns
SNOR04	t_{CLQV}	Input hold time	-4.82		ns
SNOR05	t_d	Output delay		2.151	ns
SNOR06	t_h	Output hold time	-0.37		ns
SNOR07	$t_{R\_CS/SCLK}$	CS low to SF_SCLK rising edge (read)	1.5 / SCLK	9.5 / SCLK	ns
SNOR08	$t_{R\_SCLK/CS}$	SF_SCLK falling edge to CS high (read)	3 / SCLK	10 / SCLK	ns

1. The specification is based on the assumed load capacity value of 30 pF.

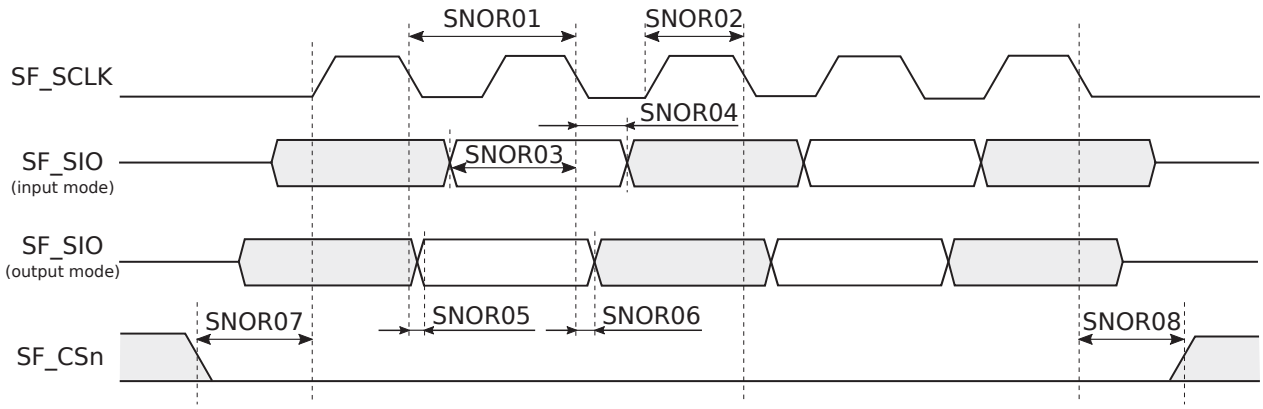


Figure 3-11 SNOR Timing Diagram

3.8 Display

The video data processing and display subsystem is also called Video data Processing Pipeline Subsystem (VPPSYS). It provides a variety of video data processing functions and display input/output interfaces. The video data processing functions can be served as video data post processing for Imaging or VDEC applications, or as video data pre-processing for VENC, APU or Display applications. The input data to VPPSYS can be channeled from DRAM buffer or HDMI. The output data of VPPSYS can be channeled to DRAM buffer or to device display output interfaces. The display output interfaces include MIPI DSI, eDP, DP and HDMI.

The multimedia data path (MDP) inside VPPSYS is further divided into several categories:

- Video data processing pipelines: SVPP-0 through SVPP-3 (see Section 3.8.1 Video Data Processing Pipelines (SVPP) and Interfaces)
- Display video data processing pipelines: DVPP-0 and DVPP-1 (see Section 3.8.2 Display Video Data Processing Pipelines (DVPP) and Interfaces)
- Image geometry warping engines: WPE0 and WPE1 (see Section 3.8.3 Warp Engine (WPE))

All the data processing pipelines inside VPPSYS can be operated in either Standalone mode or In-line mode. In Standalone mode, the video data input come from DRAM buffer and the processed video data go to DRAM buffer as well. The start, stop and reset of the data processing in Standalone mode are fully controlled by software. In In-line mode, the data processing pipeline is directly connected with display input or output interfaces. In this mode, the start of video data processing is controlled by display interface timings. Software controls stop and reset of the data processing, and only updates the processing configuration when needed. Both standalone and in-line mode are conducted through the Display MUTEX block (see Section 3.8.2.17 Display MUTEX (DISP_MUTEX)), which acts like an information dispatcher to all function blocks of VPPSYS about the start and stop of the video data processing.

3.8.1 Video Data Processing Pipelines (SVPP) and Interfaces

The SVPP-0 and SVPP-1 pipelines can operate standalone or in-line linked with the WPE engines. SVPP-2 and SVPP-3 can operate standalone or in-line linked with the DVPP pipelines.

The SVPP-0 and SVPP-1 pipelines provide the following features and corresponding functional blocks:

- Read DRAM agent: See Section 3.8.1.1 MDP Read DMA (MDP_RDMA)
- Fill grain noise for supporting AV1 standard: See Section 3.8.1.2 MDP Film Grain (MDP_FG)
- HDR transcode: See Section 3.8.1.3 MDP High Dynamic Range (MDP_HDR) Remapping
- Local contrast enhancement: See Section 3.8.1.4 MDP Adaptive Ambient Light Controller (MDP_AAL)
- Image resizer and sharpness: See Section 3.8.1.5 MDP Resizer (MDP_RSZ) and Section 3.8.1.6 MDP 2D Sharpness Engine (MDP_TDSHP)
- Preference color enhancement: See Section 3.8.1.8 MDP Color Engine (MDP_COLOR)
- Multi-layer image blender (self-equipped read DRAM agent): See Section 3.8.1.7 MDP Overlay (MDP_OVL)
- Image aspect ratio converter: See Section 3.8.1.11 SVPP Padding (SVPP_PADDING)
- HDR10+ meta data statistics: See Section 3.8.1.9 MDP Tone Curve Conversion (MDP_TCC)
- Dual image horizontal stitching (requires in-line mode with WPE): See Section 3.8.1.12 SVPP Stitch Engine (SVPP_STITCH)
- Write DRAM agent with right angle (90-, 180-, 270-degree, left/right flip) image rotation: See Section 3.8.1.10 MDP Write Rotation DMA (MDP_WROT)
- Digital video input data dispatcher: See Section 3.8.1.13 SVPP Split (SVPP_SPLIT)
- HDMI receiver: See Section 3.8.1.14 High-Definition Multimedia Interface Receiver (HDMIRX)
- Maximum throughput of each SVPP: 420 Mpixel/s

The SVPP-2 and SVPP-3 pipelines provide the following features and corresponding functional blocks:

- Same as SVPP-0 and SVPP-1, except for MDP_OVL and VPP_TCC, which are not included
- Maximum throughput of each SVPP: 420 Mpixel/s

3.8.1.1 MDP Read DMA (MDP_RDMA)

The MDP_RDMA is a raster scan DMA engine used to access different input formats in memory. The MDP_RDMA reads data from memory, applies processing operations such as decode compression, block to raster, up-sampling, and color conversion, and outputs data in YUV444 or ARGB format to the next SVPP engine.

The MDP_RDMA provides the following main features:

- Multiple input image formats:
  - RGB (1 plane 8-bit)
  - ARGB (1 plane 8-bit/10-bit)
  - YUV444 (1 plane 8-bit /10-bit)
  - YUV422 (1 plane 8-bit, 2 planes 8-bit, 3 planes 8-bit)
  - YUV420 (2 planes 8-bit/10-bit, 3 planes 8-bit, 2 planes 8-bit/10-bit block mode)
  - Arm Frame Buffer Compression (AFBC) formats: YUV420 8-bit/10-bit, ARGB 8-bit/10-bit, Hybrid FBC YUV420 8-bit/10-bit
- AFBC v1.1 support for the following configurations only:
  - 8-bit AFBC YUV420 (Layout1, no split, non-tiled)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, no YUV transformation)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, YUV transformation)
- Byte swap for switching input UV/RB data
- YUV444/ARGB/RGB output
- Clipping/cropping functions
- YUV420/422 chroma up-sampling to YUV444
- Color Space Conversion (CSC)
- AFBC and Hybrid FBC decompression into raster data

3.8.1.2 MDP Film Grain (MDP_FG)

The MDP_FG adds back film grain to the output video frames of the AV1 decoder.

The MDP_FG supports the following key features:

- AOMedia Video 1 (AV1) film grain
- 8-bit/10-bit mode
- Relay mode

3.8.1.3 MDP High Dynamic Range (MDP_HDR) Remapping

The MDP_HDR module processes HDR and wide-gamut signals, which can reach up to 10000 nits of dynamic range, to be displayed on a panel with much smaller dynamic range and gamut. The HDR remapped signals shown on a consumer display panel would look perceptually similar to the unprocessed signals shown on a HDR panel.

The MDP_HDR supports the following features:

- Electro-Optical Transfer Function (EOTF) options:
  - SMPTE ST 2084 (also called Perceptual Quantizer (PQ) or HDR10), providing a maximum of 4000 nits (2.5 times of PQ curve of 10000 nits) to better utilize the dynamic range of existing video streams
  - British Broadcasting Corporation (BBC) / NHK Hybrid Log Gamma (HLG)
  - ITU-R BT.709
  - SRGB
  - ITU-R BT.1886
- Optical-Electro Transfer Function (OETF) options:
  - ITU-R BT.709
  - BBC/NHK HLG
  - SMPTE ST 2084
  - SRGB
  - ITU-R BT.1886
- Programmable gamut
- YUV to RGB programmable color space conversion options:
  - Limited YCbCr BT.709 to full RGB
  - Limited YCbCr BT.2020 non-constant luminance to full RGB
  - Limited BT.2020 constant luminance to full RGB
- RGB to YUV programmable color space conversion:
  - Full RGB to limited YCbCr BT.709
- Adjustable tone-mapping curve (16 control points) and gain curve (1024 control points) to fine tune picture quality
- SMPTE ST 2086 static metadata and SMPTE ST 2094-40 dynamic metadata

3.8.1.4 MDP Adaptive Ambient Light Controller (MDP_AAL)

The MDP_AAL is coupled with the Smart Contrast Local Tone Mapping (SCLTM) and is used to improve picture quality by enhancing the contrast.

The MDP_AAL supports the following features:

- Color format: YUV
- 17-bin weighted histogram for each block
- 8 × 16 blocks for local contrast

3.8.1.5 MDP Resizer (MDP_RSZ)

The MDP_RSZ module is used to scale input image and video frames while preserving the signal energy at the same time.

The MDP_RSZ supports the following key features:

- Input/output data format: 10-bit YUV444
- Scaling ratio between 1/128× and 64×
- Up-scaling operation: 6-tap FIR (1 ≤ scaling ratio < 64)
- Down-scaling operations:
  - 4n-tap FIR (1/24 ≤ scaling ratio < 1)
  - Source accumulation (1/128 ≤ scaling ratio < 1/24)
- Fixed coefficients of the 6-tap and 4n-tap FIR filters

3.8.1.6 MDP 2D Sharpness Engine (MDP_TDSHP)

The sharpness function provides a better picture quality for display panels by restoring the image details, sharpening the edge and delivering a vivid feeling for pictures and videos.

The MDP_TDSHP supports the following features:

- Color format: YUV444
- 2-dimensional sharpness filter
- Peaking by Color (PBC)
- Gain curve control
- Content analyzer

3.8.1.7 MDP Overlay (MDP_OVL)

The MDP_OVL provides four flexible layers to implement alpha blending. The size, placement, format, and source of each layer can be set independently.

The MDP_OVL supports the following features:

- Four-layer alpha blending
- Maximum layer width: 8191 pixels
- Output throughput: 420 Mpixels/s
- Direct-link input color formats:
  - RGB101010/RGB888
  - YUV444 (10-bit, 1-plane)/YUV444 (8-bit, 1-plane)
- DRAM uncompressed input color formats:
  - ARGB2101010/ARGB8888/ARGB1555/ARGB4444/RGB101010/RGB888
  - YUV444 (10-bit, 1-plane) / YUV444 (8-bit, 1-plane) / Y1
- YUV to RGB, and RGB to YUV color space conversion with custom coefficients
- Privacy mask
- Dynamic Clock Management (DCM) for power consumption reduction

3.8.1.8 MDP Color Engine (MDP_COLOR)

The MDP_COLOR is a multi-stage processing engine used for achieving better picture quality and making one display panel resemble another in their output characteristics. It provides color space conversion functions and various hue/luma/saturation adjustments.

The COLOR supports the following key features:

- Color format: YUV444
- Input/output color space conversion
- C2P function: Transfer from Cartesian coordinates to Polar coordinates
- Hue engine functions:
  - Partial hue: Modifies hue angle of specific hue phase
- Luma engine functions:
  - Partial luma: Modifies luma value of specific hue phase
  - Global contrast/brightness adjustment
  - Chroma boost: Compensates saturation value due to Y change
- Saturation engine functions:
  - Partial S: Modifies saturation value of specific hue phase
  - Saturation Gain by Y (SGainByY)
  - Global saturation adjustment
  - Low Saturation Protection (LSP) function for avoiding worsening side-effects of camera sensors, such as color shading protection
- 3D color function for designing a color mapping window with adjustable location and size
- P2C function: Transfer from Polar coordinates to Cartesian coordinates

3.8.1.9 MDP Tone Curve Conversion (MDP_TCC)

The MDP_TCC module is used to support HDR gamma curve conversion for HDR displays by focusing on non-linear RGB domain tone mapping to fit HDR gamma curve.

The MDP_TCC supports the following main features:

- 256-point Look-up Table (LUT) for specifying tone curves for each RGB channel
- Statistic calculation of non-linear domain maximum RGB histogram result (after tone mapping) using 105 fixed bins index

- Crop function
- Input/output color format: YUV444 10-bit
- Internal color space conversion for RGB to YUV444, and YUV444 to RGB

3.8.1.10 MDP Write Rotation DMA (MDP_WROT)

The MDP_WROT is a write-DMA agent with rotation and flip functions. It packs and transforms the input pixel-based data into a 16 byte-wide output data.

The MDP_WROT provides the following key features:
- Rotation angles: 0°, 0° + H_Flip, 90°, 90° + H_Flip, 180°, 180° + H_Flip, 270°, and 270° + H_Flip
- Output image formats:
  - RGB888 (1 plane 8-bit), ARGB8888 (1 plane 8-bit/10-bit)
  - YUV444 (1 plane 8-bit/10-bit), YUV422 format (1 plane 8-bit, 2 planes 8-bit, 3 planes 8-bit), YUV420 format (2 planes 8-bit/10-bit, 3 planes 8-bit)
  - Compression format (AFBC YUV420 8-bit/10-bit, AFBC ARGB 8-bit/10-bit)
- AFBC v1.1 support for the following configurations only:
  - 8-bit AFBC YUV 4:2:0 (Layout1, no split, non-tiled)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, no YUV transformation)
  - AFBC_R8G8B8A8 (Layout3, split, non-tiled, YUV transformation)
- Byte swap for switching output UV/RB data
- Cropping function
- Color space conversion
- YUV down-sampling for output formats YUV420 or YUV422

3.8.1.11 SVPP Padding (SVPP_PADDING)

The SVPP_PADDING module adjusts the aspect ratio of image source for different kinds of display panels.

The SVPP_PADDING supports the following features:
- RGB101010 and 8-bit alpha formats
- Padding of the pre-defined color for configurable top/down/left/right side distance

3.8.1.12 SVPP Stitch Engine (SVPP_STITCH)

The SVPP_STITCH is used to merge two input images into one image.

3.8.1.13 SVPP Split (SVPP_SPLIT)

The SVPP_SPLIT module is used to split an input into two slice-per-line outputs, in order to lower the required clock rate for the downstream modules.

The SVPP_SPLIT supports the following main features:
- Input/output RGB/YUV channel swap
- Input color formats, color ranges and frame rates:
  - HDMI: RGB/YCbCr444/YCbCr422, 16-bit, full range, 60 Hz
- Output color formats and color range: RGB/YCbCr444, 10-bit, full range, 60 Hz
- YCbCr422 to YCbCr444 up-sampling
- Dither function for picture quality optimization
- Timing generator

3.8.1.14 High-Definition Multimedia Interface Receiver (HDMIRX)

The HDMIRX module receives uncompressed digital data streams in TMDS format from an HDMI-compatible source device and decodes the video, audio and control data based on HDMI Specification 2.0b.

The HDMIRX supports the following video features:
- Deep Color mode: up to 16 bits
- Maximum operating frequency: up to 594 MHz

- Video color space options: RGB444, YCbCr 4:2:2 (ITU BT.601 and BT.709), YCbCr 4:4:4 (ITU BT.601 and BT.709), YCbCr 4:2:0, and xvYCC
- 3D HDMI function
- SD mode resolutions:
  - 1440 × 480i (pixel repeat 2) @ 59.94/60 Hz
  - 720 × 480p @ 59.94/60 Hz
  - 1440 × 576i (pixel repeat 2) @ 50 Hz
  - 720 × 576p @ 50 Hz
- HD/FHD/UFHD mode resolutions:
  - 1280 × 720p @ 59.94/60/50 Hz
  - 1920 × 1080i @ 59.94/60/50 Hz
  - 1920 × 1080p @ 59.94/60/50 Hz
  - 1920 × 1080p @ 23.97/24 Hz
  - 1920 × 1080p @ 25 Hz
  - 1920 × 1080p @ 29.97/30 Hz
  - 3840 × 2160p @ 29.97/30 Hz
  - 3840 × 2160p @ 59.94/60/50 Hz

The HDMIRX supports the following audio features:

- Single compressed Digital Interface (SPDIF) format IEC61937 (up to 192 kHz)
- Single Linear Pulse Code (LPC) S/PDIF IEC60958 (up to 192 kHz and up to 24 bits), 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz
- Multi-channel Pulse Code Modulation (PCM) input (maximum 8 channels)
- Direct Stream Digital (DSD) audio
- Compressed lossless audio according to HDMI 2.0 (Dolby™ TrueHD and DTS-HD™)

Additionally, the HDMIRX supports the following features:

- Internal Extended Display Identification Data (EDID), 512 bytes
- High-bandwidth Digital Content Protection (HDCP) 1.4 / HDCP 2.3 key revocation scheme
- Compatibility with Digital Visual Interface (DVI) 1.0
- HDR10+ / Dolby dynamic metadata
- Consumer Electronics Control (CEC) channel shared with HDMITX
- Single Hot Plug Detect (HPD) line

3.8.1.14.1 HDMIRX Signal Descriptions

Table 3-18 presents HDMIRX signal descriptions.

Table 3-18 HDMIRX Signal Descriptions

Signal Name	Type	Description	Ball Location
HDMIRX20_HTPLG	DO	HDMIRX HPD line	AN25
HDMIRX20_PWR5V	DI	HDMIRX power supply (+5 V)	AN24
HDMIRX20_SCL	DI	HDMIRX DDC/I2C clock	AM25
HDMIRX20_SDA	DIO	HDMIRX DDC/I2C data	AP24
HDMIRX21_CH0_M	AI	HDMIRX TMDS data lane 0 (negative)	AR26
HDMIRX21_CH0_P	AI	HDMIRX TMDS data lane 0 (positive)	AR27
HDMIRX21_CH1_M	AI	HDMIRX TMDS data lane 1 (negative)	AU28
HDMIRX21_CH1_P	AI	HDMIRX TMDS data lane 1 (positive)	AT28
HDMIRX21_CH2_M	AI	HDMIRX TMDS data lane 2 (negative)	AR29
HDMIRX21_CH2_P	AI	HDMIRX TMDS data lane 2 (positive)	AR30
HDMIRX21_CLK_M	AI	HDMIRX TMDS clock lane (negative)	AU25
HDMIRX21_CLK_P	AI	HDMIRX TMDS clock lane (positive)	AT25

3.8.2 Display Video Data Processing Pipelines (DVPP) and Interfaces

The DVPP-0 pipeline provides image blending and display image enhancement for on-device display through MIPI DSI and eDP interfaces. DVPP-1 provides image blending and High Dynamic Range (HDR) format conversion for external display connection through DP and HDMI interfaces.

The DVPP-0 pipeline provides the following features and corresponding functional blocks:

- Multi-layer image blender with wide color gamut support (self-equipped with read DRAM agent): See Section 3.8.2.1 Display Overlay (DISP_OVL)
- Preference color enhancement: See Section 3.8.2.2 Display Color Engine (DISP_COLOR)
- Display image tuning for on-device display panel, including Color Space Conversion (CSC), global contrast, gamma, and dither functions:
  - See Section 3.8.2.5 Display Color Correction (DISP_CCORR)
  - See Section 3.8.2.6 Display Adaptive Ambient Light Controller (DISP_AAL)
  - See Section 3.8.2.7 Display Gamma Engine (DISP_GAMMA)
  - See Section 3.8.2.8 Display Dither Engine (DISP_DITHER)
- Data pipeline merger: See Section 3.8.2.9 Display Video Data Processing Pipeline Merger (DVPP_MERGE)
- MIPI Display Stream Compression (DSC): See Section 3.8.2.10 Display Stream Compression (DSC) Engine
- MIPI DSI controller: See Section 3.8.2.15 Display Serial Interface (DSI)
- eDP interface: See Section 3.8.2.14 Embedded DisplayPort Interface (EDPTX)
- Video data interface to EDPTX
- Maximum pixel throughput: 4K @ 60 Hz (594 Mpixel/sec)

The DVPP-1 pipeline provides the following features and corresponding functional blocks:

- HDR block supporting external display with HDR10+: See Section 3.8.2.11.1 High Dynamic Range (HDR) Engine
- Four read DRAM agents to support 4× HDR image layers: See Section 3.8.2.11.2 Display Mixer (DISP_MIXER)
- Data pipeline merger: See Section 3.8.2.9 Display Video Data Processing Pipeline Merger (DVPP_MERGE)
- DP interface: See Section 3.8.2.13 DisplayPort Interface (DPTX)
- HDMI transmitter: See Section 3.8.2.16 High-Definition Multimedia Interface Transmitter (HDMITX)
- Digital video output: See Section 3.8.2.12 Display Digital Parallel Interface (DPI)
- Video data interface to DPTX and HDMITX
- Maximum pixel throughput: 4K @ 60 Hz (594 Mpixel/sec)

3.8.2.1 Display Overlay (DISP_OVL)

The DISP_OVL provides four flexible layers to implement alpha blending. The size, placement, format, and source of each layer can be configured independently. Data can be sourced from DRAM, MMSYSRAM, or directly from an upstream module in the display path.

The DISP_OVL supports the following key features:

- Four-layer alpha blending
- Maximum layer width:
  - 8191 pixels for data sourced from direct-link module, MMSYSRAM, or DRAM uncompressed data
  - 1920 pixels for DRAM AFBC compressed data
- Output throughput: 450 Mpixels/s
- Direct-link input color formats:
  - RGB101010/RGB888
  - YUV444 (10-bit, 1-plane) / YUV444 (8-bit, 1-plane)
- SYSRAM input color formats:
  - ARGB2101010/ARGB8888/ARGB1555/ARGB4444/RGB101010/RGB888
  - YUV444 (10-bit, 1-plane) / YUV444 (8-bit, 1-plane)
- DRAM uncompressed input color formats:
  - ARGB2101010/ARGB8888/ARGB1555/ARGB4444/RGB101010/RGB888
  - YUV444 (10-bit, 1-plane) / YUV444 (8-bit, 1-plane)
- DRAM AFBC v1.1 compressed input color formats:
  - AFBC_R10G10B10A2 (Layout 3, split, non-tiled, no YUV transform)
  - AFBC_R10G10B10A2 (Layout 3, split, non-tiled, YUV transform)
  - AFBC_R8G8B8A8 (Layout 3, split, non-tiled, no YUV transform)

  - AFBC_R8G8B8A8 (Layout 3, split, non-tiled, YUV transform)
  - AFBC_R8G8B8 (Layout 3, split, non-tiled, no YUV transform)
  - AFBC_R8G8B8 (Layout 3, split, non-tiled, YUV transform)
- YUV to RGB, and RGB to RGB color space conversion options with custom coefficients
- Inverse gamma conversion and gamma conversion
- In-line rotation control for reads from MMSYSRAM
- Dynamic Clock Management (DCM) for power consumption reduction

3.8.2.2 Display Color Engine (DISP_COLOR)

The DISP_COLOR is a multi-stage processing engine used for achieving better picture quality and making one display panel resemble another in their output characteristics. It provides color space conversion functions and various hue/luma/saturation adjustments.

The DISP_COLOR supports the following key features:
- Color format: RGB
- Input/output color space conversion
- C2P function: Transfer from Cartesian coordinates to Polar coordinates
- Hue engine functions:
  - Partial hue: Modifies hue angle of specific hue phase
- Luma engine functions:
  - Partial luma: Modifies luma value of specific hue phase
  - Global contrast/brightness adjustment
  - Chroma boost: Compensates saturation value due to Y change
- Saturation engine functions:
  - Partial S: Modifies saturation value of specific hue phase
  - Saturation Gain by Y (SGainByY)
  - Global saturation adjustment
  - LSP function for avoiding worsening side-effects of camera sensors, such as color shading protection
- 3D color function for designing a color mapping window with adjustable location and size
- P2C function: Transfer from Polar coordinates to Cartesian coordinates

3.8.2.3 Display Read DMA (DISP_RDMA)

The DISP_RDMA engine reads out the data in the display pipeline from DRAM. The DISP_RDMA can also serve as a buffer for direct link data transfers from upstream modules.

The DISP_RDMA supports the following key features:
- Direct link input mode (DISP_RDMA receives data from an upstream module and serves as a buffer)
  - Input color formats: RGB888, RGB101010
  - Output color formats: RGB888, RGB101010
- Memory input mode (DISP_RDMA reads data from DRAM and provides buffering)
  - Input color formats:
    - YUYV422 (UYVY 8-bit, YUY2 8-bit, UYVY 10-bit, YUY2 10-bit)
    - RGB565, RGB888, ARGB4444, ARGB8888, ARGB2101010
    - Android_UYVY_10b, Android_YUY2_10b
  - Output color formats: RGB888, RGB101010
- Swapping and cropping functions
- Programmable color space conversion
- Maximum resolution and data depth: 3840 × 3840, 10-bit
- Universal FeynRules Output (UFO) decoding for RGB888 and RGB101010 data

3.8.2.4 Display Write DMA (DISP_WDMA)

The DISP_WDMA writes out the data in the display pipeline into DRAM. The device includes two DISP_WDMA modules, DISP_WDMA0 and DISP_WDMA1.

Each DISP_WDMA provides the following key features:

- Input color formats: YUV444/RGB888/ARGB8888/ARGB2101010
- Output color formats:
  - YUV422 (UYVY, YUY2) / YUV420 (YV12, NV12, P010) / Y8
  - RGB565/RGB888/ARGB8888/ARGB2101010
- UFO encoding for RGB888 and RGB101010 data
- Programmable color space conversion
- 3-tap filter in horizontal direction and 2-tap filter in vertical direction for YUV444 down-sampling
- Swapping and clipping functions
- Maximum supported resolutions:
  - DISP_WDMA0: 2560 × 3420
  - DISP_WDMA1: 1920 × 3420

3.8.2.5 Display Color Correction (DISP_CCORR)

The DISP_CCORR engine changes the overall mixture of RGB colors to fit the characteristics of the target display panel.

The DISP_CCORR supports the following key features:
- Fixed-coefficient inverse gamma table (conversion of non-linear sRGB data to linear RGB data)
- Fixed-coefficient gamma table (conversion of linear RGB data back to non-linear sRGB data)
- Programmable 3 × 3 matrix

3.8.2.6 Display Adaptive Ambient Light Controller (DISP_AAL)

The DSIP_AAL controller provides content adaptive and ambient light adaptive functions. It is responsible for backlight power saving and sunlight visibility improvement.

The DISP_AAL provides the following key features:
- 33-bin weighted RGB histogram
- Dark Region Enhancement (DRE) mapping for sunlight visibility
- Content Adaptive Backlight Control (CABC) compensation for backlight power saving

3.8.2.7 Display Gamma Engine (DISP_GAMMA)

The DISP_GAMMA engine provides gamma correction by changing the overall mixture of RGB colors to fit the characteristics of the display panel.

The DISP_GAMMA supports the following key features:
- 10-bit gamma table with 1024 entries
- Non-block gamma LUT programming

3.8.2.8 Display Dither Engine (DISP_DITHER)

The DISP_DITHER engine is used to decrease the RGB depth while mitigating the loss of image quality at the same time.

3.8.2.9 Display Video Data Processing Pipeline Merger (DVPP_MERGE)

The VPP_MERGE module is used to merge two slice-per-line inputs into one side-by-side output. The device includes two VPP_MERGE modules, VPP_MERGE0 and VPP_MERG1.

Each VPP_MERGE module supports the following features:
- Input color formats and ranges:
  - Input 0: ARGB/AYCbCr444/YCbCr422; 8-bit Alpha, 10-bit color, full range
  - Input 1: ARGB/AYCbCr444; 8-bit Alpha, 10-bit color, full range
- Output color formats and ranges;
  - Output 0: ARGB/AYCbCr444; 8-bit Alpha, 12-bit color, full range
  - Output 1: ARGB/AYCbCr444; 8-bit Alpha, 10-bit color, full range
- Input/output RGB/YUV channels swap
- YCbCr422 to YCbCr444 up-sampling
- Color range extension from 10-bit to 12-bit

3.8.2.10 Display Stream Compression (DSC) Engine

The DSC engine is a video data compressor. Data compression allows less data transmission for the purpose of achieving power saving or higher video frame rate.

The DSC engine contains two processing cores, which perform the data compression.

The DSC engine supports the following main features:
- Compliance with VESA DSC 1.2a
- 8-bit/10-bit RGB data formats
- Maximum horizontal slices: 2
- Maximum slice width: 3840 pixels
- Rate Control (RC) buffer size: 32955-bit
- Maximum line buffer bit depth: 11-bit
- Block prediction function

3.8.2.11 Display Video Data Output High Dynamic Range (VDO_HDR)

The VDO_HDR block provides HDR10+ function for external displays.

3.8.2.11.1 High Dynamic Range (HDR) Engine

The HDR engine converts a Standard Dynamic Range (SDR) or HDR-encoded stream into panel-displayable content, which can be SDR or HDR format.

The HDR engine supports the following key features:
- Video stream properties: 4K YCbCr 4:4:4 10-bit
- Color space conversion between RGB and YCbCr
- SDR (gamma 2.2)
- HDR10, HLG, and HDR10+
- Tone-mapping when converting HDR into SDR, with content maximally preserved
- Tone-mapping when converting SDR into HDR, with optimized visual effect
- Compliance with BT. 2100 standard
- Compliance with HDR10+ technical specification

3.8.2.11.2 Display Mixer (DISP_MIXER)

The DISP_MIXER performs alpha blending of up to four layers of HDR display content. Two layers are sourced from the main video and sub-video data paths, while the other two layers are sourced from the Ultra High Definition On-Screen Display (UHD OSD) and Full High-Definition On-Screen Display (FHD OSD) graphics paths.

The DISP_MIXER supports the following main features:
- Video frame resolution: Up to 4096 × 2160
- Pre-multiplied and non-pre-multiplied alpha blending
- Pixel alpha blending
- Flexible Region of Interest (ROI)

3.8.2.12 Display Digital Parallel Interface (DPI)

The device includes two DPI controllers, DPI0 and DPI1, which output digital video data and timing signals. DPI0 is used to directly interface an external display panel, while DPI1 provides data and timings to HDMITX module.

Each DPI controller supports the following key features:
- Flexible output data bus width and formats:
  - DPI0 up to 16-bit bus: RGB565/YUV422 8-bit
  - DPI1 up to 30-bit bus: RGB565 / RGB 8-bit, 10bit / YUV444 8-bit, 10-bit / YUV422 8-bit, 10-bit, 12-bit
- Resolution up to 1920 × 1080 @ 60fps (for DPI0 only)
- Fixed-coefficient color space conversion
- Embedded synchronization timings for BT.656-like output format
- Dual edge output format

- YUV444 to YUV422 chroma down-sampling
- Internal pattern generator

3.8.2.12.1 DPI Signal Descriptions

Table 3-19 presents DPI signal descriptions.

Table 3-19 DPI Signal Descriptions

Signal Name	Type	Description	Ball Location
DPI_CK	DO	DPI pixel clock	AT14
DPI_D0	DO	DPI data 0	AN14
DPI_D1	DO	DPI data 1	AM14
DPI_D10	DO	DPI data 10	AL12
DPI_D11	DO	DPI data 11	AK12
DPI_D12	DO	DPI data 12	AP12
DPI_D13	DO	DPI data 13	AL13
DPI_D14	DO	DPI data 14	AP13
DPI_D15	DO	DPI data 15	AN12
DPI_D2	DO	DPI data 2	AL14
DPI_D3	DO	DPI data 3	AK14
DPI_D4	DO	DPI data 4	AU15
DPI_D5	DO	DPI data 5	AR14
DPI_D6	DO	DPI data 6	AK11
DPI_D7	DO	DPI data 7	AK10
DPI_D8	DO	DPI data 8	AP14
DPI_D9	DO	DPI data 9	AR12
DPI_DE	DO	DPI data enable	AT12
DPI_HSYNC	DO	DPI horizontal synchronization	AU14
DPI_VSYNC	DO	DPI vertical synchronization	AT13

3.8.2.12.2 DPI Timing Characteristics

Table 3-20 and Figure 3-12 present timing characteristics for DPI in the device.

Table 3-20 DPI Timing Characteristics

No.	Parameter		Min	Max	Unit
DPI01	t_c	Cycle time	6.73(1)		ns
DPI02	D	Duty cycle, DPI_CK	45	55	%
DPI03	t_{RISE}	Rise time		1.374	ns
DPI04	t_{FALL}	Fall time		1.374	ns
DPI05	t_d	Delay time, other signals to DBPI_CK	1.683		ns

1. For maximum operating clock frequency refer to Table 6-1.

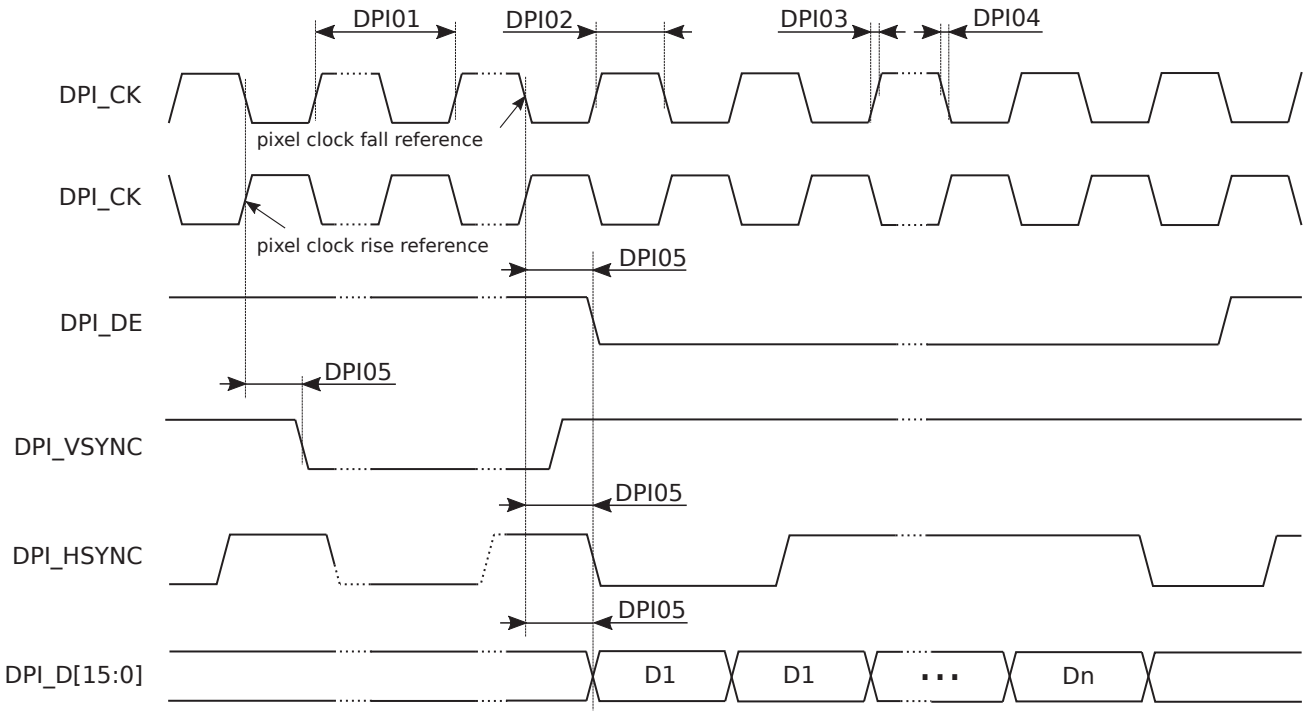


Figure 3-12 DPI Timing Diagram

3.8.2.13 DisplayPort Interface (DPTX)

The DPTX provides digital video and auxiliary data transfer between the device and an external display module. The communication link is handled through the DP Auxiliary Channel (DPAUX).

The DPTX supports the following key features:

- Compliance with DP v1.4 standard
- Single link output port with 4× main lanes, configured as follows:
  - 4× lanes with up to 8.1 Gbps per lane (HBR3)
- Hot Plug Detect (HPD) line
- Auxiliary channel lane:
  - Manchester-II coding
  - Clock extracted from the data stream
  - 1 Mbps bit rate
- Input data formats: RGB 8-bit/10-bit, YUV444 8-bit/10-bit, YUV422 8-bit/10-bit
- Output data format: RGB444 8-bit/10-bit
- 8-bit to 10-bit encoder
- Alternative Scrambler Seed Reset (ASSR) function
- Interlane skew function
- Up to 4K2K @ 60 Hz resolution (10-bit, HBR2 without DSC)

3.8.2.13.1 DPTX Signal Descriptions

Table 3-21 presents DPTX signal descriptions.

Table 3-21 DPTX Signal Descriptions

Signal Name	Type	Description	Ball Location
DP_LN0_TXN	AIO	DPTX lane 0 (negative)	AH35
DP_LN0_TXP	AIO	DPTX lane 0 (positive)	AG35
DP_LN1_TXN	AIO	DPTX lane 1 (negative)	AJ37
DP_LN1_TXP	AIO	DPTX lane 1 (positive)	AJ36
DP_LN2_TXN	AIO	DPTX lane 2 (negative)	AK34

Signal Name	Type	Description	Ball Location
DP_LN2_TXP	AIO	DPTX lane 2 (positive)	AJ34
DP_LN3_TXN	AIO	DPTX lane 3 (negative)	AL33
DP_LN3_TXP	AIO	DPTX lane 3 (positive)	AL32
DP_TX_HPD	DI	DPTX hot plug detect	H32, AP25
DPAUXN	AIO	DPTX auxiliary channel (negative)	AG31
DPAUXP	AIO	DPTX auxiliary channel (positive)	AG30

3.8.2.14 Embedded DisplayPort Interface (EDPTX)

The EDPTX provides the electrical transport for video and auxiliary data between the device and an external display module. The communication link is handled through the eDP Auxiliary Channel (EDPAUX).

The EDPTX supports the following key features:

- Compliance with eDP v1.4 standard
- Single link output port with 4× main lanes
- Up to 5.4 Gbps per lane (HBR2)
- Hot Plug Detect (HPD) line
- Auxiliary channel lane:
  - Manchester-II coding
  - Clock extracted from the data stream
  - 1 Mbps bit rate
- Input data formats: RGB 8-bit/10-bit, YUV444 8-bit/10-bit, YUV422 8-bit/10-bit
- RGB444 8-bit/10-bit color format
- 8-bit to 10-bit encoder
- Alternative Scrambler Seed Reset (ASSR) function
- Interlane skew function
- Up to 4K2K @ 60 Hz resolution (10-bit, HBR2 without DSC)

3.8.2.14.1 EDPTX Signal Descriptions

Table 3-22 presents EDPTX signal descriptions.

Table 3-22 EDPTX Signal Descriptions

Signal Name	Type	Description	Ball Location
EDP_LN0_TXN	AIO	EDPTX lane 0 (negative)	AD33
EDP_LN0_TXP	AIO	EDPTX lane 0 (positive)	AD34
EDP_LN1_TXN	AIO	EDPTX lane 1 (negative)	AD37
EDP_LN1_TXP	AIO	EDPTX lane 1 (positive)	AD36
EDP_LN2_TXN	AIO	EDPTX lane 2 (negative)	AF36
EDP_LN2_TXP	AIO	EDPTX lane 2 (positive)	AE35
EDP_LN3_TXN	AIO	EDPTX lane 3 (negative)	AF33
EDP_LN3_TXP	AIO	EDPTX lane 3 (positive)	AF34
EDP_TX_HPD	DI	EDPTX hot plug detect	H34, AN10
EDPAUXN	AIO	EDPTX auxiliary channel (negative)	AE31
EDPAUXP	AIO	EDPTX auxiliary channel (positive)	AE32

3.8.2.15 Display Serial Interface (DSI)

The DSI is based on MIPI Alliance Specification, supporting high-speed serial data transfer between host processor and peripheral devices such as display modules.

The device includes two DSI controllers, DSI0 and DSI1. Each DSI controller receives frame pixels from memory, performs frames packing and lane distribution, and then sends the data to a dedicated MIPI D-PHY/C-PHY TX core for serializing.

Each DSI controller provides the following key features:

- Compliance with MIPI DSI Specification v01-02-00
- Supports video and command mode data transfers
- Pixel formats supported: RGB888 / RGB101010 / compressed pixel stream
- 128-entry command queue for command transmission
- 3 types of video modes: Sync-event, sync-pulse, and burst modes
- Limited high-speed residual packet transmission during video mode blanking period
- Ultra-low power mode control
- Peripheral and external Tearing Effect (TE) signals detection
- MIPI D-PHY interface, with the following features:
  - 1 clock lane and up to 4 data lanes
  - Throughput up to 1.5 Gbps per data lane
  - Bi-directional data transmission in Low-Power mode for data lane 0
  - Uni-directional data transmission in High-Speed mode for data lanes 0 through 3
  - Non-continuous high-speed transmission for clock and data lanes
  - Lane swapping
  - Compliance with MIPI D-PHY Specification v1.2
- MIPI C-PHY interface, with the following features:
  - Single 3-trio port
  - Throughput up to 1.1 Gsps per trio
  - Trio swapping
  - Compliance with MIPI C-PHY Specification v1.0

Each D-PHY/C-PHY TX core provides the following main features:

- Sigma-Delta Modulation (SDM) PLL configuration
- Spread Spectrum Clocking (SSC) control
- Bandgap control
- Output pads control

3.8.2.15.1 DSI Signal Descriptions

Table 3-23 presents DSI signal descriptions.

Table 3-23 DSI Signal Descriptions

Signal Name	Type	Description		Ball Location
DSI1		**D-PHY Mode**	**C-PHY Mode**	
DSI1_CKN_T1C	AIO	DSI1 clock lane (negative)	DSI1 Trio1 C	AR3
DSI1_CKP_T1B	AIO	DSI1 clock lane (positive)	DSI1 Trio1 B	AR2
DSI1_D0N_T1A	AIO	DSI1 data lane 0 (negative)	DSI1 Trio1 A	AR1
DSI1_D0P_T0C	AIO	DSI1 data lane 0 (positive)	DSI1 Trio0 C	AP2
DSI1_D1N_T2B	AIO	DSI1 data lane 1 (negative)	DSI1 Trio2 B	AU4
DSI1_D1P_T2A	AIO	DSI1 data lane 1 (positive)	DSI1 Trio2 A	AU3
DSI1_D2N_T0B	AO	DSI1 data lane 2 (negative)	DSI1 Trio0 B	AN1
DSI1_D2P_T0A	AIO	DSI1 data lane 2 (positive)	DSI1 Trio0 A	AN2
DSI1_D3N	AIO	DSI1 data lane 3 (negative)	-	AR4
DSI1_D3P_T2C	AIO	DSI1 data lane 3 (positive)	DSI1 Trio2 C	AT4
DSI1_TE	DI	DSI1 tearing effect control	DSI1 tearing effect control	AM8, AT9
DSI0		**D-PHY Mode**	**C-PHY Mode**	
DSI0_CKN_T1C	AIO	DSI0 clock lane (negative)	DSI0 Trio1 C	AL2
DSI0_CKP_T1B	AIO	DSI0 clock lane (positive)	DSI0 Trio1 B	AM2
DSI0_D0N_T1A	AIO	DSI0 data lane 0 (negative)	DSI0 Trio1 A	AK3
DSI0_D0P_T0C	AIO	DSI0 data lane 0 (positive)	DSI0 Trio0 C	AK4

Signal Name	Type	Description		Ball Location
DSI0_D1N_T2B	AIO	DSI0 data lane 1 (negative)	DSI0 Trio2 B	AM3
DSI0_D1P_T2A	AIO	DSI0 data lane 1 (positive)	DSI0 Trio2 A	AL3
DSI0_D2N_T0B	AIO	DSI0 data lane 2 (negative)	DSI0 Trio0 B	AJ4
DSI0_D2P_T0A	AIO	DSI0 data lane 2 (positive)	DSI0 Trio0 A	AJ3
DSI0_D3N	AIO	DSI0 data lane 3 (negative)	-	AN4
DSI0_D3P_T2C	AIO	DSI0 data lane 3 (positive)	DSI0 Trio2 C	AM4
DSI_TE	DI	DSI0 tearing effect control	DSI0 tearing effect control	AT10, AT11

3.8.2.15.2 DSI Timing Characteristics

The DSI interface timing and electrical characteristics are compliant with MIPI DSI Specification v01-02-00, MIPI D-PHY Specification v1.2, and MIPI C-PHY Specification v1.0.

3.8.2.16 High-Definition Multimedia Interface Transmitter (HDMITX)

The HDMITX module encodes video, audio and control data into Transition-Minimized Differential Signaling (TMDS) format for digital transmission based on HDMI Specification 2.0b, and transfers the uncompressed digital data streams to an HDMI-compatible sink device.

The HDMITX supports the following video features:

- Deep Color mode: up to 16 bits
- Maximum operating frequency: up to 594 MHz
- Video color space options: RGB444, YCbCr 4:2:2 (ITU 601 and 709), YCbCr 4:4:4 (ITU 601 and 709), YCbCr 4:2:0, and xvYCC
- 3D HDMI function
- SD mode resolutions:
  - 1440 × 480i (pixel repeat 2) @59.94/60 Hz
  - 720 × 480p @ 59.94/60 Hz
  - 1440 × 576i (pixel repeat 2) @50 Hz
  - 720 × 576p @50 Hz
- HD/FHD/UFHD mode resolutions:
  - 1280 × 720p @ 59.94/60/50 Hz
  - 1920 × 1080i @ 59.94/60/50 Hz
  - 1920 × 1080p @ 59.94/60/50 Hz
  - 1920 × 1080p @ 23.97/24 Hz
  - 1920 × 1080p @ 25 Hz
  - 1920 × 1080p @ 29.97/30 Hz
  - 3840 × 2160p @ 29.97/30 Hz
  - 3840 × 2160p @ 59.94/60/50 Hz

The HDMITX supports the following audio features:

- Single compressed S/PDIF IEC61937 (up to 192 kHz)
- Single LPC S/PDIF IEC60958 (up to 192 kHz and up to 24 bits), 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz
- Multi-channel PCM input (maximum 8 channels)
- DSD audio
- Compressed lossless audio according to HDMI 2.0 (Dolby TrueHD and DTS-HD)

Additionally, the HDMITX supports the following general features:

- HPD line
- Discovery by EDID
- Compatible with DVI 1.0
- HDCP 1.4 / HDCP 2.3 function
- Support of dynamic metadata maximum to 2KB
- I^2C-based Display Data Channel (DDC) with clock stretching

- Variable Refresh Rate (VRR) / Auto Low Latency Mode (ALLM)
- CEC channel shared with HDMIRX

3.8.2.16.1 HDMITX Signal Descriptions

Table 3-24 presents HDMITX signal descriptions.

Table 3-24 HDMITX Signal Descriptions

Signal Name	Type	Description	Ball Location
HDMITX20_CEC	DIO	HDMITX CEC channel (shared with HDMIRX)	AM23
HDMITX20_HTPLG	DI	HDMITX HPD line	AM24
HDMITX20_PWR5V	DO	HDMITX power supply (+5 V)	AL24
HDMITX20_SCL	DIO	HDMITX DDC/I2C clock	AL23
HDMITX20_SDA	DIO	HDMITX DDC/I2C data	AL25
HDMITX21_CH0_M	AO	HDMITX TMDS data lane 0 (negative)	AR32
HDMITX21_CH0_P	AO	HDMITX TMDS data lane 0 (positive)	AR33
HDMITX21_CH1_M	AO	HDMITX TMDS data lane 1 (negative)	AT34
HDMITX21_CH1_P	AO	HDMITX TMDS data lane 1 (positive)	AU34
HDMITX21_CH2_M	AO	HDMITX TMDS data lane 2 (negative)	AR35
HDMITX21_CH2_P	AO	HDMITX TMDS data lane 2 (positive)	AR36
HDMITX21_CLK_M	AO	HDMITX TMDS clock lane (negative)	AT31
HDMITX21_CLK_P	AO	HDMITX TMDS clock lane (positive)	AU31

3.8.2.17 Display MUTEX (DISP_MUTEX)

The device supports multiple display paths. The DISP_MUTEX is used to synchronize the start trigger signal of each submodule in the display paths. Each display path can be configured with different and independent timings, and multiple DISP_MUTEX cores are assigned to each path.

The DISP_MUTEX supports the following key features:

- Up to 16 MUTEX cores in parallel
- Each submodule in the display path can be assigned to any one of the MUTEX cores
- The start trigger signal selection for each MUTEX core is driven either from SW or from a display interface controller (DSI, DPI, EDPTX/DPTX, HDMITX)

The start trigger method determines the operation mode of the display path:

- Single mode (SW trigger):
  - Single frame processing upon every SW trigger
  - Memory in - memory out path
  - Memory in and direct link to command mode display output (for example, DSI command mode)
- Refresh mode (display interface trigger):
  - Frame-by-frame processing after start
  - Memory in and direct link to video mode display output (for example, DSI video mode, DPI)

3.8.2.18 Display Pulse Width Modulation (DISP_PWM) and Reset

The DISP_PWM module provides PWM signals for the LED driver of an LCM in order to reduce its backlight power consumption.

The DISP PWM supports the following features:

- Gradual PWM control
- Operating clocks: 16 MHz, 26 MHz, 65 MHz, 104 MHz, or 130 MHz

Additionally, the device provides reset signals for the DPI interface, which can be used to reset an external LCM.

3.8.2.18.1 DISP_PWM and Reset Signal Descriptions

Table 3-25 presents the DISP_PWM and reset signal descriptions.

Table 3-25 DISP_PWM and Reset Signal Descriptions

Signal Name	Type	Description	Ball Location
DISP_PWM0	DO	Display PWM output 0	AP9
DISP_PWM1	DO	Display PWM output 1	AN11
LCM_RST	DO	DPI reset signal 0	AL10
LCM1_RST	DO	DPI reset signal 1	AL18

3.8.3 Warp Engine (WPE)

The WPE provide image geometry warping function which can be standalone or in-line linked with SVPP-0 and SVPP-1. The WPE uses backward mapping method to process lens distortion. The WPE reads image data from DRAM and outputs image data to DRAM.

The WPE supports the following key features:

- Input/output color formats:
  - Y/U/V only 8-/10-bit
  - UV420 8-/10-bit
  - UV422 8-/10-bit
  - YUV420 8-/10-bit (including of Arm Frame Buffer Compression (AFBC) format)
  - YUV422 8-/10-bit
- Input/output color range: Full 8-bit (0-255), or 10-bit (0-1023)
- Input/output maximum image size: 8000 × 6000
- Frame rate: 30fps
- WarpMap size: From 2×2 up to 640 × 480
- Latency (one frame delay): 33 ms
- Interpolation methods:
  - Bi-linear interpolation for WarpMap processing
  - Bi-cubic filtering for output image processing
- WPE cache size: 32KB

3.8.4 Multimedia SRAM (MMSYSRAM)

The MMSYSRAM is a shared SRAM used by some modules in the video and display data paths, such as VENC，CAMSYS and MCUSYS/APUSYS.

The MMSYSRAM supports the following main features:

- Size: 2.375 MB
- Address Protection Controller (APC)
- Memory Protection Unit (MPU)
- Up to 8 masters at the same time
- Up to 8 regions split

3.8.5 In-Line Rotation Controller (INLINEROT)

The INLINEROT module is used by MDP_WROT and DISP_OVL to exchange data through MMSYSRAM in order to decrease DRAM transactions bandwidth.

3.9 Imaging

The Camera Imaging Subsystem (CAMSYS) is built around a feature-rich Image Signal Processor (ISP) and a deep learning Face Detection (FD) engine. The ISP processes data received either from camera sensors through MIPI CSI-2 interface or system DRAM.

3.9.1 Camera Image Signal Processor (ISP)

The ISP consists of two engines—a real-time engine (pass 1) and an offline engine (pass 2). The processed data is stored into system DRAM.

The ISP supports the following key features:

- 3× MIPI CSI-2 high-speed camera serial interfaces:
  - Up to 4× data lanes of MIPI D-PHY 2.5 Gbps per lane
  - Up to 3× trios of MIPI C-PHY 4.5 Gsps per trio
- Single camera capture: up to 48MP at 30fps
- Dual camera capture: up to 16MP + 16MP at 30fps
- Video High Dynamic Range (HDR) with stagger HDR sensor: up to 12MP at 30fps
- Full size image capture for preview
- Image processing functions:
  - Auto sensor defect pixel correction
  - Lens shading correction
  - Edge enhancement
  - Video stabilization
  - Motion compensated temporal noise reduction for video recording
  - Electronic image stabilization
  - Multiple frame noise reduction for image capture
  - Zero shutter delay image capture
  - Preference color adjustment
  - AE/AWB/AF statistics collection
  - Three-frame stagger HDR fusion
  - Color aberration correction
  - Anti-blooming correction
  - YUV frame buffer compression

3.9.1.1 Camera Signal Descriptions

Table 3-26 presents camera signal descriptions.

Table 3-26 Camera Signal Descriptions

Signal Name	Type	Description	Ball Location
CMFLASH0	DO	Camera flash strobe 0	AN25
CMFLASH1	DO	Camera flash strobe 1	AN24
CMFLASH2	DO	Camera flash strobe 2	AM25
CMFLASH3	DO	Camera flash strobe 3	AP24
CMMCLK0	DO	Sensor reference clock 0	AL27
CMMCLK1	DO	Sensor reference clock 1	AK27
CMMCLK2	DO	Sensor reference clock 2	AM28
CMMCLK3	DO	Sensor reference clock 3	AL26
CMMCLK4	DO	Sensor reference clock 4	AM26
CMMPDN	DO	Power down to sensor	AM26
CMMRST	DO	Reset control to sensor	AL26
CMVREF0	DO	Camera frame sync 0	AM23
CMVREF1	DO	Camera frame sync 1	AL23
CMVREF2	DO	Camera frame sync 2	AL25
CMVREF3	DO	Camera frame sync 3	H32
CMVREF4	DO	Camera frame sync 4	H34

3.9.2 Face Detection (FD)

The Face Detection (FD) engine uses a convolutional neural network algorithm to detect faces on a source image and output the detected coordinates of the face windows and their confidence values.

The FD engine supports the following key features:

- Input image formats:
  - YUV420: 2 plane (Y/UV)
  - YUV422: 2 plane (Y/UV, Y/VU)
  - YUV422: 1 plane (YUYV, YVYU, UYVY, VYUY)
  - Mono 8-bit 1 plane
- YUV to RGB888 format conversion
- Image up/down-scaling
  - Maximum resize width: 640 pixels

3.9.3 Camera Serial Interface (CSI)

The CSI is based on MIPI Alliance Specification for Camera Serial Interface 2 (MIPI CSI-2) Version 2.1. The CSI provides high-speed serial data transfer between the ISP and external camera image sensors.

The device features two MIPI CSI-2 controllers (CSI0 and CSI1), which are fully compliant with the MIPI CSI-2 specification. The CSI0 contoller uses a MIPI D-PHY physical layer, while the CSI1 controller utilizes a combined MIPI D-PHY/C-PHY physical layer. The PHY layer is based on MIPI D-PHY Specification Revision 1.2 and acts as a physical link between the CSI controllers and image sensors.

The MIPI CSI-2 implementation in the device provides the following key features:

- Primary CSI-2 interface (CSI0), which can be used in the following configuration:
  - Two 4-data lane interfaces in D-PHY mode
- Secondary CSI-2 interface (CSI1), which can be used in one of the following configurations:
  - Two 2-data lane interfaces in D-PHY mode, or
  - One 4-data lane interface in D-PHY mode, or
  - One 3-trio interface in C-PHY mode, or
  - Two 2-trio interfaces in C-PHY mode
- Pixel formats: RAW8/RAW10/RAW12/RAW14/YUV422 8-bit
- No support for D-PHY escape mode and bus turnaround

3.9.3.1 CSI Signal Descriptions

Table 3-27 presents CSI0 signal descriptions.

Table 3-27 CSI0 Signal Descriptions

Signal Name[1]	Type	Description	Ball Location
		2 × D-PHY 4-lane Mode	
CSI0A_L0N	AIO	CSI0 port 0 data lane 2 (negative)	J36
CSI0A_L0P	AIO	CSI0 port 0 data lane 2 (positive)	J35
CSI0A_L1N	AIO	CSI0 port 0 data lane 0 (negative)	L34
CSI0A_L1P	AIO	CSI0 port 0 data lane 0 (positive)	K35
CSI0A_L2N	AIO	CSI0 port 0 clock lane (negative)	K33
CSI0A_L2P	AIO	CSI0 port 0 clock lane (positive)	K34
CSI0B_L0N	AIO	CSI0 port 0 data lane 1 (negative)	L33
CSI0B_L0P	AIO	CSI0 port 0 data lane 1 (positive)	L32
CSI0B_L1N	AIO	CSI0 port 0 data lane 3 (negative)	M32
CSI0B_L1P	AIO	CSI0 port 0 data lane 3 (positive)	M33
CSI0C_L0N	AIO	CSI0 port 1 data lane 2 (negative)	M35
CSI0C_L0P	AIO	CSI0 port 1 data lane 2 (positive)	N35
CSI0C_L1N	AIO	CSI0 port 1 data lane 0 (negative)	N33

Signal Name(1)	Type	Description	Ball Location
CSI0C_L1P	AIO	CSI0 port 1 data lane 0 (positive)	N34
CSI0C_L2N	AIO	CSI0 port 1 clock lane (negative)	N32
CSI0C_L2P	AIO	CSI0 port 1 clock lane (positive)	N31
CSI0D_L0N	AIO	CSI0 port 1 data lane 1 (negative)	L37
CSI0D_L0P	AIO	CSI0 port 1 data lane 1 (positive)	L36
CSI0D_L1N	AIO	CSI0 port 1 data lane 3 (negative)	M36
CSI0D_L1P	AIO	CSI0 port 1 data lane 3 (positive)	M37

1. Unused CSI ports could be connected to GND or set in not connected.

Table 3-28 presents CSI1 signal descriptions.

Table 3-28 CSI1 Signal Descriptions

Signal Name(2)	Type	Description			Ball Location
		1 × D-PHY 4-lane Mode	2 × D-PHY 2-lane Mode	1 × C-PHY 3-trio Mode	
CSI1A_L0N_T0B	AIO	CSI1 data lane 2 (negative)	CSI1 port 0 data lane 0 (negative)	CSI1 Trio0 B	R33
CSI1A_L0P_T0A	AIO	CSI1 data lane 2 (positive)	CSI1 port 0 data lane 0 (positive)	CSI1 Trio0 A	R32
CSI1A_L1N_ T1A	AIO	CSI1 data lane 0 (negative)	CSI1 port 0 clock lane (negative)	CSI1 Trio1 A	R35
CSI1A_L1P_T0C	AIO	CSI1 data lane 0 (positive)	CSI1 port 0 clock lane (positive)	CSI1 Trio0 C	R34
CSI1A_L2N_T1C	AIO	CSI1 clock lane (negative)	CSI1 port 0 data lane 1 (negative)	CSI1 Trio1 C	R37
CSI1A_L2P_T1B	AIO	CSI1 clock lane (positive)	CSI1 port 0 data lane 1 (positive)	CSI1 Trio1 B	R36
CSI1B_L0N_T0B	AIO	CSI1 data lane 1 (negative)	CSI1 port 1 data lane 0 (negative)	CSI1 Trio2 B	T37
CSI1B_L0P_T0A	AIO	CSI1 data lane 1 (positive)	CSI1 port 1 data lane 0 (positive)	CSI1 Trio2 A	T36
CSI1B_L1N_T1A	AIO	CSI1 data lane 3 (negative)	CSI1 port 1 clock lane (negative)	-	T34
CSI1B_L1P_T0C	AIO	CSI1 data lane 3 (positive)	CSI1 port 1 clock lane (positive)	CSI1 Trio2 C	T35
CSI1B_L2N_T1C	AIO	-	CSI1 port 1 data lane 1 (negative)	-	T32
CSI1B_L2P_T1B	AIO	-	CSI1 port 1 data lane 1 (positive)	-	T33

2. Unused CSI ports could be connected to GND or set in not connected.

3.9.3.2 CSI Timing Characteristics

The CSI interface timing characteristics are compliant with MIPI CSI-2 Specification v2.1, MIPI D-PHY Specification v1.2, and MIPI C-PHY Specification v1.0.

3.10 Video

The device has two video accelerators—Video Encoder (VENC) and Video Decoder (VDEC).

3.10.1 Video Encoder (VENC)

The VENC accelerator supports main stream H.264 and HEVC video encoding. It is capable of encoding 4K video at 60 fps superior video quality. The VENC supports various encoding methods that satisfy basic requirements of easy control by software. The VENC brings astonishing high quality and low memory bandwidth requirements, with advanced encoding technology. The accelerator also considers the usage of portable devices and provides several power saving capabilities.

The VENC has the following main features:

- Uses DRAM as an input, output, and working buffer
- Reads input frame buffers, executes video encoding and writes encoded bit stream to the output buffer
- Support of YUV420 two-plane scan line (NV12/NV21) and YUV420 three-plane scan line (YV12/I420) color spaces

Table 3-29 presents the supported video formats and their capabilities.

Table 3-29 VENC Supported Formats

Format	Feature	Details
H.264 Encoding	Profile	High (10-bit)
	Level	L5.2
	Speed	4K @ 60 fps (100 Mbps)
HEVC Encoding	Profile	Main (10-bit)
	Level	L5.1
	Speed	4K @ 60 fps (100 Mbps)

3.10.2 Video Decoder (VDEC)

The VDEC accelerator provides multi-standard video decoding feature. The main purpose of the accelerator is to relieve CPU usage while providing high performance video decompression. The input to VDEC is a compressed video bitstream. After decoding process, the reconstructed video is written into DRAM and then sent to the display subsystem.

The VDEC supports various multimedia video formats, including:

- HEVC decoder:
  - Main profile / Main 10 profile
  - Maximum level: L5.1
  - 4K2K @ 90fps (160 Mbps)
- H.264 decoder:
  - Constrained Baseline Profile (CBP) / Main profile / High profile / High 10 profile
  - Maximum level: L5.2
  - 4K2K @ 90fps (160 Mbps)
- MPEG-4 decoder:
  - Simple Profile (SP)
    - Maximum level: L6
    - 1080p @ 60 fps (60 Mbps)
  - Advanced Simple Profile (ASP)
    - Maximum level: L5
    - 1080p @ 60 fps (60 Mbps)
- MPEG-1/MPEG-2 decoder:
  - Main profile
  - Maximum level: High
  - 1080p @ 60 fps (60 Mbps)
- VP8 decoder:
  - 1080p @ 60 fps (40 Mbps)
- VP9 decoder:
  - Profile 0 / profile 2
  - 4K2K @ 90 fps (120 Mbps)
- AV1 decoder:
  - Main profile
  - Maximum level: L5.1
  - 4K2K @ 90 fps (120 Mbps)
- H.263 decoder:
  - Baseline profile
  - 1080p @ 60 fps (60 Mbps)
- Sorenson H.263

- High Efficiency Image File (HEIF) format decoder:
  - Main profile / Main10 profile
  - Maximum resolution 16383 × 16383
- De-blocking filter for MPEG-2, H.263
- Error handling

The VDEC supports 8K @ 30 fps under the below limitations:

- Maximum picture width/height: 8192 pixels/lines
- If picture width is > 4096 pixels, then picture height is ≤ 4096 lines
- If picture height is > 4096 lines, then picture width is ≤ 4096 pixels
- Maximum pixel number per frame is 8192 × 4096

3.11 Audio

The audio subsystem provides audio data exchange between the device and external audio components. The device has the following audio interfaces:

- One master I^2S output:
  - 24-channel I^2S output. Sampling rates from 8 kHz to 384 kHz, up to 32 bits
  - 16-channel Time Division Multiplexing (TDM) output. Sampling rates from 8 kHz to 48 kHz, up to 32 bits
  - 6-channel Direct Stream Digital (DSD) with clock rate of 2.8 MHz or 2-channel DSD with clock rates of 5.6 MHz or 11.2 MHz
- One master or slave I^2S output:
  - 8-channel I^2S output. Sampling rates from 8 kHz to 384 kHz, up to 32 bits
  - 24-channel TDM output with 16 kHz sampling rate or 16-channel @ 48 kHz
- One master or slave I^2S input:
  - 8-channel I^2S input. Sampling rates from 8 kHz to 384 kHz and resolution up to 32 bits
  - 8-channel TDM input. Sampling rates from 8 kHz to 48 kHz, up to 32 bits, or 16-channel direct path to memory
- One master or slave TDM input:
  - 24-channel TDM output with 16 kHz sampling rate and bit resolution up to 32 bits or 16-channel @ 48 kHz
  - 2-channel I^2S input. Sampling rates from 8 kHz to 384 kHz and resolution up to 32 bits
- One master 8-channel High-Definition Multimedia Interface (HDMI™) audio output (HDMITX):
  - Sampling rates from 8 kHz to 192 kHz with resolution of up to 24 bits
  - 6-channel DSD Out with clock rate of 2.8 MHz or 2-channel DSD Out with clock rates of 5.6 MHz or 11.2 MHz, or
  - 8-channel DisplayPort™ audio output with sampling rates from 8 kHz to 192 kHz, up to 24 bits
- HDMIRX audio input with Direct Stream Digital (DSD) support
- One S/PDIF input. Sampling rates include 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
- One S/PDIF output with 32, 44.1, 48, 88.2, 96, and 192 kHz sampling rates
- One master or slave PCM interface with Sampling Rate Converter (SRC). Supported sampling rates: 8, 16, 32, 44.1, and 48 kHz
- One slave 8-channel I^2S input (AUDIO IN)
- 4 × Pulse Density Modulation (PDM) interfaces for up to 4 stereo Digital Microphones (DMICs). Support of one-wire and two-wire modes with 8, 16, 32, and 48 kHz PCM sampling rates and 24 bits
- A proprietary audio interface for PMIC CODEC
  - 2-channel DAC. Supports up to 192 kHz sampling rate
  - 3-channel ADC. Supports up to 192 kHz sampling rate

Audio subsystem features:

- Audio playing
  - Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2,96, 176.4, 192, 352.8, and 384 kHz sampling rates
- Audio recording
  - Support of 8, 16, 32, 48, 96, and 192 kHz sampling rates
  - Support of recording of up to 8-channel audio data
- 20 × stereo general-purpose Asynchronous Sample Rate Converters (ASRC) for sampling rate conversion and slave mode clock tracking
- 12 × stereo memory-based ASRC
- 2 × stereo hardware gain
- 32-channel channel merge

- 5 × APLL can support up to 5 clock rates at the same time
- 64KB internal audio SRAM

Figure 3-13 shows the Audio interfaces block diagram.

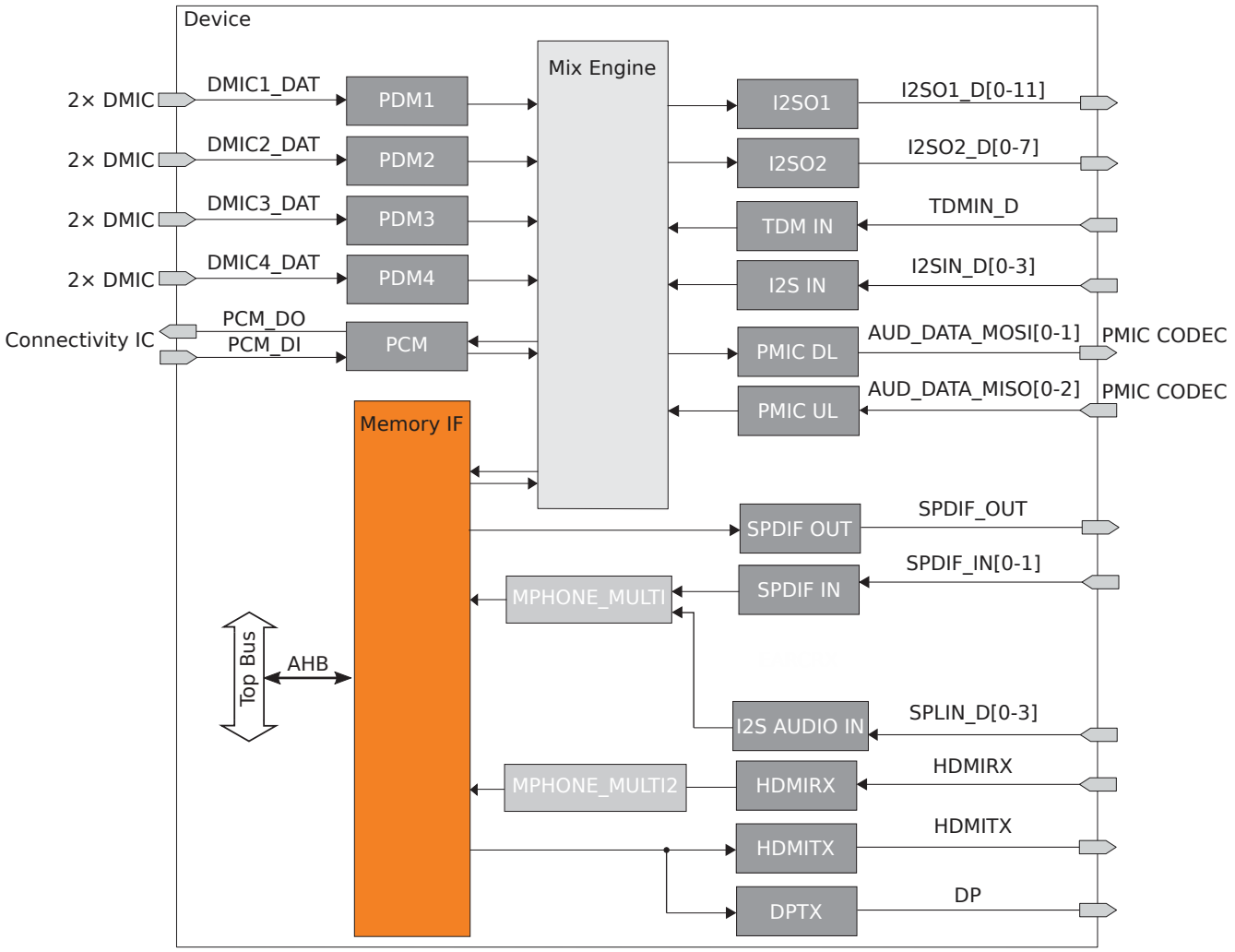


Figure 3-13 Audio Interfaces Block Diagram

3.11.1 Inter-IC Sound (I2S)

3.11.1.1 I2S Signal Descriptions

Table 3-30 presents I2S signal descriptions.

Table 3-30 I2S Signal Descriptions

Signal Name	Type	Description	Ball Location
I2SIN			
I2SIN_BCK	DIO	I2SIN serial bit clock	AK20, AL10
I2SIN_D0	DI	I2SIN serial data input 0	AP20, AM8
I2SIN_D1	DI	I2SIN serial data input 1	AT12, AT10
I2SIN_D2	DI	I2SIN serial data input 2	AT14, AR8
I2SIN_D3	DI	I2SIN serial data input 3	AP8, AT9
I2SIN_MCK	DIO	I2SIN master clock	AL20, AT11
I2SIN_WS	DIO	I2SIN word select (left/right audio channel)	AR20, AT9
I2SO1			
I2SO1_BCK	DO	I2SO1 serial bit clock	AK19

Signal Name	Type	Description	Ball Location
I2SO1_D0	DO	I2SO1 serial data output 0	AR18
I2SO1_D1	DO	I2SO1 serial data output 1	AP18
I2SO1_D2	DO	I2SO1 serial data output 2	AN18
I2SO1_D3	DO	I2SO1 serial data output 3	AM18
I2SO1_D4	DO	I2SO1 serial data output 4	H32
I2SO1_D5	DO	I2SO1 serial data output 5	H34
I2SO1_D6	DO	I2SO1 serial data output 6	E37
I2SO1_D7	DO	I2SO1 serial data output 7	F34
I2SO1_D8	DO	I2SO1 serial data output 8	AM8
I2SO1_D9	DO	I2SO1 serial data output 9	AT10
I2SO1_D10	DO	I2SO1 serial data output 10	AR8
I2SO1_D11	DO	I2SO1 serial data output 11	AP8
I2SO1_MCK	DO	I2SO1 master clock	AN19
I2SO1_WS	DO	I2SO1 word select (left/right audio channel)	AT19
I2SO2			
I2SO2_BCK	DIO	I2SO2 serial bit clock	AK18, AP17
I2SO2_D0	DO	I2SO2 serial data output 0	AT20, AT6
I2SO2_D1	DO	I2SO2 serial data output 1	AN12, AT7
I2SO2_D2	DO	I2SO2 serial data output 2	AU14, AT8
I2SO2_D3	DO	I2SO2 serial data output 3	AT13, AU8
I2SO2_MCK	DO	I2SO2 master clock	AL18
I2SO2_WS	DIO	I2SO2 word select (left/right audio channel)	AU20, AL17
SPLIN			
SPLIN_BCK	DI	SPLIN serial bit clock	AR20
SPLIN_D0	DI	SPLIN data 0	AP20
SPLIN_D1	DI	SPLIN data 1	AP18
SPLIN_D2	DI	SPLIN data 2	AN18
SPLIN_D3	DI	SPLIN data 3	AM18
SPLIN_LRCK	DI	SPLIN word select	AK20
SPLIN_MCK	DI	SPLIN master clock	AL20

3.11.1.2 I2S Timing Characteristics

Table 3-31, Figure 3-14, and Figure 3-15 present timing characteristics for the I2S modules in the device.

Table 3-31 I2S Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
-	f_S	Sampling frequency	8		384	kHz
IIS01	f_{c_MCK}	Cycle time, MCK (master clock)			49.152	MHz
-	f_{OP_BCK}	Operation frequency, BCK	$32 \times f_S$		$64 \times f_S$	MHz
IIS03	t_{c_BCK}	Cycle time, BCK	81		3906	ns
IIS04	$t_{w\_BCK\_H}$	Pulse duration, BCK high		0.5		$1 / t_{c\_BCK}$
IIS05	$t_{w\_BCK\_L}$	Pulse duration, BCK low		0.5		$1 / t_{c\_BCK}$
-	t_{LRCK}	LRCK period	32		64	$1 / t_{c\_BCK}$
IIS06	t_{v_LRCK}	BCK negative edge to LRCK valid			0.2	$1 / t_{c\_BCK}$
IIS07	t_{v_DO}	BCK negative edge to DO valid			0.2	$1 / t_{c\_BCK}$
IIS08	t_{su}	Setup time, DI	0.2			$1 / t_{c\_BCK}$
IIS10	t_h	Hold time, DI	0.2			$1 / t_{c\_BCK}$

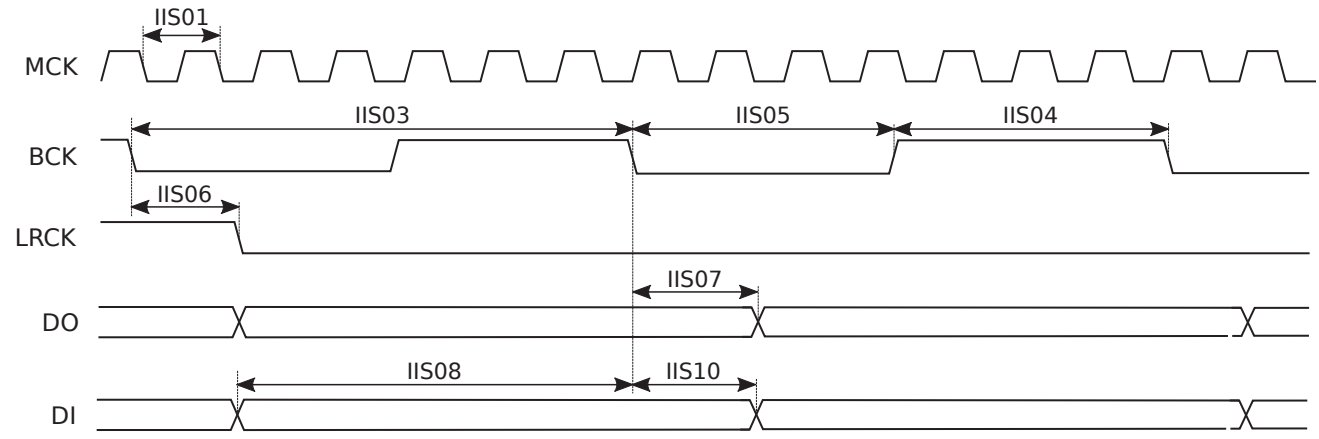


Figure 3-14 I2S Master Mode Timing Diagram

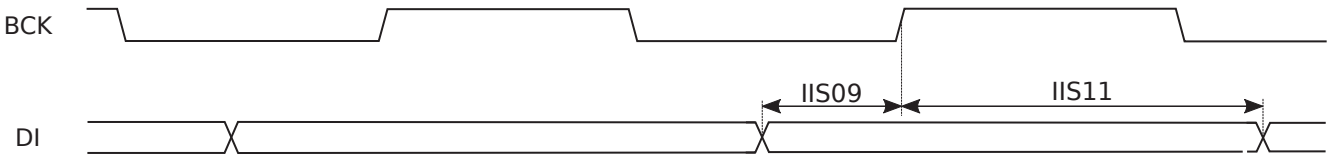


Figure 3-15 I2S Slave Mode Timing Diagram

3.11.2 Pulse-Code Modulation (PCM)

3.11.2.1 PCM Signal Descriptions

Table 3-34 presents PCM signal descriptions.

Table 3-32 PCM Signal Descriptions

Signal Name	Type	Description	Ball Location
PCM_CLK	DIO	PCM clock	AP16
PCM_DI	DI	PCM data input	AN16
PCM_DO	DO	PCM data output	AR16
PCM_SYNC	DIO	PCM synchronization	AM16

3.11.2.2 PCM Timing Characteristics

Table 3-33, Figure 3-16 and Figure 3-17 present timing characteristics for the PCM interfaces in the device.

Table 3-33 PCM Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_S	Sampling frequency	8		48	kHz
PCM1	f_{CLK}	Serial clock frequency	0.256		3.072	MHz
	t_{SYNC}	Sync period	32		64	$1 / f_{CLK}$
PCM2	$t_{w\_CLK\_H}$	Pulse duration, CLK high		0.5		$1 / f_{CLK}$
PCM3	$t_{w\_CLK\_L}$	Pulse duration, CLK low		0.5		$1 / f_{CLK}$
PCM4	$t_{d\_CLK\_SYNC}$	Delay time, output CLK low to SYNC valid			0.2	ns
PCM5	$t_{d\_CLK\_TX}$	Delay time, output CLK low to TX valid			0.2	ns
PCM6	t_{su}	Setup time, RX master mode	0.2			ns
PCM7	t_h	Hold time, RX master mode	0.2			ns
PCM8	t_{su}	Setup time, RX slave mode	0.2			ns
PCM9	t_h	Hold time, RX slave mode	0.2			ns

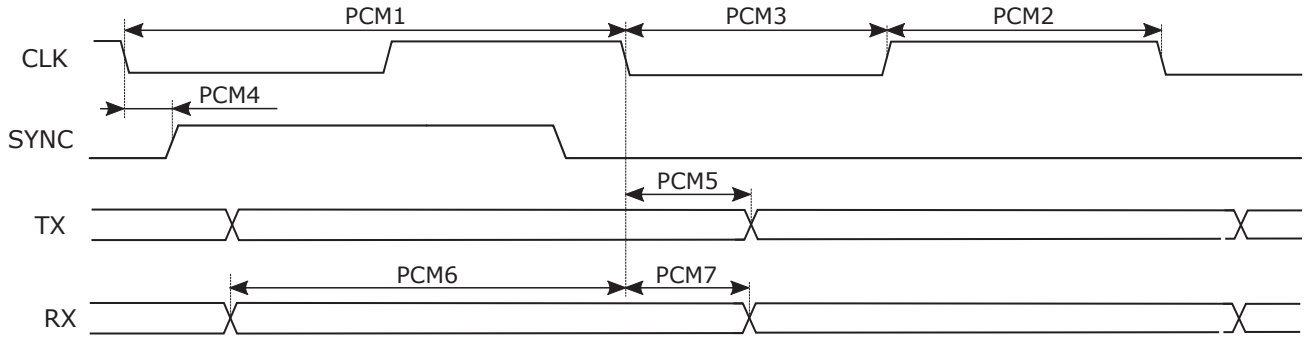


Figure 3-16 PCM Master Mode Timing Diagram

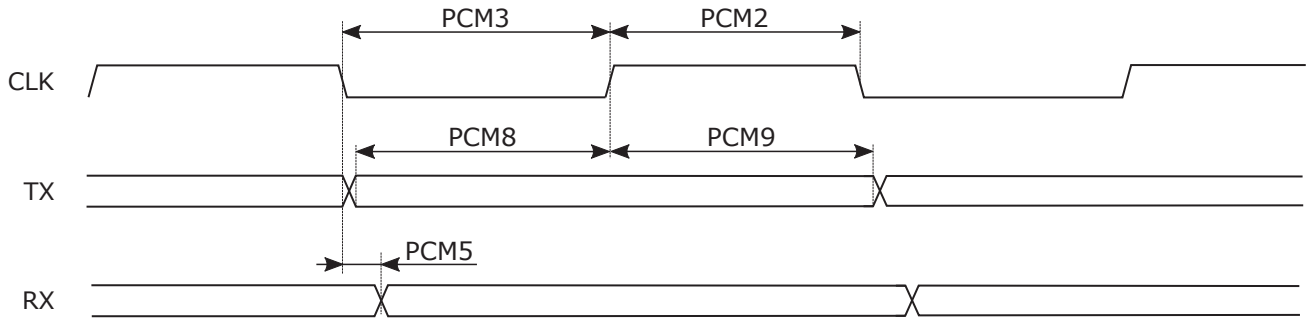


Figure 3-17 PCM Slave Mode Timing Diagram

3.11.3 Time Division Multiplexed (TDM) Interface

3.11.3.1 TDM Signal Descriptions

Table 3-34 presents TDM signal descriptions.

Table 3-34 TDM Signal Descriptions

Signal Name	Type	Description	Ball Location
TDMIN_BCK	DIO	TDM clock	G33, G36
TDMIN_DI	DI	TDM receive data input	G34, F37
TDMIN_LRCK	DIO	TDM word select (left/right audio channel)	J31, F36
TDMIN_MCK	DIO	TDM receive master clock	H31, F35

3.11.3.2 TDM Timing Characteristics

Table 3-35 and Figure 3-18 present timing characteristics for the TDM interfaces in the device.

Table 3-35 TDM Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_S	Sampling frequency	8		192	kHz
TDM1	f_{MCK}	Master clock frequency	0.768		49.152	MHz
TDM2	f_{BCK}	Serial clock frequency	0.256		49.152	MHz
TDM3	$t_{w\_BCK\_H}$	Pulse duration, BCK high		0.5		1 / f_{BCK}
TDM4	$t_{w\_BCK\_L}$	Pulse duration, BCK low		0.5		1 / f_{BCK}
TDM5	$t_{d\_BCLK\_WS}$	Delay time, output BCLK low to WS valid			0.2	ns

No.	Parameter		Min	Typ	Max	Unit
TDM6	$t_{d\_BCLK\_SDOUT}$	Delay time, output BCLK low to SDOUT valid			0.2	ns
TDM7	t_{su_DI}	Setup time, DI	0.2			ns
TDM8	t_{h_DI}	Hold time, DI	0.2			ns

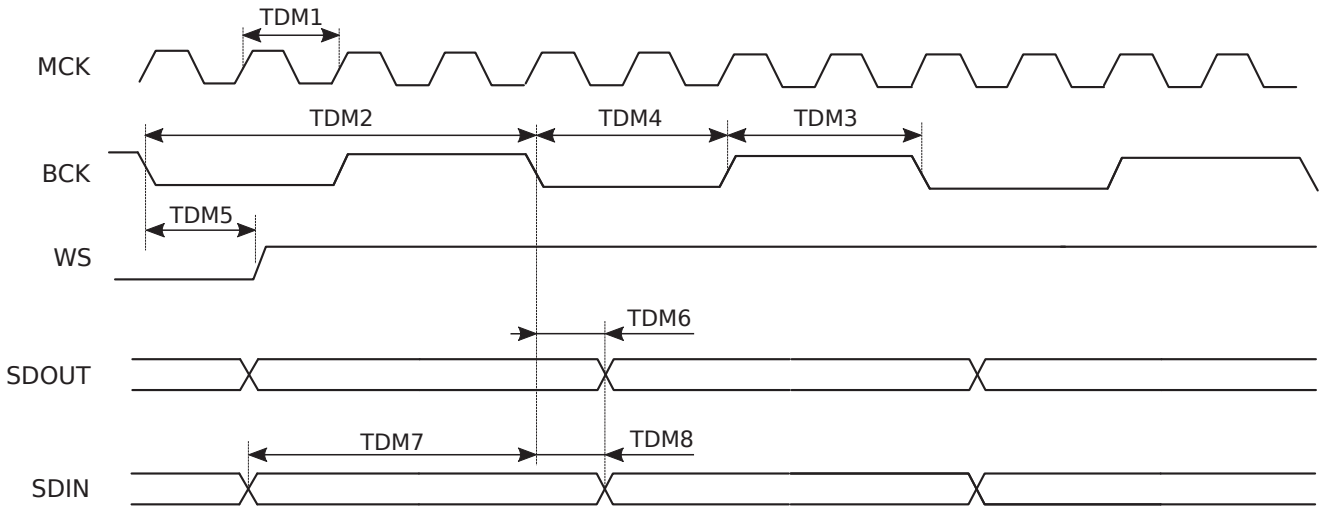


Figure 3-18 TDM Master Mode Timing Diagram

3.11.4 Pulse Density Modulation (PDM)

3.11.4.1 PDM Timing Characteristics

Table 3-36 and Figure 3-19 present timing characteristics for the PDM interface in the device.

Table 3-36 PDM Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
	f_{CLK}	Operating frequency, PDM CLK	0.40625	-	3.25	MHz
PDM2	$t_{W\_CLK\_H}$	Pulse duration, CLK high	-	0.5	-	1 / f_{CLK}
PDM3	$t_{W\_CLK\_L}$	Pulse duration, CLK low	-	0.5	-	1 / f_{CLK}
PDM4	t_{SU_DAT}	Setup time, DAT	0.2	-	-	1 / f_{CLK}
PDM5	t_{H_DAT}	Hold time, DAT	0.2	-	-	1 / f_{CLK}

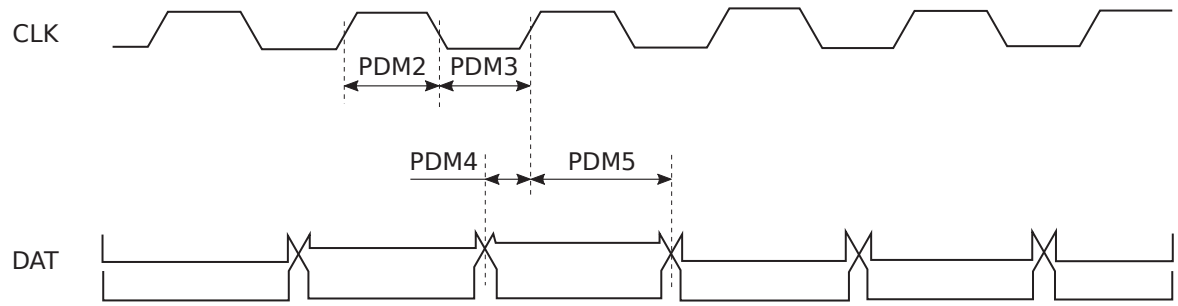


Figure 3-19 PDM Timing Diagram

3.11.4.2 Digital Microphone (DMIC)

3.11.4.2.1 DMIC Signal Descriptions

Table 3-37 presents DMIC signal descriptions.

Table 3-37 DMIC Signal Descriptions

Signal Name	Type	Description	Ball Location
DMIC1_CLK	DO	DMIC1 clock	AK27, AP17
DMIC1_DAT	DI	DMIC1 data in one-wire mode or data left	AM28, AL17
DMIC1_DAT_R	DI	DMIC1 data right	AL24
DMIC2_CLK	DO	DMIC2 clock	J31, AU18
DMIC2_DAT	DI	DMIC2 data in one-wire mode or data left	G33, AT18
DMIC2_DAT_R	DI	DMIC2 data right	AL21
DMIC3_CLK	DO	DMIC3 clock	H32, F37, AP22
DMIC3_DAT	DI	DMIC3 data in one-wire mode or data left	H34, F35, AN23
DMIC3_DAT_R	DI	DMIC3 data right	E37
DMIC4_CLK	DO	DMIC4 clock	H31, G36, AP23
DMIC4_DAT	DI	DMIC4 data in one-wire mode or data left	G34, F36, AN22
DMIC4_DAT_R	DI	DMIC4 data right	F34

3.11.5 Digital Interface (SPDIF)

3.11.5.1 SPDIF Signal Descriptions

Table 3-38 presents SPDIF signal descriptions.

Table 3-38 SPDIF Signal Descriptions

Signal Name	Type	Description	Ball Location
SPDIF_IN0	DI	SPDIF input 0	H33, E35
SPDIF_IN1	DI	SPDIF input 1	G35, E36
SPDIF_OUT	DO	SPDIF output	D36, AL26

3.11.6 Power Management Integrated Circuit (PMIC)

3.11.6.1 PMIC Audio Interface Signal Descriptions

Table 3-39 presents PMIC audio interface signal descriptions.

Table 3-39 PMIC Audio Interface Signal Descriptions

Signal Name	Type	Description	Ball Location
AUD_CLK_MOSI(1)	DO	PMIC CODEC clock master output	AL16
AUD_DAT_MISO0	DI	PMIC CODEC data master input 0	AK15
AUD_DAT_MISO1	DI	PMIC CODEC data master input 1	AU17
AUD_DAT_MISO2	DI	PMIC CODEC data master input 2	AT17
AUD_DAT_MOSI0(1)	DO	PMIC CODEC data master output 0	AT16
AUD_DAT_MOSI1(1)	DO	PMIC CODEC data master output 1	AN15
AUD_SYNC_MOSI(1)	DO	PMIC CODEC sync master output	AK16

1. These pins should be left unconnected when unused.

3.12 Connectivity

3.12.1 Inter-Integrated Circuit (I2C) and Improved I2C (I3C)

The device contains six I2C and two I3C controllers providing an interface between the internal hosts and any I2C™ or MIPI I3C® bus compatible devices.

Each I2C module supports the following key features:

- Compliant with Philips I^2C-bus Specification version 2.1
- Standard-Speed (SS) communication mode (up to 100 Kbps)
- Fast-Speed (FS) communication mode (up to 400 Kbps)
- Fast-Speed Plus (FS+) communication mode (up to 1 Mbps)
- High-Speed (HS) communication mode (up to 3.4 Mbps)
- Adjustable clock speed for SS and FS modes
- Master mode of operation
- Support of manual transfer mode
- Multi-byte writes and reads per transfer
- Multi-byte write and read messages per transfer
- Combined format transfer with length change capability
- Repeated START condition in multiple transfer

Each I3C module supports the following additional features:

- Single Data Rate (SDR) transfer
- Serial Camera Control Bus (SCCB)
- Dynamic Address Assignment (DAA)
- Common Command Code (CCC)

The I2C/I3C controller is designed to monitor when the SCL and SDA signals are low to turn off the internal pull-up resistance, thus saving power. I2C/I3C PAD control supports:

- Eight settings of internal pull-up resistance: 1 kΩ, 1.5 kΩ, 2 kΩ, 3 kΩ, 4 kΩ, 5 kΩ, 10 kΩ (POR default), and 75 kΩ
- Four open-drain drive strengths: 0.31 mA, 0.63 mA, 1.12 mA, and 1.43 mA
- The IO_CONFIG register must be configured to 0x33 for open-drain

3.12.1.1 I2C/I3C Signal Descriptions

Table 3-40 presents I2C/I3C signal descriptions.

Table 3-40 I2C/I3C Signal Descriptions

Signal Name	Type	Description	Ball Location
I3C0(1)			
SCL0	DIO	I3C0 serial clock	D37
SDA0	DIO	I3C0 serial data	D36
I3C1(1)			
SCL1	DIO	I3C1 serial clock	E35
SDA1	DIO	I3C1 serial data	E36
I2C2(1)			
SCL2	DIO	I2C2 serial clock	H33, F34
SDA2	DIO	I2C2 serial data	G35, E37
I2C3(1)			
SCL3	DIO	I2C3 serial clock	F37
SDA3	DIO	I2C3 serial data	F35
I2C4(1)			
SCL4	DIO	I2C4 serial clock	G36, AM28
SDA4	DIO	I2C4 serial data	F36, AK27
I2C5			

Signal Name	Type	Description	Ball Location
SCL5	DIO	I2C5 serial clock	AM25, AN20
SDA5	DIO	I2C5 serial data	AP24, AM20
I2C6			
SCL6	DIO	I2C6 serial clock	AL28, AM26, AL23
SDA6	DIO	I2C6 serial data	AM29, AL26, AL25
I2C7			
SCL7	DIO	I2C7 serial clock	AN25, AL23
SDA7	DIO	I2C7 serial data	AN24, AL25

1. These modules have HW default internal 10 kΩ pull-up changed by the SW initialization to 1 kΩ and external pull-up resistors are not required.

3.12.1.2 I2C Timing Characteristics

Table 3-41 and Figure 3-20 present timing characteristics for the I2C interfaces in in SS/FS/FS+ modes.

Table 3-41 I2C Timing Characteristics (SS/FS/FS+ modes)

No.	Parameter		SS		FS		FS+		Unit
			Min	Max	Min	Max	Min	Max	
	t_c	Cycle time		10000		2500		1000	ns
IIC2	$t_{w\ high}$	Pulse duration, SCL high	4.0		0.6		0.26		µs
IIC3	$t_{w\ low}$	Pulse duration, SCL low	4.7		1.3		0.5		µs
IIC4	t_{RISE}	Rise time of SDA and SCL signals		100	20	300		120	ns
IIC5	t_{FALL} (1)	Fall time of SDA and SCL signals		300	20 × (VDD / 5.5 V)	300	20 × (VDD / 5.5 V)	120	ns
IIC6	t_{su}	Setup time, SDA to SCL	250		100		50		ns
IIC7	t_h (2)	Hold time, SDA to SCL	5.0		0		0		µs
IIC8	$t_{su\ start}$	Setup time, SCL to repeated START (Sr) condition	4.7		0.6		0.26		µs
IIC9	$t_{h\ start}$	Hold time, START (S) condition to SCL	4.0		0.6		0.26		µs
IIC10	$t_{h\ stop}$	Setup time, SCL to STOP (P) condition	4.0		0.6		0.26		ns
IIC11	$t_{(BUF)}$	Bus free time between STOP (P) and START (S) condition	4.7		1.3		0.5		ns
IIC12	t_{DV}	Data valid time		3.45		0.9		0.45	µs
IIC13	t_{DV_ACK}	Data valid acknowledge time		3.45		0.9		0.45	µs

1. VDD: I2C IO voltage
2. I2C-bus devices

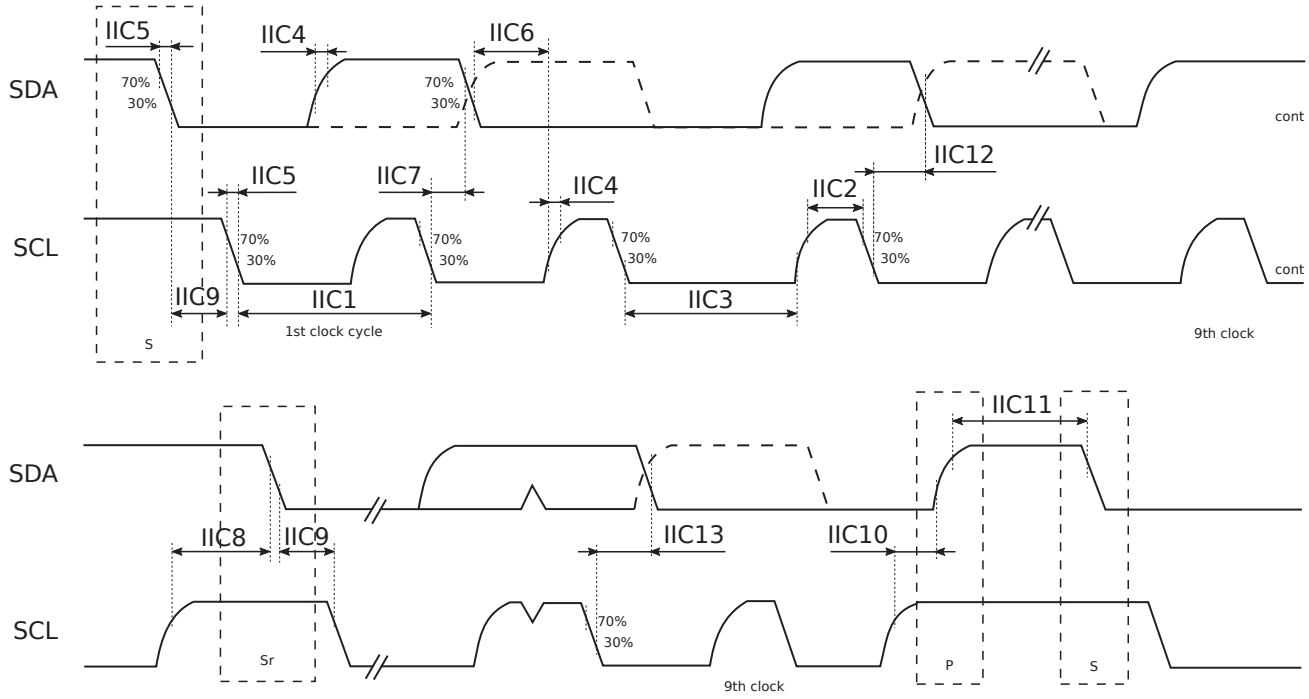


Figure 3-20 I2C Timing Diagram (SS/FS/FS+ modes)

Table 3-42 I2C Timing Characteristics (HS mode)

No.	Parameter		C_b = 100 pF (max)		C_b = 400 pF (max)		Unit
			Min	Max	Min	Max	
IIC1	t_c	Cycle time	0	294	0	588	ns
IIC2	$t_{su\ start}$	Setup time, SCL to repeated START condition	160		160		ns
IIC3	$t_{h\ start}$	Hold time, (repeated) START condition to SCL	160		160		ns
IIC4	$t_{w\ low}$	Pulse duration, SCL low	160		320		ns
IIC5	$t_{w\ high}$	Pulse duration, SCL high	60		120		ns
IIC6	t_h (1)	Hold time, SDA to SCL	0	70	0	150	ns
IIC7	t_{su}	Setup time, SDA to SCL	10		10		ns
IIC8	t_{RISE}	Rise time of SDA and SCL signals	10	40	20	80	ns
IIC9	t_{FALL}	Fall time of SDA and SCL signals	10	40	20	80	ns
IIC10	$t_{h\ stop}$	Setup time, SCL to STOP condition	160		160		ns

1. I2C-bus devices

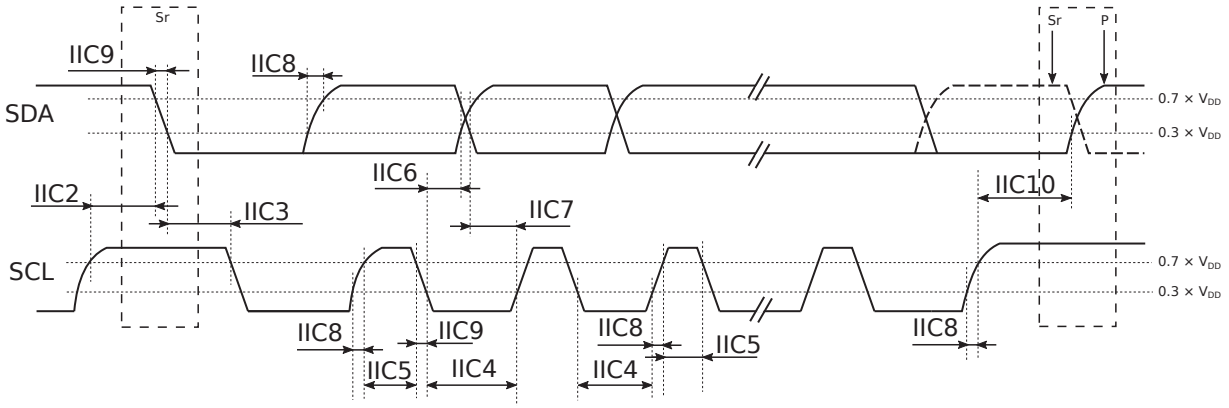


Figure 3-21 I2C Timing Diagram (HS mode)

3.12.2 Universal Asynchronous Receiver/Transmitter (UART)

The device supports six UART modules, which provide full-duplex serial communication with external devices. UART1 and UART2 are 4-pin channels (TX, RX, CTS, RTS) while UART0, UART3, UART4, and UART5 are 2-pin channels (TX, RX).

Each UART module supports the following key features:

- 16C450-compatible
- 16550A-compatible
- Configurable communication format:
  - 5, 6, 7, or 8 data bits
  - Optional parity bit
  - 1 or 2 stop bits
- Internal 16-bit programmable baud rate generator
- 8-bit scratch register
- Separate transmit and receive 32-byte FIFOs
- Programmable baud rates from 300 bps up to 3 Mbps
- Baud rate error less than 0.25%
- Two DMA handshake lines
- Internal diagnostic capabilities with loopback
- Polling, DMA, and interrupt modes of operation
- Hardware flow control (RTS/CTS)
- Software flow control (Xon/Xoff)

3.12.2.1 UART Signal Descriptions

Table 3-43 presents UART signal descriptions.

Table 3-43 UART Signal Descriptions

Signal Name	Type	Description	Ball Location
UART0			
URXD0	DI	UART0 receive data	AP10
UTXD0	DO	UART0 transmit data	AR10
UART1			
URXD1	DI	UART1 receive data	AP8
UTXD1	DO	UART1 transmit data	AR8
UCTS1	DI	UART1 clear to send (active low)	AT10
URTS1	DO	UART1 request to send (active low)	AM8
UART2			
URXD2	DI	UART2 receive data	AP24, AM16, AT14
UTXD2	DO	UART2 transmit data	AM25, AN16, AT12
UCTS2	DI	UART2 clear to send (active low)	AN25, AR16, AL9
URTS2	DO	UART2 request to send (active low)	AN24, AP16, AM10
UART3			
URXD3	DI	UART3 receive data	H33
UTXD3	DO	UART3 transmit data	G35
UART4			
URXD4	DI	UART4 receive data	H34
UTXD4	DO	UART4 transmit data	H32
UART5			
URXD5	DI	UART5 receive data	AM20, AM10
UTXD5	DO	UART5 transmit data	AN20, AL9

3.12.3 Infrared Receiver (IRRX)

The device has one IRRX module, which serves as a receiver for Infrared (IR) assistive applications.

The IRRX module supports the following key features:
- Hardware decoding support for certain IR transmission protocols:
  - Pulse width coding (NEC, RC-MM)—decoding the IR signal by a variable-period sampling pulse
  - Bi-phase coding (RC5, RC6)—decoding the IR signal by a constant-period sampling pulse with inversion in phase
- Software decoding support for other protocols
- Wake-up interrupt generation in hardware decoding mode

3.12.3.1 IRRX Signal Descriptions

Table 3-44 presents IRRX signal descriptions.

Table 3-44 IRRX Signal Descriptions

Signal Name	Type	Description	Ball Location
IR_IN	DI	Infrared receiver module input	D37, AM26

3.12.4 Serial Peripheral Interface (SPI)

3.12.4.1 SPI Master

The SPI Master (SPIM) is a four-pin synchronous serial interface used for short-distance communication, primarily in embedded systems. The device features six SPIM controllers.

The SPIM supports the following key features:
- SPIM[0-3] support up to 52 MHz
- SPIM[4-5] support up to 27 MHz
- Two configurable transmit modes:
  - TX DMA mode—the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory
  - TX FIFO mode—the data to be transmitted on the MOSI line is written to FIFO before the start of the transaction.
- Two configurable receive modes:
  - RX DMA mode—the SPI controller automatically stores the received data (from MISO line) to memory.
  - RX FIFO mode—the received data is kept in RX FIFO of the SPI controller. The processor must read back the data by itself.
- Configurable chip-select setup, hold, and idle times
- Programmable serial clock high and low times
- Configurable transmit and receive bit order (MSB or LSB)
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission using dedicated pause mode
- Configurable option to control chip-select de-assertion between byte transfers
- Supports all clock polarity and phase modes

3.12.4.1.1 SPI Master Signal Descriptions

Table 3-45 presents SPIM signal descriptions.

Table 3-45 SPIM Signal Descriptions

Signal Name	Type	Description	Ball Location
SPI0 Master			
SPIM0_CLK	DO	SPIM0 clock	F32
SPIM0_CSB	DO	SPIM0 chip select	F31
SPIM0_MI	DI	SPIM0 data in	G31
SPIM0_MO	DO	SPIM0 data out	G32

Signal Name	Type	Description	Ball Location
SPI1 Master			
SPIM1_CLK	DO	SPIM1 clock	AU23
SPIM1_CSB	DO	SPIM1 chip select	AT22
SPIM1_MI	DI	SPIM1 data in	AR23
SPIM1_MO	DO	SPIM1 data out	AT23
SPI2 Master			
SPIM2_CLK	DO	SPIM2 clock	AP22
SPIM2_CSB	DO	SPIM2 chip select	AN23
SPIM2_MI	DI	SPIM2 data in	AP23
SPIM2_MO	DO	SPIM2 data out	AN22
SPI3 Master			
SPIM3_CLK	DO	SPIM3 clock	AT21
SPIM3_CSB	DO	SPIM3 chip select	AU21
SPIM3_MI	DI	SPIM3 data in	AN21
SPIM3_MO	DO	SPIM3 data out	AP21
SPI4 Master			
SPIM4_CLK	DO	SPIM4 clock	AN14
SPIM4_CSB	DO	SPIM4 chip select	AL14
SPIM4_MI	DI	SPIM4 data in	AK14
SPIM4_MO	DO	SPIM4 data out	AM14
SPI5 Master			
SPIM5_CLK	DO	SPIM5 clock	AU15
SPIM5_CSB	DO	SPIM5 chip select	AK11
SPIM5_MI	DI	SPIM5 data in	AK10
SPIM5_MO	DO	SPIM5 data out	AR14

3.12.4.1.2 SPI Master Timing Characteristics

Table 3-46 and Figure 3-22 present timing characteristics for the SPIM in the device.

Table 3-46 SPIM Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_{OP_MCK}	SPI clock frequency			52	MHz
SPI02	t_c	Cycle time, SPI clock (SPI_CLK)	19.23(1)			ns
SPI05	$t_{w\_CLK\_L}$	Pulse duration, SPI_CLK low	7.2			ns
SPI06	$t_{w\_CLK\_H}$	Pulse duration, SPI_CLK high	7.2			ns
SPI07	t_{su_cs}(4)	SPI_CSB falling to SPI_SCK rising setup time	1.8			ns
SPI08	t_{h_cs}(4)	SPI_SCK falling to SPI_CSB rising hold time	1.8			ns
SPI09	t_{su_MOSI}	SPI_MO to SPI_CK rising setup time	6.6			ns
SPI10	t_{h_MOSI}	SPI_SCK rising to SPI_MO hold time	6.6			ns
SPI11	t_{su_MISO}(2)	SPI_MI to _SPI SCK rising setup time requirement	0			ns
SPI12	t_{h_MISO}(3)	SPI_SCK rising to SPI_MI hold time requirement	0			ns

1. For maximum operating clock frequency refer to Table 6-1.
2. To achieve the minimum value of t_{su_MISO}, the internal sample clock delay of SPIM should be adjusted.
3. t_{h_MISO} data valid time should be one cycle of f_{OP_MCK}.
4. In CS GPIO mode, SPI_CSB is handled by SW. SW should pull down SPI_CSB pin before SPI starts transferring and pull up SPI_CSB pin when SPI completes the transaction.

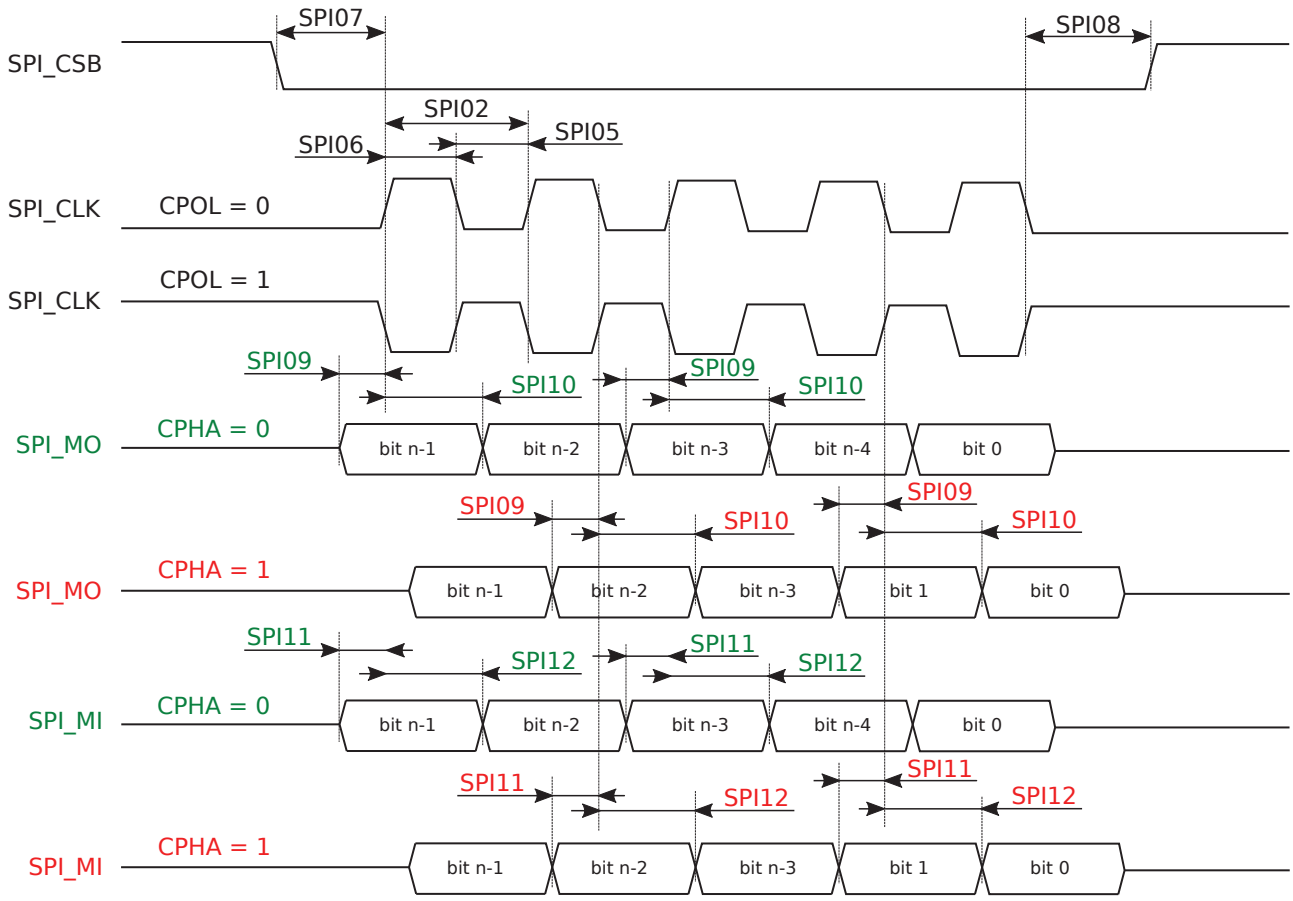


Figure 3-22 SPIM Timing Diagram

3.12.4.2 SPI Slave

The SPI Slave (SPIS) is a four-pin synchronous serial interface used for short-distance communication, primarily in embedded systems. The device features two SPIS controllers.

The SPIS supports the following key features:

- SPIS[0-1] support up to 26 MHz
- Configurable transmit and receive bit order (MSB or LSB)
- Four SPI communication modes (M0, M1, M2, and M3)
- Enable or disable transmit and receive modes
- DMA mode programmable byte length:
  - TX DMA: from 1 byte to 1MB
  - RX DMA: from 1 byte to 1MB - 4 bytes
- PIO mode transfer
- RX FIFO full/empty and TX FIFO full/empty interrupts
- TX FIFO and RX FIFO depths: 32 × 4 bytes

3.12.4.2.1 SPI Slave Signal Descriptions

Table 3-47 presents SPIS signal descriptions.

Table 3-47 SPIS Signal Descriptions

Signal Name	Type	Description	Ball Location
SPI0 Slave			
SPIS0_CLK	DI	SPIS0 clock	F32
SPIS0_CSB	DI	SPIS0 chip select	F31

Signal Name	Type	Description	Ball Location
SPIS0_SI	DI	SPIS0 data in	G32
SPIS0_SO	DO	SPIS0 data out	G31
SPI1 Slave			
SPIS1_CLK	DI	SPIS1 clock	AU23
SPIS1_CSB	DI	SPIS1 chip select	AT22
SPIS1_SI	DI	SPIS1 data in	AT23
SPIS1_SO	DO	SPIS1 data out	AR23

3.12.4.2.2 SPI Slave Timing Characteristics

Table 3-48 and Table 3-48 present timing characteristics for the SPIS in the device.

Table 3-48 SPIS Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_{OP_MCK} (2)	SPI clock frequency			26	MHz
SPI02	t_c	Cycle time, SPI clock (SPI_CLK)	38.46(1)			ns
SPI05	$t_{w\_CLK\_L}$	Pulse duration, SPI_CLK low	14.5			ns
SPI06	$t_{w\_CLK\_H}$	Pulse duration, SPI_CLK high	14.5			ns
SPI07	t_{su_cs}	SPI_CSB falling to SPI_SCK rising setup time	19.2			ns
SPI08	t_{h_cs}	SPI_SCK falling to SPI_CSB rising hold time	19.2			ns
SPI09	t_{su_MOSI}	SPI_MO to SPI_CK rising setup time	7.8			ns
SPI10	t_{h_MOSI}	SPI_SCK rising to SPI_MO hold time	7.8			ns
SPI11	t_{su_MISO}	SPI_MI to _SPI SCK rising setup time requirement	6.6			ns
SPI12	t_{h_MISO}	SPI_SCK rising to SPI_MI hold time requirement	26.4			ns

1. For maximum operating clock frequency refer to Table 6-1.
2. If the SPIM can adjust sample clock delay, the maximum value of f_{OP_MCK} can be up to 52 MHz.

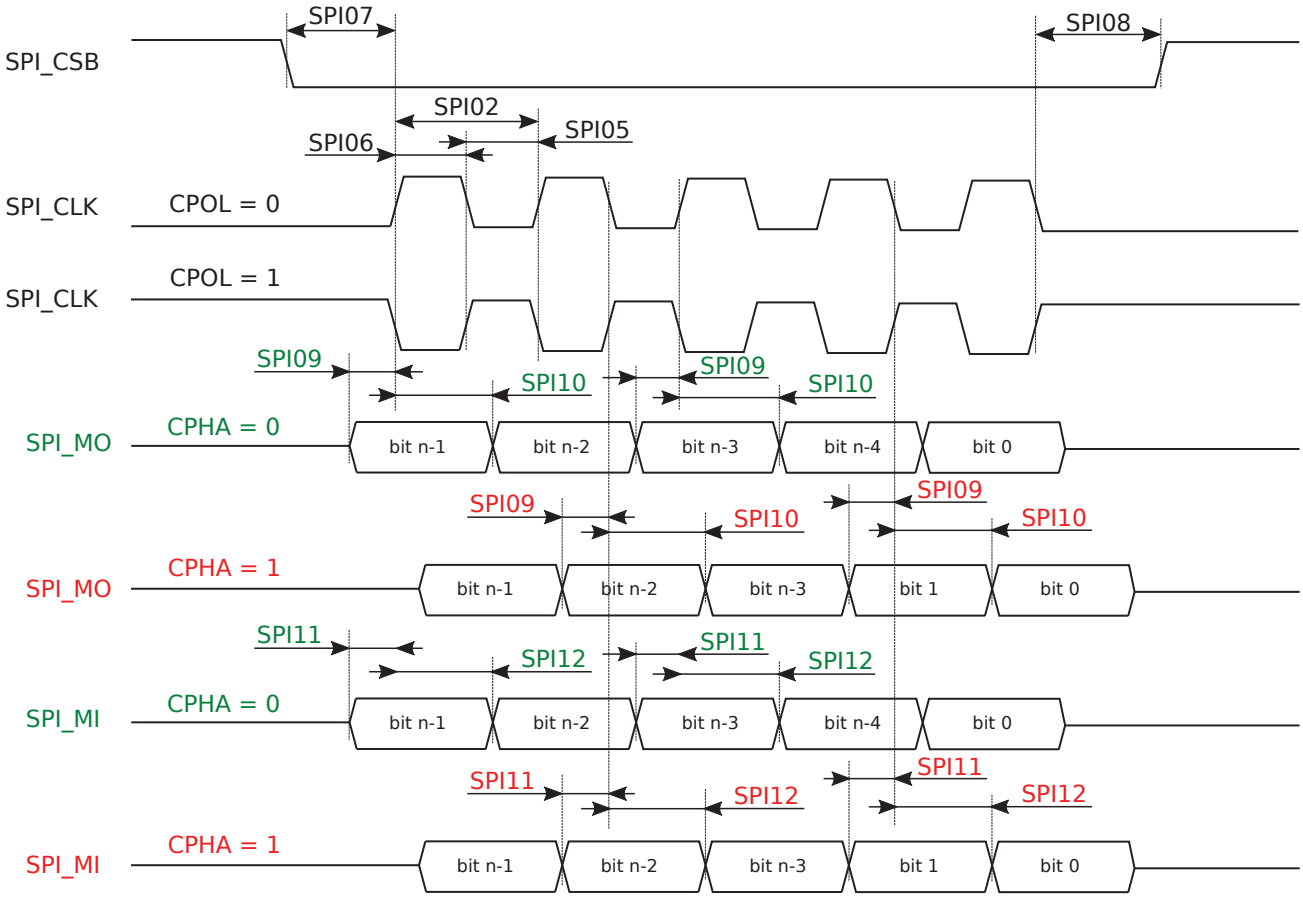


Figure 3-23 SPIS Timing Diagram

3.12.5 Universal Serial Bus (USB)

The device has four USB subsystems with integrated PHYs—two SuperSpeed (SS) USB 3.1 Gen1 and two USB 2.0 Dual-Role-Device (DRD).

- USB Port 0 supports SS USB 3.1 Gen1 DRD.
- USB Port 1 supports SS USB 3.1 Gen1 Host. The SS USB Port 1 is shared with PCIe Port 1.
- USB Port 2 and USB Port 3 are USB 2.0 DRD ports.

The features of the USB subsystems include:

- USB 3.1 SS Gen1 with 5 Gbps TX and 5 Gbps RX (USB Port 0 and USB Port 1 only)
  - Embedded USB 3.1 Gen1 PHY with 32-bit @ 125 MHz PIPE interface
  - U0/U1/U2/U3 states
- USB 2.0 Full-Speed (FS) 12 Mbps and High-Speed (HS) 480 Mbps
  - Embedded USB 2.0 PHY with 16-bit @ 30 MHz UTMI+ interface
  - Lower Power Management (LPM)
- Host role features:
  - Host controller based on eXtensible Host Controller Interface (xHCI) Revision 1.1
  - Dedicated DMA channel for USB 3.1 data transfer
  - Support of all USB compliant data transfer types (Control/Bulk/Interrupt/Isochronous)
  - Support of connection to USB 2.0/USB 3.0 Hubs
  - Support of up to 15 devices
  - Support of up to 64 endpoints
- Device (peripheral) role features:
  - Proprietary application layer device controller
  - Embedded queue management function with scatter/gather DMA capability
  - Shared endpoint and buffer hardware for USB 2.0 and USB 3.1 Gen1 ports
  - Up to 8 OUT endpoints and 8 IN endpoints

- Up to 8 packet slots for each endpoint
- Software configurable FIFO size allocation for each endpoint
- Software configurable transfer type (Bulk/Interrupt/Isochronous) for each endpoint
- Software configurable interrupt with the following interrupt statuses: VBUS On/Off, suspend/resume, USB Reset
- Software configurable period from VBUS connection to D+ pull-up
- Data alignment for Device DMA descriptor: 16-Byte
- Data alignment for Device data: Byte alignment

3.12.5.1 USB Signal Descriptions

Table 3-49 presents USB signal descriptions.

Table 3-49 USB Signal Descriptions

Signal Name	Type	Description	Ball Location
USB Port 0			
SSUSB_RXN	AI	USB SuperSpeed receive data negative	AK31
SSUSB_RXP	AI	USB SuperSpeed receive data positive	AJ31
SSUSB_TXN	AO	USB SuperSpeed transmit data negative	AH32
SSUSB_TXP	AO	USB SuperSpeed transmit data positive	AH33
USB_DP_P0	AIO	USB D+ bi-directional differential data	AM35
USB_DM_P0	AIO	USB D- bi-directional differential data	AM36
IDDIG	DI	USB OTG ID. Cable end detector: • GND: micro-A • Floating: micro-B	AL9
USB_DRVVBUS	DO	USB drive VBUS—signal to external power switch enable	AM10
VBUSVALID	DI	Digital VBUS—valid signal from external circuitry	AU18
USB Port 1			
PCIE_LN0_RXP_P1	AI	USB SuperSpeed receive data negative(1)	V33
PCIE_LN0_RXN_P1	AI	USB SuperSpeed receive data positive(1)	V34
PCIE_LN0_TXP_P1	AO	USB SuperSpeed transmit data negative(1)	W31
PCIE_LN0_TXN_P1	AO	USB SuperSpeed transmit data positive(1)	W32
USB_DP_P1	AIO	USB D+ bi-directional differential data	AC31
USB_DM_P1	AIO	USB D- bi-directional differential data	AC32
VBUSVALID_1P	DI	Normally not used	AT18
USB Port 2			
USB_DP_P2	AIO	USB D+ bi-directional differential data	AD8
USB_DM_P2	AIO	USB D- bi-directional differential data	AE8
IDDIG_1P	DI	USB OTG ID. Micro-A/B cable end detector	H31, AL7
USB_DRVVBUS_1P	DO	USB drive VBUS—signal to external power switch enable	G34, AL8
VBUSVALID_2P	DI	Digital VBUS-valid signal from external circuitry	AR8
USB Port 3			
USB_DP_P3	AIO	USB D+ bi-directional differential data	AH7
USB_DM_P3	AIO	USB D- bi-directional differential data	AG7
IDDIG_2P	DI	USB OTG ID. Micro-A/B cable end detector	G35, AT16
USB_DRVVBUS_2P	DO	USB drive VBUS—signal to external power switch enable	H33, AN15
VBUSVALID_3P	DI	Digital VBUS-valid signal from external circuitry	AP8

1. Shared with PCIe Port 1.

3.12.6 Ethernet Network Interface Controller (ENIC)

The device features one ENIC supporting the following key features:

- Compliance to standards:
  - MII/RMII/RGMII
  - IEEE 802.3-2015 for Ethernet MAC
  - IEEE 1588-2008 for precision networked clock synchronization
  - IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic
  - IEEE 802.1Qbv-2015, 802.1Qbu-2016, and 802.1AS-Rev D5.0 for Time-Sensitive Networking (TSN) traffic
  - IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE)
- MAC features:
  - 10/100/1000 Mbps speed mode
  - Half-duplex operation:
    - Support of CSMA/CD protocol
    - Support of flow control using backpressure
  - Full-duplex flow control operation (IEEE 802.3x pause packets and priority flow control)
  - Receive:
    - Automatic pad and CRC stripping options
    - Preamble and Start Frame Delimiter (SFD) deletion
    - Option to disable automatic CRC checking
    - Flexible address filtering modes:
      - Up to 31 additional 48-bit destination address filters with masks for each byte
      - Up to 31 x 48-bit source address comparison check with masks for each byte
      - 256-bit hash filter for multicast and unicast destination addresses
      - Option to pass all multicast addressed packets
      - Promiscuous mode to pass all packets without any filtering for network monitoring
    - Additional packet filtering:
      - VLAN tag-based: Perfect match and hash-based filtering. Filtering based on either outer or inner VLAN tag is possible.
      - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
      - Extended VLAN tag based with 4 filters selection
  - Transmit:
    - Automatic pad and CRC generation control ability on a per-packet basis
    - Preamble and start of packet data insertion
    - Programmable packet length to support standard or jumbo Ethernet packets of up to 16 KB
    - Programmable inter packet gap (40-bit to 96-bit times in steps of 8)
    - IEEE 802.3x flow control automatic transmission of zero-quanta pause packet when the flow control input transitions from assertion to de-assertion (in full-duplex mode)
    - Source address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
    - Insertion, replacement, or deletion of up to two queue/channel-based VLAN tags
- MAC Transaction Layer (MTL) features:
  - Recieve:
    - 16KB RX FIFO and 4 RX queues
  - Transmit:
    - 16KB TX FIFO and 4 TX queues
    - Store-and-forward mechanism or threshold mode (cut-through) for transmission to the MAC
    - Calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksums
    - Scheduling algorithms:
      - Weighted Round Robin (WRR)
      - Strict Priority (SP)
      - Credit-Based Shaper (CBS) when audio-video bridging is enabled
- Clause 22 and Clause 45 MDIO master interface for PHY configuration and management

3.12.6.1 ENIC Signal Descriptions

Table 3-50 presents ENIC signal descriptions.

Table 3-50 ENIC Signal Descriptions

Signal Name	Type	Description	Ball Location
ENIC Receive Data Bus—GBE_RXD[3:0]			
GBE_RXD0	DI	Gigabit Ethernet RX data 0	AK10
GBE_RXD1	DI	Gigabit Ethernet RX data 1	AK11
GBE_RXD2	DI	Gigabit Ethernet RX data 2	AR14
GBE_RXD3	DI	Gigabit Ethernet RX data 3	AU15
ENIC Transmit Data Bus—GBE_TXD[3:0]			
GBE_TXD0	DO	Gigabit Ethernet TX data 0	AK14
GBE_TXD1	DO	Gigabit Ethernet TX data 1	AL14
GBE_TXD2	DO	Gigabit Ethernet TX data 2	AM14
GBE_TXD3	DO	Gigabit Ethernet TX data 3	AN14
ENIC Command, Status, Clock and Interrupt Signals			
GBE_COL	DI	Gigabit Ethernet collision detected	AU14
GBE_INTR	DI	Gigabit Ethernet interrupt from external PHY	AT13
GBE_RXC	DI	Gigabit Ethernet RX clock	AR12
GBE_RXDV	DI	Gigabit Ethernet RX data valid	AL12
GBE_RXER	DI	Gigabit Ethernet RX error	AN12
GBE_TXC	DIO	Gigabit Ethernet TX clock	AP14
GBE_TXEN	DO	Gigabit Ethernet TX data valid	AK12
GBE_TXER	DO	Gigabit Ethernet TX error	AP13
ENIC Management Bus			
GBE_MDC	DO	Gigabit Ethernet MDC	AP12
GBE_MDIO	DIO	Gigabit Ethernet MDIO	AL13

3.12.6.2 ENIC Timing Characteristics

Table 3-51 and Figure 3-24 present timing characteristics for the ENIC MII in the device.

Table 3-51 ENIC MII Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
MII1	$t_{c\_TXC\_RXC}$	Cycle time, TXC/RXC		40		ns
MII2	t_{d_TX}	Delay time, transmission			9.764	ns
MII3	t_{d_TXC}	Delay time, TXC	1.323		2.273	ns
MII4	t_{d_TXD}	Delay time, TXD/TXEN/TXER	4.149		7.491	ns
MII5	t_{d_RXC}	Delay time, RXC	1.514		2.654	ns
MII6	t_{d_RXD}	Delay time, RXD/RXDV/RXER	2.041		4.021	ns
MII7	t_{su_RX}	Setup time, RXD/RXDV/RXER	3.507			ns
MII8	t_{h_RX}	Hold time, RXD/RXDV/RXER	0.473			ns
	D	Duty cycle, TXC/RXC	40	50	60	%
MII10	t_{RISE}	Rise time, TXC/RXC (20% ~ 80%)			0.75	ns
MII11	t_{FALL}	Fall time, TXC/RXC (20% ~ 80%)			0.75	ns

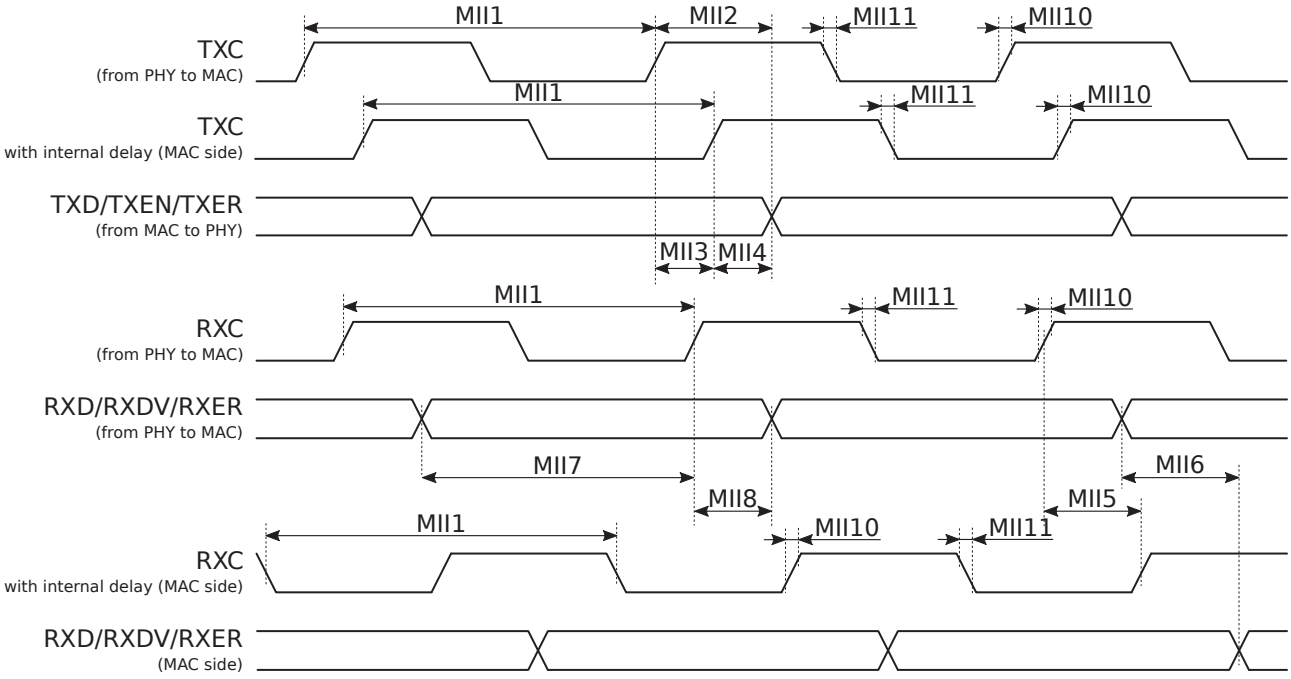


Figure 3-24 ENIC MII Timing Diagram

Table 3-52 and Figure 3-25 present timing characteristics for the ENIC RMII in the device.

Table 3-52 ENIC RMII Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
RMII1	t_{c_REFCLK}	Cycle time, REFCLK		20		ns
RMII2	t_{d_TX}	Delay time, transmission			7.235	ns
RMII3	t_{d_TXC}	Delay time, REFCLK (when transmitting)	1.144		2.2	ns
RMII4	t_{d_TXD}	Delay time, TXD/TXEN	2.8		5.035	ns
RMII5	t_{d_RXC}	Delay time, REFCLK (when receiving)	1.798		3.071	ns
RMII6	t_{d_RXD}	Delay time, RXD/RXDV	1.925		3.469	ns
RMII7	t_{su_RX}	Setup time, RXD/RXDV	2.671			ns
RMII8	t_{h_RX}	Hold time, RXD/RXDV	0.873			ns
	D	Duty cycle, REFCLK	45	50	55	%
RMII10	t_{RISE}	Rise time, REFCLK (20%~80%)			0.75	ns
RMII11	t_{FALL}	Fall time, REFCLK (20%~80%)			0.75	ns

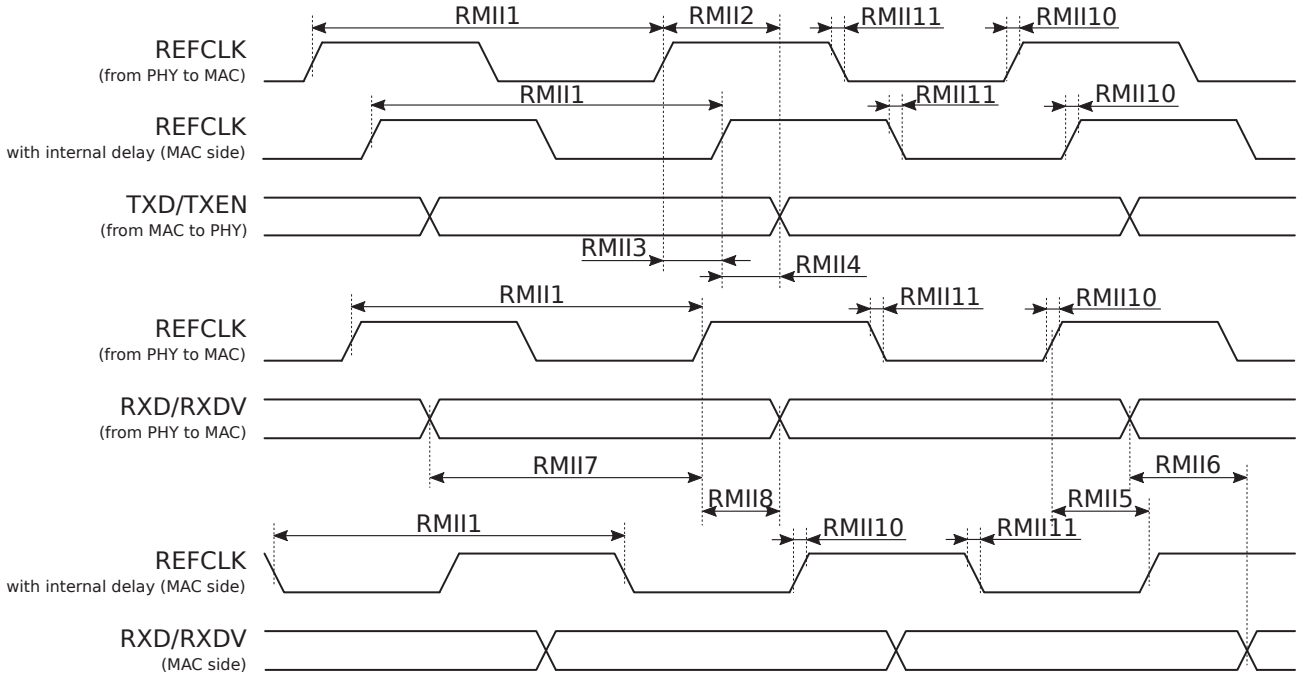


Figure 3-25 ENIC RMII Timing Diagram

Table 3-53 and Figure 3-26 present timing characteristics for the ENIC RGMII in the device.

Table 3-53 ENIC RGMII Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
RGMII1	t_{TXC_RXC}	Cycle time, TXC/RXC (10M/100M/1000M)		400/40/8		ns
RGMII2	t_{d_TX}	Delay time, transmission			4.1 + K(1)	ns
RGMII3	t_{d_TXC}	Delay time, TXC	3.489		8.169	ns
RGMII4	t_{d_TXD}	Delay time, TXD/TX_CTL	4.141		7.491	ns
RGMII5	t_{d_RXC}	Delay time, RXC	1.998		3.575	ns
RGMII6	t_{d_RXD}	Delay time, RXD/RX_CTL	1.913		3.548	ns
RGMII7	t_{su_RX}	Setup time, RXD/RX_CTL	2.55 - Q(2)			ns
RGMII8	t_{h_RX}	Hold time, RXD/RX_CTL	1.085 + Q(2)			ns
	D	Duty cycle, TXC/RXC (1000M)	45	50	55	%
		Duty cycle, TXC/RXC (10M/100M)	40	50	60	%
RGMII10	t_{RISE}	Rise time, TXC/RXC (20%~80%)			0.75	ns
RGMII11	t_{FALL}	Fall time, TXC/RXC (20%~80%)			0.75	ns

1. K is programmable MAC internal delay (32-levels). The maximum delay is from 12.6001 ns to 28.5724 ns.
2. Q is programmable MAC internal delay (32-levels). The maximum delay is from 12.6001 ns to 28.5724 ns.

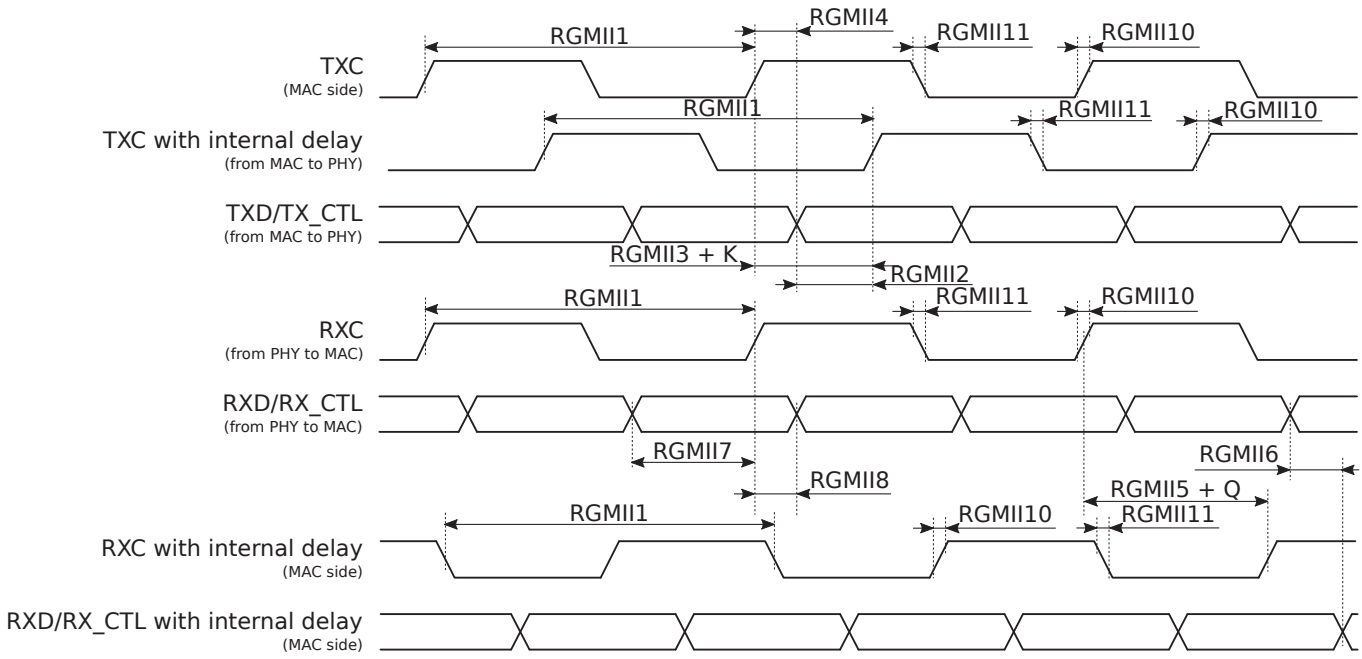


Figure 3-26 ENIC RGMII Timing Diagram

Table 3-54 and Figure 3-27 present timing characteristics for the ENIC MDIO in the device.

Table 3-54 ENIC MDIO Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
MDIO1	t_{c_MDC}	Cycle time, MDC	400			ns
MDIO2	t_{d_MDO}	Delay time, MDIO output		MDIO4 - MDIO3		ns
MDIO3	t_{d_MDC}	Delay time, MDC	3.631		9.043	ns
MDIO4	$t_{d\_MDO\_MAC}$	Delay time, MDIO output (MAC to PHY)	4.804		11.479	ns
MDIO5	t_{d_MDI}	Delay time, MDIO input	1.92		4.203	ns
MDIO6	t_{su_MDI}	Setup time, MDIO input	1 + MDIO5 + MDIO3			ns
MDIO7	t_{h_MDI}	Hold time, MDIO input	1 - MDIO5 - MDIO3			ns

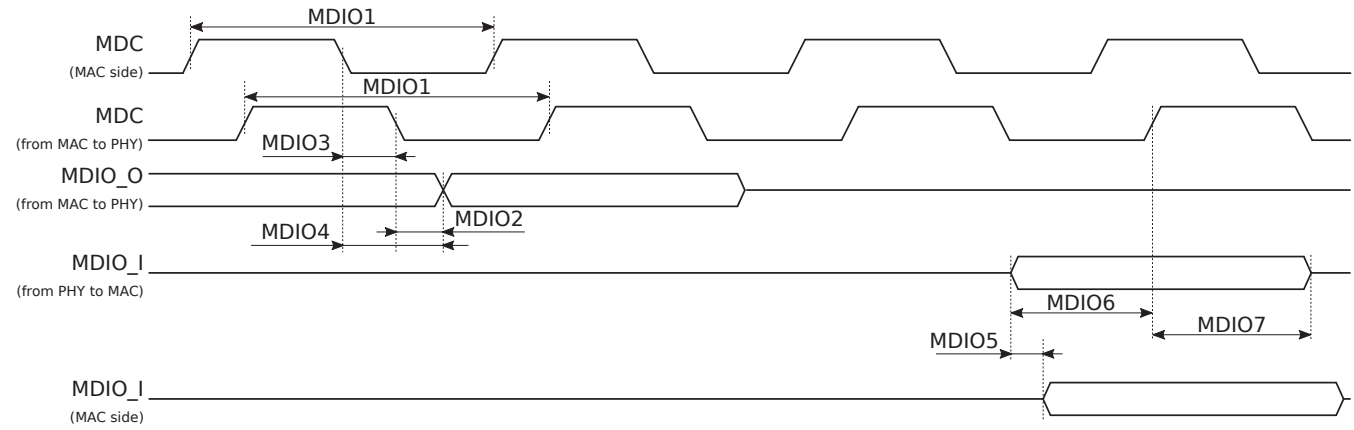


Figure 3-27 ENIC MDIO Timing Diagram

3.12.7 Peripheral Component Interconnect Express (PCIe) Controller

The device features one Peripheral Component Interconnect Express (PCIe®) Controller that supports the following key features:

- Two ports: Port 0 and Port 1 (shared with USB Port 1)
- Compliant with the Intel® Physical Interface for PCI Express (PIPE) interface, allowing integration with PIPE-compliant PHY
- AMBA AXI4 specification compliant
- PCIe interface:
  - Mode:
    - Port 0: Root Complex (RC) and Endpoint (EP)
    - Port 1: RC
  - Link width:
    - Port 0: x1 and x2
    - Port 1: x1
  - Per lane link rate:
    - Port 0: 2.5 GT/s (Gen1), 5.0 GT/s (Gen2), and 8.0 GT/s (Gen3)
    - Port 1: 2.5 GT/s (Gen1) and 5.0 GT/s (Gen2)
  - PCI Express Base Specification Revision 3.0 compliant
  - PIPE 4.0 compliant
  - Memory transactions support
  - I/O transactions:
    - Maximum I/O read request of 4 bytes
    - Maximum I/O write request of 4 bytes
    - 32-bit addressing
  - Configuration transactions:
    - Maximum configuration read request of 4 bytes
    - Maximum configuration write request of 4 bytes
    - Extended register number support (4 KB extended PCIe configuration header space)
  - Message transactions:
    - INTx interrupt signaling
    - Power management
    - Error signaling
    - Slot power limit support
    - Vendor-defined messages
    - Latency Tolerance Reporting (LTR) message
  - 256-byte maximum payload size
  - 512-byte maximum read request size
  - One Virtual Channel (VC)
  - One physical function
  - Advanced Error Reporting (AER)
  - Endpoint Cyclic Redundancy Check (ECRC) generation and check
  - Lane reversal
  - Polarity inverse support
  - Legacy PCI power management support
  - Active State Power Management (ASPM) L0s and L1 state support
  - L1 Power Management Substates (L1PMSS) with CLKREQ# support
  - Message Signaled Interrupt (MSI), per function up to 32
- AHB and AXI interfaces:
  - One AHB slave interface for bridge configuration
  - One AXI master interface supporting up to 24 outstanding write/read requests
  - One AXI slave interface supporting up to 8 outstanding write/read requests
  - 128-bit data support for AXI master and slave interfaces

3.12.7.1 PCIe Signal Descriptions

Table 3-55 presents PCIe signal descriptions.

Table 3-55 PCIe Signal Descriptions

Signal Name	Type	Description	Ball Location
PCIe Port 0			
PCIEG3_LN0_RXP	AI	Lane 0 receive data differential pair	Y35
PCIEG3_LN0_RXN	AI		W35
PCIEG3_LN0_TXP	AO	Lane 0 transmit data differential pair	AA30
PCIEG3_LN0_TXN	AO		AA31
PCIEG3_LN1_RXP	AI	Lane 1 receive data differential pair	AC35
PCIEG3_LN1_RXN	AI		AB35
PCIEG3_LN1_TXP	AO	Lane 1 transmit data differential pair	AA37
PCIEG3_LN1_TXN	AO		AA36
PCIEG3_CLKP	AI	Reference clock differential pair	AA34
PCIEG3_CLKN	AI		AA33
PCIe Port 1 (Shared with USB Port 1)			
PCIE_LN0_RXP_P1	AI	Lane 0 receive data differential pair	V33
PCIE_LN0_RXN_P1	AI		V34
PCIE_LN0_TXP_P1	AO	Lane 0 transmit data differential pair	W31
PCIE_LN0_TXN_P1	AO		W32
PCIE_CKRXP_P1	AI	Reference clock differential pair	V36
PCIE_CKRXN_P1	AI		V37
PCIe Control Signals Port 0			
PERSTN	DO	Fundamental reset	AL28, AL24, AK16
CLKREQN	DIO	Clock request	AL29, AM24, AT16
WAKEN	DI	Link reactivation	AM29, AM23, AL16
PCIe Control Signals Port 1			
PERSTN_1	DO	Fundamental reset	H31, AL27, AN15
CLKREQN_1	DIO	Clock request	G34, AK27, AK15
WAKEN_1	DI	Link reactivation	J31, AM28, AU17

3.12.8 KeyPad Scanner (KeyPad)

The KeyPad module implements scanning algorithm for hardware-based key-press decoding and reduces overhead to the CPU.

The KeyPad supports the following key features:

- Two types of keyboards:
  - 3 × 3 single keys
  - 3 × 3 configurable double keys
- Double keypad supports 18 keys matrix divided into nine subgroups of 2 keys and a 20 Ω resistor
- Key detection block providing key pressed, key released and de-bounce mechanisms
- Interrupt event detection on pressed and released keys
- Detection of one or two keys pressed simultaneously with any combination

3.12.8.1 KeyPad Signal Descriptions

Table 3-56 presents KeyPad signal descriptions.

Table 3-56 KeyPad Signal Descriptions

Signal Name	Type	Description	Ball Location
KPCOL0	DIO	KeyPad column 0	AU11
KPCOL1	DIO	KeyPad column 1	AT11, AL10
KPCOL2	DIO	KeyPad column 2	AT10

Signal Name	Type	Description	Ball Location
KPROW0	DIO	KeyPad row 0	AN11
KPROW1	DIO	KeyPad row 1	AN10
KPROW2	DIO	KeyPad row 2	AM8

3.12.8.2 KeyPad Applications

The 3 × 3 double KeyPad supports a 3 × 3 × 2 = 18 keys matrix. The eighteen keys are divided into nine subgroups, and each group consists of 2 keys and a 20 Ω resistor.

NOTE: KeyPad does not support detection of simultaneously pressed keys on the same column and row.

Figure 3-28 represents 3 × 3 double KeyPad matrix (18 keys) example configuration.

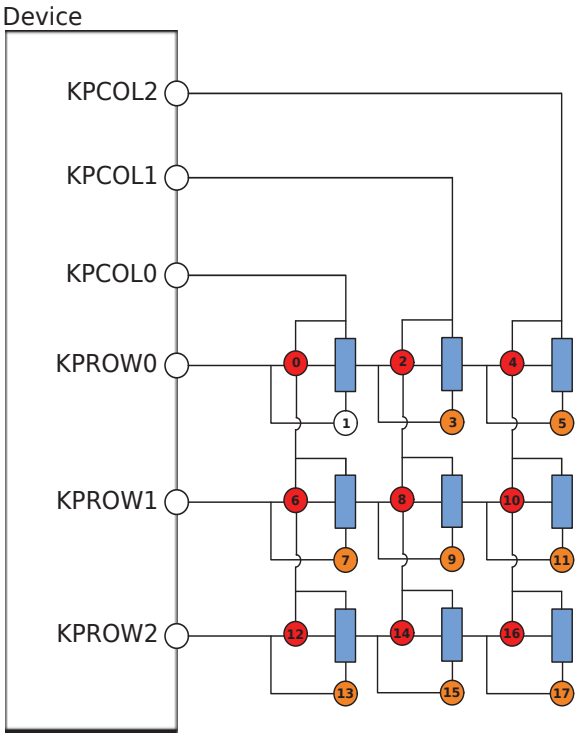


Figure 3-28 3 × 3 KeyPad Matrix (18 Keys)

3.12.9 General-Purpose I/O (GPIO)

The GPIO peripheral provides 144 dedicated GPIO pins, multiplexed with other functions to reduce the pin count.

Each GPIO pin has the following key functions:

- Configurable direction: input or output
- Control of the state driven on the output pin when GPIO is configured as an output
- Detection of the state of the pin when GPIO is configured as an input
- Configurable interrupt event generation

3.12.9.1 GPIO Signal Descriptions

Table 3-57 presents GPIO signal descriptions.

Table 3-57 GPIO Signal Descriptions

Signal Name	Type	Description	Ball Location
GPIO0	DIO	General-purpose input and output	H31
GPIO1	DIO	General-purpose input and output	G34

Signal Name	Type	Description	Ball Location
GPIO2	DIO	General-purpose input and output	J31
GPIO3	DIO	General-purpose input and output	G33
GPIO4	DIO	General-purpose input and output	G35
GPIO5	DIO	General-purpose input and output	H33
GPIO6	DIO	General-purpose input and output	H32
GPIO7	DIO	General-purpose input and output	H34
GPIO8	DIO	General-purpose input and output	D36
GPIO9	DIO	General-purpose input and output	D37
GPIO10	DIO	General-purpose input and output	E36
GPIO11	DIO	General-purpose input and output	E35
GPIO12	DIO	General-purpose input and output	E37
GPIO13	DIO	General-purpose input and output	F34
GPIO14	DIO	General-purpose input and output	F35
GPIO15	DIO	General-purpose input and output	F37
GPIO16	DIO	General-purpose input and output	F36
GPIO17	DIO	General-purpose input and output	G36
GPIO18	DIO	General-purpose input and output	AP25
GPIO19	DIO	General-purpose input and output	AM29
GPIO20	DIO	General-purpose input and output	AL28
GPIO21	DIO	General-purpose input and output	AL29
GPIO22	DIO	General-purpose input and output	AL27
GPIO23	DIO	General-purpose input and output	AK27
GPIO24	DIO	General-purpose input and output	AM28
GPIO25	DIO	General-purpose input and output	AL26
GPIO26	DIO	General-purpose input and output	AM26
GPIO27	DIO	General-purpose input and output	AN25
GPIO28	DIO	General-purpose input and output	AN24
GPIO29	DIO	General-purpose input and output	AM25
GPIO30	DIO	General-purpose input and output	AP24
GPIO31	DIO	General-purpose input and output	AL24
GPIO32	DIO	General-purpose input and output	AM24
GPIO33	DIO	General-purpose input and output	AM23
GPIO34	DIO	General-purpose input and output	AL23
GPIO35	DIO	General-purpose input and output	AL25
GPIO36	DIO	General-purpose input and output	AR21
GPIO37	DIO	General-purpose input and output	AM22
GPIO38	DIO	General-purpose input and output	AM21
GPIO39	DIO	General-purpose input and output	AL21
GPIO40	DIO	General-purpose input and output	AU21
GPIO41	DIO	General-purpose input and output	AT21
GPIO42	DIO	General-purpose input and output	AP21
GPIO43	DIO	General-purpose input and output	AN21
GPIO44	DIO	General-purpose input and output	AN20
GPIO45	DIO	General-purpose input and output	AM20
GPIO46	DIO	General-purpose input and output	AL20
GPIO47	DIO	General-purpose input and output	AK20
GPIO48	DIO	General-purpose input and output	AR20
GPIO49	DIO	General-purpose input and output	AP20

Signal Name	Type	Description	Ball Location
GPIO50	DIO	General-purpose input and output	AN19
GPIO51	DIO	General-purpose input and output	AK19
GPIO52	DIO	General-purpose input and output	AT19
GPIO53	DIO	General-purpose input and output	AR18
GPIO54	DIO	General-purpose input and output	AP18
GPIO55	DIO	General-purpose input and output	AN18
GPIO56	DIO	General-purpose input and output	AM18
GPIO57	DIO	General-purpose input and output	AL18
GPIO58	DIO	General-purpose input and output	AK18
GPIO59	DIO	General-purpose input and output	AU20
GPIO60	DIO	General-purpose input and output	AT20
GPIO61	DIO	General-purpose input and output	AP17
GPIO62	DIO	General-purpose input and output	AL17
GPIO63	DIO	General-purpose input and output	AU18
GPIO64	DIO	General-purpose input and output	AT18
GPIO65	DO	General-purpose input and output	AR16
GPIO66	DIO	General-purpose input and output	AP16
GPIO67	DI	General-purpose input and output	AN16
GPIO68	DIO	General-purpose input and output	AM16
GPIO69	DIO	General-purpose input and output	AL16
GPIO70	DIO	General-purpose input and output	AK16
GPIO71	DIO	General-purpose input and output	AT16
GPIO72	DIO	General-purpose input and output	AN15
GPIO73	DIO	General-purpose input and output	AK15
GPIO74	DIO	General-purpose input and output	AU17
GPIO75	DIO	General-purpose input and output	AT17
GPIO76	DIO	General-purpose input and output	AT15
GPIO77	DIO	General-purpose input and output	AN14
GPIO78	DIO	General-purpose input and output	AM14
GPIO79	DIO	General-purpose input and output	AL14
GPIO80	DIO	General-purpose input and output	AK14
GPIO81	DIO	General-purpose input and output	AU15
GPIO82	DIO	General-purpose input and output	AR14
GPIO83	DIO	General-purpose input and output	AK11
GPIO84	DIO	General-purpose input and output	AK10
GPIO85	DIO	General-purpose input and output	AP14
GPIO86	DIO	General-purpose input and output	AR12
GPIO87	DIO	General-purpose input and output	AL12
GPIO88	DIO	General-purpose input and output	AK12
GPIO89	DIO	General-purpose input and output	AP12
GPIO90	DIO	General-purpose input and output	AL13
GPIO91	DIO	General-purpose input and output	AP13
GPIO92	DIO	General-purpose input and output	AN12
GPIO93	DIO	General-purpose input and output	AU14
GPIO94	DIO	General-purpose input and output	AT13
GPIO95	DIO	General-purpose input and output	AT12
GPIO96	DIO	General-purpose input and output	AT14
GPIO97	DIO	General-purpose input and output	AP9

Signal Name	Type	Description	Ball Location
GPIO98	DIO	General-purpose input and output	AR10
GPIO99	DIO	General-purpose input and output	AP10
GPIO100	DIO	General-purpose input and output	AM8
GPIO101	DIO	General-purpose input and output	AT10
GPIO102	DIO	General-purpose input and output	AR8
GPIO103	DIO	General-purpose input and output	AP8
GPIO104	DIO	General-purpose input and output	AN11
GPIO105	DIO	General-purpose input and output	AN10
GPIO106	DIO	General-purpose input and output	AU11
GPIO107	DIO	General-purpose input and output	AT11
GPIO108	DIO	General-purpose input and output	AL10
GPIO109	DIO	General-purpose input and output	AT9
GPIO110	DIO	General-purpose input and output	AN8
GPIO111	DIO	General-purpose input and output	AU9
GPIO112	DIO	General-purpose input and output	AT6
GPIO113	DIO	General-purpose input and output	AT7
GPIO114	DIO	General-purpose input and output	AT8
GPIO115	DIO	General-purpose input and output	AU8
GPIO116	DIO	General-purpose input and output	E32
GPIO117	DIO	General-purpose input and output	E33
GPIO118	DIO	General-purpose input and output	E34
GPIO119	DIO	General-purpose input and output	D35
GPIO120	DIO	General-purpose input and output	B35
GPIO121	DIO	General-purpose input and output	C36
GPIO122	DIO	General-purpose input and output	B36
GPIO123	DIO	General-purpose input and output	C35
GPIO124	DIO	General-purpose input and output	D32
GPIO125	DIO	General-purpose input and output	D33
GPIO126	DIO	General-purpose input and output	D34
GPIO127	DIO	General-purpose input and output	A35
GPIO128	DIO	General-purpose input and output	AL9
GPIO129	DIO	General-purpose input and output	AM10
GPIO130	DIO	General-purpose input and output	AL7
GPIO131	DIO	General-purpose input and output	AL8
GPIO132	DIO	General-purpose input and output	F31
GPIO133	DIO	General-purpose input and output	F32
GPIO134	DIO	General-purpose input and output	G32
GPIO135	DIO	General-purpose input and output	G31
GPIO136	DIO	General-purpose input and output	AT22
GPIO137	DIO	General-purpose input and output	AU23
GPIO138	DIO	General-purpose input and output	AT23
GPIO139	DIO	General-purpose input and output	AR23
GPIO140	DIO	General-purpose input and output	AN23
GPIO141	DIO	General-purpose input and output	AP22
GPIO142	DIO	General-purpose input and output	AN22
GPIO143	DIO	General-purpose input and output	AP23

3.12.10 Pulse Width Modulation (PWM)

The device features four generic PWM modules to generate pulse sequences with programmable frequency and duration for a variety of applications.

Each PWM module supports the following key features:
- Old mode, FIFO mode
- Periodical memory and random modes

3.12.10.1 PWM Signal Descriptions

Table 3-58 presents PWM signal descriptions.

Table 3-58 PWM Signal Descriptions

Signal Name	Type	Description	Ball Location
PWM_0	DO	PWM output 0	D36, AL16, AM8
PWM_1	DO	PWM output 1	D37, AK16, AT10
PWM_2	DO	PWM output 2	E36, AT16, AN10
PWM_3	DO	PWM output 3	E35, AN15, AT11

3.12.10.2 PWM Output Frequency and Duty Cycle

Table 3-59 PWM Output Frequency and Duty Cycle(1)

Mode	Duty cycle	Output frequency
Old mode	PWM_THRESH / (PWM_DATA_WIDTH + 1)	SRCLK / [CLK_DIV × (PWM_DATA_WIDTH + 1)]

1. BCLK can be selected as 26 MHz or 78 MHz by PWM_CK_26M_SEL.

3.13 Miscellaneous

3.13.1 Timers and Counters

3.13.1.1 System Timer (SYSTMR)

The SYSTMR is a 64-bit, always-on, up-counter used as an universal timer in the device. The counter value of SYSTMR is passed to the application cores (A78 and A55), SCP, GPU, and other processors to provide uniform system timestamps for operating systems like Android™, Linux®, and RTOS.

The SYSTMR supports the following key features:
- Enabled by default to tick with 13 MHz clock period
- HW counter incremented compensation when switching to 32 kHz clock source
- 4 × 32-bit counter timeout value (read as 32-bit down counter)
- Security access permission control for each control register (with one-time lock bit)

3.13.1.2 General-Purpose Timer (GPT)

The device has one GPT module that includes five 32-bit and one 64-bit timers. Each GPT can operate on one of the two clock sources, RTC clock (32.768 kHz) or system clock (13 MHz).

Each GPT supports:
- ONE-SHOT mode
- REPEAT mode
- KEEP-GO mode
- FREERUN mode

3.13.1.3 Watchdog Timer (WDT)

The WDT module is a part of TOPRGU. For more information refer to Section 5.5 Reset.

3.13.2 PMIC Wrapper (PWRAP)

The PWRAP serves as a bridge for the communication between CPU and PMIC.

The PWRAP supports the following key features:
- Fast auto SPI format generator for PMIC registers read/write
- APB3.0 bus lock scheme when SPI is busy
- Manual SPI format generator
- Dual I/O SPI mode
- Separated frequency between controller and SPI

3.13.2.1 PWRAP Signal Descriptions

Table 3-60 presents PWRAP signal descriptions.

Table 3-60 PWRAP Signal Descriptions

Signal Name	Type	Description	Ball Location
PWRAP SPI0			
PWRAP_SPI0_CK	DO	PWRAP PMIC SPI clock	AT21
PWRAP_SPI0_CSN	DO	PWRAP SPI chip select	AU21
PWRAP_SPI0_MI	DI	PWRAP SPI master input	AP21, AN21
PWRAP_SPI0_MO	DO	PWRAP SPI master output	AP21, AN21
PMIC I2C			
SPMI_M_SCL	DIO	PMIC I2C clock	AN20
SPMI_M_SDA	DIO	PMIC I2C data	AM20

3.13.3 Auxiliary Analog-to-Digital Converter (AUXADC)

The device features one AUXADC module. It is used to identify the plugged peripherals and perform temperature/voltage measurements.

The AUXADC module key features are:
- 12-bit Successive Approximation Register (SAR) ADC architecture
- 6 input channels operating in immediate mode
- Configurable auto-sampling function per channel
- Sequential channel serving from high to low channel
- Immediate analog-digital conversion with auto-set option
- Temperature/voltage measurement

3.13.3.1 AUXADC Signal Descriptions

Table 3-61 presents the AUXADC signal descriptions.

Table 3-61 AUXADC Signal Descriptions

Signal Name	Type	Description	Ball Location
AUXIF_CLK0	DO	Auxiliary analog/digital converter clock 0	AP16
AUXIF_CLK1	DO	Auxiliary analog/digital converter clock 1	AM16
AUXIF_ST0	DO	Auxiliary analog/digital converter status 0	AR16
AUXIF_ST1	DO	Auxiliary analog/digital converter status 1	AN16
AUXIN0[(1)(2)]	AIO	AUXADC external input channel 0	AP5
AUXIN1[(1)(2)]	AIO	AUXADC external input channel 1	AP6
AUXIN2[(1)(2)]	AIO	AUXADC external input channel 2	AN6
AUXIN3[(1)(2)]	AIO	AUXADC external input channel 3	AM6
AUXIN4[(1)(2)]	AIO	AUXADC external input channel 4	AL6
AUXIN5[(1)(2)]	AIO	AUXADC external input channel 5	AK6

Signal Name	Type	Description	Ball Location
REFP(3)	AIO	Positive reference port for internal circuit	AM7

1. This pin should be connected to GND when unused.
2. All AUXIN* pins should be connected via a 0.1-µF capacitor to GND, as close as possible to the device, when used.
3. The REFP pin should be connected via a 1-µF capacitor to GND, as close as possible to the device, when used.

3.13.3.2 AUXADC Timing and Functional Characteristics

Table 3-62 presents timing and functional characteristics for AUXADC in the device.

Table 3-62 AUXADC Specifications

Parameter		Min	Typ	Max	Unit
f_{OP}	Operating frequency		3.25		MHz
N	Resolution			12	Bit
f_S	Sampling rate at N-bit		3.25 / (N+8)		MSPS
IN_{SW}	Input swing	0.05		1.45	V
C_{IN}	Input capacitance unselected channel		50		pF
	Input capacitance selected channel		4		pF
R_{IN}	Input resistance unselected channel	400			MΩ
$F_{cycle\_latency}$	Cycle latency		N+8		$1/f_{OP}$
D_{NL}	Differential non-linearity		+1.0/-1.0		LSB
I_{NL}	Integral non-linearity		+2.0/-2.0		LSB
SNR+D	Signal to noise and distortion ratio (1 kHz full swing input; 1.0833 MHz clock rate)	60	67		dB

3.13.4 Thermal Control Subsystem (TCSYS)

The device Thermal Control Subsystem (TCSYS) is based on several temperature sensors in the hot spots on the die. The thermal control module executes periodic measurements for each hot spot. The temperature readings are readable by software. In order to minimize the software effort to monitor temperature, the thermal controller generates interrupts to inform microprocessors of any abnormal condition.

The TCSYS supports the following key features:
- 7 banks with up to four thermal sensors
- Programmable periodic temperature measurement
- Two independent Finite State Machines (FSM) for temperature monitoring
- Different types of low pass filters for thermal sensor reading

The TCSYS has three major building blocks:
- Sensing device: Thermal Sensing Micro Circuit Unit (TSMCU)
- Converter: Low Voltage Thermal Sensor (LVTS) converter
- Digital Controller: LVTS_CTRL

Figure 3-29 shows the TCSYS top level block diagram.

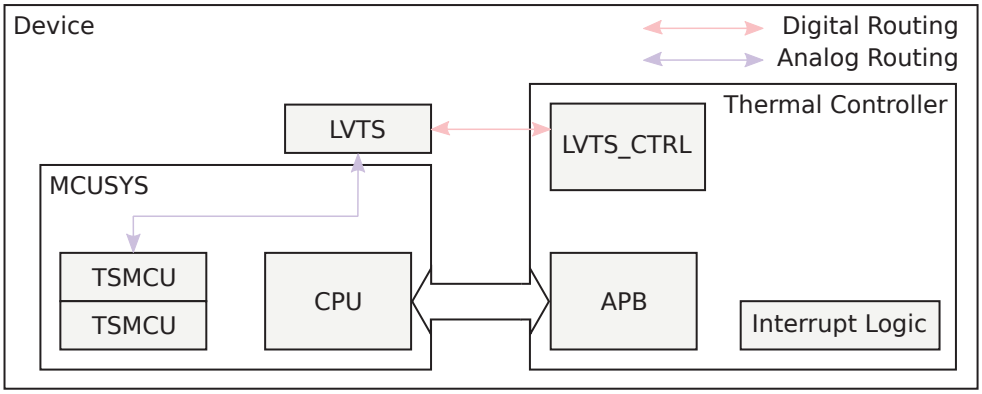


Figure 3-29 Thermal Control Subsystem

Table 3-63 presents the temperature sensors monitoring locations.

Table 3-63 Temperature Sensor Monitoring Locations

Module	Sensor
A78 (Bottom)	0, 1
A78 (Top)	0, 1
A55	0, 1, 2, 3
APU	0, 1
GPU	0, 1
SOC/TOP	0, 1, 2
ISP	0, 1

3.13.4.1 TCSYS Signal Descriptions

Table 3-64 presents TCSYS signal descriptions.

Table 3-64 TCSYS Signal Descriptions

Signal Name	Type	Description	Ball Location
LVTS_26M	DI	LVTS supported 26 MHz input frequency	AM28
LVTS_FOUT	DO	LVTS output clock frequency	D36
LVTS_SCF	DI	LVTS serial clock frequency	E36
LVTS_SCK	DI	LVTS serial clock	E35
LVTS_SDI	DI	LVTS data input	E37
LVTS_SDO	DO	LVTS data output	D37

3.14 Boot Flash

The device supports the following boot flash:

- eMMC
- UFS
- SPI NOR

Table 3-65 presents the boot flash selection options.

Table 3-65 Boot Flash Selection

AUD_SYNC_MOSI	AUD_CLK_MOSI	Boot Flash
0	0	eMMC (default)
0	1	UFS
1	1	SPI NOR

3.15 ROM Power Down Mode

After system boot, ROM can be powered down and prevented from any probe of ROM content.

4 Ball Map

Figure 4-1 presents simplified diagram of the location of the balls on the package.

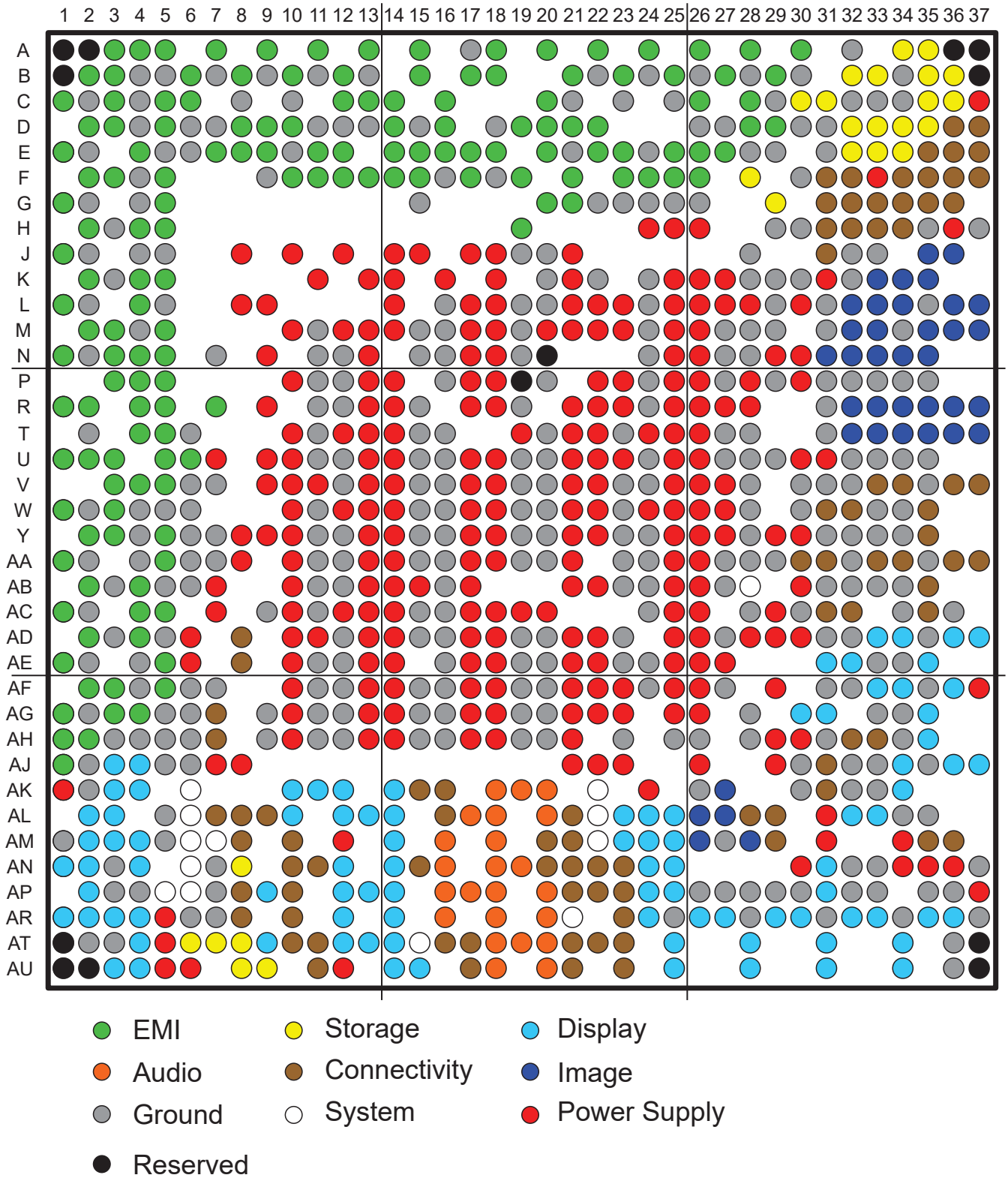


Figure 4-1 Ball Map Diagram

For detailed information about package outlines, thermal characteristics, and markings, see Section 7 Package Information.

4.1 Quadrant Pinout

Figure 4-2 shows a top view mapping of the package quadrants.

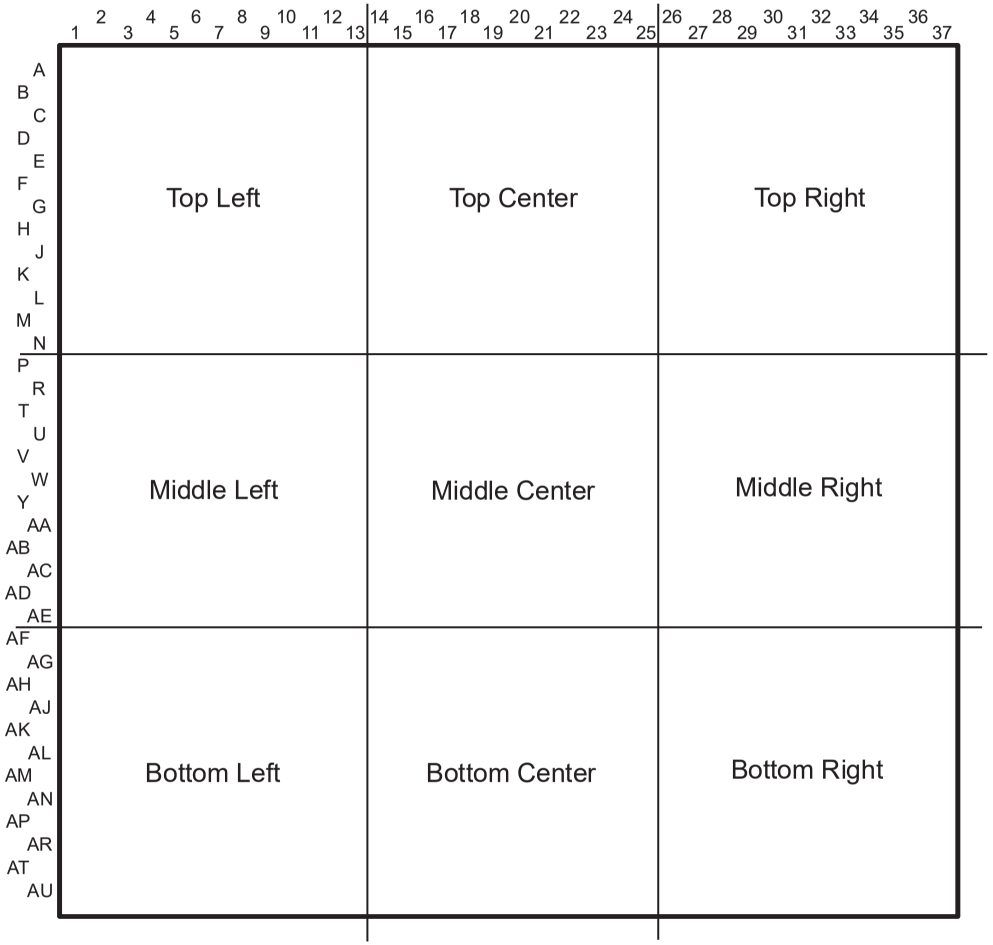


Figure 4-2 Package Quadrants Mapping

Table 4-1 shows pin mapping on the top left part of the package.

Table 4-1 Ball Map—Top Left

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DUMMY	DUMMY	EMI1_DQ2	EMI1_DQ5	EMI1_DMI0		EMI1_DQ7		EMI1_DQ8		EMI1_DMI1		EMI1_CA4
B	DUMMY	EMI2_ RESET_N	EMI0_EXTR	DVSS	DVSS	EMI1_DQ6	DVSS	EMI1_DQ15	DVSS	EMI1_DQ9	DVSS	EMI1_DQ14	DVSS
C	EMI2_DQ0	DVSS	EMI2_ DQS0_T	DVSS	EMI1_ DQS0_T	EMI1_DQ0		DVSS		DVSS		EMI1_DQ13	EMI1_CA3
D		EMI2_DQ1	EMI2_ DQS0_C	DVSS	EMI1_ DQS0_C	DVSS	DVSS	EMI1_DQ3	EMI1_ DQS1_T	EMI1_DQ10	DVSS	DVSS	DVSS
E	EMI2_ DMI0	DVSS		EMI2_DQ5	DVSS	DVSS	EMI1_DQ1	EMI1_DQ4	EMI1_ DQS1_C	DVSS	NC-PAD_ BRCKE1	EMI1_DQ12	
F		EMI2_DQ6	EMI2_DQ2	DVSS	EMI2_DQ4				DVSS	EMI1_DQ11	NC-PAD_ BRCKE0	NC-PAD_ BRCS1	NC_PAD_ BRDQ7_B1
G	EMI2_DQ7	DVSS		DVSS	EMI2_DQ3								
H		EMI2_DQ15	DVSS	EMI2_ DQS1_T	EMI2_ DQS1_C								
J	EMI2_DQ8	DVSS		DVSS	DVSS			AVDD18_ EMI		AVDD075_ EMI0		AVDD075_ EMI0	
K		EMI2_DQ9	DVSS	EMI2_DQ11	EMI2_DQ10						AVDDQ_ EMI0		AVDDQ_ EMI0
L	EMI2_DMI1	DVSS		EMI2_DQ13	DVSS			AVDD12_EMI	AVDD075_ EMI2				
M		EMI2_DQ14	EMI2_DQ12	DVSS	EMI2_CS0					AVDDQ_ EMI2	DVSS	DVDD_CORE	DVDD_ CORE
N	EMI2_CA4	DVSS	EMI2_CA3	EMI2_CS1	EMI2_CA0		DVSS		AVDD075_ EMI2		DVSS	DVSS	DVDD_ SRAM_CORE

PRELIMINARY INFORMATION

Table 4-2 shows pin mapping on the top center part of the package.

Table 4-2 Ball Map—Top Center

	14	15	16	17	18	19	20	21	22	23	24	25
A		EMI1_CA2		DVSS	EMI0_CA2		EMI0_CA4		EMI0_DMI1		EMI0_DQ8	
B		EMI1_CA5		EMI0_CA1	EMI0_CA0			EMI0_DQ14	DVSS	EMI0_DQ9	DVSS	EMI0_DQ15
C	EMI1_CKE1		EMI1_CA1				EMI0_CA3	DVSS		DVSS		DVSS
D	EMI1_CKE0	DVSS	EMI1_CK_C		DVSS	EMI0_CA5	NC-PAD_ ARDQ7_B1	EMI0_DQ12	EMI0_DQ13			
E	NC-PAD_ BRDQ6_B1	EMI1_CA0	EMI1_CK_T	EMI0_CK_T	EMI0_CS1		NC-PAD_ ARDQ6_B1	DVSS	NC-PAD_ ARCKE0	EMI0_DQ11	DVSS	EMI0_ DQS1_T
F	EMI1_CS0	EMI1_CS1	DVSS	EMI0_CK_C	DVSS	EMI0_CS0		NC-PAD_ ARCS1		NC-PAD_ ARCKE1	EMI0_DQ10	EMI0_ DQS1_C
G		DVSS					EMI0_CKE1	EMI0_CKE0	DVSS	DVSS	DVSS	DVSS
H						EMI0_TP					AVDD12_ UFS	AVDD12_ CKBUF_UFS
J	AVDD075_ EMI0	AVDD075_ EMI0		AVDD075_ EMI0	AVDD075_ EMI0	DVSS	DVSS	DVDD_CORE				
K	AVDDQ_ EMI0		AVDDQ_ EMI0		AVDDQ_EMI0		DVSS	DVDD_CORE	DVSS		DVSS	DVDD_ PROC_B
L	DVDD_CORE		DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVDD_CORE	DVSS	DVDD_ PROC_B
M	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_ SRAM_CORE	DVSS	DVDD_CORE	DVDD_CORE	DVDD_ SRAM_CORE	DVDD_CORE	DVSS	DVDD_ PROC_B
N		DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	TN_APPLLGP				DVSS	DVDD_ PROC_B

Table 4-3 shows pin mapping on the top right part of the package.

Table 4-3 Ball Map—Top Right

26	27	28	29	30	31	32	33	34	35	36	37	
EMI0_DQ7		EMI0_DMI0		EMI0_DQ2		DVSS		UFS_RST_N	EMMC_DSL	DUMMY	DUMMY	A
DVSS	EMI0_DQ6	DVSS	EMI0_DQ5	DVSS		UFS_RX0N	UFS_RX0P	DVSS	EMMC_RSTB	EMMC_CLK	DUMMY	B
EMI0_DQ4		EMI0_DQS0_T	DVSS	UFS_TX0P	UFS_TX0N	DVSS	DVSS	DVSS	EMMC_DAT3	EMMC_CMD	DVDD18_IOEMMC	C
DVSS	DVSS	EMI0_DQS0_C	EMI0_RESET_N	DVSS	DVSS	EMMC_DAT2	EMMC_DAT1	EMMC_DAT0	EMMC_DAT4	SDA0	SCL0	D
EMI0_DQ3	EMI0_DQ0	DVSS	DVSS		DVSS	EMMC_DAT7	EMMC_DAT6	EMMC_DAT5	SCL1	SDA1	SDA2	E
EMI0_DQ1		UFS_REFCK_OUT		DVSS	SPIM0_CSB	SPIM0_CLK	DVDD18_IOT	SCL3	SDA3	SDA4	SCL2	F
DVSS			UFS_PLL_CKREF		SPIM0_MI	SPIM0_MO	GPIO_03	GPIO_01	GPIO_04	SCL4		G
AVDD18_UFS			DVSS	DVSS	GPIO_00	GPIO_06	GPIO_05	GPIO_07	DVSS	DVDD28_MSDC2	DVSS	H
		DVSS			GPIO_02	DVSS	DVSS		CSI0A_L0P	CSI0A_L0N		J
DVDD_PROC_B	DVDD_PROC_B	DVSS	DVSS	DVSS	DVDD18_MSDC2	DVSS	CSI0A_L2N	CSI0A_L2P	CSI0A_L1P			K
DVDD_PROC_B	DVDD_PROC_B	DVDD_PROC_B	DVSS	DVDD_CORE	DVSS	CSI0B_L0P	CSI0B_L0N	CSI0A_L1N	DVSS	CSI0D_L0P	CSI0D_L0N	L
DVDD_PROC_B	DVSS	DVSS	DVSS		DVSS	CSI0B_L1N	CSI0B_L1P	DVSS	CSI0C_L0N	CSI0D_L1N	CSI0D_L1P	M
DVDD_PROC_B	DVSS	DVSS	DVDD_SRAM_PROC_B	AVDD18_CSI	CSI0C_L2P	CSI0C_L2N	CSI0C_L1N	CSI0C_L1P	CSI0C_L0P			N

Table 4-4 shows pin mapping on the middle left part of the package.

Table 4-4 Ball Map—Middle Left

	1	2	3	4	5	6	7	8	9	10	11	12	13
P			EMI2_CA5	EMI2_CA2	EMI2_CA1					AVDDQ_EMI2	DVSS	DVSS	DVDD_CORE
R	EMI2_CKE1	EMI2_CKE0		EMI2_CK_T	EMI2_CK_C		EMI2_TP		AVDD075_EMI2		DVSS	DVSS	DVDD_CORE
T		DVSS		EMI3_CK_T	EMI3_CK_C	DVSS				AVDDQ_EMI2	DVSS	DVDD_SRAM_CORE	DVDD_CORE
U	EMI3_CKE1	EMI3_CKE0	EMI3_CA2		EMI3_CA1	EMI3_CA0	DVSS		AVDD075_EMI2	AVDDQ_EMI2	DVSS	DVSS	DVDD_CORE
V			EMI3_CA5	EMI3_CS1	EMI3_CS0	DVSS	DVSS		AVDD075_EMI2	AVDDQ_EMI2	AVDD12_APPLLGP2	DVSS	DVDD_CORE
W	EMI3_CA4	DVSS	EMI3_CA3	DVSS	DVSS	DVSS				AVDDQ_EMI2	DVSS	AVDD18_APPLLGP2	DVDD_CORE
Y		EMI3_DQ14	EMI3_DQ13	DVSS	EMI3_DQ12	DVSS	DVSS	AVDD18_USB_P2	AVDD075_EMI2	DVDD_GPU	DVSS	DVSS	DVDD_GPU
AA	EMI3_DMI1	DVSS		DVSS	EMI3_DQ11	DVSS	DVSS	AVDD18_USB_P3		DVDD_GPU	DVSS	DVSS	DVDD_GPU
AB		EMI3_DQ9	DVSS	EMI3_DQ10	DVSS	DVSS	AVDD33_USB_P2			DVDD_GPU	DVSS	DVSS	DVDD_GPU
AC	EMI3_DQ8	DVSS		EMI3_DQS1_T	EMI3_DQS1_C		AVDD33_USB_P3		DVSS	DVDD_GPU	DVSS	DVDD_SRAM_GPU	DVDD_GPU
AD		EMI3_DQ15	DVSS	EMI3_DQ3	DVSS	AVDD12_USB_P2		USB_DP_P2		DVDD_GPU	DVDD_SRAM_GPU	DVSS	DVDD_GPU
AE	EMI3_DQ7	DVSS		DVSS	EMI3_DQ4	AVDD12_USB_P3		USB_DM_P2		DVDD_GPU	DVSS	DVSS	DVDD_GPU

Table 4-5 shows pin mapping on the middle center part of the package.

Table 4-5 Ball Map—Middle Center

	14	15	16	17	18	19	20	21	22	23	24	25
P	DVDD_CORE		DVSS	DVDD_CORE	DVDD_CORE	TP_APPLLGP	DVSS		AVDD12_APPLLGP1	DVDD_CORE	DVSS	DVDD_PROC_L
R	DVDD_CORE	DVSS		DVDD_CORE	DVDD_CORE	DVSS		AVDD18_APPLLGP1	DVDD_CORE	DVDD_CORE	DVSS	DVDD_PROC_L
T	DVDD_CORE	DVSS	DVSS			DVDD_SRAM_CORE	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVDD_PROC_L	DVDD_PROC_L
U	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVDD_SRAM_PROC_B	DVSS	DVDD_PROC_B
V	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_PROC_B
W	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVDD_PROC_B	DVDD_PROC_B
Y	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_PROC_B
AA	DVDD_GPU	DVSS	DVSS	DVDD_SRAM_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE		DVSS	DVSS	DVDD_CORE
AB	DVDD_GPU	DVDD18_VQPS	DVSS	DVDD_DLA				DVDD_CORE	DVDD_CORE	DVSS	DVSS	DVDD_CORE
AC	AVDD12_APPLLGP4	DVSS	DVSS	DVDD_DLA	DVDD_DLA	AVDD18_APPLLGP_APU	AVDD12_APPLLGP_APU				DVSS	DVDD_CORE
AD	AVDD18_APPLLGP4	DVSS	DVSS	DVDD_DLA	DVDD_DLA	DVSS	DVSS	DVDD_APU	DVDD_APU	DVSS		DVDD_CORE
AE	DVDD_GPU		DVSS	DVDD_DLA	DVDD_SRAM_APU	DVSS	DVSS	DVDD_APU	DVDD_APU	DVSS	DVSS	DVDD_SRAM_CORE

PRELIMINARY INFORMATION

Table 4-6 shows pin mapping on the middle right part of the package.

Table 4-6 Ball Map—Middle Right

26	27	28	29	30	31	32	33	34	35	36	37	
DVDD_PROC_L	DVSS	AVDD18_PROC	DVSS	AVDD12_CSI	DVSS	DVSS	DVSS	DVSS	DVSS			P
DVDD_PROC_L	DVDD_PROC_L	DVDD_SRAM_PROC_L			DVSS	CSI1A_L0P_T0A	CSI1A_L0N_T0B	CSI1A_L1P_T0C	CSI1A_L1N_T1A	CSI1A_L2P_T1B	CSI1A_L2N_T1C	R
DVDD_PROC_L	DVSS	DVSS			DVSS	CSI1B_L2N_T1C	CSI1B_L2P_T1B	CSI1B_L1N_T1A	CSI1B_L1P_T0C	CSI1B_L0P_T0A	CSI1B_L0N_T0B	T
DVDD_PROC_B	DVSS	DVSS	DVSS	AVDD18_CKSQ	AVDD12_CKSQ	DVSS	DVSS	DVSS	DVSS			U
DVDD_PROC_B	DVDD_PROC_B	DVSS		DVSS	DVSS	DVSS	PCIE_LN0_RXP_P1	PCIE_LN0_RXN_P1	DVSS	PCIE_CKRXP_P1	PCIE_CKRXN_P1	V
DVDD_PROC_B	DVDD_PROC_B	DVSS		DVSS	PCIE_LN0_TXP_P1	PCIE_LN0_TXN_P1	DVSS	DVSS	PCIEG3_LN0_RXN			W
DVDD_PROC_B	DVDD_PROC_B	DVSS	AVDD12_PCIE_P1	AVDD18_PCIE_P1	DVSS	DVSS	DVSS	DVSS	PCIEG3_LN0_RXP			Y
DVDD_CORE	DVSS	DVSS	DVSS	PCIEG3_LN0_TXP	PCIEG3_LN0_TXN	DVSS	PCIEG3_CLKN	PCIEG3_CLKP	DVSS	PCIEG3_LN1_TXN	PCIEG3_LN1_TXP	AA
DVDD_CORE	DVSS	X26M_IN		AVDD18_PCIEG3	DVSS	DVSS	DVSS	DVSS	PCIEG3_LN1_RXN			AB
DVDD_CORE		DVSS	AVDD12_PCIEG3	DVSS	USB_DP_P1	USB_DM_P1		DVSS	PCIEG3_LN1_RXP	DVSS		AC
DVDD_CORE	DVSS	AVDD12_DPTX	AVDD18_USB_P1	AVDD33_USB_P1	DVSS	DVSS	EDP_LN0_TXN	EDP_LN0_TXP	DVSS	EDP_LN1_TXP	EDP_LN1_TXN	AD
DVDD_CORE	DVDD_CORE				EDPAUXN	EDPAUXP	DVSS	DVSS	EDP_LN2_TXP			AE

Table 4-7 shows pin mapping on the bottom left part of the package.

Table 4-7 Ball Map—Bottom Left

	1	2	3	4	5	6	7	8	9	10	11	12	13
AF		EMI3_DQ6	EMI3_DQ5	DVSS	EMI3_DQ2	DVSS	DVSS			DVDD_GPU	DVSS	DVSS	DVDD_GPU
AG	EMI3_DMI0	DVSS	EMI3_DQS0_C	EMI3_DQS0_T	DVSS	DVSS	USB_DM_P3		DVSS	DVDD_GPU	DVSS	DVSS	DVDD_GPU
AH	EMI3_DQ1	EMI3_DQ0	DVSS	DVSS	DVSS	DVSS	USB_DP_P3		DVSS	DVDD_GPU	DVSS	DVSS	DVDD_GPU
AJ	EMI2_EXTR	DVSS	DSI0_D2P_T0A	DSI0_D2N_T0B	DVSS	DVSS	DVDD18_IOBR	DVDD_SRAM_CORE					
AK	AVDD12_DSI	DVSS	DSI0_D0N_T1A	DSI0_D0P_T0C		AUXIN5				DGI_D7	DGI_D6	DGI_D11	
AL		DSI0_CKN_T1C	DSI0_D1P_T2A		DVSS	AUXIN4	USB_IDDIG_1P	USB_DRV_VBUS_1P	USB_IDDIG	DSI_LCM_RST		DGI_D10	DGI_D13
AM	DVSS	DSI0_CKP_T1B	DSI0_D1N_T2B	DSI0_D3P_T2C	DVSS	AUXIN3	REFP	UART1_RTS		USB_DRV_VBUS		DVDD28_IODGI	
AN	DSI1_D2N_T0B	DSI1_D2P_T0A	DVSS	DSI0_D3N		AUXIN2	DVSS	MSDC1_CMD		KPROW1	KPROW0	DGI_D15	
AP		DSI1_D0P_T0C	DVSS	DVSS	AUXIN0	AUXIN1	DVSS	UART1_RXD	DISP_PWM0	UART0_RXD		DGI_D12	DGI_D14
AR	DSI1_D0N_T1A	DSI1_CKP_T1B	DSI1_CKN_T1C	DSI1_D3N	AVDD18_AUXADC	DVSS	DVSS	UART1_TXD		UART0_TXD		DGI_D9	
AT	DUMMY	DVSS	DVSS	DSI1_D3P_T2C	AVDD12_AUXADC	MSDC1_DAT0	MSDC1_DAT1	MSDC1_DAT2	DSI_DSI_TE	UART1_CTS	KPCOL1	DGI_DE	DGI_VSYNC
AU	DUMMY	DUMMY	DSI1_D1P_T2A	DSI1_D1N_T2B	DVDD18_MSDC1	DVDD28_MSDC1		MSDC1_DAT3	MSDC1_CLK		KPCOL0		

Table 4-8 shows pin mapping on the bottom center part of the package.

Table 4-8 Ball Map—Bottom Center

	14	15	16	17	18	19	20	21	22	23	24	25
AF	DVDD_GPU	DVSS	DVSS	DVDD_DLA	DVDD_DLA	DVSS	DVSS	DVDD_SRAM_APU	DVDD_APU	AVDD12_APPLLGP3	DVSS	DVDD_CORE
AG	DVDD_GPU	DVSS	DVSS	DVDD_DLA	DVDD_DLA	DVSS	DVSS	DVDD_APU	DVDD_APU	AVDD18_APPLLGP3		DVDD_CORE
AH	DVDD_GPU	DVSS	DVSS	DVDD_DLA	DVDD_DLA	DVSS	DVSS	DVDD_APU		DVSS		DVSS
AJ								DVDD_CORE	DVDD18_IOBM	DVDD_CORE		
AK	DGI_D3	AUD_DAT_MISO0	AUD_SYNC_MOSI		I2SO2_BCK	I2SO1_BCK	I2SIN_BCK		TESTMODE		AVDD18_HDMIRX21	
AL	DGI_D2		AUD_CLK_MOSI	DMIC1_DAT	I2SO2_MCK		I2SIN_MCK	PMIC_SRCLKEN_IN1	SYSRSTB	HDMITX_SCL	HDMITX_PWR5V	HDMITX_SDA
AM	DGI_D1		PCM_SYNC		I2SO1_D3		SPMI_M_SDA	PMIC_SRCLKEN_IN0	PMIC_WATCHDOG	HDMITX_CEC	HDMITX_HTPLG	HDMIRX_SCL
AN	DGI_D0	AUD_DAT_MOSI1	PCM_DI		I2SO1_D2	I2SO1_MCK	SPMI_M_SCL	PWRAP_SPI_MI	SPIM2_MO	SPIM2_CSB	HDMIRX_PWR5V	HDMIRX_HTPLG
AP	DGI_D8		PCM_CLK	DMIC1_SCK	I2SO1_D1		I2SIN_D0	PWRAP_SPI_MO	SPIM2_CLK	SPIM2_MI	HDMIRX_SDA	DPTX_HPD
AR	DGI_D5		PCM_DO		I2SO1_D0		I2SIN_WS	PMIC_RTC32K_CK		SPIM1_MI	AVDD08_HDMIRX21	DVSS
AT	DGI_CK	SCP_VREQ_VAO	AUD_DAT_MOSI0	AUD_DAT_MISO2	DMIC2_DAT	I2SO1_WS	I2SO2_D0	PWRAP_SPI_CK	SPIM1_CSB	SPIM1_MO		HDMIRX21_CLK_P
AU	DGI_HSYNC	DGI_D4		AUD_DAT_MISO1	DMIC2_SCK		I2SO2_WS	PWRAP_SPI_CSN		SPIM1_CLK		HDMIRX21_CLK_M

Table 4-9 shows pin mapping on the bottom right part of the package.

Table 4-9 Ball Map—Bottom Right

DVDD_CORE	DVSS		AVDD18_DPTX		DVSS	DVSS	EDP_LN3_TXN	EDP_LN3_TXP	DVSS	EDP_LN2_TXN	AVDD18_EDPTX	AF
DVDD_CORE		DVSS		DPAUXP	DPAUXN		DVSS	DVSS	DP_LN0_TXP			AG
DVSS		DVSS	AVDD12_EDPTX	AVDD12_USB_P1	DVSS	SSUSB_TXN	SSUSB_TXP	DVSS	DP_LN0_TXN			AH
AVDD33_HDMIRX21			AVDD12_HDMITX21	DVSS	SSUSB_RXP	DVSS	DVSS	DP_LN2_TXP	DVSS	DP_LN1_TXP	DP_LN1_TXN	AJ
DVSS	CMMCLK1			DVSS	SSUSB_RXN	DVSS	DVSS	DP_LN2_TXN				AK
CMMRST	CMMCLK0	PCIE_PERESET_N	PCIE_CLKREQ_N		AVDD18_HDMITX21	DP_LN3_TXP	DP_LN3_TXN	DVSS	DVSS			AL
CMMPDN	DVSS	CMMCLK2	PCIE_WAKE_N					AVDD33_USB_P0	USB_DP_P0	USB_DM_P0		AM
						DVSS	DVSS	AVDD18_USB_P0	AVDD18_SSUSB	AVDD12_SSUSB		AN
DVSS	DVSS	DVSS	DVSS	DVSS		DVSS	DVSS		DVSS	DVSS	AVDD12_USB_P0	AP
HDMIRX21_CH0_M	HDMIRX21_CH0_P	DVSS	HDMIRX21_CH2_M	HDMIRX21_CH2_P	DVSS	HDMITX21_CH0_M	HDMITX21_CH0_P	DVSS	HDMITX21_CH2_M	HDMITX21_CH2_P	DVSS	AR
		HDMIRX21_CH1_P			HDMITX21_CLK_M			HDMITX21_CH1_M		DVSS	DUMMY	AT
		HDMIRX21_CH1_M			HDMITX21_CLK_P			HDMITX21_CH1_P		DVSS	DUMMY	AU
26	27	28	29	30	31	32	33	34	35	36	37	

4.2 Pin Characteristics

Table 4-10 describes the pin characteristics and the multiplexed signals on each ball.

Table 4-10 Pin Characteristics

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO_00	H31	GPIO0	DIO	0	0		DVDD18	OFF	I
		TP_GPIO0_AO	DIO	1					
		MSDC2_CMD	DIO	2					
		TDMIN_MCK	DIO	3					
		CLKM0	DO	4					
		PERSTN_1	DO	5					
		IDDIG_1P	DI	6					
		DMIC4_CLK	DO	7					
GPIO_01	G34	GPIO1	DIO	0	0		DVDD18	OFF	I
		TP_GPIO1_AO	DIO	1					
		MSDC2_CLK	DIO	2					
		TDMIN_DI	DI	3					
		CLKM1	DO	4					
		CLKREQN_1	DIO	5					
		USB_DRVVBUS_1P	DO	6					
		DMIC4_DAT	DI	7					
GPIO_02	J31	GPIO2	DIO	0	0		DVDD18	OFF	I
		TP_GPIO2_AO	DIO	1					
		MSDC2_DAT3	DIO	2					
		TDMIN_LRCK	DIO	3					
		CLKM2	DO	4					
		WAKEN_1	DI	5					
		DMIC2_CLK	DO	7					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO_03	G33	GPIO3	DIO	0	0		DVDD18	OFF	I
		TP_GPIO3_AO	DIO	1					
		MSDC2_DAT0	DIO	2					
		TDMIN_BCK	DIO	3					
		CLKM3	DO	4					
		DMIC2_DAT	DI	7					
GPIO_04	G35	GPIO4	DIO	0	0		DVDD18	OFF	I
		TP_GPIO4_AO	DIO	1					
		MSDC2_DAT2	DIO	2					
		SPDIF_IN1	DI	3					
		UTXD3	DO	4					
		SDA2	DIO	5					
		IDDIG_2P	DI	7					
GPIO_05	H33	GPIO5	DIO	0	0		DVDD18	OFF	I
		TP_GPIO5_AO	DIO	1					
		MSDC2_DAT1	DIO	2					
		SPDIF_IN0	DI	3					
		URXD3	DI	4					
		SCL2	DIO	5					
		USB_DRVVBUS_2P	DO	7					
GPIO_06	H32	GPIO6	DIO	0	0		DVDD18	OFF	I
		TP_GPIO6_AO	DIO	1					
		DP_TX_HPD	DI	2					
		I2SO1_D4	DO	3					
		UTXD4	DO	4					
		CMVREF3	DO	5					
		DMIC3_CLK	DO	7					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO_07	H34	GPIO7	DIO	0	0		DVDD18	OFF	I
		TP_GPIO7_AO	DIO	1					
		EDP_TX_HPD	DI	2					
		I2SO1_D5	DO	3					
		URXD4	DI	4					
		CMVREF4	DO	5					
		DMIC3_DAT	DI	7					
SDA0	D36	GPIO8	DIO	0	1		DVDD18	PU	I
		SDA0	DIO	1					
		PWM_0	DO	2					
		SPDIF_OUT	DO	4					
		LVTS_FOUT	DO	6					
SCL0	D37	GPIO9	DIO	0	1		DVDD18	PU	I
		SCL0	DIO	1					
		PWM_1	DO	2					
		IR_IN	DI	4					
		LVTS_SDO	DO	6					
SDA1	E36	GPIO10	DIO	0	1		DVDD18	PU	I
		SDA1	DIO	1					
		PWM_2	DO	2					
		SPDIF_IN1	DI	4					
		LVTS_SCF	DI	6					
SCL1	E35	GPIO11	DIO	0	1		DVDD18	PU	I
		SCL1	DIO	1					
		PWM_3	DO	2					
		SPDIF_IN0	DI	4					
		LVTS_SCK	DI	6					
SDA2	E37	GPIO12	DIO	0	1		DVDD18	PU	I
		SDA2	DIO	1					
		DMIC3_DAT_R	DI	2					
		I2SO1_D6	DO	3					
		LVTS_SDI	DI	6					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
SCL2	F37	GPIO15	DIO	0	1		DVDD18	PU	I
		SCL3	DIO	1					
		DMIC3_CLK	DO	2					
		TDMIN_DI	DI	3					
SDA3	F35	GPIO14	DIO	0	1		DVDD18	PU	I
		SDA3	DIO	1					
		DMIC3_DAT	DI	2					
		TDMIN_MCK	DIO	3					
SCL3	F34	GPIO13	DIO	0	1		DVDD18	PU	I
		SCL2	DIO	1					
		DMIC4_DAT_R	DI	2					
		I2SO1_D7	DO	3					
SDA4	F36	GPIO16	DIO	0	1		DVDD18	PU	I
		SDA4	DIO	1					
		DMIC4_DAT	DI	2					
		TDMIN_LRCK	DIO	3					
SCL4	G36	GPIO17	DIO	0	1		DVDD18	PU	I
		SCL4	DIO	1					
		DMIC4_CLK	DO	2					
		TDMIN_BCK	DIO	3					
DPTX_HPD	AP25	GPIO18	AIO	0	0		DVDD18_IOBM	OFF	I
		DP_TX_HPD	DI	1					
PCIE_WAKE_N	AM29	GPIO19	AIO	0	0		DVDD18_IOBM	OFF	I
		WAKEN	DIO	1					
		SCP_SDA1	DIO	2					
		SDA6	DIO	5					
PCIE_PERESET_N	AL28	GPIO20	AIO	0	0		DVDD18_IOBM	OFF	I
		PERSTN	DIO	1					
		SCP_SCL1	DIO	2					
		SCL6	DIO	5					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
PCIE_CLKREQ_N	AL29	GPIO21	AIO	0	0		DVDD18_IOBM	OFF	I
		CLKREQN	DIO	1					
		SCP_SDA1	DIO	5					
CMMCLK0	AL27	GPIO22	DIO	0	0		DVDD18	OFF	I
		CMMCLK0	DO	1					
		PERSTN_1	DO	2					
		SCP_SCL1	DIO	5					
CMMCLK1	AK27	GPIO23	DIO	0	0		DVDD18	OFF	I
		CMMCLK1	DO	1					
		CLKREQN_1	DIO	2					
		SDA4	DIO	3					
		DMIC1_CLK	DO	4					
		SCP_SDA0	DIO	5					
CMMCLK2	AM28	GPIO24	DIO	0	0		DVDD18	OFF	I
		CMMCLK2	DO	1					
		WAKEN_1	DI	2					
		SCL4	DIO	3					
		DMIC1_DAT	DI	4					
		SCP_SCL0	DIO	5					
		LVTS_26M	DI	6					
CMMRST	AL26	GPIO25	DIO	0	0		DVDD18	OFF	I
		CMMRST	DO	1					
		CMMCLK3	DO	2					
		SPDIF_OUT	DO	3					
		SDA6	DIO	4					
CMMPDN	AM26	GPIO26	DIO	0	0		DVDD18	OFF	I
		CMMPDN	DO	1					
		CMMCLK4	DO	2					
		IR_IN	DI	3					
		SCL6	DIO	4					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
HDMIRX_HTPLG	AN25	GPIO27	DIO	0	0		DVDD18	OFF	I
		HDMIRX20_HTPLG	DO	1					
		CMFLASH0	DO	2					
		TP_UTXD2_AO	DO	4					
		SCL7	DIO	5					
		UCTS2	DI	6					
HDMIRX_PWR5V	AN24	GPIO28	DIO	0	0		DVDD18	OFF	I
		HDMIRX20_PWR5V	DI	1					
		CMFLASH1	DO	2					
		TP_URXD2_AO	DI	4					
		SDA7	DIO	5					
		URTS2	DO	6					
HDMIRX_SCL	AM25	GPIO29	DIO	0	0		DVDD18	OFF	I
		HDMIRX20_SCL	DI	1					
		CMFLASH2	DO	2					
		SCL5	DIO	3					
		TP_URTS2_AO	DO	4					
		UTXD2	DO	6					
HDMIRX_SDA	AP24	GPIO30	DIO	0	0		DVDD18	OFF	I
		HDMIRX20_SDA	DIO	1					
		CMFLASH3	DO	2					
		SDA5	DIO	3					
		TP_UCTS2_AO	DI	4					
		URXD2	DI	6					
HDMITX_PWR5V	AL24	GPIO31	DIO	0	0		DVDD18	OFF	I
		HDMITX20_PWR5V	DO	1					
		DMIC1_DAT_R	DI	2					
		PERSTN	DIO	3					
HDMITX_HTPLG	AM24	GPIO32	DIO	0	0		DVDD18	OFF	I
		HDMITX20_HTPLG	DI	1					
		CLKREQN	DIO	3					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
HDMITX_CEC	AM23	GPIO33	DIO	0	0		DVDD18	OFF	I
		HDMITX20_CEC	DIO	1					
		CMVREF0	DO	2					
		WAKEN	DIO	3					
HDMITX_SCL	AL23	GPIO34	DIO	0	0		DVDD18	OFF	I
		HDMITX20_SCL	DIO	1					
		CMVREF1	DO	2					
		SCL7	DIO	3					
		SCL6	DIO	4					
HDMITX_SDA	AL25	GPIO35	DIO	0	0		DVDD18	OFF	I
		HDMITX20_SDA	DIO	1					
		CMVREF2	DO	2					
		SDA7	DIO	3					
		SDA6	DIO	4					
SPIM2_CSB	AN23	GPIO140	DIO	0	1		DVDD18	PU	OH
		SPIM2_CSB	DO	1					
		SPINOR_CS	DO	2					
		SNFI_CS	DO	3					
		DMIC3_DAT	DI	4					
SPIM2_CLK	AP22	GPIO141	DIO	0	0		DVDD18	OFF	I
		SPIM2_CLK	DO	1					
		SPINOR_CK	DO	2					
		SNFI_CLK	DO	3					
		DMIC3_CLK	DO	4					
SPIM2_MO	AN22	GPIO142	DIO	0	0		DVDD18	OFF	I
		SPIM2_MO	DO	1					
		SPINOR_IO0	DIO	2					
		SNFI_MOSI	DIO	3					
		DMIC4_DAT	DI	4					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
SPIM2_MI	AP23	GPIO143	DIO	0	1		DVDD18	OFF	I
		SPIM2_MI	DI	1					
		SPINOR_IO1	DIO	2					
		SNFI_MISO	DIO	3					
		DMIC4_CLK	DO	4					
SPIM1_CSB	AT22	GPIO136	DIO	0	0		DVDD18	OFF	I
		SPIM1_CSB	DO	1					
		SCP_SPI1_A_CS	DO	2					
		SPIS1_CSB	DI	3					
SPIM1_CLK	AU23	GPIO137	DIO	0	0		DVDD18	OFF	I
		SPIM1_CLK	DO	1					
		SCP_SPI1_A_CK	DO	2					
		SPIS1_CLK	DI	3					
SPIM1_MO	AT23	GPIO138	DIO	0	0		DVDD18	OFF	I
		SPIM1_MO	DO	1					
		SCP_SPI1_A_MO	DO	2					
		SPIS1_SI	DI	3					
SPIM1_MI	AR23	GPIO139	DIO	0	0		DVDD18	OFF	I
		SPIM1_MI	DI	1					
		SCP_SPI1_A_MI	DI	2					
		SPIS1_SO	DO	3					
PMIC_RTC32K_CK	AR21	GPIO36	DIO	0	1		DVDD18	OFF	I
		RTC32K_CK	DI	1					
PMIC_WATCHDOG	AM22	GPIO37	DIO	0	1		DVDD18	OFF	OL
		WATCHDOG	DO	1					
PMIC_SRCLKEN_IN0	AM21	GPIO38	DIO	0	1		DVDD18	PU	OH
		SRCLKENA0	DO	1					
PMIC_SRCLKEN_IN1	AL21	GPIO39	DIO	0	1		DVDD18	PU	OH
		SRCLKENA1	DO	1					
		DMIC2_DAT_R	DI	2					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
PWRAP_SPI_CSN	AU21	GPIO40	DIO	0	1		DVDD18	PU	OH
		PWRAP_SPI0_CSN	DO	1					
		SPIM3_CSB	DO	3					
PWRAP_SPI_CK	AT21	GPIO41	DIO	0	1		DVDD18	OFF	OL
		PWRAP_SPI0_CK	DO	1					
		SPIM3_CLK	DO	3					
PWRAP_SPI_MO	AP21	GPIO42	DIO	0	1		DVDD18	OFF	I
		PWRAP_SPI0_MO	DIO	1					
		PWRAP_SPI0_MI	DIO	2					
		SPIM3_MO	DO	3					
PWRAP_SPI_MI	AN21	GPIO43	DIO	0	1		DVDD18	OFF	I
		PWRAP_SPI0_MI	DIO	1					
		PWRAP_SPI0_MO	DIO	2					
		SPIM3_MI	DI	3					
SPMI_M_SCL	AN20	GPIO44	DIO	0	1		DVDD18	OFF	OL
		SPMI_M_SCL	DIO	1					
		SCL5	DIO	3					
		UTXD5	DO	4					
SPMI_M_SDA	AM20	GPIO45	DIO	0	1		DVDD18	OFF	I
		SPMI_M_SDA	DIO	1					
		SDA5	DIO	3					
		URXD5	DI	4					
I2SIN_MCK	AL20	GPIO46	DIO	0	0		DVDD18	OFF	I
		I2SIN_MCK	DIO	1					
		SPLIN_MCK	DI	3					
I2SIN_BCK	AK20	GPIO47	DIO	0	0		DVDD18	OFF	I
		I2SIN_BCK	DIO	1					
		SPLIN_LRCK	DI	3					
I2SIN_WS	AR20	GPIO48	DIO	0	0		DVDD18	OFF	I
		I2SIN_WS	DIO	1					
		SPLIN_BCK	DI	3					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
I2SIN_D0	AP20	GPIO49	DIO	0	0		DVDD18	OFF	I
		I2SIN_D0	DI	1					
		SPLIN_D0	DI	3					
I2SO1_MCK	AN19	GPIO50	DIO	0	0		DVDD18	OFF	I
		I2SO1_MCK	DO	1					
I2SO1_BCK	AK19	GPIO51	DIO	0	0		DVDD18	OFF	I
		I2SO1_BCK	DO	1					
I2SO1_WS	AT19	GPIO52	DIO	0	0		DVDD18	OFF	I
		I2SO1_WS	DO	1					
I2SO1_D0	AR18	GPIO53	DIO	0	0		DVDD18	OFF	I
		I2SO1_D0	DO	1					
I2SO1_D1	AP18	GPIO54	DIO	0	0		DVDD18	OFF	I
		I2SO1_D1	DO	1					
		SPLIN_D1	DI	3					
I2SO1_D2	AN18	GPIO55	DIO	0	0		DVDD18	OFF	I
		I2SO1_D2	DO	1					
		SPLIN_D2	DI	3					
I2SO1_D3	AM18	GPIO56	DIO	0	0		DVDD18	OFF	I
		I2SO1_D3	DO	1					
		SPLIN_D3	DI	3					
I2SO2_MCK	AL18	GPIO57	DIO	0	0		DVDD18	OFF	I
		I2SO2_MCK	DO	1					
		LCM1_RST	DO	3					
I2SO2_BCK	AK18	GPIO58	DIO	0	0		DVDD18	OFF	I
		I2SO2_BCK	DIO	1					
I2SO2_WS	AU20	GPIO59	DIO	0	0		DVDD18	OFF	I
		I2SO2_WS	DIO	1					
I2SO2_D0	AT20	GPIO60	DIO	0	0		DVDD18	OFF	I
		I2SO2_D0	DO	1					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
DMIC1_SCK	AP17	GPIO61	DIO	0	0		DVDD18_IOBM	OFF	I
		DMIC1_CLK	DO	1					
		I2SO2_BCK	DIO	2					
		SCP_SPI2_CK	DO	3					
DMIC1_DAT	AL17	GPIO62	DIO	0	0		DVDD18_IOBM	OFF	I
		DMIC1_DAT	DI	1					
		I2SO2_WS	DIO	2					
		SCP_SPI2_MI	DI	3					
DMIC2_SCK	AU18	GPIO63	DIO	0	0		DVDD18_IOBM	OFF	I
		DMIC2_CLK	DO	1					
		VBUSVALID	DI	2					
		SCP_SPI2_MO	DO	3					
		SCP_SCL2	DIO	4					
DMIC2_DAT	AT18	GPIO64	DIO	0	0		DVDD18_IOBM	OFF	I
		DMIC2_DAT	DI	1					
		VBUSVALID_1P	DI	2					
		SCP_SPI2_CS	DO	3					
		SCP_SDA2	DIO	4					
PCM_DO	AR16	GPIO65	DO	0	0		DVDD18_IOBM	OFF	I
		PCM_DO	DO	1					
		AUXIF_ST0	DO	2					
		UCTS2	DI	3					
PCM_CLK	AP16	GPIO66	DIO	0	0		DVDD18_IOBM	OFF	I
		PCM_CLK	DIO	1					
		AUXIF_CLK0	DO	2					
		URTS2	DO	3					
PCM_DI	AN16	GPIO67	DI	0	0		DVDD18_IOBM	OFF	I
		PCM_DI	DI	1					
		AUXIF_ST1	DO	2					
		UTXD2	DO	3					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
PCM_SYNC	AM16	GPIO68	DIO	0	0		DVDD18_IOBM	OFF	I
		PCM_SYNC	DIO	1					
		AUXIF_CLK1	DO	2					
		URXD2	DI	3					
AUD_CLK_MOSI	AL16	GPIO69	DIO	0	0		DVDD18	OFF	I
		AUD_CLK_MOSI	DO	1					
		PWM_0	DO	3					
		WAKEN	DIO	4					
AUD_SYNC_MOSI	AK16	GPIO70	DIO	0	0		DVDD18	OFF	I
		AUD_SYNC_MOSI	DO	1					
		PWM_1	DO	3					
		PERSTN	DIO	4					
AUD_DAT_MOSI0	AT16	GPIO71	DIO	0	0		DVDD18	OFF	I
		AUD_DAT_MOSI0	DO	1					
		IDDIG_2P	DI	2					
		PWM_2	DO	3					
		CLKREQN	DIO	4					
AUD_DAT_MOSI1	AN15	GPIO72	DIO	0	0		DVDD18	OFF	I
		AUD_DAT_MOSI1	DO	1					
		USB_DRVVBUS_2P	DO	2					
		PWM_3	DO	3					
		PERSTN_1	DO	4					
AUD_DAT_MISO0	AK15	GPIO73	DIO	0	0		DVDD18	OFF	I
		AUD_DAT_MISO0	DI	1					
		CLKREQN_1	DIO	4					
		VOW_DAT_MISO	DI	5					
AUD_DAT_MISO1	AU17	GPIO74	DIO	0	0		DVDD18	OFF	I
		AUD_DAT_MISO1	DI	1					
		WAKEN_1	DI	4					
		VOW_CLK_MISO	DI	5					
AUD_DAT_MISO2	AT17	GPIO75	DIO	0	0		DVDD18	OFF	I
		AUD_DAT_MISO2	DI	1					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
SCP_VREQ_VAO	AT15	GPIO76	DIO	0	0		DVDD18	OFF	I
		SCP_VREQ_VAO	DO	1					
DGI_D0	AN14	GPIO77	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D0	DO	2					
		SPIM4_CLK	DO	4					
		GBE_TXD3	DO	5					
DGI_D1	AM14	GPIO78	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D1	DO	2					
		SPIM4_MO	DO	4					
		GBE_TXD2	DO	5					
DGI_D2	AL14	GPIO79	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D2	DO	2					
		SPIM4_CSB	DO	4					
		GBE_TXD1	DO	5					
DGI_D3	AK14	GPIO80	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D3	DO	2					
		SPIM4_MI	DI	4					
		GBE_TXD0	DO	5					
DGI_D4	AU15	GPIO81	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D4	DO	2					
		SPIM5_CLK	DO	4					
		GBE_RXD3	DI	5					
DGI_D5	AR14	GPIO82	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D5	DO	2					
		SPIM5_MO	DO	4					
		GBE_RXD2	DI	5					
DGI_D6	AK11	GPIO83	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D6	DO	2					
		SPIM5_CSB	DO	4					
		GBE_RXD1	DI	5					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
DGI_D7	AK10	GPIO84	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D7	DO	2					
		SPIM5_MI	DI	4					
		GBE_RXD0	DI	5					
DGI_D8	AP14	GPIO85	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D8	DO	2					
		SCP_SPI1_B_CK	DO	4					
		GBE_TXC	DIO	5					
DGI_D9	AR12	GPIO86	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D9	DO	2					
		SCP_SPI1_B_MI	DI	4					
		GBE_RXC	DI	5					
DGI_D10	AL12	GPIO87	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D10	DO	2					
		SCP_SPI1_B_CS	DO	4					
		GBE_RXDV	DI	5					
DGI_D11	AK12	GPIO88	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D11	DO	2					
		SCP_SPI1_B_MO	DO	4					
		GBE_TXEN	DO	5					
DGI_D12	AP12	GPIO89	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D12	DO	2					
		MSDC2_CMD_A	DIO	3					
		GBE_MDC	DO	5					
DGI_D13	AL13	GPIO90	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D13	DO	2					
		MSDC2_CLK_A	DIO	3					
		GBE_MDIO	DIO	5					
DGI_D14	AP13	GPIO91	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D14	DO	2					
		MSDC2_DAT3_A	DIO	3					
		GBE_TXER	DO	5					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
DGI_D15	AN12	GPIO92	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_D15	DO	2					
		MSDC2_DAT0_A	DIO	3					
		I2SO2_D1	DO	4					
		GBE_RXER	DI	5					
DGI_HSYNC	AU14	GPIO93	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_HSYNC	DO	2					
		MSDC2_DAT2_A	DIO	3					
		I2SO2_D2	DO	4					
		GBE_COL	DI	5					
DGI_VSYNC	AT13	GPIO94	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_VSYNC	DO	2					
		MSDC2_DAT1_A	DIO	3					
		I2SO2_D3	DO	4					
		GBE_INTR	DI	5					
DGI_DE	AT12	GPIO95	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_DE	DO	2					
		UTXD2	DO	3					
		I2SIN_D1	DI	5					
DGI_CK	AT14	GPIO96	DIO	0	0		DVDD28_IODGI	OFF	I
		DPI_CK	DO	2					
		URXD2	DI	3					
		I2SIN_D2	DI	5					
DISP_PWM0	AP9	GPIO97	DIO	0	0		DVDD18	OFF	I
		DISP_PWM0	DO	1					
UART0_TXD	AR10	GPIO98	DIO	0	1		DVDD18	PU	OH
		UTXD0	DO	1					
UART0_RXD	AP10	GPIO99	DIO	0	1		DVDD18	PU	I
		URXD0	DI	1					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
UART1_RTS	AM8	GPIO100	DIO	0	0		DVDD18	OFF	I
		URTS1	DO	1					
		DSI_TE	DI	2					
		I2SO1_D8	DO	3					
		KPROW2	DIO	4					
		PWM_0	DO	5					
		TP_URTS1_AO	DO	6					
		I2SIN_D0	DI	7					
UART1_CTS	AT10	GPIO101	DIO	0	0		DVDD18	OFF	I
		UCTS1	DI	1					
		DSI1_TE	DI	2					
		I2SO1_D9	DO	3					
		KPCOL2	DIO	4					
		PWM_1	DO	5					
		TP_UCTS1_AO	DI	6					
		I2SIN_D1	DI	7					
UART1_TXD	AR8	GPIO102	DIO	0	0		DVDD18	OFF	I
		UTXD1	DO	1					
		VBUSVALID_2P	DI	2					
		I2SO1_D10	DO	3					
		TP_UTXD1_AO	DO	5					
		I2SIN_D2	DI	7					
UART1_RXD	AP8	GPIO103	DIO	0	0		DVDD18	OFF	I
		URXD1	DI	1					
		VBUSVALID_3P	DI	2					
		I2SO1_D11	DO	3					
		TP_URXD1_AO	DI	5					
		I2SIN_D3	DI	7					
KPROW0	AN11	GPIO104	DIO	0	1		DVDD18	OFF	OL
		KPROW0	DIO	1					
		DISP_PWM1	DO	2					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
KPROW1	AN10	GPIO105	DIO	0	0		DVDD18	OFF	I
		KPROW1	DIO	1					
		EDP_TX_HPD	DI	2					
		PWM_2	DO	3					
KPCOL0	AU11	GPIO106	DIO	0	1		DVDD18	PU	I
		KPCOL0	DIO	1					
KPCOL1	AT11	GPIO107	DIO	0	0		DVDD18	OFF	I
		KPCOL1	DIO	1					
		DSI1_TE	DI	2					
		PWM_3	DO	3					
		SCP_SCL3	DIO	4					
		I2SIN_MCK	DIO	5					
DSI_LCM_RST	AL10	GPIO108	DIO	0	0		DVDD18	OFF	I
		LCM_RST	DO	1					
		KPCOL1	DIO	2					
		SCP_SDA3	DIO	4					
		I2SIN_BCK	DIO	5					
DSI_DSI_TE	AT9	GPIO109	DIO	0	0		DVDD18	OFF	I
		DSI_TE	DI	1					
		I2SIN_D3	DI	2					
		I2SIN_WS	DIO	5					
USB_IDDIG	AL9	GPIO128	AIO	0	0		DVDD18_IOBR	OFF	I
		IDDIG	DI	1					
		UCTS2	DI	2					
		UTXD5	DO	3					
		UFS_MPHY_SCL	DI	4					
		SCP_SCL2	DIO	7					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
USB_DRV_VBUS	AM10	GPIO129	AIO	0	0		DVDD18_IOBR	OFF	I
		USB_DRVVBUS	DO	1					
		URTS2	DO	2					
		URXD5	DI	3					
		UFS_MPHY_SDA	DIO	4					
		SCP_SDA2	DIO	7					
USB_IDDIG_1P	AL7	GPIO130	AIO	0	0		DVDD18_IOBR	OFF	I
		IDDIG_1P	DI	1					
		SPINOR_IO2	DIO	2					
		SNFI_WP	DIO	3					
USB_DRV_VBUS_1P	AL8	GPIO131	AIO	0	0		DVDD18_IOBR	OFF	I
		USB_DRVVBUS_1P	DO	1					
		SPINOR_IO3	DIO	2					
		SNFI_HOLD	DIO	3					
MSDC1_CMD	AN8	GPIO110	DIO	0	1	MSDC1IO	DVDD28_MSDC1	PU	I
		MSDC1_CMD	DIO	1					
MSDC1_CLK	AU9	GPIO111	DIO	0	1	MSDC1IO	DVDD28_MSDC1	OFF	OL
		MSDC1_CLK	DIO	1					
MSDC1_DAT0	AT6	GPIO112	DIO	0	1	MSDC1IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT0	DIO	1					
		I2SO2_D0	DO	4					
MSDC1_DAT1	AT7	GPIO113	DIO	0	1	MSDC1IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT1	DIO	1					
		I2SO2_D1	DO	4					
MSDC1_DAT2	AT8	GPIO114	DIO	0	1	MSDC1IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT2	DIO	1					
		I2SO2_D2	DO	4					
MSDC1_DAT3	AU8	GPIO115	DIO	0	1	MSDC1IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT3	DIO	1					
		I2SO2_D3	DO	4					
EMMC_DAT7	E32	GPIO116	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT7	DIO	1					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMMC_DAT6	E33	GPIO117	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT6	DIO	1					
EMMC_DAT5	E34	GPIO118	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT5	DIO	1					
EMMC_DAT4	D35	GPIO119	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT4	DIO	1					
EMMC_RSTB	B35	GPIO120	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	OH
		MSDC0_RSTB	DO	1					
EMMC_CMD	C36	GPIO121	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_CMD	DIO	1					
EMMC_CLK	B36	GPIO122	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	OFF	OL
		MSDC0_CLK	DIO	1					
EMMC_DAT3	C35	GPIO123	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT3	DIO	1					
EMMC_DAT2	D32	GPIO124	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT2	DIO	1					
EMMC_DAT1	D33	GPIO125	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT1	DIO	1					
EMMC_DAT0	D34	GPIO126	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	PU	I
		MSDC0_DAT0	DIO	1					
EMMC_DSL	A35	GPIO127	DIO	0	1	MSDC0IO	DVDD18_IOEMMC	OFF	I
		MSDC0_DSL	DIO	1					
SPIM0_CSB	F31	GPIO132	DIO	0	0		DVDD18	OFF	I
		SPIM0_CSB	DO	1					
		SCP_SPI0_CS	DO	2					
		SPIS0_CSB	DI	3					
SPIM0_CLK	F32	GPIO133	DIO	0	0		DVDD18	OFF	I
		SPIM0_CLK	DO	1					
		SCP_SPI0_CK	DO	2					
		SPIS0_CLK	DI	3					

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
SPIM0_MO	G32	GPIO134	DIO	0	0		DVDD18	OFF	I
		SPIM0_MO	DO	1					
		SCP_SPI0_MO	DO	2					
		SPIS0_SI	DI	3					
SPIM0_MI	G31	GPIO135	DIO	0	0		DVDD18	OFF	I
		SPIM0_MI	DI	1					
		SCP_SPI0_MI	DI	2					
		SPIS0_SO	DO	3					
SYSRSTB	AL22	SYSRSTB	DI				DVDD18		
TESTMODE	AK22	TESTMODE	DI				DVDD18		
X26M_IN	AB28	X26M_IN	DIO				DVDD18		
EMI0_CA2	A18	EMI0_CA2	DIO			DDRIO	AVDDQ_EMI		
EMI0_CA4	A20	EMI0_CA4	DIO			DDRIO	AVDDQ_EMI		
EMI0_DMI1	A22	EMI0_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ8	A24	EMI0_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ7	A26	EMI0_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI0_DMI0	A28	EMI0_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ2	A30	EMI0_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI0_EXTR	B3	EMI0_EXTR	DIO			DDRIO	AVDDQ_EMI		
EMI0_CA1	B17	EMI0_CA1	DIO			DDRIO	AVDDQ_EMI		
EMI0_CA0	B18	EMI0_CA0	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ14	B21	EMI0_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ9	B23	EMI0_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ15	B25	EMI0_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ6	B27	EMI0_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ5	B29	EMI0_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI0_CA3	C20	EMI0_CA3	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ4	C26	EMI0_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS0_T	C28	EMI0_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI0_CA5	D19	EMI0_CA5	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ12	D21	EMI0_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ13	D22	EMI0_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS0_C	D28	EMI0_DQS0_C	DIO			DDRIO	AVDDQ_EMI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI0_RESET_N	D29	EMI0_RESET_N	DIO			DDRIO	AVDD12_EMI		
EMI0_CK_T	E17	EMI0_CK_T	DIO			DDRIO	AVDDQ_EMI		
EMI0_CS1	E18	EMI0_CS1	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ11	E23	EMI0_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS1_T	E25	EMI0_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ3	E26	EMI0_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ0	E27	EMI0_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI0_CK_C	F17	EMI0_CK_C	DIO			DDRIO	AVDDQ_EMI		
EMI0_CS0	F19	EMI0_CS0	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ10	F24	EMI0_DQ10	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQS1_C	F25	EMI0_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI0_DQ1	F26	EMI0_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI0_CKE1	G20	EMI0_CKE1	DIO			DDRIO	AVDD12_EMI		
EMI0_CKE0	G21	EMI0_CKE0	DIO			DDRIO	AVDD12_EMI		
EMI0_TP	H19	EMI0_TP	DIO			DDRIO	AVDD12_EMI		
EMI1_DQ2	A3	EMI1_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ5	A4	EMI1_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI1_DMI0	A5	EMI1_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ7	A7	EMI1_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ8	A9	EMI1_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI1_DMI1	A11	EMI1_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI1_CA4	A13	EMI1_CA4	DIO			DDRIO	AVDDQ_EMI		
EMI1_CA2	A15	EMI1_CA2	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ6	B6	EMI1_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ15	B8	EMI1_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ9	B10	EMI1_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ14	B12	EMI1_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI1_CA5	B15	EMI1_CA5	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS0_T	C5	EMI1_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ0	C6	EMI1_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ13	C12	EMI1_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI1_CA3	C13	EMI1_CA3	DIO			DDRIO	AVDDQ_EMI		
EMI1_CKE1	C14	EMI1_CKE1	DIO			DDRIO	AVDD12_EMI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI1_CA1	C16	EMI1_CA1	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS0_C	D5	EMI1_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ3	D8	EMI1_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS1_T	D9	EMI1_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ10	D10	EMI1_DQ10	DIO			DDRIO	AVDDQ_EMI		
EMI1_CKE0	D14	EMI1_CKE0	DIO			DDRIO	AVDD12_EMI		
EMI1_CK_C	D16	EMI1_CK_C	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ1	E7	EMI1_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ4	E8	EMI1_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQS1_C	E9	EMI1_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ12	E12	EMI1_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI1_CA0	E15	EMI1_CA0	DIO			DDRIO	AVDDQ_EMI		
EMI1_CK_T	E16	EMI1_CK_T	DIO			DDRIO	AVDDQ_EMI		
EMI1_DQ11	F10	EMI1_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI1_CS0	F14	EMI1_CS0	DIO			DDRIO	AVDDQ_EMI		
EMI1_CS1	F15	EMI1_CS1	DIO			DDRIO	AVDDQ_EMI		
EMI2_RESET_N	B2	EMI2_RESET_N	DIO			DDRIO	AVDD12_EMI		
EMI2_DQ0	C1	EMI2_DQ0	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS0_T	C3	EMI2_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ1	D2	EMI2_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS0_C	D3	EMI2_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI2_DMI0	E1	EMI2_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ5	E4	EMI2_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ6	F2	EMI2_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ2	F3	EMI2_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ4	F5	EMI2_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ7	G1	EMI2_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ3	G5	EMI2_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ15	H2	EMI2_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS1_T	H4	EMI2_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQS1_C	H5	EMI2_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ8	J1	EMI2_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ9	K2	EMI2_DQ9	DIO			DDRIO	AVDDQ_EMI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI2_DQ11	K4	EMI2_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ10	K5	EMI2_DQ10	DIO			DDRIO	AVDDQ_EMI		
EMI2_DMI1	L1	EMI2_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ13	L4	EMI2_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ14	M2	EMI2_DQ14	DIO			DDRIO	AVDDQ_EMI		
EMI2_DQ12	M3	EMI2_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI2_CS0	M5	EMI2_CS0	DIO			DDRIO	AVDDQ_EMI		
EMI2_CA4	N1	EMI2_CA4	DIO			DDRIO	AVDDQ_EMI		
EMI2_CA3	N3	EMI2_CA3	DIO			DDRIO	AVDDQ_EMI		
EMI2_CS1	N4	EMI2_CS1	DIO			DDRIO	AVDDQ_EMI		
EMI2_CA0	N5	EMI2_CA0	DIO			DDRIO	AVDDQ_EMI		
EMI2_CA5	P3	EMI2_CA5	DIO			DDRIO	AVDDQ_EMI		
EMI2_CA2	P4	EMI2_CA2	DIO			DDRIO	AVDDQ_EMI		
EMI2_CA1	P5	EMI2_CA1	DIO			DDRIO	AVDDQ_EMI		
EMI2_CKE1	R1	EMI2_CKE1	DIO			DDRIO	AVDD12_EMI		
EMI2_CKE0	R2	EMI2_CKE0	DIO			DDRIO	AVDD12_EMI		
EMI2_CK_T	R4	EMI2_CK_T	DIO			DDRIO	AVDDQ_EMI		
EMI2_CK_C	R5	EMI2_CK_C	DIO			DDRIO	AVDDQ_EMI		
EMI2_TP	R7	EMI2_TP	DIO			DDRIO	AVDD12_EMI		
EMI2_EXTR	AJ1	EMI2_EXTR	DIO			DDRIO	AVDDQ_EMI		
EMI3_CK_T	T4	EMI3_CK_T	DIO			DDRIO	AVDDQ_EMI		
EMI3_CK_C	T5	EMI3_CK_C	DIO			DDRIO	AVDDQ_EMI		
EMI3_CKE1	U1	EMI3_CKE1	DIO			DDRIO	AVDD12_EMI		
EMI3_CKE0	U2	EMI3_CKE0	DIO			DDRIO	AVDD12_EMI		
EMI3_CA2	U3	EMI3_CA2	DIO			DDRIO	AVDDQ_EMI		
EMI3_CA1	U5	EMI3_CA1	DIO			DDRIO	AVDDQ_EMI		
EMI3_CA0	U6	EMI3_CA0	DIO			DDRIO	AVDDQ_EMI		
EMI3_CA5	V3	EMI3_CA5	DIO			DDRIO	AVDDQ_EMI		
EMI3_CS1	V4	EMI3_CS1	DIO			DDRIO	AVDDQ_EMI		
EMI3_CS0	V5	EMI3_CS0	DIO			DDRIO	AVDDQ_EMI		
EMI3_CA4	W1	EMI3_CA4	DIO			DDRIO	AVDDQ_EMI		
EMI3_CA3	W3	EMI3_CA3	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ14	Y2	EMI3_DQ14	DIO			DDRIO	AVDDQ_EMI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI3_DQ13	Y3	EMI3_DQ13	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ12	Y5	EMI3_DQ12	DIO			DDRIO	AVDDQ_EMI		
EMI3_DMI1	AA1	EMI3_DMI1	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ11	AA5	EMI3_DQ11	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ9	AB2	EMI3_DQ9	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ10	AB4	EMI3_DQ10	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ8	AC1	EMI3_DQ8	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS1_T	AC4	EMI3_DQS1_T	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS1_C	AC5	EMI3_DQS1_C	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ15	AD2	EMI3_DQ15	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ3	AD4	EMI3_DQ3	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ7	AE1	EMI3_DQ7	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ4	AE5	EMI3_DQ4	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ6	AF2	EMI3_DQ6	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ5	AF3	EMI3_DQ5	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ2	AF5	EMI3_DQ2	DIO			DDRIO	AVDDQ_EMI		
EMI3_DMI0	AG1	EMI3_DMI0	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS0_C	AG3	EMI3_DQS0_C	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQS0_T	AG4	EMI3_DQS0_T	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ1	AH1	EMI3_DQ1	DIO			DDRIO	AVDDQ_EMI		
EMI3_DQ0	AH2	EMI3_DQ0	DIO			DDRIO	AVDDQ_EMI		
DSI0_D2P_T0A	AJ3	DSI0_D2P_T0A	AIO				AVDD12_DSI		
DSI0_D2N_T0B	AJ4	DSI0_D2N_T0B	AIO				AVDD12_DSI		
DSI0_D0N_T1A	AK3	DSI0_D0N_T1A	AIO				AVDD12_DSI		
DSI0_D0P_T0C	AK4	DSI0_D0P_T0C	AIO				AVDD12_DSI		
DSI0_CKN_T1C	AL2	DSI0_CKN_T1C	AIO				AVDD12_DSI		
DSI0_D1P_T2A	AL3	DSI0_D1P_T2A	AIO				AVDD12_DSI		
DSI0_CKP_T1B	AM2	DSI0_CKP_T1B	AIO				AVDD12_DSI		
DSI0_D1N_T2B	AM3	DSI0_D1N_T2B	AIO				AVDD12_DSI		
DSI0_D3P_T2C	AM4	DSI0_D3P_T2C	AIO				AVDD12_DSI		
DSI0_D3N	AN4	DSI0_D3N	AIO				AVDD12_DSI		
DSI1_D2N_T0B	AN1	DSI1_D2N_T0B	AO				AVDD12_CSI		
DSI1_D2P_T0A	AN2	DSI1_D2P_T0A	AIO				AVDD12_CSI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
DSI1_D0P_T0C	AP2	DSI1_D0P_T0C	AIO				AVDD12_CSI		
DSI1_D0N_T1A	AR1	DSI1_D0N_T1A	AIO				AVDD12_CSI		
DSI1_CKP_T1B	AR2	DSI1_CKP_T1B	AIO				AVDD12_CSI		
DSI1_CKN_T1C	AR3	DSI1_CKN_T1C	AIO				AVDD12_CSI		
DSI1_D3N	AR4	DSI1_D3N	AIO				AVDD12_CSI		
DSI1_D3P_T2C	AT4	DSI1_D3P_T2C	AIO				AVDD12_CSI		
DSI1_D1P_T2A	AU3	DSI1_D1P_T2A	AIO				AVDD12_CSI		
DSI1_D1N_T2B	AU4	DSI1_D1N_T2B	AIO				AVDD12_CSI		
CSI0A_L0P	J35	CSI0A_L0P	AIO				AVDD12_CSI		
CSI0A_L0N	J36	CSI0A_L0N	AIO				AVDD12_CSI		
CSI0A_L2N	K33	CSI0A_L2N	AIO				AVDD12_CSI		
CSI0A_L2P	K34	CSI0A_L2P	AIO				AVDD12_CSI		
CSI0A_L1P	K35	CSI0A_L1P	AIO				AVDD12_CSI		
CSI0B_L0P	L32	CSI0B_L0P	AIO				AVDD12_CSI		
CSI0B_L0N	L33	CSI0B_L0N	AIO				AVDD12_CSI		
CSI0A_L1N	L34	CSI0A_L1N	AIO				AVDD12_CSI		
CSI0D_L0P	L36	CSI0D_L0P	AIO				AVDD12_CSI		
CSI0D_L0N	L37	CSI0D_L0N	AIO				AVDD12_CSI		
CSI0B_L1N	M32	CSI0B_L1N	AIO				AVDD12_CSI		
CSI0B_L1P	M33	CSI0B_L1P	AIO				AVDD12_CSI		
CSI0C_L0N	M35	CSI0C_L0N	AIO				AVDD12_CSI		
CSI0D_L1N	M36	CSI0D_L1N	AIO				AVDD12_CSI		
CSI0D_L1P	M37	CSI0D_L1P	AIO				AVDD12_CSI		
CSI0C_L2P	N31	CSI0C_L2P	AIO				AVDD12_CSI		
CSI0C_L2N	N32	CSI0C_L2N	AIO				AVDD12_CSI		
CSI0C_L1N	N33	CSI0C_L1N	AIO				AVDD12_CSI		
CSI0C_L1P	N34	CSI0C_L1P	AIO				AVDD12_CSI		
CSI0C_L0P	N35	CSI0C_L0P	AIO				AVDD12_CSI		
CSI1A_L0P_T0A	R32	CSI1A_L0P_T0A	AIO				AVDD12_CSI		
CSI1A_L0N_T0B	R33	CSI1A_L0N_T0B	AIO				AVDD12_CSI		
CSI1A_L1P_T0C	R34	CSI1A_L1P_T0C	AIO				AVDD12_CSI		
CSI1A_L1N_T1A	R35	CSI1A_L1N_T1A	AIO				AVDD12_CSI		
CSI1A_L2P_T1B	R36	CSI1A_L2P_T1B	AIO				AVDD12_CSI		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
CSI1A_L2N_T1C	R37	CSI1A_L2N_T1C	AIO				AVDD12_CSI		
CSI1B_L2N_T1C	T32	CSI1B_L2N_T1C	AIO				AVDD12_CSI		
CSI1B_L2P_T1B	T33	CSI1B_L2P_T1B	AIO				AVDD12_CSI		
CSI1B_L1N_T1A	T34	CSI1B_L1N_T1A	AIO				AVDD12_CSI		
CSI1B_L1P_T0C	T35	CSI1B_L1P_T0C	AIO				AVDD12_CSI		
CSI1B_L0P_T0A	T36	CSI1B_L0P_T0A	AIO				AVDD12_CSI		
CSI1B_L0N_T0B	T37	CSI1B_L0N_T0B	AIO				AVDD12_CSI		
SSUSB_TXN	AH32	SSUSB_TXN	AIO				AVDD12_SSUSB		
SSUSB_TXP	AH33	SSUSB_TXP	AIO				AVDD12_SSUSB		
SSUSB_RXP	AJ31	SSUSB_RXP	AIO				AVDD12_SSUSB		
SSUSB_RXN	AK31	SSUSB_RXN	AIO				AVDD12_SSUSB		
PCIE_LN0_RXP_P1	V33	PCIE_LN0_RXP_P1	AIO				AVDD12_PCIE_P1		
PCIE_LN0_RXN_P1	V34	PCIE_LN0_RXN_P1	AIO				AVDD12_PCIE_P1		
PCIE_CKRXP_P1	V36	PCIE_CKRXP_P1	AIO				AVDD12_PCIE_P1		
PCIE_CKRXN_P1	V37	PCIE_CKRXN_P1	AIO				AVDD12_PCIE_P1		
PCIE_LN0_TXP_P1	W31	PCIE_LN0_TXP_P1	AIO				AVDD12_PCIE_P1		
PCIE_LN0_TXN_P1	W32	PCIE_LN0_TXN_P1	AIO				AVDD12_PCIE_P1		
PCIEG3_LN0_RXP	Y35	PCIEG3_LN0_RXP	AIO				AVDD12_PCIEG3		
PCIEG3_LN0_RXN	W35	PCIEG3_LN0_RXN	AIO				AVDD12_PCIEG3		
PCIEG3_LN0_TXP	AA30	PCIEG3_LN0_TXP	AIO				AVDD12_PCIEG3		
PCIEG3_LN0_TXN	AA31	PCIEG3_LN0_TXN	AIO				AVDD12_PCIEG3		
PCIEG3_LN1_RXP	AC35	PCIEG3_LN1_RXP	AIO				AVDD12_PCIEG3		
PCIEG3_LN1_RXN	AB35	PCIEG3_LN1_RXN	AIO				AVDD12_PCIEG3		
PCIEG3_LN1_TXP	AA37	PCIEG3_LN1_TXP	AIO				AVDD12_PCIEG3		
PCIEG3_LN1_TXN	AA36	PCIEG3_LN1_TXN	AIO				AVDD12_PCIEG3		
PCIEG3_CLKP	AA34	PCIEG3_CLKP	AIO				AVDD12_PCIEG3		
PCIEG3_CLKN	AA33	PCIEG3_CLKN	AIO				AVDD12_PCIEG3		
DP_LN0_TXP	AG35	DP_LN0_TXP	AIO				AVDD12_DPTX		
DP_LN0_TXN	AH35	DP_LN0_TXN	AIO				AVDD12_DPTX		
DP_LN1_TXP	AJ36	DP_LN1_TXP	AIO				AVDD12_DPTX		
DP_LN1_TXN	AJ37	DP_LN1_TXN	AIO				AVDD12_DPTX		
DP_LN2_TXP	AJ34	DP_LN2_TXP	AIO				AVDD12_DPTX		
DP_LN2_TXN	AK34	DP_LN2_TXN	AIO				AVDD12_DPTX		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
DP_LN3_TXP	AL32	DP_LN3_TXP	AIO				AVDD12_DPTX		
DP_LN3_TXN	AL33	DP_LN3_TXN	AIO				AVDD12_DPTX		
DPAUXP	AG30	DPAUXP	AIO				AVDD12_DPTX		
DPAUXN	AG31	DPAUXN	AIO				AVDD12_DPTX		
EDP_LN0_TXN	AD33	EDP_LN0_TXN	AIO				AVDD12_EDPTX		
EDP_LN0_TXP	AD34	EDP_LN0_TXP	AIO				AVDD12_EDPTX		
EDP_LN1_TXP	AD36	EDP_LN1_TXP	AIO				AVDD12_EDPTX		
EDP_LN1_TXN	AD37	EDP_LN1_TXN	AIO				AVDD12_EDPTX		
EDP_LN2_TXP	AE35	EDP_LN2_TXP	AIO				AVDD12_EDPTX		
EDP_LN2_TXN	AF36	EDP_LN2_TXN	AIO				AVDD12_EDPTX		
EDP_LN3_TXN	AF33	EDP_LN3_TXN	AIO				AVDD12_EDPTX		
EDP_LN3_TXP	AF34	EDP_LN3_TXP	AIO				AVDD12_EDPTX		
EDPAUXN	AE31	EDPAUXN	AIO				AVDD12_EDPTX		
EDPAUXP	AE32	EDPAUXP	AIO				AVDD12_EDPTX		
USB_DP_P0	AM35	USB_DP_P0	AIO				AVDD33_USB_P0		
USB_DM_P0	AM36	USB_DM_P0	AIO				AVDD33_USB_P0		
USB_DP_P1	AC31	USB_DP_P1	AIO				AVDD33_USB_P1		
USB_DM_P1	AC32	USB_DM_P1	AIO				AVDD33_USB_P1		
USB_DP_P2	AD8	USB_DP_P2	AIO				AVDD33_USB_P2		
USB_DM_P2	AE8	USB_DM_P2	AIO				AVDD33_USB_P2		
USB_DP_P3	AH7	USB_DP_P3	AIO				AVDD33_USB_P3		
USB_DM_P3	AG7	USB_DM_P3	AIO				AVDD33_USB_P3		
UFS_PLL_CKREF	G29	UFS_PLL_CKREF	AIO				AVDD12_UFS		
UFS_REFCK_OUT	F28	UFS_REFCK_OUT	AIO				AVDD12_UFS		
UFS_TX0P	C30	UFS_TX0P	AIO				AVDD12_UFS		
UFS_TX0N	C31	UFS_TX0N	AIO				AVDD12_UFS		
UFS_RX0P	B33	UFS_RX0P	AIO				AVDD12_UFS		
UFS_RX0N	B32	UFS_RX0N	AIO				AVDD12_UFS		
UFS_RST_N	A34	UFS_RST_N	AIO				AVDD12_UFS		
AUXIN0	AP5	AUXIN0	AIO				AVDD18_AUXADC		
AUXIN1	AP6	AUXIN1	AIO				AVDD18_AUXADC		
AUXIN2	AN6	AUXIN2	AIO				AVDD18_AUXADC		
AUXIN3	AM6	AUXIN3	AIO				AVDD18_AUXADC		

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
AUXIN4	AL6	AUXIN4	AIO				AVDD18_AUXADC		
AUXIN5	AK6	AUXIN5	AIO				AVDD18_AUXADC		
REFP	AM7	REFP	AIO				AVDD18_AUXADC		
HDMITX21_CH0_M	AR32	HDMITX21_CH0_M	DIO				AVDD18_HDMITX21		
HDMITX21_CH0_P	AR33	HDMITX21_CH0_P	DIO				AVDD18_HDMITX21		
HDMITX21_CH1_M	AT34	HDMITX21_CH1_M	DIO				AVDD18_HDMITX21		
HDMITX21_CH1_P	AU34	HDMITX21_CH1_P	DIO				AVDD18_HDMITX21		
HDMITX21_CH2_M	AR35	HDMITX21_CH2_M	DIO				AVDD18_HDMITX21		
HDMITX21_CH2_P	AR36	HDMITX21_CH2_P	DIO				AVDD18_HDMITX21		
HDMITX21_CLK_M	AT31	HDMITX21_CLK_M	DIO				AVDD18_HDMITX21		
HDMITX21_CLK_P	AU31	HDMITX21_CLK_P	DIO				AVDD18_HDMITX21		
HDMIRX21_CH0_M	AR26	HDMIRX21_CH0_M	AIO				AVDD33_HDMIRX21		
HDMIRX21_CH0_P	AR27	HDMIRX21_CH0_P	AIO				AVDD33_HDMIRX21		
HDMIRX21_CH1_M	AU28	HDMIRX21_CH1_M	AIO				AVDD33_HDMIRX21		
HDMIRX21_CH1_P	AT28	HDMIRX21_CH1_P	AIO				AVDD33_HDMIRX21		
HDMIRX21_CH2_M	AR29	HDMIRX21_CH2_M	AIO				AVDD33_HDMIRX21		
HDMIRX21_CH2_P	AR30	HDMIRX21_CH2_P	AIO				AVDD33_HDMIRX21		
HDMIRX21_CLK_M	AU25	HDMIRX21_CLK_M	AIO				AVDD33_HDMIRX21		
HDMIRX21_CLK_P	AT25	HDMIRX21_CLK_P	AIO				AVDD33_HDMIRX21		

4.3 Power Rails

Table 4-11 lists the device power rails.

Table 4-11 Power Rails

Signal Name	Ball Location	Type	Description
AVDD08_HDMIRX21	AR24	P	Analog power input 0.8 V for HDMI RX
AVDD12_APPLLGP_APU	AC20	P	Analog power for APPLL APU
AVDD12_APPLLGP1	P22	P	Analog power for APPLL
AVDD12_APPLLGP2	V11	P	Analog power for APPLL
AVDD12_APPLLGP3	AF23	P	Analog power for APPLL
AVDD12_APPLLGP4	AC14	P	Analog power for APPLL
AVDD12_AUXADC	AT5	P	Analog power for AUXADC
AVDD12_CKBUF_UFS	H25	P	Analog power for UFS
AVDD12_CKSQ	U31	P	Analog power for CKSQ
AVDD12_CSI	P30	P	Analog power for CSI
AVDD12_DPTX	AD28	P	Analog power for DPTX
AVDD12_DSI	AK1	P	Analog power for DSI
AVDD12_EDPTX	AH29	P	Analog power for EDPTX
AVDD12_HDMITX21	AJ29	P	Analog power input for HDMITX
AVDD12_PCIE_P1	Y29	P	Analog power for PCIe
AVDD12_PCIEG3	AC29	P	Analog power for PCIe Port 0
AVDD12_SSUSB	AN36	P	Analog power for SSUSB
AVDD12_UFS	H24	P	Analog power for UFS
AVDD12_USB_P0	AP37	P	Analog power input USB Port 0
AVDD12_USB_P1	AH30	P	Analog power input USB Port 1
AVDD12_USB_P2	AD6	P	Analog power input USB Port 2
AVDD12_USB_P3	AE6	P	Analog power input USB Port 3
AVDD12_EMI	L8	P	Analog power input EMI
AVDD18_APPLLGP_APU	AC19	P	Analog power input 1.8 V for APPLL
AVDD18_APPLLGP1	R21	P	Analog power input 1.8 V for APPLL
AVDD18_APPLLGP2	W12	P	Analog power input 1.8 V for APPLL
AVDD18_APPLLGP3	AG23	P	Analog power input 1.8 V for APPLL
AVDD18_APPLLGP4	AD14	P	Analog power input 1.8 V for APPLL
AVDD18_AUXADC	AR5	P	Analog power 1.8 V for AUXADC
AVDD18_CKSQ	U30	P	Analog power input 1.8 V for CKSQ
AVDD18_CSI	N30	P	Analog power 1.8 V for CSI
AVDD18_DPTX	AF29	P	Analog power input 1.8 V for DPTX
AVDD18_EDPTX	AF37	P	Analog power input 1.8 V for EDPTX
AVDD18_HDMITX21	AL31	P	Analog power input 1.8 V for HDMITX
AVDD18_HDMIRX21	AK24	P	Analog power input 1.8 V for HDMIRX
AVDD18_PCIE_P1	Y30	P	Analog power 1.8 V for PCIe Port 1
AVDD18_PCIEG3	AB30	P	Analog power 1.8 V for PCIe Port 0
AVDD18_PROC	P28	P	Analog power 1.8 V for A78/A55
AVDD18_SSUSB	AN35	P	Analog power 1.8 V for SSUSB
AVDD18_UFS	H26	P	Analog power 1.8 V for UFS
AVDD18_USB_P0	AN34	P	Analog power 1.8 V for USB Port 0
AVDD18_USB_P1	AD29	P	Analog power 1.8 V for USB Port 1
AVDD18_USB_P2	Y8	P	Analog power 1.8 V for USB Port 2

Signal Name	Ball Location	Type	Description
AVDD18_USB_P3	AA8	P	Analog power 1.8 V for USB Port 3
AVDD18_EMI	J8	P	Analog power input EMI
AVDD33_HDMIRX21	AJ26	P	Analog power input 3.3 V for HDMI RX
AVDD33_USB_P0	AM34	P	Analog power 3.3 V for USB Port 0
AVDD33_USB_P1	AD30	P	Analog power 3.3 V for USB Port 1
AVDD33_USB_P2	AB7	P	Analog power 3.3 V for USB Port 2
AVDD33_USB_P3	AC7	P	Analog power 3.3 V for USB Port 3
AVDD075_EMI0	J10	P	Analog power 0.75 V for EMI
AVDD075_EMI2	L9	P	Analog power 0.75 V for EMI
AVDDQ_EMI0	K11	P	V_{DDQ} power
AVDDQ_EMI2	M10	P	V_{DDQ} power
DVDD_APU	AD21	P	Digital power input for APU
DVDD_CORE	J21, K21, L14, L17, L18, L21, L22, L23, L30, M12, M13, M14, M17, M20, M21, M23, N17, N18, P13, P14, P17, P18, P23, R13, R14, R17, R18, R22, R23, T13, T14, T21, T22, U13, U14, U17, U18, U21, U22, V13, V14, V17, V18, V21, V22, W13, W14, W17, W18, W21, W22, Y14, Y17, Y18, Y21, Y22, AA18, AA21, AA25, AA26, AB21, AB22, AB25, AB26, AC25, AC26, AD25, AD26, AE26, AE27, AF25, AF26, AG25, AG26, AJ21, AJ23	P	Digital power input for DSP, GPU, and other SoC resources
DVDD_DLA	AB17	P	Digital power input for DLA
DVDD_GPU	Y10, Y13, AA10, AA13, AA14, AB10, AB13, AB14, AC10, AC13, AD10, AD13, AE10, AE13, AE14, AF10, AF13, AF14, AG10, AG13, AG14, AH10, AH13, AH14	P	Digital power input for GPU
DVDD_PROC_B	K25, K26, K27, L25, L26, L27, L28, M25, M26, N25, N26, U25, U26, V25, V26, V27, W24, W25, W26, W27, Y25, Y26, Y27	P	Digital power input for A78 core
DVDD_PROC_L	P25	P	Digital power input for A55 core
DVDD_SRAM_APU	AE18	P	Digital power input for APU SRAM
DVDD_SRAM_CORE	M18	P	Digital power input for Core SRAM
DVDD_SRAM_GPU	AC12	P	Digital power input for GPU SRAM
DVDD_SRAM_PROC_B	N29	P	Digital power input for A78 core SRAM
DVDD_SRAM_PROC_L	R28	P	Digital power input for A55 core SRAM
DVDD18_IOBM	AJ22	P	Digital power input for 1.8 V I/O
DVDD18_IOBR	AJ7	P	Digital power input for 1.8 V I/O
DVDD18_IOEMMC	C37	P	Digital power input for MSDC0
DVDD18_IOT	F33	P	Digital power input for 1.8 V I/O

Signal Name	Ball Location	Type	Description
DVDD18_MSDC1	AU5	P	Digital power input for MSDC1
DVDD18_MSDC2	K31	P	Digital power input for MSDC2
DVDD18_VQPS	AB15	P	eFUSE blowing power supply
DVDD28_IODGI	AM12	P	Digital power input for I/O
DVDD28_MSDC1	AU6	P	Digital power input for MSDC1
DVDD28_MSDC2	H36	P	Digital power input for MSDC2
DVSS	A17, A32, B4, B5, B7, B9, B11, B13, B22, B24, B26, B28, B30, B34, C2, C4, C8, C10, C21, C23, C25, C29, C32, C33, C34, D4, D6, D7, D11, D12, D13, D15, D18, D26, D27, D30, D31, E2, E5, E6, E10, E21, E24, E28, E29, E31, F4, F9, F16, F18, F30, G2, G4, G15, G22, G23, G24, G25, G26, H3, H29, H30, H35, H37, J2, J4, J5, J19, J20, J28, J32, J33, K3, K20, K22, K24, K28, K29, K30, K32, L2, L5, L16, L19, L20, L24, L29, L31, L35, M4, M11, M15, M16, M19, M24, M27, M28, M29, M31, M34, N2, N7, N11, N12, N15, N16, N19, N24, N27, N28, P11, P12, P16, P20, P24, P27, P29, P31, P32, P33, P34, P35, R11, R12, R15, R19, R24, R31, T2, T6, T11, T15, T16, T20, T23, T27, T28, T31, U7, U11, U12, U15, U16, U19, U20, U24, U27, U28, U29, U32, U33, U34, U35, V6, V7, V12, V15, V16, V19, V20, V23, V24, V28, V30, V31, V32, V35, W2, W4, W5, W6, W11, W15, W16, W19, W20, W23, W28, W30, W33, W34, Y4, Y6, Y7, Y11, Y12, Y15, Y16, Y19, Y20, Y23, Y24, Y28, Y31, Y32, Y33, Y34, AA2, AA4, AA6, AA7, AA11, AA12, AA15, AA16, AA19, AA20, AA23, AA24, AA27, AA28, AA29, AA32, AA35, AB3, AB5, AB6, AB11, AB12, AB16, AB23, AB24, AB27, AB31, AB32, AB33, AB34, AC2, AC9, AC11, AC15, AC16, AC24, AC28, AC30, AC34, AC36, AD3, AD5, AD12,	G	Digital ground

Signal Name	Ball Location	Type	Description
	AD15, AD16, AD19, AD20, AD23, AD27, AD31, AD32, AD35, AE2, AE4, AE11, AE12, AE16, AE19, AE20, AE23, AE24, AE33, AE34, AF4, AF6, AF7, AF11, AF12, AF15, AF16, AF19, AF20, AF24, AF27, AF31, AF32, AF35, AG2, AG5, AG6, AG9, AG11, AG12, AG15, AG16, AG19, AG20, AG28, AG33, AG34, AH3, AH4, AH5, AH6, AH9, AH11, AH12, AH15, AH16, AH19, AH20, AH23, AH25, AH26, AH28, AH31, AH34, AJ2, AJ5, AJ6, AJ30, AJ32, AJ33, AJ35, AK2, AK26, AK30, AK32, AK33, AL5, AL34, AL35, AM1, AM5, AM27, AN3, AN7, AN32, AN33, AN37, AP3, AP4, AP7, AP26, AP27, AP28, AP29, AP30, AP32, AP33, AP35, AP36, AR6, AR7, AR25, AR28, AR31, AR34, AR37, AT2, AT3, AT36, AU36		

4.4 Reserved and Unused Pin Handling Recommendations

Table 4-12 provides specific ball handling recommendations for the case when the pins are not used.

Table 4-12 Reserved and Unused Pin Handling Recommendations

Ball Name	Requirement	Ball Location
TESTMODE	Normal mode (tie to GND)	AK22
DUMMY, NC_PAD_BRDQ7_B1, NC-PAD_ARCKE0, NC-PAD_ARCKE1, NC-PAD_ARCS1, NC-PAD_ARDQ6_B1, NC-PAD_ARDQ7_B1, NC-PAD_BRCKE0, NC-PAD_BRCKE1, NC-PAD_BRCS1, NC-PAD_BRDQ6_B1, AUD_CLK_MOSI, AUD_SYNC_MOSI, AUD_DAT_MOSI0, AUD_DAT_MOSI1	Leave unconnected	A1, A2, A36, A37, B1, B37, AT1, AT37, AU1, AU2, AU37, F13, E22, F23, F21, E20, D20, F11, E11, F12, E14, AL16, AT16, AN15, AK16
AUXIN0, AUXIN1, AUXIN2, AUXIN3, AUXIN4, AUXIN5	These pins should be connected to GND when unused	AP5, AP6, AN6, AM6, AL6, AK6
TN_APPLLGP, TP_APPLLGP	Reserved, leave unconnected	N20, P19

NOTE: All other unused signal balls can be left floating.

5 Electrical Characteristics

Stresses above the values listed in Table 5.1 may cause permanent damage to the device. The recommended minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies based on characterization results. Exposure to absolute maximum rating conditions may affect device reliability.
The operating conditions in Table 5.2 must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in this document refer to these operating conditions, unless noted otherwise.

5.1 Absolute Maximum Ratings

Table 5-1 represents the absolute maximum ratings of the device power pins.

Table 5-1 Absolute Maximum Ratings

Parameter	Conditions	Max	Unit
Digital power input for A78 core	DVDD_PROC_B, DVDD_SRAM_PROC_B	1.08	V
Digital power input for A55 core	DVDD_PROC_L, DVDD_SRAM_PROC_L	1.08	V
Digital power input for core	DVDD_CORE	0.825	V
Digital power input for GPU	DVDD_GPU	0.8	V
Analog power input	AVDD12_APPLLGP1, AVDD12_APPLLGP2, AVDD12_APPLLGP3, AVDD12_APPLLGP4, AVDD12_APPLLGP_APU, AVDD12_USB_P0, AVDD12_USB_P1, AVDD12_USB_P2, AVDD12_USB_P3, AVDD12_SSUSB, AVDD12_UFS, AVDD12_CKBUF_UFS, AVDD12_DPTX, AVDD12_EDPTX, AVDD12_HDMITX21, AVDD12_AUXADC, AVDD12_DSI, AVDD12_CSI, AVDD12_PCIE_P1, AVDD12_PCIEG3, AVDD12_CKSQ	1.26	V
	AVDD18_APPLLGP1, AVDD18_APPLLGP2, AVDD18_APPLLGP3, AVDD18_APPLLGP4, AVDD18_APPLLGP_APU, AVDD18_USB_P0, AVDD18_USB_P1, AVDD18_USB_P2, AVDD18_USB_P3, AVDD18_SSUSB, AVDD18_UFS, AVDD18_DPTX, AVDD18_EDPTX, AVDD18_HDMITX21, AVDD18_HDMIRX21, AVDD18_AUXADC, AVDD18_CSI, AVDD18_PCIE_P1, AVDD18_PCIEG3, AVDD18_CKSQ, AVDD18_PROC, AVDD18_EMI	1.89	V
	AVDD33_USB_P0, AVDD33_USB_P1, AVDD33_USB_P2, AVDD33_USB_P3	3.22	V
	AVDD33_HDMIRX21	3.465	V
	AVDDQ_EMI0, AVDDQ_EMI2	0.65	V
	AVDD075_EMI0, AVDD075_EMI2	0.825	V
	AVDD12_EMI	1.26	V
Digital power input	DVDD_SRAM_GPU	0.787	V
	DVDD_SRAM_APU	0.88	V
	DVDD_APU	0.84	V
	DVDD18_IOEMMC, DVDD18_MSDC1, DVDD18_MSDC2	1.89	V
	DVDD28_IODGI, DVDD28_MSDC1, DVDD28_MSDC2	3.15	V
	DVDD18_IOT, DVDD18_IOBM, DVDD18_IOBR	1.89	V
	DVDD_DLA	0.825	V
	DVDD_SRAM_CORE	0.75	V
ESD ratings	Human Body Model (HBM), per JESD22-A114-F — All pins	±2000	V

Parameter		Conditions	Max	Unit
	Charged Device Model (CDM), per JESD22-C101-D	RF/HSS pins	±250	V
		All other pins	±500	V

5.1.1 Storage Conditions

Table 5-2 defines storage conditions specifics.

Table 5-2 Storage Conditions

Parameter		Min	Max	Unit
Shelf life in sealed bag	40 °C / 90% RH		12	months
After bag opened(1)				
Mounted	30 °C / 60% RH		168	h
Stored			20	% RH
Baking				
Low temperature device containers	40 °C +5 °C/-0 °C and < 5% RH	192		h
High temperature device containers	125 °C +5 °C/-0 °C	24		h

1. For devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing.

5.2 Recommended Operating Conditions

Table 5-3 presents the recommended operating conditions of the device power pins.

Table 5-3 Recommended Operating Conditions

Pin Name	Description	Min	Typ	Max	Unit
AVDD12_APPLLGP1	Analog power for APPLLGP1	1.14	1.2	1.26	V
AVDD12_APPLLGP2	Analog power for APPLLGP2	1.14	1.2	1.26	V
AVDD12_APPLLGP3	Analog power for APPLLGP3	1.14	1.2	1.26	V
AVDD12_APPLLGP4	Analog power for APPLLGP4	1.14	1.2	1.26	V
AVDD12_APPLLGP_APU	Analog power for APPLLGP_APU	1.14	1.2	1.26	V
AVDD12_USB_P0	Analog power for USB Port 0	1.14	1.2	1.26	V
AVDD12_USB_P1	Analog power for USB Port 1	1.14	1.2	1.26	V
AVDD12_USB_P2	Analog power for USB Port 2	1.14	1.2	1.26	V
AVDD12_USB_P3	Analog power for USB Port 3	1.14	1.2	1.26	V
AVDD12_SSUSB	Analog power for SSUSB	1.14	1.2	1.26	V
AVDD12_UFS	Analog power for UFS	1.14	1.2	1.26	V
AVDD12_CKBUF_UFS	Analog power for UFS	1.14	1.2	1.26	V
AVDD12_DPTX	Analog power for DPTX	1.14	1.2	1.26	V
AVDD12_EDPTX	Analog power for EDPTX	1.14	1.2	1.26	V
AVDD12_HDMITX21	Analog power for HDMITX	1.14	1.2	1.26	V
AVDD12_AUXADC	Analog power for AUXADC	1.14	1.2	1.26	V
AVDD12_DSI	Analog power for DSI	1.14	1.2	1.26	V
AVDD12_CSI	Analog power for CSI	1.14	1.2	1.26	V
AVDD12_PCIE_P1	Analog power for PCIe Port 1	1.14	1.2	1.26	V
AVDD12_PCIEG3	Analog power for PCIe Port 0	1.14	1.2	1.26	V
AVDD12_CKSQ	Analog power for CKSQ	1.14	1.2	1.26	V
AVDD18_APPLLGP1	Analog power for APPLLGP1	1.71	1.8	1.89	V
AVDD18_APPLLGP2	Analog power for APPLLGP2	1.71	1.8	1.89	V

Pin Name	Description	Min	Typ	Max	Unit
AVDD18_APPLLGP3	Analog power for APPLLGP3	1.71	1.8	1.89	V
AVDD18_APPLLGP4	Analog power for APPLLGP4	1.71	1.8	1.89	V
AVDD18_APPLLGP_APU	Analog power for APPLLGP_APU	1.71	1.8	1.89	V
AVDD18_USB_P0	Analog power for USB Port 0	1.71	1.8	1.89	V
AVDD18_USB_P1	Analog power for USB Port 1	1.71	1.8	1.89	V
AVDD18_USB_P2	Analog power for USB Port 2	1.71	1.8	1.89	V
AVDD18_USB_P3	Analog power for USB Port 3	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power for SSUSB	1.71	1.8	1.89	V
AVDD18_UFS	Analog power for UFS	1.71	1.8	1.89	V
AVDD18_DPTX	Analog power for DPTX	1.71	1.8	1.89	V
AVDD18_EDPTX	Analog power for EDPTX	1.71	1.8	1.89	V
AVDD18_HDMITX21	Analog power for HDMITX	1.71	1.8	1.89	V
AVDD18_HDMIRX21	Analog power for HDMIRX	1.71	1.8	1.89	V
AVDD18_AUXADC	Analog power for AUXADC	1.71	1.8	1.89	V
AVDD18_CSI	Analog power for CSI	1.71	1.8	1.89	V
AVDD18_PCIE_P1	Analog power for PCIe Port 1	1.71	1.8	1.89	V
AVDD18_PCIEG3	Analog power for PCIe Port 0	1.71	1.8	1.89	V
AVDD18_CKSQ	Analog power for CKSQ	1.71	1.8	1.89	V
AVDD18_PROC	Analog power for A78/A55	1.71	1.8	1.89	V
AVDD33_USB_P0	Analog power for USB Port 0	2.92	3.07	3.22	V
AVDD33_USB_P1	Analog power for USB Port 1	2.92	3.07	3.22	V
AVDD33_USB_P2	Analog power for USB Port 2	2.92	3.07	3.22	V
AVDD33_USB_P3	Analog power for USB Port 3	2.92	3.07	3.22	V
AVDD33_HDMIRX21	Analog power for HDMIRX	3.135	3.3	3.465	V
AVDDQ_EMI0	Analog power for EMI0	0.57	0.6	0.65	V
AVDDQ_EMI2	Analog power for EMI2	0.57	0.6	0.65	V
AVDD075_EMI0	Analog power for EMI0	0.675	0.75	0.825	V
AVDD075_EMI2	Analog power for EMI2	0.675	0.75	0.825	V
AVDD12_EMI	Analog power for LPDDR4X	1.14	1.2	1.26	V
AVDD18_EMI	Analog power for LPDDR4X	1.62	1.8	1.98	V
DVDD18_IOT	Digital power input for 1.8 V I/O	1.71	1.8	1.89	V
DVDD18_IOBM					
DVDD18_IOBR					
DVDD18_IOEMMC	Digital power input for I/O	1.71	1.8	1.89	V
DVDD18_MSDC1	Digital power input for I/O	1.71	1.8	1.89	V
DVDD28_MSDC1	Digital power input for MSDC1	2.7	3	3.15	V
DVDD18_MSDC2	Digital power input for I/O	1.71	1.8	1.89	V
DVDD28_MSDC2	Digital power input for MSDC2	2.7	3	3.15	V
DVDD28_IODGI	Digital power input for I/O	2.7	3	3.15	V
DVDD_CORE	Digital power input for core	0.712	0.75	0.787	V
DVDD_GPU	Digital power input for GPU	0.712	0.75	0.787	V
DVDD_PROC_B	Digital power input for A78 core	0.9375	1	1.08	V
DVDD_PROC_L	Digital power input for A55 core	0.9375	1	1.08	V
DVDD_APU	Digital power input for APU	0.76	0.8	0.84	V
DVDD_DLA	Digital power input for DLA	0.783	0.825	0.866	V
DVDD_SRAM_CORE	Digital power input for core SRAM	0.712	0.75	0.787	V
DVDD_SRAM_APU	Digital power input for APU SRAM	0.72	0.8	0.88	V

Pin Name	Description	Min	Typ	Max	Unit
DVDD_SRAM_GPU	Digital power input for GPU SRAM	0.712	0.75	0.787	V
DVDD_SRAM_PROC_B	Digital power input for A78 core SRAM	0.9375	1	1.08	V
DVDD_SRAM_PROC_L	Digital power input for A55 core SRAM	0.9375	1	1.08	V

5.3 DC Electrical Specifications

This section provides DC electrical characteristics per buffer type.

5.3.1 RTCIO DC Specifications

Table 5-4 shows RTC DC buffer (RTCIO) electrical characteristics.

Table 5-4 RTCIO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
F_{RTC}	Input clock frequency		32		kHz
DC_{RTC}	Input signal duty cycle	45	50	55	%
OUTPUT					
V_{OH}	DC output logic high voltage	0.75 × VDDIO(1)			V
V_{OL}	DC output logic low voltage			0.25 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e DVDD18_IOBM). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.2 SPII2SIO DC Specifications

Table 5-5 shows SPI, I2S DC buffer (SPII2SIO) electrical characteristics.

Table 5-5 SPII2SIO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	0.75 × VDDIO(1)			V
V_{OL}	DC Output logic low voltage			0.25 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOBM). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.3 I2CI3CIO DC Specifications

Table 5-6 shows I2C/I3C DC buffer (I2CI3CIO) electrical characteristics.

Table 5-6 I2CI3CIO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V

Parameters		Min	Typ	Max	Unit
OUTPUT					
V_{OL}	DC output logic low voltage			0.2 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOT). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.4 I2C3IO DC Specifications

Table 5-7 shows I2C3 DC buffer (I2C3IO) specifications.

Table 5-7 I2C3IO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OL}	DC output logic low voltage			0.2 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOT). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.5 MSDC0IO DC Specifications

Table 5-8 shows MSDC0 DC buffer (MSDC0IO) specifications.

Table 5-8 MSDC0IO DC Specifications

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	1.4			V
V_{OL}	DC output logic low voltage			0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IOEMMC). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.6 MSDC1IO DC Specifications

Table 5-9 shows MSDC1 DC buffer (MSDC1IO) specifications.

Table 5-9 MSDC1IO DC Specifications (2.8 V / 3.3 V)

Parameters		Min	Typ	Max	Unit
Operating voltage = 2.8 V / 3.3 V					
INPUT					
V_{IH}	Input logic high voltage	0.75 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{IL}	Input logic low voltage	-0.3		0.25 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	0.625 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{OL}	DC output logic low voltage	-0.3		0.125 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD28_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

Table 5-10 MSDC1IO DC Specifications (1.8 V)

Parameters		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.7 × VDDIO(1)		VDDIO(1) + 0.15	V
V_{IL}	Input logic low voltage	-0.3		0.3 × VDDIO(1)	V
OUTPUT					
V_{OH}	DC output logic high voltage	1.4		VDDIO(1) + 0.15	V
V_{OL}	DC output logic low voltage	-0.3		0.45	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, *Power Domain* column.

5.3.7 DDRIO DC Specifications

The EMI LPDDR4X electrical characteristics are compliant with JEDEC Standard—JESD209-4B.

5.4 Power Management

5.4.1 Power Sequences

Refer to the respective PMIC (MT6365/MT6360/MT6315) datasheet for detailed timing sequence.

5.5 Reset

The TOPRGU generates reset signals and distributes them to each system. A WDT is also included in this module.

The TOPRGU supports the following features:

- Hardware reset signals for the whole chip
- Software controllable reset
- WDT
- Reset output signals for companion chips

Figure 5-1 shows the block diagram of TOPRGU in MT8395.

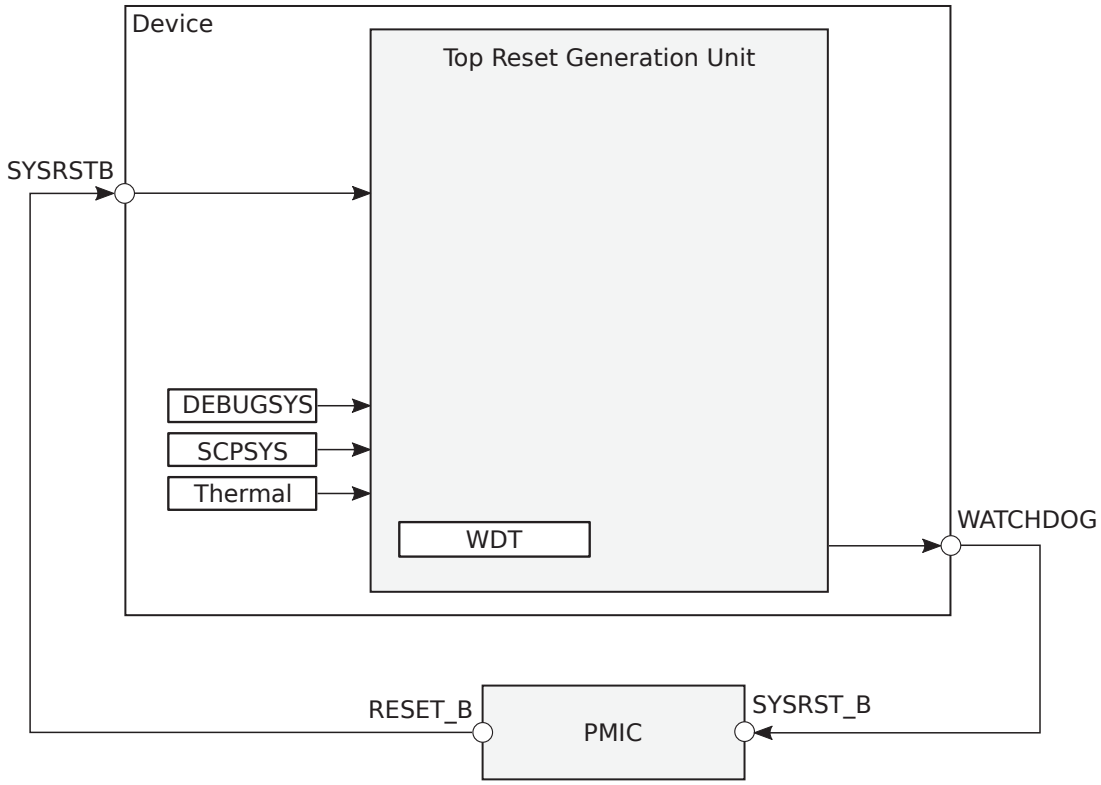


Figure 5-1 Reset Block Diagram

5.5.1 Reset Signal Descriptions

Table 5-11 presents Reset signal description.

Table 5-11 Reset Signal Descriptions

Signal Name	Type	Description	Ball Location
SYSRSTB	DI	System reset input	AL22
WATCHDOG	DO	Watchdog reset output	AM22

5.6 DSI Specifications

Table 5-12 presents MIPI D-PHY TX electrical characteristics.

Table 5-12 DSI D-PHY TX Electrical Characteristics

Description	Min	Typ	Max	Unit
High-Speed date rate	125		1500	Mbps
High-Speed common mode voltage	150	200	250	mV
High-Speed differential output voltage	140	200	270	mV
High-Speed single ended output high voltage			360	mV
High-Speed single ended output impedance	40	50	62.5	Ω
High-Speed 20%-80% rise time and fall time			0.3(1)	UI
			0.35(2)	UI
	100(3)			ps
Low-Power output high level	0.95	1.2	1.3	V
Low-Power output low level	-50		50	mV
Low-Power output impedance	110			Ω
Low-Power 15%-85% rise time and fall time			25	ns

1. Applicable when supporting maximum HS bit rates ≤ 1 Gbps (UI ≥ 1 ns)
2. Applicable when supporting maximum HS bit rates > 1 Gbps (UI ≤ 1 ns) but ≤ 1.5 Gbps
3. Applicable when supporting maximum HS bit rates > 1.5 Gbps

Table 5-13 presents MIPI C-PHY TX electrical characteristics.

Table 5-13 DSI C-PHY TX Electrical Characteristics

Description	Min	Typ	Max	Unit
High-Speed date rate	125		1100	Msps
High-Speed common mode voltage	175	225 - 250	310	mV
High-Speed differential output voltage of strong one			300	mV
High-Speed differential output voltage of weak one	97			mV
High-Speed single ended output high voltage			425	mV
High-Speed single ended output impedance	40	50	60	Ω
High-Speed rise time and fall time from -58 mV to 58 mV			0.4	UI
Low-Power output high level	0.95	1.2	1.3	V
Low-Power output low level	-50		50	mV
Low-Power output impedance	110			Ω
Low-Power 15%-85% rise time and fall time			25	ns

5.7 CSI-2 Specifications

Table 5-14 presents MIPI D-PHY RX electrical characteristics.

Table 5-14 CSI D-PHY RX Electrical Characteristics

Description	Min	Typ	Max	Unit
High-Speed date rate	80		2500	Mbps
High-Speed common point voltage	70		330	mV
High-Speed differential input high voltage			40	mV
High-Speed differential input low voltage	-40			mV
High-Speed single ended input high voltage			460	mV
High-Speed single ended input low voltage	-40			mV
High-Speed single ended input impedance	80	100	125	Ω
Low-Power logic 1 input voltage	740			mV
Low-Power logic 0 input voltage			550	mV
Low-Power input hysteresis	25			mV
Minimum pulse width response	20			ns

6 Clock Characteristics

The device has two external input clocks—low frequency (RTC32K_CK) and high frequency (X26M_IN).

Figure 6-1 shows the external clock sources and clock outputs.

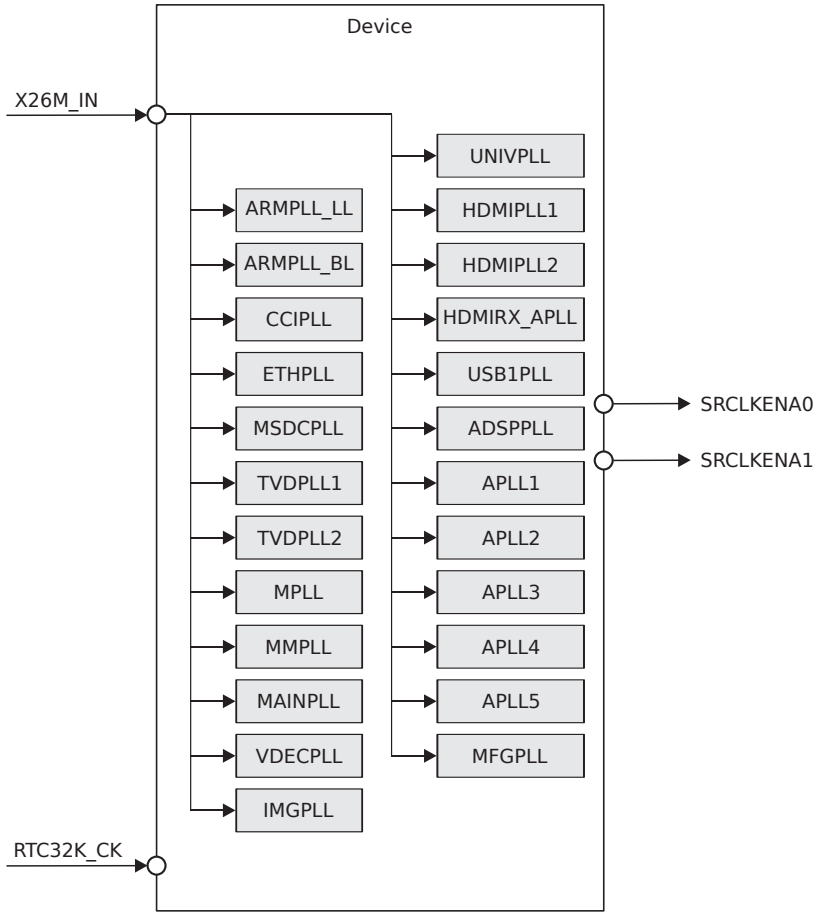


Figure 6-1 Device Clock Diagram

6.1 Maximum Performance Ratings

Table 6-1 presents the maximum core and peripheral performance limitations and correlations.

Table 6-1 Maximum Performance Ratings

Module		Max	Unit
Quad-core Arm Cortex-A78	A78	2200	MHz
Quad-core Arm Cortex-A55	A55	2000	MHz
Graphics Accelerator	GPU	880	MHz
HiFi 4 DSP	DSP	720	MHz
AI Processor Unit	APU	832	MHz
System Companion Processor	SCP	416	MHz
External Memory Interface	LPDDR4X	4266	MHz

Module		Max	Unit
Memory Card Controller	SD Card	100	MBps
	eMMC	400	MBps
	SDIO	100	MBps
SPI NAND Flash Interface	SNFI (output)	104	MHz
Serial NOR Flash Interface	SNOR	25	MHz
Universal Flash Storage	UFS	5.8	Gbps
Digital Display Parallel Interface	DPI	148.5	MHz
High-Definition Multimedia Interface Transmitter	HDMITX	594	MHz
DisplayPort	DPTX	8.1	Gbps/lane
Embedded DispalyPort	EDPTX	5.4	Gbps/lane
Display Serial Interface	DSI D-PHY	1.5	Gbps/lane
	DSI C-PHY	1.1	Gsps/trio
Image Signal Processor	ISP	48	MPix@30fps
Camera Serial Interface 2	CSI D-PHY	2.5	Gbps/lane
	CSI C-PHY	4.5	Gsps/trio
High-Definition Multimedia Interface Receiver	HDMIRX	594	MHz
Video Encoder	VENC	624	MHz
Video Decoder	VDEC	312	MHz
Inter-IC Sound	I2S master mode (sampling frequency)	384	kHz
	I2S slave mode (sampling frequency)	48	kHz
Programmable Command Master Interface	PCM (sampling frequency)	48	kHz
Pulse Density Modulation	PDM	3.25	MHz
Time Division Multiplexed Interface	TDM (sampling frequency)	192	kHz
Digital Interface	SPDIF	192	kHz
Inter-Integrated Circuit	I2C mode	3.4	Mbps
	I3C mode	12.5	Mbps
Universal Asynchronous Receiver/Transmitter	UART	961,200	bps
Serial Peripheral Interface	SPI (master)	52	MHz
Universal Serial Bus	USB SuperSpeed	5	Gbps
	USB High-Speed	480	Mbps
	USB Full-Speed	12	Mbps
	USB Low-Speed	1.5	Mbps
Ethernet Network Interface Controller	MII	25	MHz
	RMII	50	MHz
	RGMII	125	MHz
Peripheral Component Interconnect Express	PCIe	8.0	GT/s
Pulse Width Modulation	PWM	39	MHz
Auxiliary ADC	AUXADC (clock rate)	3.25	MHz

6.2 PLL Specifications

Table 6-2 shows ARMPLL_LL specifications.

Table 6-2 ARMPLL_LL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz

Parameter		Min	Typ	Max	Unit
F_{OUT}	Output clock frequency		2000		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-3 shows ARMPLL_BL specifications.

Table 6-3 ARMPLL_BL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2252.25		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-4 shows CCIPLL specifications.

Table 6-4 CCIPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		1800		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-5 shows ETHPLL specifications.

Table 6-5 ETHPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		500		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-6 shows MSDCPLL specifications.

Table 6-6 MSDCPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		416.146		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-7 shows TVDPLL1 specifications.

Table 6-7 TVDPLL1 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		594.177		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-8 shows TVDPLL2 specifications.

Table 6-8 TVDPLL2 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		594.177		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-9 shows MPLL specifications.

Table 6-9 MPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		208.03		MHz
t_{SET}	Settling time		20		µs

Parameter		Min	Typ	Max	Unit
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-10 shows MMPLL specifications.

Table 6-10 MMPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2750.048		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-11 shows MAINPLL specifications.

Table 6-11 MAINPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2184.359		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-12 shows VDECPLL specifications.

Table 6-12 VDECPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		680.04		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-13 shows IMGPLL specifications.

Table 6-13 IMGPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		650.026		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-14 shows UNIVPLL specifications.

Table 6-14 UNIVPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		2496.004		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-15 shows HDMIPLL1 specifications.

Table 6-15 HDMIPLL1 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		884.016		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-16 shows HDMIPLL2 specifications.

Table 6-16 HDMIPLL2 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		600.024		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps

Parameter		Min	Typ	Max	Unit
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-17 shows HDMIRX_APLL specifications.

Table 6-17 HDMIRX_APLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		294.915		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-18 shows USB1PLL specifications.

Table 6-18 USB1PLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		192.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-19 shows ADSPPLL specifications.

Table 6-19 ADSPPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		720		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-20 shows APLL1 specifications.

Table 6-20 APLL1 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-21 shows APLL2 specifications.

Table 6-21 APLL2 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		180.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-22 shows APLL3 specifications.

Table 6-22 APLL3 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-23 shows APLL4 specifications.

Table 6-23 APLL4 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps

Parameter		Min	Typ	Max	Unit
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-24 shows APLL5 specifications.

Table 6-24 APLL5 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.001		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-25 shows MFGPLL specifications.

Table 6-25 MFGPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		240		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.71	1.8	1.89	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

6.3 Clock Squarer

The Clock Squarer (CKSQ) is designed to receive clock signal from the X26M_IN input and distribute it to the chip internally.

Table 6-26 shows the CKSQ specifications.

Table 6-26 CKSQ Specifications

Parameter		Min	Typ	Max	Unit
V_{IN}	Input signal amplitude	1000	1200	1250	mVpp
D_{cycIN}	Input signal duty cycle		50		%
D_{cycOUT}	Output signal duty cycle	D_{cycIN}-5		D_{cycIN}+5	%
	Maximum positive overshoot			1.3	V
	Minimum negative overshoot	-0.1			V

6.4 Clock Signal Descriptions

Table 6-27 presents clock signal descriptions.

Table 6-27 Clock Signal Descriptions

Signal Name	Type	Description	Ball Location
RTC32K_CK	DI	RTC 32 kHz clock input	AR21
X26M_IN	AI	26 MHz clock input	AB28
SRCLKENA0	DO	Output signal; control of PMIC 26 MHz / Buck / LDO normal mode or sleep • High: Normal mode • Low: Sleep mode or low power mode	AM21
SRCLKENA1	DO	Output signal; control of PMIC 26 MHz / Buck / LDO on or off	AL21

7 Package Information

7.1 Thermal Specifications

7.1.1 Thermal Operating Specifications

Table 7-1 presents the thermal resistance characteristics and maximum operating temperatures of the device.

Table 7-1 Thermal Operating Specifications

Parameter		Value	Unit
θ_{JA}	Package thermal resistances in natural convection	18.6	°C/Watt
θ_{JB}	Package thermal resistance (junction-to-board)	3.5	°C/Watt
θ_{JC}	Package thermal resistance (junction-to-case)	2.86	°C/Watt
T_j	Maximum operating junction temperature	105	°C

7.2 Top Marking

Figure 7-1 shows the device top marking definition.

Figure 7-1 Device Top Marking

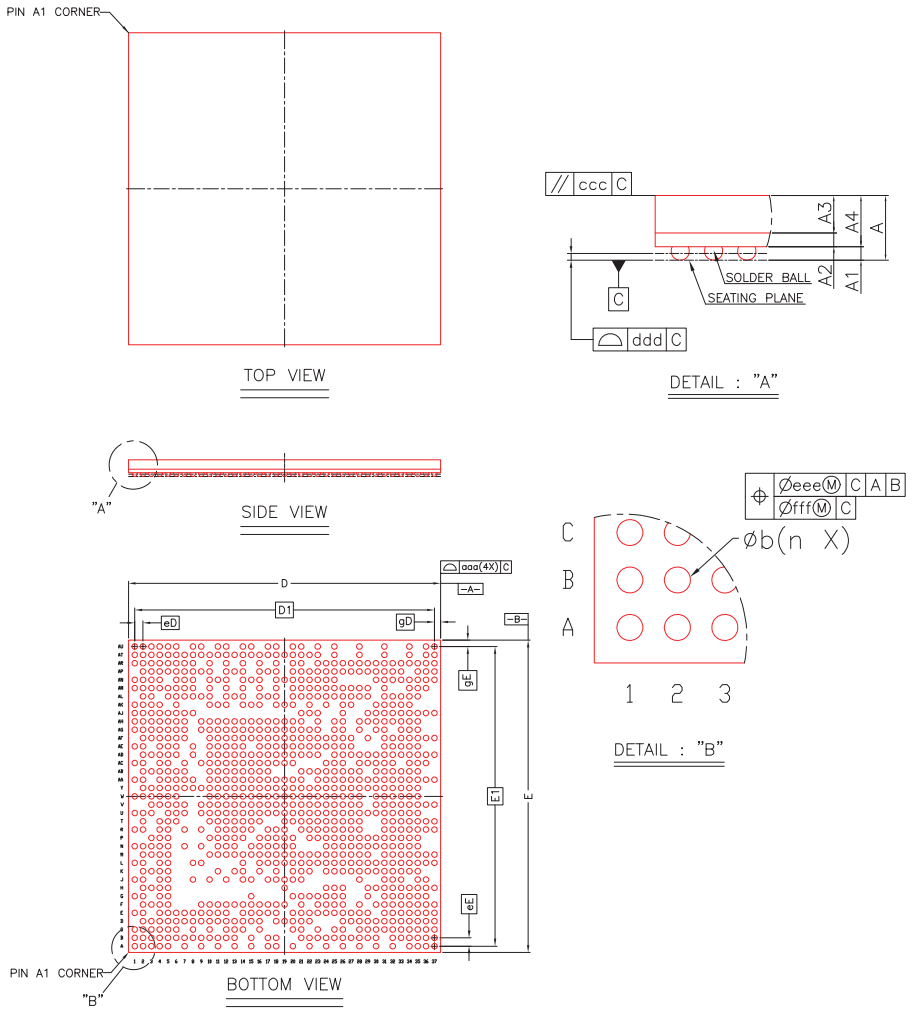
Table 7-2 presents the printed device reference and decoding.

Table 7-2 Printed Device Reference and Decoding

Parameter		Value	Description
NNNNNN#N	Part number	MT8395#V	Multimedia system
#	Function code 1		For internal use only
YYWW	Date code		2-digits year and week code
&&&&&	Random code		For internal use only
XXXXXX	Lot number		For internal use only
%	Function code 2		For internal use only
O	Pin one designator		Pin one location

7.3 Mechanical Drawing

Figure 7-2 shows printed device reference diagram (MFC VFBGA 15.0 mm × 15.0 mm, 1046-ball, 0.4 mm pitch package).



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	14.950	15.000	15.050
	Y	E	14.950	15.000	15.050
Ball Pitch	X	eD		0.400	
	Y	eE		0.400	
Mold Thickness		A3		0.450 Ref.	
Substrate Thickness		A2		0.168 Ref.	
Substrate+Mold Thickness		A4	0.568	0.618	0.668
Total Thickness		A	–	–	0.900
Ball Diameter				0.250	
Ball Stand Off		A1	0.140	0.180	0.220
Ball Width		b	0.220	0.270	0.320
Package Edge Tolerance		aaa		0.050	
Mold Flatness		ccc		0.100	
Coplanarity		ddd		0.100	
Ball Offset (Package)		eee		0.150	
Ball Offset (Ball)		fff		0.050	
Ball Count		n		1046	
Edge Ball Center to Center	X	D1		14.400	
	Y	E1		14.400	
Edge Ball Center to Package Edge	X	gD		0.300	
	Y	gE		0.300	

TITLE	PACKAGE OUTLINE MFC VFBGA 1046L 15 X 15 X 0.9 max		
DWG. NO.	REV.	SHEET	UNIT
MT-SP01479	A	1 OF 2	MM

Figure 7-2 Mechanical Drawing

PRELIMINARY INFORMATION

8 Legal and Support Information

8.1 Related Documents and Products

Documents:

- **MMD (MediaTek Module Design)**—Power Delivery Network (PDN) and DRAM design implementation solutions
- **MT8395 Baseband Design Notice**—Application note including schematic examples for peripheral interfaces such as GPIO, MSDC, NAND flash, UFS, LPDDR4X, I2C/I3C, SPI, Display, Camera, USB, DPI, Ethernet, HDMI, PCIe, Audio, and power design implementation recommendations.
- **MT6315 Application Note for MT8395**—MediaTek MT6315 PMIC application note covering functional description and PCB layout guidelines.
- **MT6360 Application Note for MT8395**—MediaTek MT6360 PMIC application note covering functional description and PCB layout guidelines.
- **MT6365 Application Note for MT8395**—MediaTek MT6365 PMIC application note covering functional description and PCB layout guidelines.

Companion chips:

- **MT6315**—Integrated Power Management IC (PMIC)
- **MT6360**—Integrated Power Management IC
- **MT6365**—Integrated Power Management IC

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