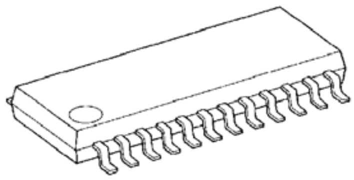
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62747AFG, TB62747AFNG

16-Output Constant Current LED Driver

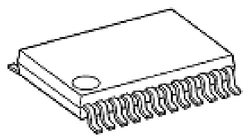
The TB62747 series is comprised of constant-current drivers designed for LEDs and LED panel displays.
The regulated current sources are designed to provide a constant current, which is adjustable through one external resistor.
The TB62747 series incorporates 16 channels of shift registers, latches, AND gates and constant-current outputs.
Fabricated using the Bi-CMOS process, the TB62747 series satisfies the system requirement of high-speed data transmission.
It operates with a 3.3 or 5.0 V power supply.

TB62747AFG



SSOP24-P-300-1.00B

TB62747AFNG



SSOP24-P-300-0.65A

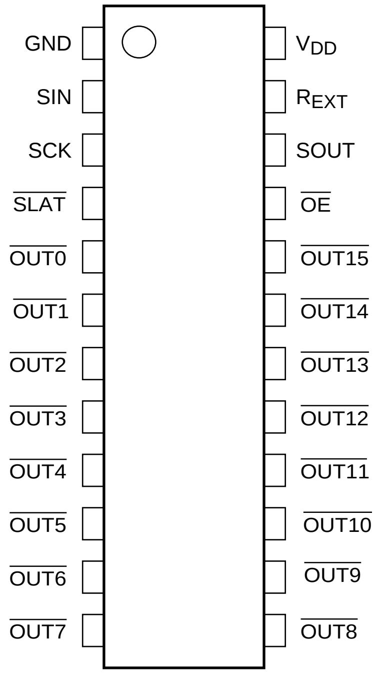
Weight
SSOP24-P-300-1.00B: 0.29 g (typ.)
SSOP24-P-300-0.65A: 0.14 g (typ.)

Features

- 16-output built-in
- Output current setting range
  : 1.5 to 35 mA @ V_{DD} = 3.3 V, V_O = 0.4 to 1.0 V
  : 1.5 to 45 mA @ V_{DD} = 5.0 V, V_O = 0.4 to 1.2 V
- Current accuracy (@ R_{EXT} = 1.2 kΩ, V_O = 0.4 V, V_{DD} = 3.3 V, 5.0 V)
  : Between outputs: ± 1.5 % (max)
  : Between devices: ± 1.5 % (max)
- high-speed output switching : $t_{wOE(L)}$ = 100 ns (min)
- Control data format : serial-in, parallel-out
- Input signal voltage level : 3.3 V and 5.0 V CMOS interfaces (Schmitt trigger input)
- Serial data transfer rate : f_{SCK} = 25 MHz (max) @cascade connection
- Power supply voltages : V_{DD} = 3.0 V to 5.5 V
- Operation temperature range: T_{opr} = -40 to 85 °C
- Output voltage : V_O = 26 V (max)
- Power on reset (POR)
- Package : AFG type : SSOP24-P-300-1.00B
  : AFNG type : SSOP24-P-300-0.65A

Pin Assignment (top view)

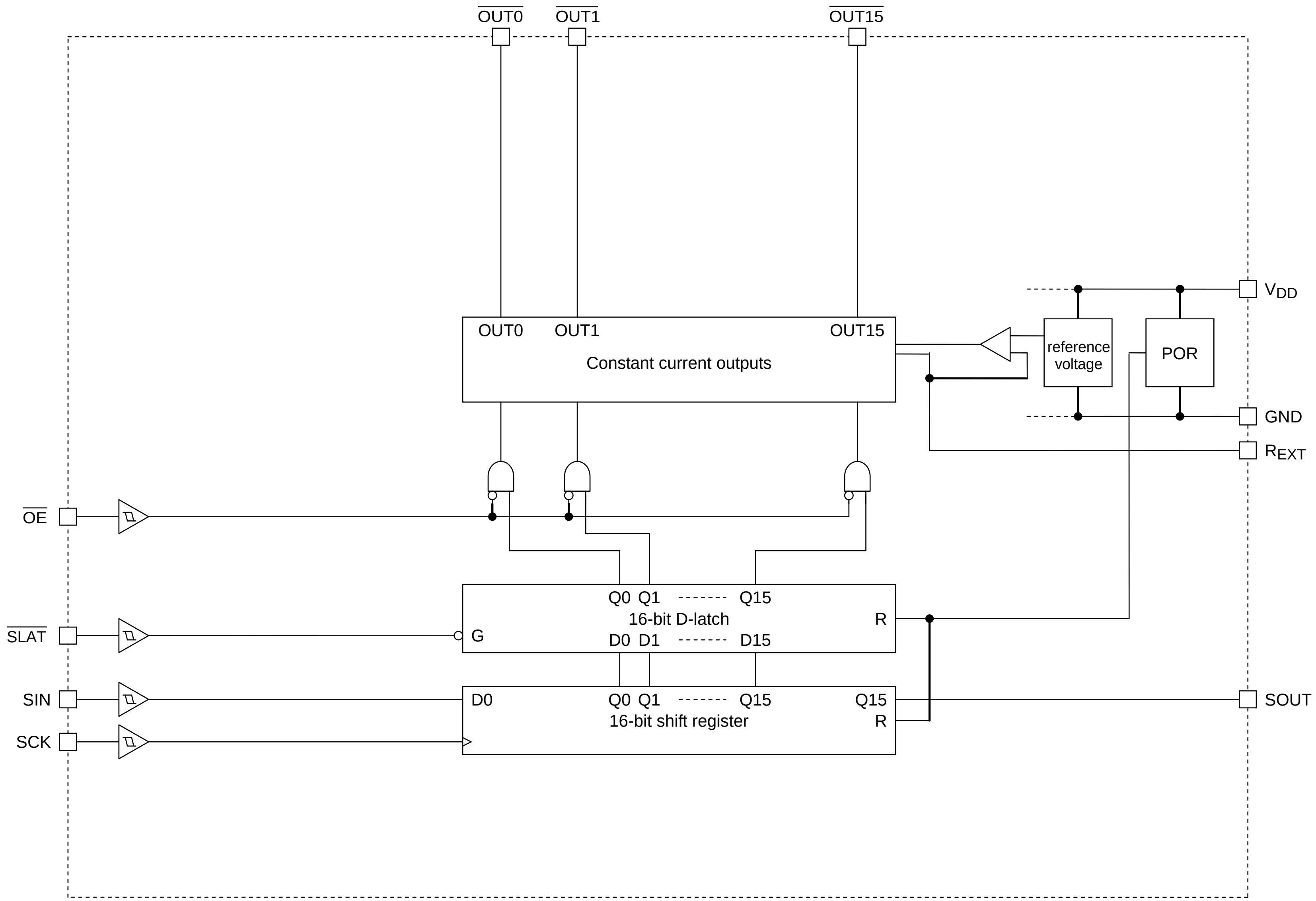
TB62747AFG/AFNG



Note1: Short circuiting an output pin to a power supply pin (V_{DD} or V_{LED}*), or short-circuiting the R_{EXT} pin to the GND pin will likely exceed the rating, which in turn may result in smoldering and/or permanent damage. Please keep this in mind when determining the wiring layout for the power supply and GND pins.

*: V_{LED}: LED power supply

Block Diagram



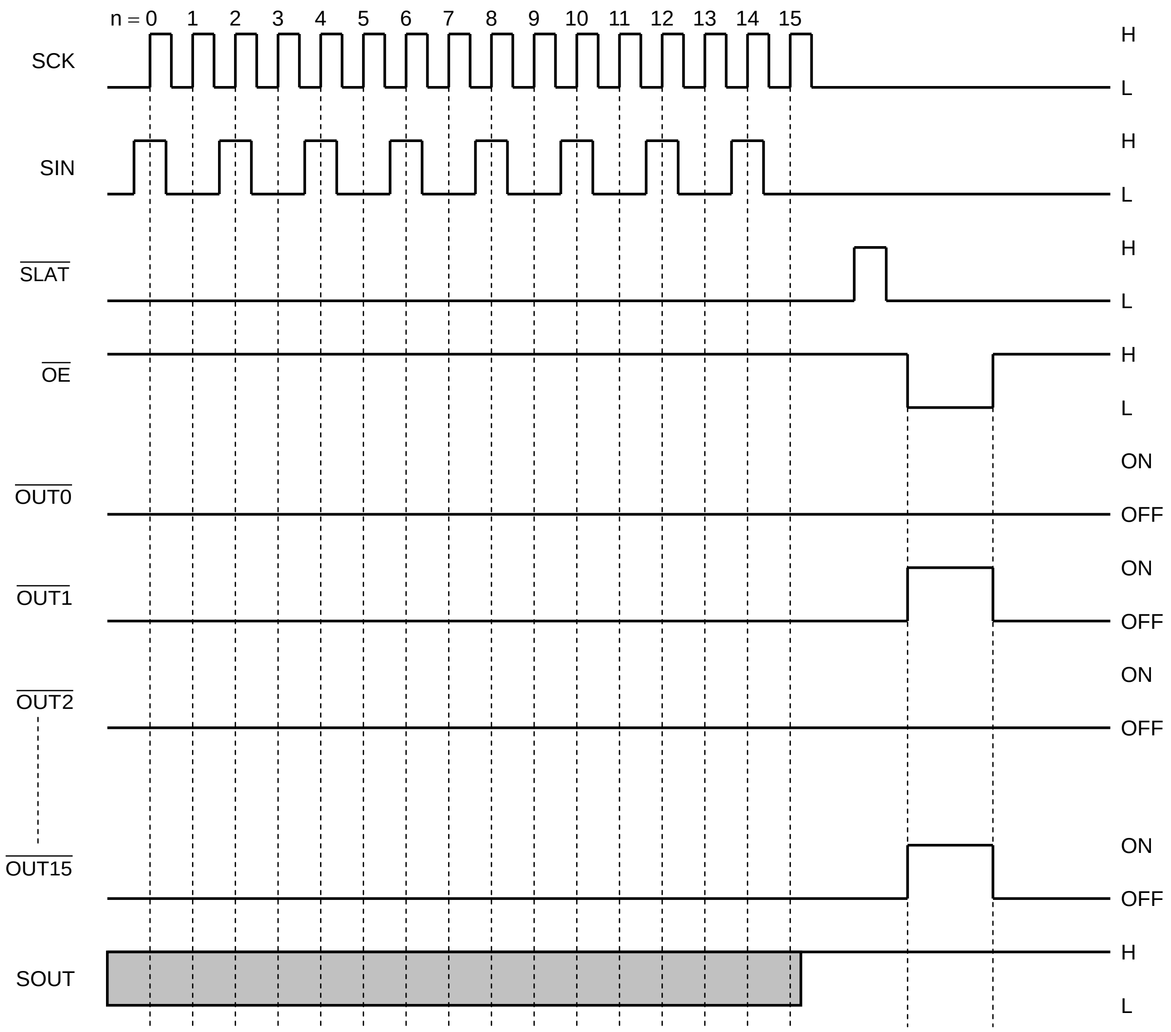
Truth Table

SCK	$\overline{SLAT}$	$\overline{OE}$	SIN	$\overline{OUT0}$ --- $\overline{OUT7}$ --- $\overline{OUT15}$ (Note1)	SOUT
↑	H	L	Dn	Dn --- Dn - 7 --- Dn - 15	Dn - 15
↑	L	L	Dn + 1	No Change	Dn - 14
↑	H	L	Dn + 2	Dn + 2 --- Dn - 5 --- Dn - 13	Dn - 13
↓	— (Note2)	L	Dn + 3	Dn + 2 --- Dn - 5 --- Dn - 13	Dn - 13
↓	— (Note2)	H	Dn + 3	OFF	Dn - 13

Note1: When $\overline{OUT0}$ to $\overline{OUT15}$ output pins are set to "H" the respective output will be ON and when set to "L" the respective output will be OFF.

Note2: "—"is irrelevant to the truth table.

Timing Diagram



Note 1: The latch circuit is a leveled-latch circuit. Please note that it is not a triggered-latch circuit.

Note 2: Keep the $\overline{SLAT}$ pin is set to "L" to enable the latch circuit to hold data. In addition, when the $\overline{SLAT}$ pin is set to "H" the latch circuit does not hold data. The data will instead pass onto output.
When the $\overline{OE}$ pin is set to "L" the $\overline{OUT0}$ to $\overline{OUT15}$ output pins will go ON and OFF in response to the data. In addition, when the $\overline{OE}$ pin is set to "H" all the output pins will be forced OFF regardless of the data.

Pin Functions

Pin No	Pin Name	I/O	Function
1	GND	—	The ground pin.
2	SIN	I	The serial data input pin.
3	SCK	I	The serial data transfer clock input pin. Data are shifted at the rising edge.
4	$\overline{\text{SLAT}}$	I	The latch signal input pin. Data is saved at L level.
5	$\overline{\text{OUT0}}$	O	A sink type constant current output pin.
6	$\overline{\text{OUT1}}$	O	A sink type constant current output pin.
7	$\overline{\text{OUT2}}$	O	A sink type constant current output pin.
8	$\overline{\text{OUT3}}$	O	A sink type constant current output pin.
9	$\overline{\text{OUT4}}$	O	A sink type constant current output pin.
10	$\overline{\text{OUT5}}$	O	A sink type constant current output pin.
11	$\overline{\text{OUT6}}$	O	A sink type constant current output pin.
12	$\overline{\text{OUT7}}$	O	A sink type constant current output pin.
13	$\overline{\text{OUT8}}$	O	A sink type constant current output pin.
14	$\overline{\text{OUT9}}$	O	A sink type constant current output pin.
15	$\overline{\text{OUT10}}$	O	A sink type constant current output pin.
16	$\overline{\text{OUT11}}$	O	A sink type constant current output pin.
17	$\overline{\text{OUT12}}$	O	A sink type constant current output pin.
18	$\overline{\text{OUT13}}$	O	A sink type constant current output pin.
19	$\overline{\text{OUT14}}$	O	A sink type constant current output pin.
20	$\overline{\text{OUT15}}$	O	A sink type constant current output pin.
21	$\overline{\text{OE}}$	I	The constant current output enable signal input pin. During the “H” level, the output will be forced off.
22	SOUT	O	The serial data output pin.
23	R_{EXT}	—	The constant current value setting resistor connection pin. Then a resistor connects to the ground. All output current is set to the same.
24	V_{DD}	—	The power supply input pin.

Absolute Maximum Ratings (T_a = 25°C)

Characteristics	Symbol	Rating (Note1)	Unit
Power supply voltage	V_{DD}	-0.4 to 6.0	V
Output current	I_O	55	mA
Logic input voltage	V_{IN}	-0.3 to V_{DD} + 0.3 (Note2)	V
Output voltage	V_O	-0.3 to 26	V
Operating temperature	T_{opr}	-40 to 85	°C
Storage temperature	T_{stg}	-55 to 150	°C
Thermal resistance	Rth(j-a)	94 (AFG), 120 (AFNG) When mounted PCB (Note3)	°C/W
Power dissipation	P_D	1.32 (AFG), 1.04 (AFNG) When mounted PCB (Note3), (Note4)	W

Note1: Voltage is ground referenced.

Note2: However, do not exceed 6 V.

Note3: PCB condition 76.2 mm x 114.3 mm x 1.6 mm, Cu 30 % (SEMI conforming, 4-Layer)

Note4: The power dissipation decreases the reciprocal of the saturated thermal resistance (1/ Rth(j-a)) for each One degree (°C) that the ambient temperature is exceeded from Ta = 25 °C.

Operating Conditions

DC Items (Unless otherwise specified, V_{DD} = 3.0 to 5.5 V, T_a = -40°C to 85°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	3.0	—	5.5	V
Output voltage when ON	$V_{O\ (ON)}$	$\overline{\text{OUTn}}$	0.4	—	4.0	V
High level logic input voltage	V_{IH}	SIN,SCK, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$	0.7 × V_{DD}	—	V_{DD}	V
Low level logic input voltage	V_{IL}	SIN,SCK, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$	GND	—	0.3 × V_{DD}	V
High level SOUT output current	I_{OH}	—	—	—	-1	mA
Low level SOUT output current	I_{OL}	—	—	—	1	mA
Constant current output	I_{O1}	$\overline{\text{OUTn}}$, V_{DD} = 3.3 V, V_O = 0.4 to 1.0 V	1.5	—	35	mA
	I_{O2}	$\overline{\text{OUTn}}$, V_{DD} = 5.0 V, V_O = 0.4 to 1.2 V	1.5	—	45	

AC Items (Unless otherwise specified, V_{DD} = 3.0 to 5.5 V, T_a = -40°C to 85°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Serial data transfer frequency	f_{SCK}	6	—	—	—	25	MHz
Hold time	t_{HOLD1}	6	—	5	—	—	ns
	t_{HOLD2}	6	—	5	—	—	ns
Setup time	t_{SETUP1}	6	—	5	—	—	ns
	t_{SETUP2}	6	—	5	—	—	ns
Maximum clock rise time	t_r	6	(Note1)	—	—	500	ns
Maximum clock fall time	t_f	6	(Note1)	—	—	500	ns

Note1: If the device is connected in a cascade and the tr/tf of the clock waveform increases due to deceleration of the clock waveform, it may not be possible to achieve the timing required for data transfer. Please keep these timing conditions in mind when designing your application.

Electrical Characteristics (Unless otherwise specified, V_{DD} = 3.3 V, T_a = 25°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH} = -1 mA	V_{DD} - 0.4	—	—	V
Low level logic output voltage	V_{OL}	1	I_{OL} = +1 mA	—	—	0.4	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD}, $\overline{OE}$, SIN, SCK	—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND, $\overline{SLAT}$, SIN, SCK	—	—	-1	μA
Power supply current	I_{DD1}	4	V_O = 25 V, R_{EXT} = OPEN, SCK = "L", $\overline{OE}$ = "H"	—	—	1.0	mA
	I_{DD2}	4	R_{EXT} = 1.2 kΩ, All output off	—	—	4.0	mA
	I_{DD3}	4	R_{EXT} = 1.2 kΩ, All output on	—	—	8.0	mA
Output current	I_O	5	V_{DD} = 3.3 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	14	—	mA
Constant current error(Ch to Ch)	$\Delta I_{O(Ch)}$	5	V_{DD} = 3.3 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±1.5	%
Constant current error(IC to IC)	$\Delta I_{O(IC)}$	5	V_{DD} = 3.3 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±1.5	%
Output OFF leak current	I_{OK}	5	V_{DD} = 3.3 V, V_O = 25 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	—	0.5	μA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD} = 3.0 to 3.6 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±2	%
Constant current output voltage regulation	$\%V_O$	5	V_{DD} = 3.3 V, V_O = 0.4 to 3.0 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	—	%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	$\overline{SLAT}$	250	500	800	kΩ

Electrical Characteristics (Unless otherwise specified, V_{DD} = 5.0 V, T_a = 25°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
High level logic output voltage	V_{OH}	1	I_{OH} = -1 mA	V_{DD} - 0.4	—	—	V
Low level logic output voltage	V_{OL}	1	I_{OL} = +1 mA	—	—	0.4	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD}, $\overline{OE}$, SIN, SCK	—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND, $\overline{SLAT}$, SIN, SCK	—	—	-1	μA
Power supply current	I_{DD1}	4	V_O = 25 V, R_{EXT} = OPEN, SCK = "L", $\overline{OE}$ = "H"	—	—	1.0	mA
	I_{DD2}	4	R_{EXT} = 1.2 kΩ, All output off	—	—	4.5	mA
	I_{DD3}	4	R_{EXT} = 1.2 kΩ, All output on	—	—	8.0	mA
Output current	I_O	5	V_{DD} = 5.0 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	14	—	mA
Constant current error(Ch to Ch)	$\Delta I_{O(Ch)}$	5	V_{DD} = 5.0 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±1.5	%
Constant current error(IC to IC)	$\Delta I_{O(IC)}$	5	V_{DD} = 5.0 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±1.5	%
Output OFF leak current	I_{OK}	5	V_{DD} = 5.0 V, V_O = 25 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	—	0.5	μA
Constant current power supply voltage regulation	$\%V_{DD}$	5	V_{DD} = 4.5 to 5.5 V, V_O = 0.4 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	±2	%
Constant current output voltage regulation	$\%V_O$	5	V_{DD} = 5.0 V, V_O = 0.4 to 3.0 V, R_{EXT} = 1.2 kΩ, $\overline{OUT0}$ to $\overline{OUT15}$	—	±1	—	%/V
Pull-up resistor	R_{UP}	3	$\overline{OE}$	250	500	800	kΩ
Pull-down resistor	R_{DOWN}	2	$\overline{SLAT}$	250	500	800	kΩ

Switching Characteristics (Unless otherwise specified, V_{DD} = 3.0 V, T_a = 25°C)

Characteristics		Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Propagation delay time	SCK- $\overline{\text{OUT0}}$	t_{pLH1}	6	$\overline{\text{SLAT}}$ = “H”, $\overline{\text{OE}}$ = “L”	—	20	300	ns
	$\overline{\text{SLAT}}$ - $\overline{\text{OUT0}}$	t_{pLH2}	6	$\overline{\text{OE}}$ = “L”	—	20	300	ns
	$\overline{\text{OE}}$ - $\overline{\text{OUT0}}$	t_{pLH3}	6	$\overline{\text{SLAT}}$ = “H”	—	20	300	ns
	SCK-SOUT	t_{pLH}	6	CL=10.5 pF	10	20	35	ns
	SCK- $\overline{\text{OUT0}}$	t_{pHL1}	6	$\overline{\text{SLAT}}$ = “H”, $\overline{\text{OE}}$ = “L”	—	30	340	ns
	$\overline{\text{SLAT}}$ - $\overline{\text{OUT0}}$	t_{pHL2}	6	$\overline{\text{OE}}$ = “L”	—	70	340	ns
	$\overline{\text{OE}}$ - $\overline{\text{OUT0}}$	t_{pHL3}	6	$\overline{\text{SLAT}}$ = “H”	—	70	340	ns
	SCK-SOUT	t_{pHL}	6	CL=10.5 pF	10	20	35	ns
Output rise time		t_{or}	6	10 to 90 % of voltage waveform	—	20	90	ns
Output fall time		t_{of}	6	90 to 10 % of voltage waveform	—	25	180	ns
Enable pulse width		$t_{wOE(L)}$	6	$\overline{\text{OE}}$ = “L” (Note1)	100	—	—	ns
Clock pulse width		t_{wSCK}	6	SCK = “H” or “L”	20	—	—	ns
Latch pulse width		t_{wSLAT}	6	$\overline{\text{SLAT}}$ = “H”	20	—	—	ns

Note1: At the condition of $t_{wOE(H)}$ = 250 ns or more

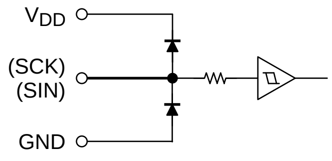
Switching Characteristics (Unless otherwise specified, V_{DD} = 5.5 V, T_a = 25°C)

Characteristics		Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Propagation delay time	SCK- $\overline{\text{OUT0}}$	t_{pLH1}	6	$\overline{\text{SLAT}}$ = “H”, $\overline{\text{OE}}$ = “L”	—	20	300	ns
	$\overline{\text{SLAT}}$ - $\overline{\text{OUT0}}$	t_{pLH2}	6	$\overline{\text{OE}}$ = “L”	—	20	300	ns
	$\overline{\text{OE}}$ - $\overline{\text{OUT0}}$	t_{pLH3}	6	$\overline{\text{SLAT}}$ = “H”	—	20	300	ns
	SCK-SOUT	t_{pLH}	6	CL=10.5 pF	10	20	35	ns
	SCK- $\overline{\text{OUT0}}$	t_{pHL1}	6	$\overline{\text{SLAT}}$ = “H”, $\overline{\text{OE}}$ = “L”	—	30	340	ns
	$\overline{\text{SLAT}}$ - $\overline{\text{OUT0}}$	t_{pHL2}	6	$\overline{\text{OE}}$ = “L”	—	70	340	ns
	$\overline{\text{OE}}$ - $\overline{\text{OUT0}}$	t_{pHL3}	6	$\overline{\text{SLAT}}$ = “H”	—	70	340	ns
	SCK-SOUT	t_{pHL}	6	CL=10.5 pF	10	20	35	ns
Output rise time		t_{or}	6	10 to 90 % of voltage waveform	—	20	90	ns
Output fall time		t_{of}	6	90 to 10 % of voltage waveform	—	25	180	ns
Enable pulse width		$t_{wOE(L)}$	6	$\overline{\text{OE}}$ = “L” (Note1)	100	—	—	ns
Clock pulse width		t_{wSCK}	6	SCK = “H” or “L”	20	—	—	ns
Latch pulse width		t_{wSLAT}	6	$\overline{\text{SLAT}}$ = “H”	20	—	—	ns

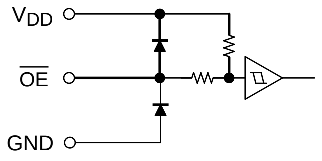
Note1: At the condition of $t_{wOE(H)}$ = 250 ns or more

I/O Equivalent Circuits

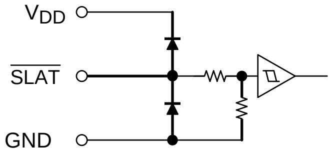
1. SCK, SIN



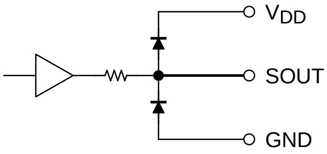
2. $\overline{OE}$



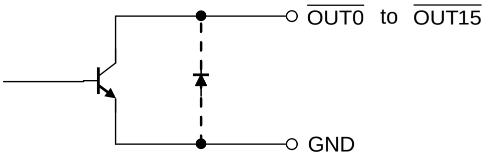
3. $\overline{SLAT}$



4. SOUT

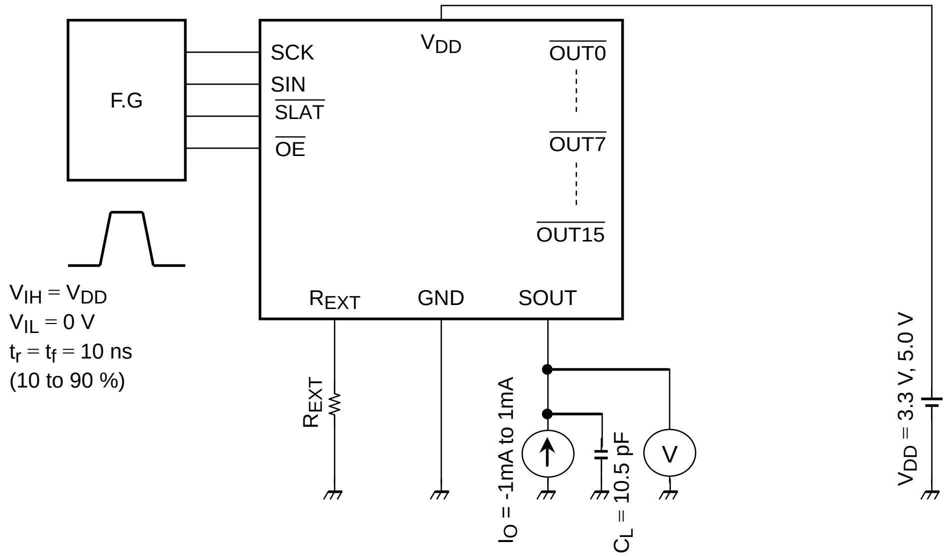


5. $\overline{OUT0}$ to $\overline{OUT15}$

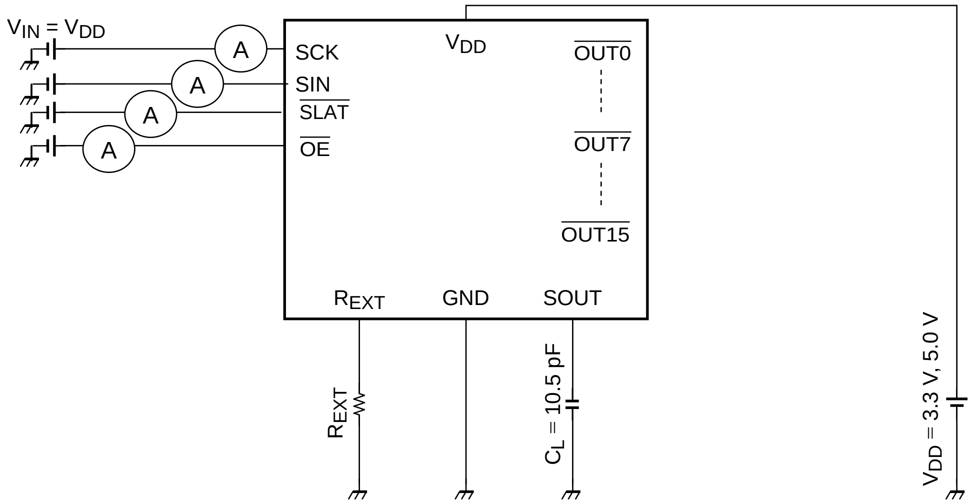


Test Circuits

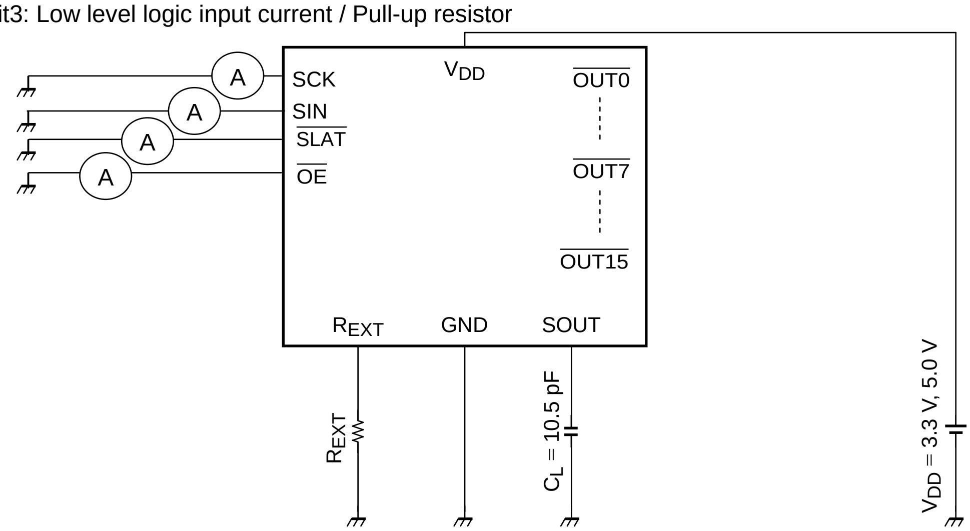
Test Circuit1: High level logic output voltage / Low level logic output voltage



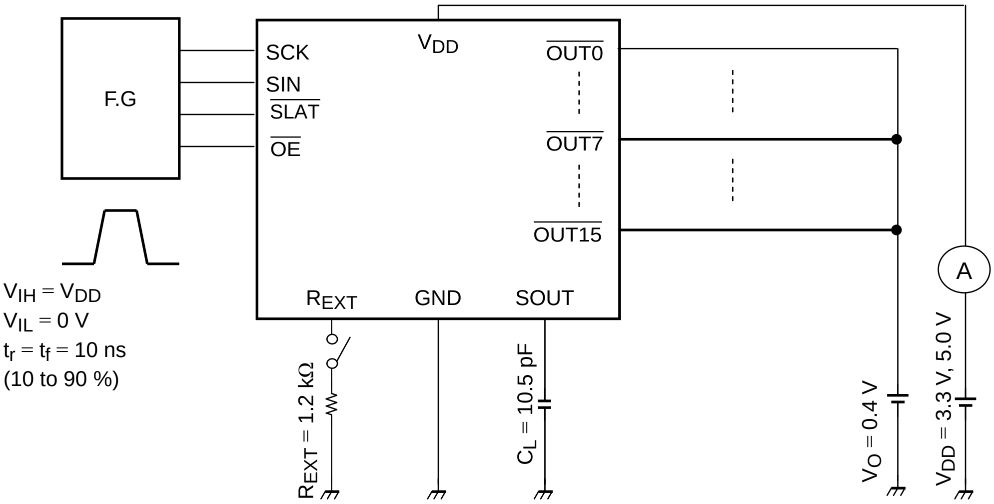
Test Circuit2: High level logic input current / Pull-down resistor



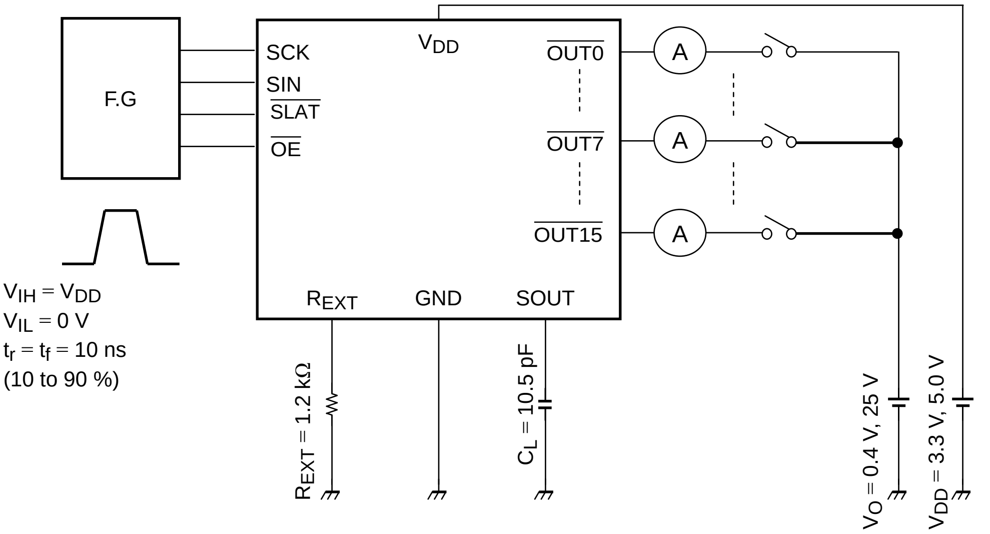
Test Circuit3: Low level logic input current / Pull-up resistor



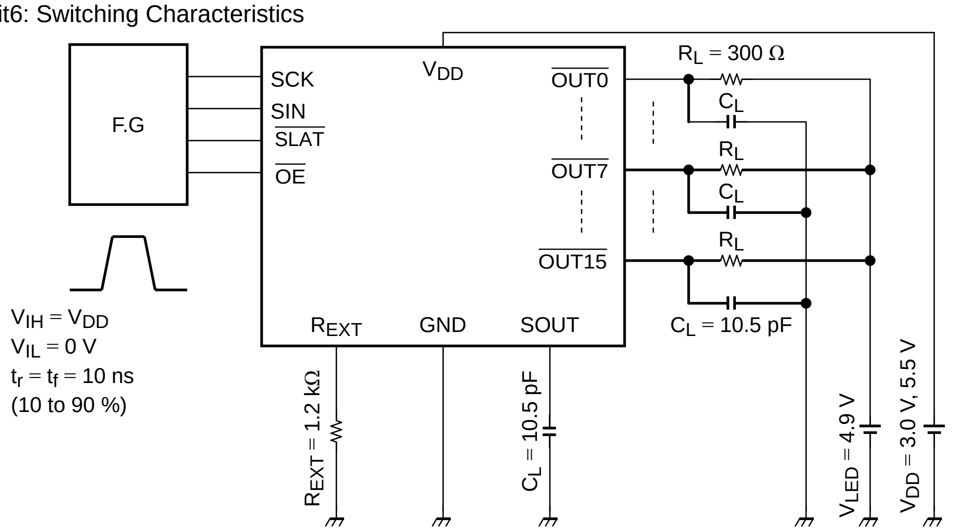
Test Circuit4: Power supply current



Test Circuit5: Constant current output / Output OFF leak current / Constant current error
Constant current power supply voltage regulation / Constant current output voltage regulation

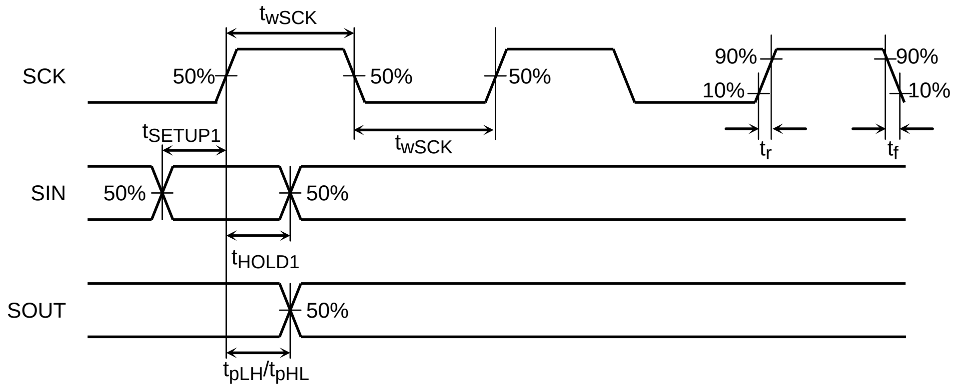


Test Circuit6: Switching Characteristics

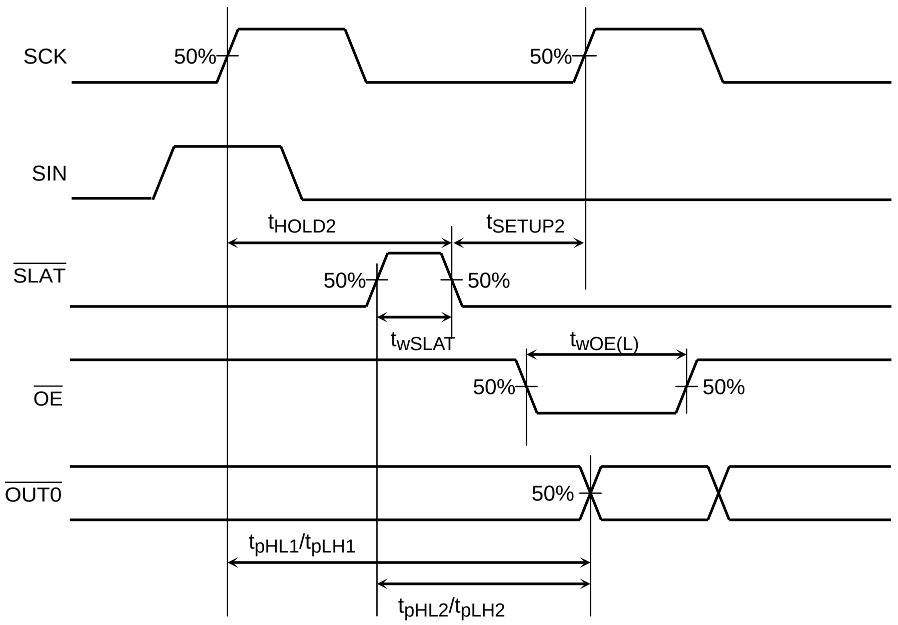


Timing Waveforms

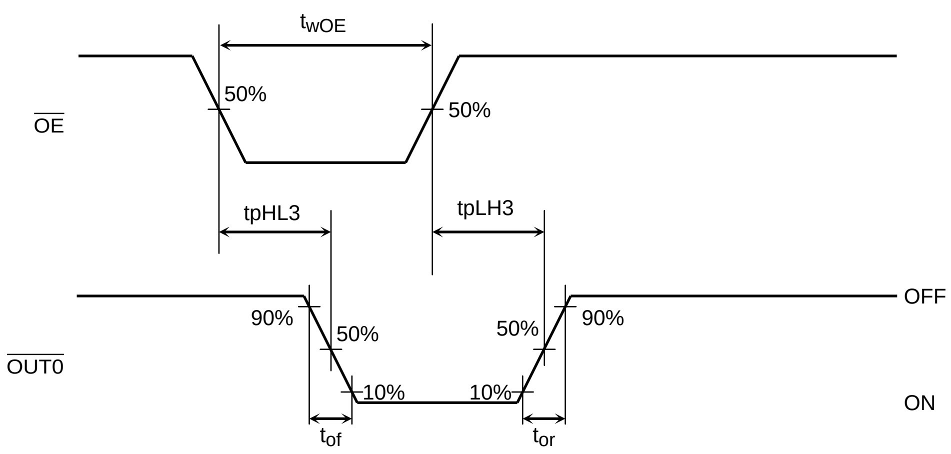
1. SCK, SIN, SOUT



2. SCK, SIN, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$, $\overline{\text{OUT0}}$



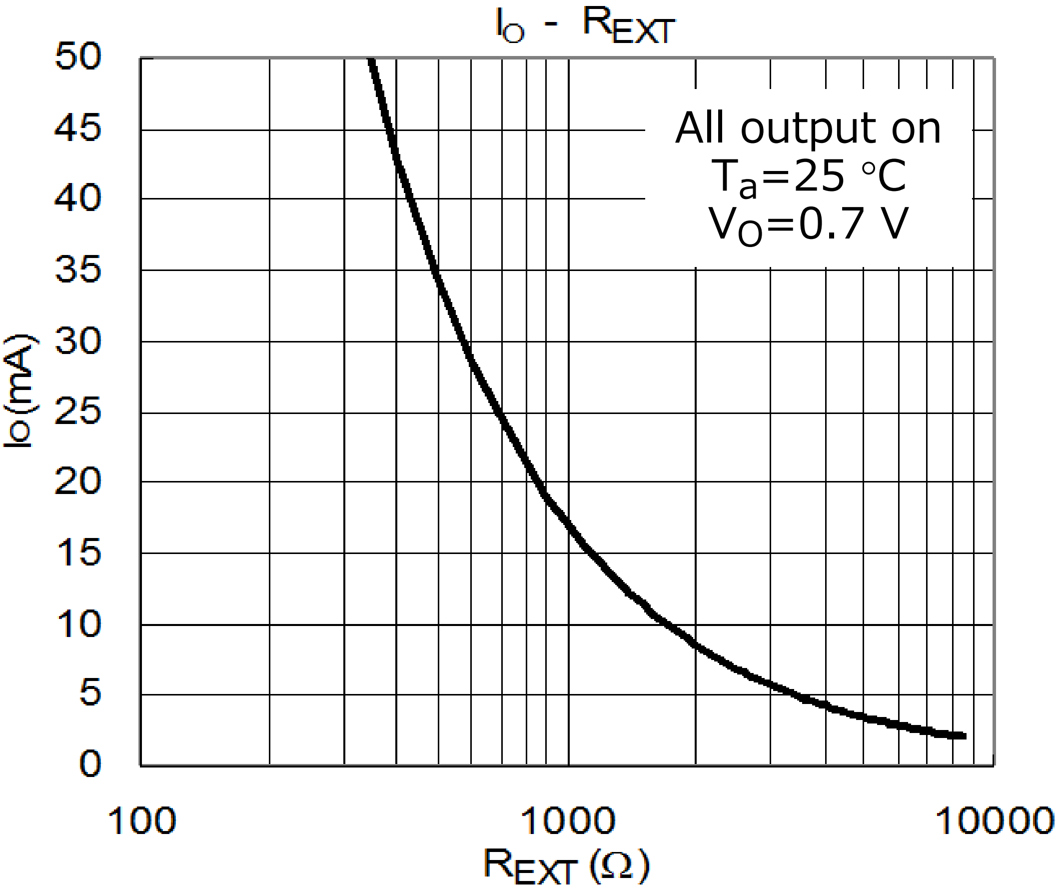
3. $\overline{\text{OE}}$, $\overline{\text{OUT0}}$



Reference data

*This data is provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

Output Current – R_{EXT} Resistor



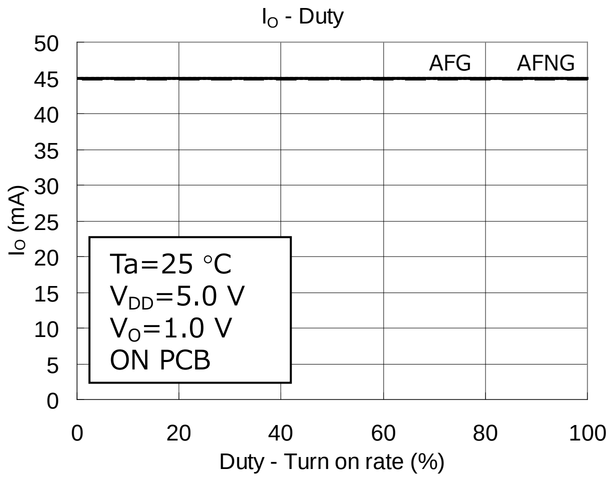
Theoretical value

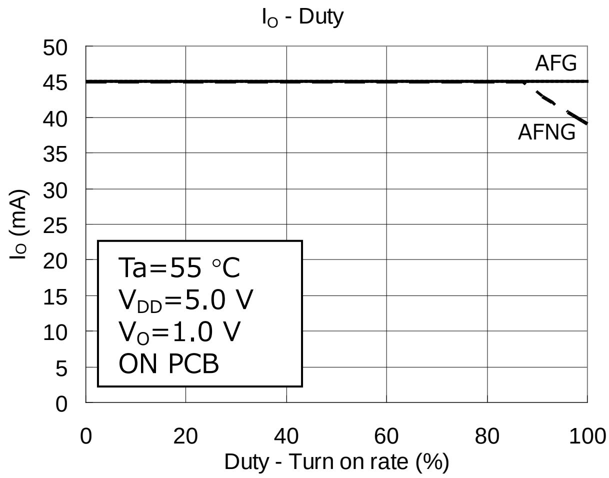
$I_{OUT\ (A)} = 1.13\ (V) \div R_{EXT}\ (\Omega) \times 14.9$

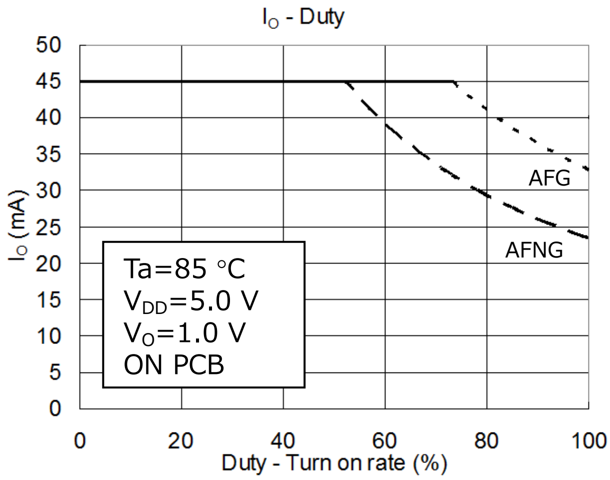
Reference data

*This data is provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

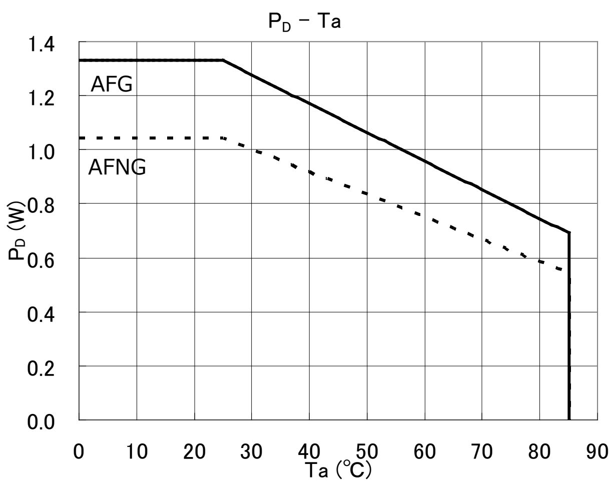
Output Current – Duty (LED turn-on rate)







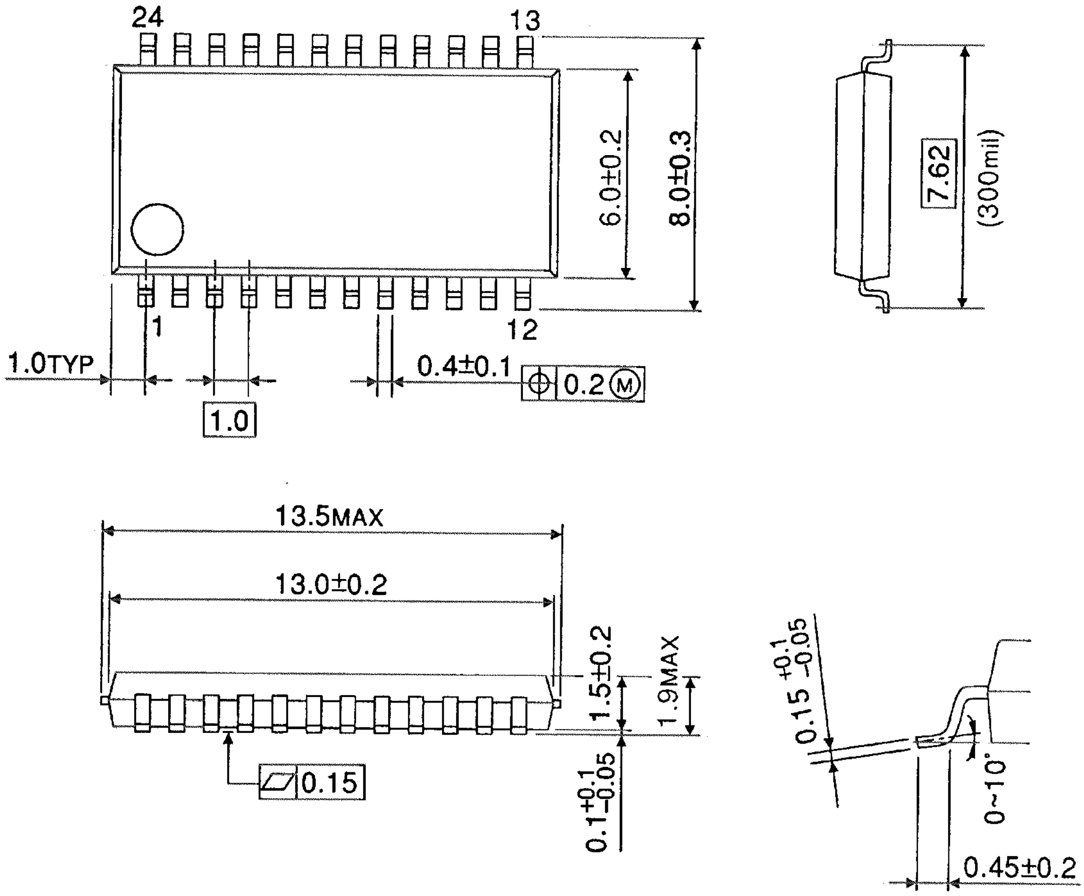
Power dissipation – Ta



Package Dimensions

SSOP24-P-300-1.00B

Unit : mm

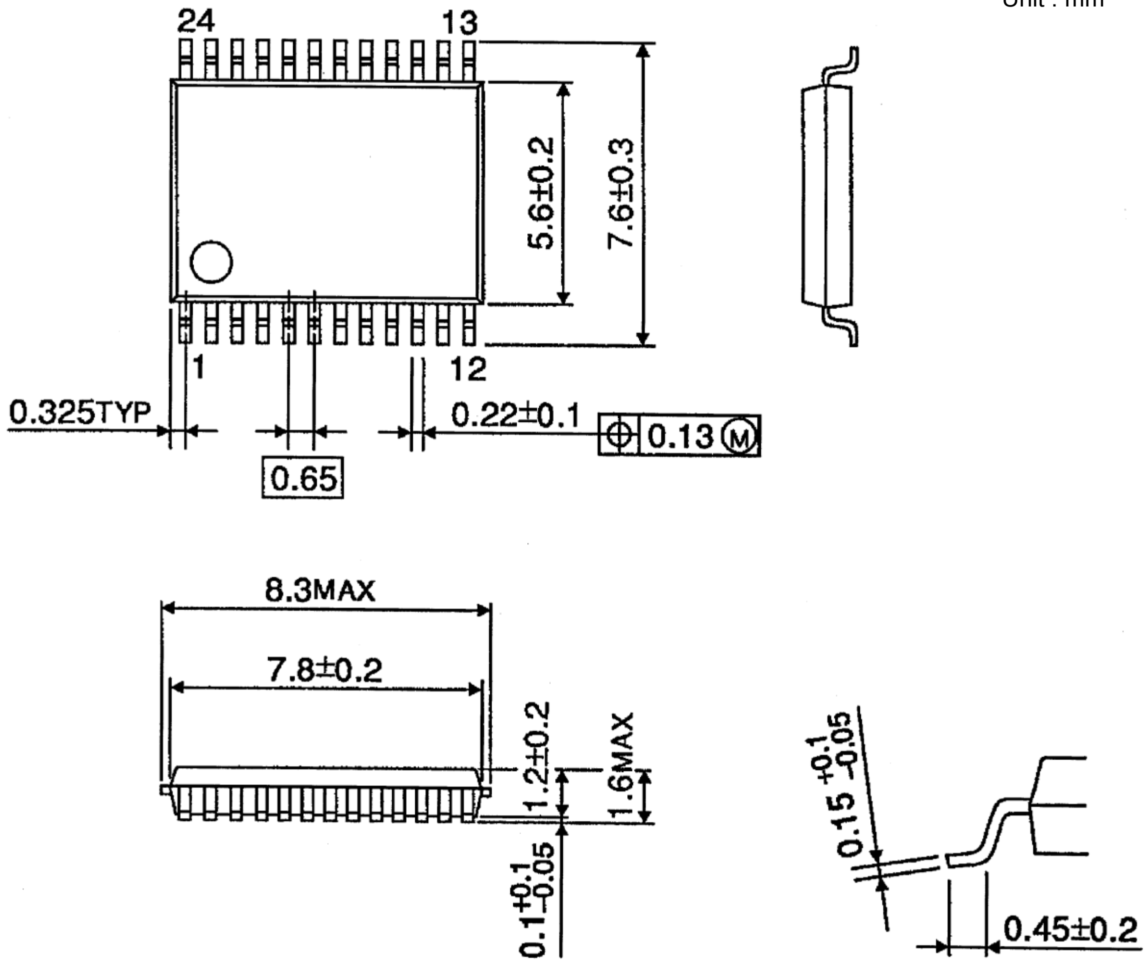


Weight: 0.29 g (typ.)

Package Dimensions

SSOP24-P-300-0.65A

Unit : mm



Weight: 0.14 g (typ.)

Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

[5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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